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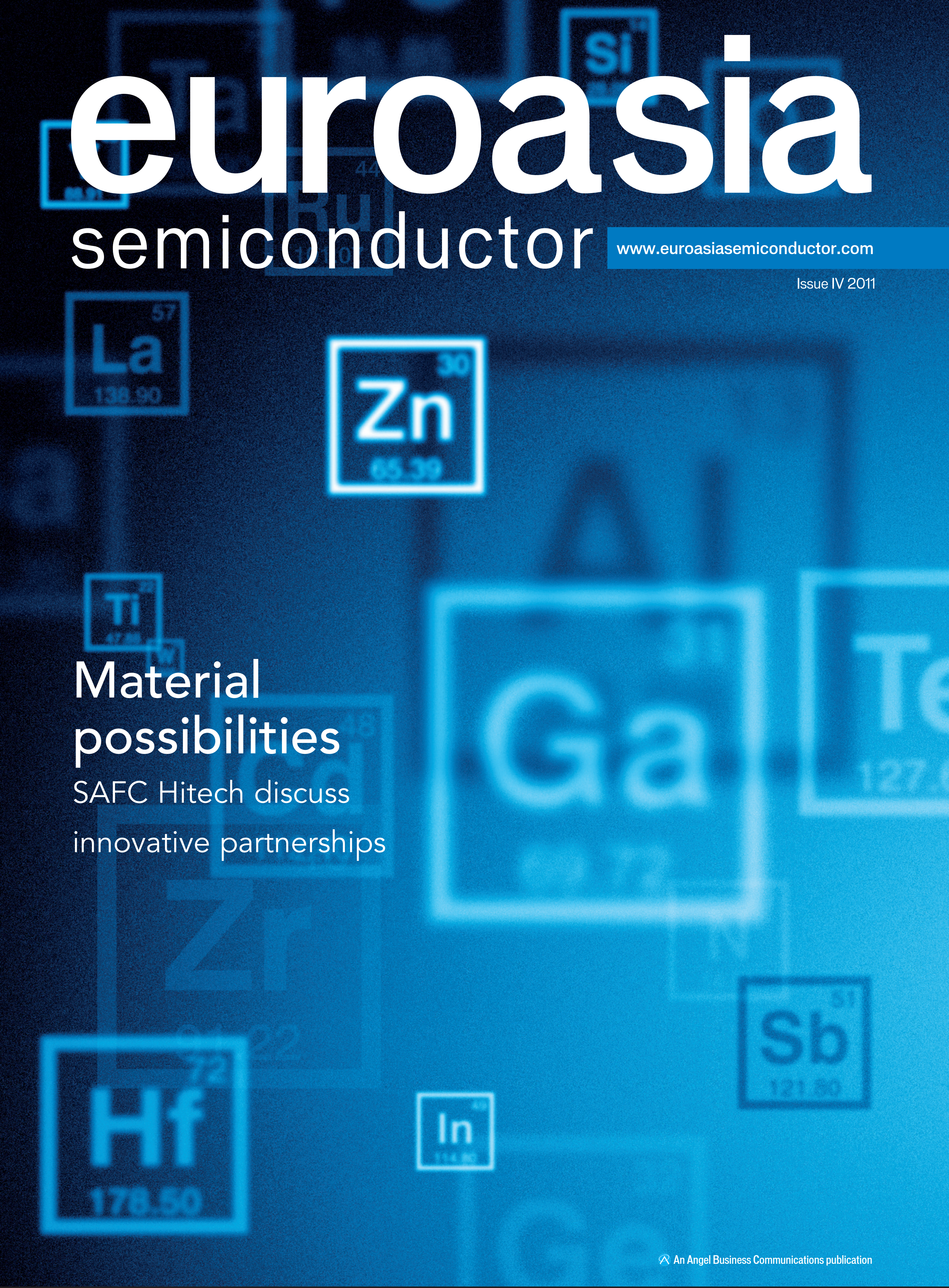

Material possibilities

SAFC Hitech discuss innovative partnerships

An Angel Business Communications publication

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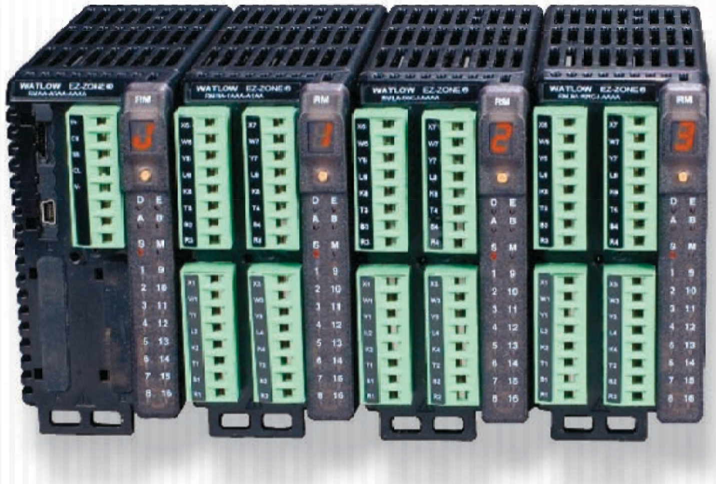

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editor's word

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Multiple opportunities

Financial concerns about future possibilities again dominates industry coverage as the realisation of eight positive quarters points to a corrective slowdown with over stocked inventories leading to an inevitable reduction in business along the value chain. With global economy uncertainty the caution expressed by financial watchers make is appear gloom and doom is on the horizon for everyone. Most of financial focus is on the commodity and volume edge of the business and even the pessimists are predicting growth for 2012 although well below 3%. These large semiconductor sectors will continue to be slave to the broader economic trends but there is plenty of opportunity in other areas of the industry.

The technological and economic transitions we see at the volume and bleeding edge part of the industry continue to occur along the value chain. With 300mm manufacturing beginning to migrate down technology nodes there are developing opportunities and job creation continuing to occur. Expertise developed at the top end is now required throughout the industry. Emerging industries continue to open up as these sectors realise the decades of knowledge accumulated in silicon manufacturing means the best chance to scale to required volumes is utilising existing proven manufacturing techniques. A number of new companies are capitalising on this trend by looking at research progress in a wide range of technologies to see if their manufacturing experience can provide solutions to manufacturing challenges. Who knows what roadblocks researchers are facing where a fresh experienced pair of eyes may see an engineering possibility.

Solar energy has cetainly being one area that semiconductor companies have benefited from but that is only one emerging market of opportunity. Medical applications of technology will be a major area of expansion and one that traditional semiconductor OEM manufacturers have barely touched. Challenges in deposition, consistency, yield and micromachining are some of the areas that this sector will need to develop.

When the semiconductor industry moved to 300mm there was a fear of a lack of knowledge but this turned out unfounded as other industries has many of the answers. There are many emerging ideas that are waiting for engineers to provide know how to manufacturers who feel they are faced with a herculean task.

David Ridsdale
Editor-in-Chief

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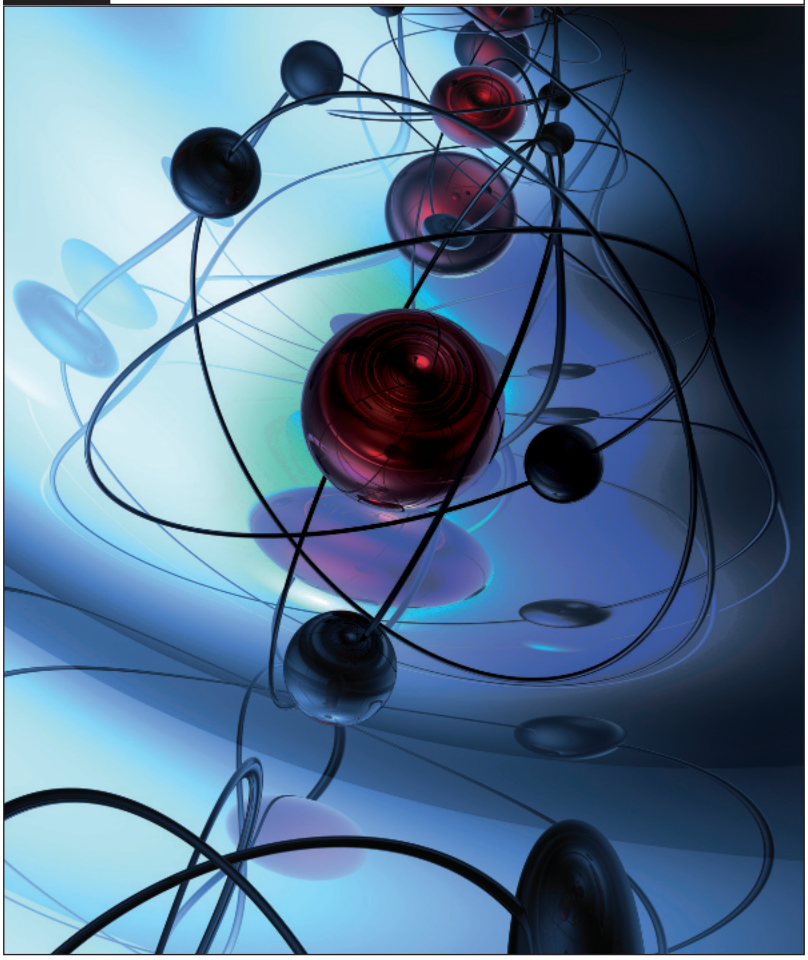

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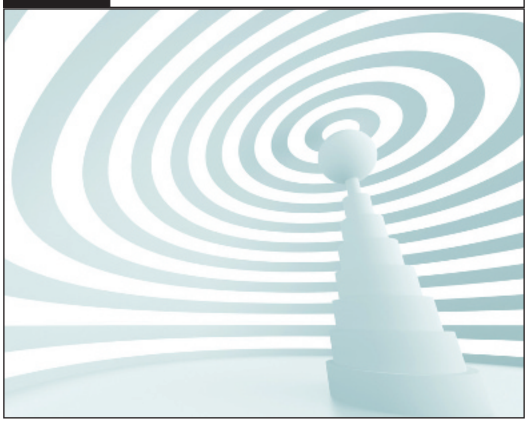

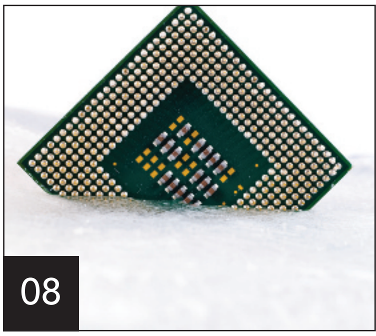

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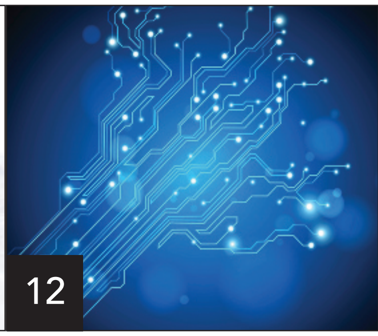

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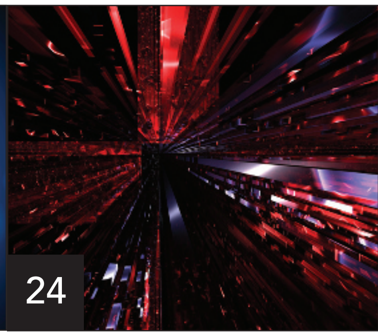

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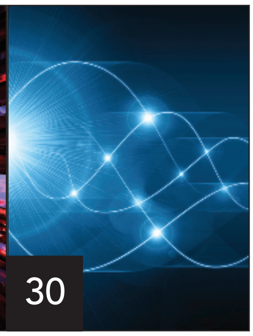

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Cool silicon

Future designs

Understanding character

Light manufacturing

Hydrogen source could be future energy key

A GRAIN of salt or two may be all that microbial electrolysis cells need to produce hydrogen from wastewater or organic byproducts, without adding carbon dioxide to the atmosphere or using grid electricity, according to Penn State engineers.

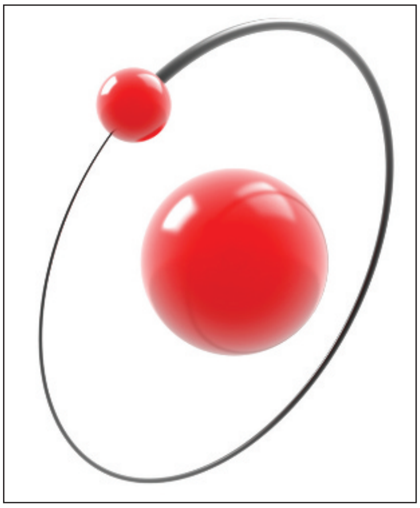
"This system could produce hydrogen anyplace there is wastewater near sea water," said Bruce E. Logan, Kappe Professor of Environmental Engineering. "It uses no grid electricity and is completely carbon neutral. It is an inexhaustible source of energy."

Microbial electrolysis cells that produce hydrogen are the basis of this recent work, but previously, to produce hydrogen, the fuel cells required some electrical input. Now, Logan, working with postdoctoral fellow Younggy Kim is using the difference between river water and seawater to add the extra energy needed to produce hydrogen.

The results, published in the Proceedings of the National Academy of Sciences, "show that pure hydrogen gas can efficiently be produced from virtually limitless supplies of seawater and river water and biodegradable organic matter."

Logan's cells were between 58 and 64 percent efficient and produced between 0.8 to 1.6 cubic meters of hydrogen for every cubic meter of liquid through the cell each day. The researchers estimated that only about 1 percent of the energy produced in the cell was needed to pump water through the system. The key is reverse electrodialysis or RED that extracts energy from the ionic differences between salt water and fresh water. A RED stack consists of alternating ion exchange membranes with each RED contributing to the electrical output.

For RED technology to hydrolyze water — split it into hydrogen and oxygen — requires 1.8 volts, which would in practice require about 25 pairs of membrane sand increase pumping resistance. However, combining RED technology with exoelectrogenic bacteria — bacteria that consume organic material and produce an electric current — reduced the number of RED stacks to five membrane pairs.



Previous work with microbial electrolysis cells showed that they could produce about 0.3 volts of electricity, but not the 0.414 volts needed to generate hydrogen in these fuel cells. Adding less than 0.2 volts of outside electricity released the hydrogen. Now, by incorporating 11 membranes, five membrane pairs that produce about 0.5 volts, the cells produce hydrogen.

"The added voltage that we need is a lot less than the 1.8 volts necessary to hydrolyze water," said Logan. "Biodegradable liquids and cellulose waste are abundant and with no energy in and hydrogen out we can get rid of wastewater and by-products. This could be an inexhaustible source of energy."

Gartner cautions oversupply

SEMICONDUCTOR days of inventory are forecast to plateau in the 3rd Q of 2011 at worrisome levels given current conditions and the likelihood that consumer and business spending will be weaker than expected, according to Gartner who expects the industry to begin an correction in late 2011.

"The semiconductor industry entered the third quarter of 2011 with moderately high levels of inventory," said Gerald Van Hoy, senior research analyst at Gartner. "The correction comes at a time when ASPs are tracking below trend levels, with overcapacity in the foundry space expected to prolong this weakness," said Peter Middleton, principal analyst at Gartner. "Excess inventory levels helped buffer the impact of the Japanese earthquake."

Gartner analysts said the industry will undergo a moderate inventory correction during the next few quarters, which will lower demand for semiconductor production in the second half of 2011 and early 2012. The proportion of total semiconductor inventory held by OEMs has begun to rise; however, it is still near historic lows, which will help reduce the impact of an order correction on semiconductor vendor sales.

Gartner's conclusions are supported by its Gartner Index of Inventory Semiconductor Supply-chain Tracking (GIISST), which remains at caution levels with days of inventory (DOI) at 1.12 in the third quarter of 2011. An above DOI level of 1.10 indicates inventories are inflated.

Below the 0.95 level indicates inventories are low, components may be on allocation and double ordering begins. The GIISST assesses "normal" inventory levels throughout the supply chain and compares them with current levels to evaluate industry trends.

It gauges the normal inventory level at each stage of production that will allow for a smooth flow of products and management of the production process without inventory shortages or surpluses.

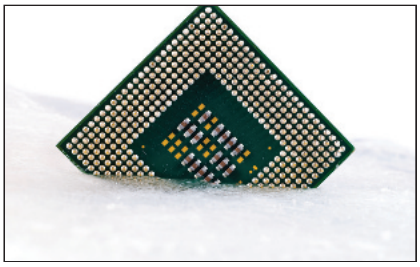
Saxony's cool silicon

FUTURE state-of-the-art technologies for the design and production of energy efficient and yet particularly high-performing analogue-digital circuits are developed by the Saxon Leading-Edge Cluster "Cool Silicon". Among other things they will contribute to decreasing the power consumption of ICs.

The research project "Design and Technology Platform for the Design of Highly Efficient Integrated High-Frequency Circuits in 28 nm CMOS (Cool-RF-28)" is a cooperation of GLOBALFOUNDRIES, the Intel Mobile Communications GmbH, the TU Dresden chair for Circuit Design And Network Theory (LSN), and the chair for Highly-Parallel VLSI-Systems and Neuromorphic Circuits, headed by Dr.-Ing. habil. René Schüffny. The project is coordinated by Dr. Carta, LSN.

The research project aims at enabling the design and production of circuits combining analogue and digital components in 28 nanometre CMOS technology. Suchlike circuits are currently produced with structures of 90 and 65 nanometres. Foregoing the 45 nanometre step, the Dresden-based team wants to drive the miniaturization forward significantly.

"Compared to the current state-of-the-art the 28 nanometre CMOS technology opens the doors for a



significantly lower energy consumption as well as considerably higher working frequencies", Professor Dr. Frank Ellinger, the coordinator of the research project, explains. Yet it usually is other types of circuits that set the pace for technological development. The miniaturization of the structures, the so-called scaling, starts with the memory chips and the processors. Along with new technologies those complex digital structures are produced the quickest and therefore design kits for them are available very early.

"Components for high-performance analog functions are usually not available at the time of the implementation of new CMOS technologies", Ellinger elaborates. "Hence, there are no optimized passive components or high-frequency bipolar transistor models providing the accuracy necessary for narrow band high-frequency circuits."

Techcet Forecasts $1.6B for 2013

THE 2010 market for crucibles and fabricated quartz OEM parts for semiconductor applications totalled $1.2B, up 89% over the 2009 low, according to a new report from Techcet Group, "Quartz for Semiconductor Applications 2011." The outlook is for continuing recovery with an additional 15% growth in 2011 and 1.5% in 2012, with growth resuming at 10% in 2013.

Hot and cold fabricated parts total 60% of the market, with 20% for crucibles and base materials (ingots, boules, rods, tubes). Fabricated quartz revenues doubled in 2010, despite some interruption at SEH from the March, 2011 earthquake and tsunami. Parts for 300mm are boosting revenues, even though this segment faces increasing competition from silicon carbide, silicon and ceramic fabricated parts. Sales for solar PV crucibles (not included in these numbers) outpaced semiconductor crucible revenues in 2010 in what is expected to be a short term bubble, as excess PV capacity moves into production. Inventory re-stocking has been driving the buying frenzy in quartz ingots, rods and tubes, pushing lead times out to six months or longer. The report provides an overview of the quartz crucible and OEM parts market that supports semiconductor device manufacturing.

Japanese researchers in synaptic discovery

RESEARCHERS working at the International Centre for Materials Nanoarchitectonics (MANA) have demonstrated for the first time the key features in the neuroscience and psychology of memory by a AgS_2 synapse.

Artificial neural networks have attracted attention as a means to a better understanding of biological neural networks, as well as aiding developments in artificial intelligence. The complex and interconnected nature of thought processes make neural behaviour difficult to reproduce in artificial structures without software programming. Now Takeo Ohno and researchers at MANA, Tsukuba, Japan, and the University of California have mimicked synaptic activity with the electroionic behavior of a nanoscale AgS2 electrode.

The researchers observed a temporary higher-conductance state in the AgS2 system following an incident electric pulse. Repetition of the input pulse over 2 s intervals led to permanently higher conductance. These two responses mimic the short-term plasticity and long-term potentiality in biological synapses. In the most widely accepted 'multistore' model of memory in human psychology, new information is stored briefly as a sensory memory. Rehearsal converts short-term memory to long-term. When demonstrating memorization of the numerals '1' and '2' in a 7 x 7 inorganic synapse array, the behaviour of the artificial synapse indicated 'multistore' memory rather than a conventional switch.

The researchers add, "The data indicate that we may apply a psychological memory model simultaneously with the emulation of biological synaptic-like behaviour."

Worldwide counterfeit control directory

A LITTLE more than nine months ago, the Semiconductor Industry Association (SIA) and Rochester Electronics created an online resource to counteract the growing problem of counterfeit and substandard semiconductors entering the global marketplace. The Electronics Authorized Directory is a free, worldwide directory of original semiconductor manufacturers and their authorized distributors. Buyers can access this list to make sure they are buying from vendors who can ensure traceability and authenticity of components, thereby eliminating the risk of procuring counterfeit or substandard devices from unauthorized sources. Recently, the Electronics Authorized Directory reached a milestone, now with more than 200 original manufacturers and their relevant authorized distributors listed on the site.

"On February 2, 2011, at the Sixth Global Congress Combating Counterfeiting and Piracy, industry experts stressed the ease of procuring authentic components," said Curt Gerrish, CEO at Rochester Electronics. "As speaker George Kearse, independent consultant to the mail, express, and logistics industries said, 'We are in the age of the one-stop shop.' The Authorized Directory is an important part of this one-stop shop model. The directory not only protects the consumer, but also the industry."

Lonnie Hurst, SIA Chairman, Anti-Counterfeit Task Force explained, "The significant number of listings in this short time frame proves that the Authorized Directory is a necessary tool to help worldwide customers find original and uncompromised components still in production and/or available in authorized distribution. The authorized distribution network delivers semiconductors through a secure supply chain with stringent chain of custody requirements that can prevent counterfeit components from entering the government or customer supply chain. This literal 'who's who' of authorized semiconductor manufacturers and/or distributors is a tool government agencies, businesses, and consumers can use to ensure the products they purchase meet reliability and safety specifications designed into the original product. The SIA Anti-Counterfeit Task Force, Rochester Electronics, and the listed semiconductor manufacturers are providing this service in order to prevent counterfeit, substandard semiconductors from being introduced into the manufacturing process or warranty replacement processes of the major manufacturers that integrate semiconductors around the world.

Our goal is to enable our customers, and their customers, to purchase legitimate products that will meet manufacturer's specifications and will not endanger the health and safety of the public and military end users, or compromise critical infrastructure or mission-critical systems. Purchasing through authorized distribution is one of the key actions customers can take to support our vision of eventually eliminating counterfeit semiconductor components from entering the supply chain."

The Electronics Authorized Directory is an easy-to-use online tool that lists every authorized distributor of a semiconductor according to original manufacturer and country. The Electronics Authorized Directory provides two quick and easy worldwide search tool options to help buyers locate authorized distributors: search by semiconductor manufacturer, or search by part number.

12 inch market to double

SEMICONDUCTOR manufacturing using 12-inch (300-millimeter) wafers will see production nearly double from 2010 to 2015 as chip producers increasingly employ them for older, more mature products, according to the IHS iSuppli. By 2015, foundries and integrated device manufacturers (IDM) will produce 8,753 million square inches of silicon on 12-inch wafers, up from 4,799.4 million in 2010, equivalent to a compound annual growth rate (CAGR) of 12.8 percent during the five-year period. This year alone, IDMs will produce some 5,608.5 million square inches of silicon on 12-inch wafers.

For semiconductor makers using mature technologies, high-volume 12-inch wafer manufacturing is the key to success. But as this ramps up, the prospect of moving to the next level—the 18-inch wafer—now is being raised, following discussions during the past few years among key suppliers about a potential transition.

From a wafer manufacturer's perspective, the transition to 18-inch represents the most logical approach to achieve the cost reductions necessary to stay on track with Moore's Law, which stipulates that the number of transistors that can be placed inexpensively on an integrated circuit doubles every two years.

Nonetheless, major questions remain regarding the benefits and costs of adopting the next-generation wafer size. For instance, it's still unknown if semiconductor manufacturers, tool suppliers and silicon suppliers can profit from 18-inch wafers—all signs point otherwise.

Yet this doesn't mean that some of the leading companies won't undertake the transition, which IHS anticipates will begin in 2015 regardless of the economics involved. Already, several industry leaders are building facilities in preparation for alpha tool installation.

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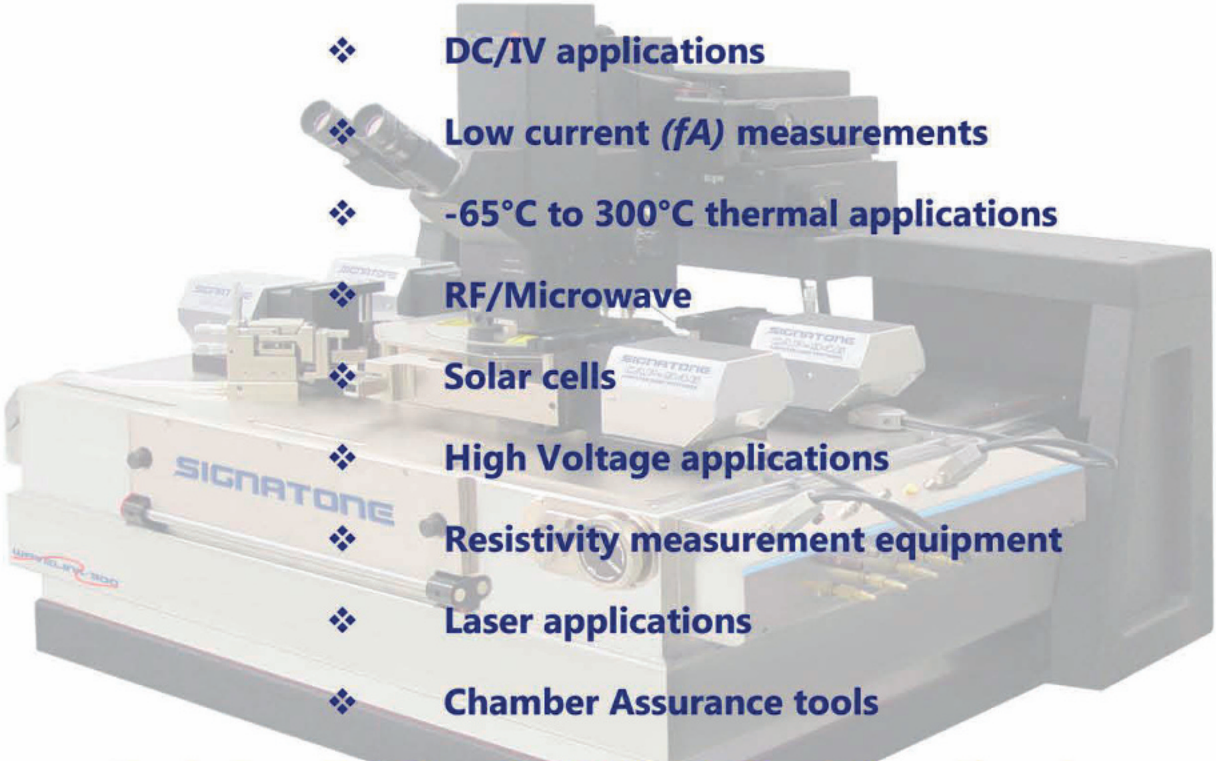

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IHS predicts gloomy DRAM returns

A DRAMATIC oversupply and freefalling prices are in store during the third quarter for the dynamic random access memory (DRAM) space, resulting in a turbulent second half for besieged DRAM suppliers, according to a new IHS iSuppli DRAM Market Brief from information and analysis provider IHS.

The average selling price for Double Data Rate 3 (DDR) in the 2-gigabit (Gb) density—the bellwether DRAM product—is projected to drop to $1.60 in the third quarter, down 24 percent from $2.10 in the second quarter. The dive would be the biggest decline for the year, following a surprisingly solid second quarter during which pricing fell only 5 percent from the first quarter, as shown in the figure below. Moving into the fourth quarter, the price could plummet another 22 percent to $1.25—dangerously close to cash costs for many manufacturers. Only a year ago in the third quarter, pricing stood at $4.70.

"Contrary to typical seasonal patterns in which prices are very soft during the second quarter, that period this year saw relatively flat, unchanged DRAM pricing compared to the first quarter," said Mike Howard, principal analyst, DRAM and memory, at IHS. "However, companies did not capitalize on the healthy pricing levels to increase shipments in the second quarter—which, in retrospect, may have been the best time to do so."

DRAM manufacturers attribute the low growth in shipments in the second quarter to two primary reasons: bloated inventory and challenges in transitioning to new process technologies.

Taiwanese-based Nanya Technology Corp., for instance, had as much as 30 days of inventory when it started to throttle shipments, reflecting its challenges in getting material from factories into the hands of customers. For its part, South Korean Hynix Semiconductor Inc. indicated it suffered poor yields at the 38-nanometer process node, the result of ramping up to a new process. And in the case of Idaho-based Micron Technology Inc., a large disparity between spot and contract prices in May—the company's final fiscal month for the third quarter—prompted the firm to build inventory instead of selling into the spot market.

Nonetheless, if trends in the past are any indicator, DRAM companies not only will shift inventory rapidly but also will move quickly up the yield curve. As a result, the events of the second quarter won't continue for long this year.

"The third quarter is shaping up to be pretty bloody for DRAM makers," Howard noted. "The combination of inventory reductions by DRAM makers and more bits coming out of the fabs is resulting in a very soft pricing environment."

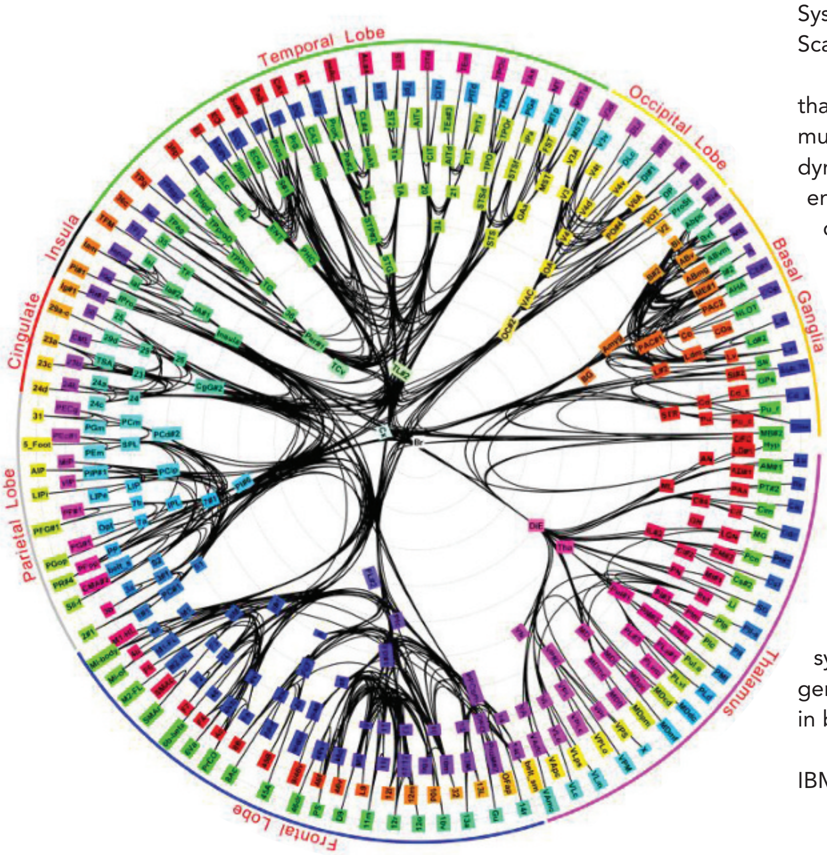
As much as a 15.9 percent increase in shipments is anticipated in the third quarter, and prices are not expected to firm up anytime soon because of that, IHS believes.

IBM unveils cognitive computing chips

IBM researchers have unveiled a new generation of experimental computer chips designed to emulate the brain's abilities for perception, action and cognition. The technology could yield many orders of magnitude less power consumption and space than used in today's computers.

In a sharp departure from traditional concepts in designing and building computers, IBM's first neurosynaptic computing chips recreate the phenomena between spiking neurons and synapses in biological systems, such as the brain, through advanced algorithms and silicon circuitry. Its first two prototype chips have already been fabricated and are currently undergoing testing.

Called cognitive computers, systems built with these chips won't be programmed the same way traditional computers are today. Rather, cognitive computers are expected to learn through experiences, find correlations, create hypotheses, and remember, and learn from, the outcomes, mimicking the brains structural and synaptic plasticity.



To do this, IBM is combining principles from nanoscience, neuroscience and supercomputing as part of a multi-year cognitive computing initiative. The company and its university collaborators also announced they have been awarded approximately $21 million in new funding from the Defence Advanced Research Projects Agency (DARPA) for Phase 2 of the Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) project.

The goal of SyNAPSE is to create a system that not only analyses complex information from multiple sensory modalities at once, but also dynamically rewires itself as it interacts with its environment – all while rivalling the brain's compact size and low power usage. The IBM team has already successfully completed Phases 0 and 1.

"This is a major initiative to move beyond the von Neumann paradigm that has been ruling computer architecture for more than half a century," said Dharmendra Modha, project leader for IBM Research. "Future applications of computing will increasingly demand functionality that is not efficiently delivered by the traditional architecture. These chips are another significant step in the evolution of computers from calculators to learning systems, signalling the beginning of a new generation of computers and their applications in business, science and government."

While they contain no biological elements, IBM's first cognitive computing prototype chips use digital silicon circuits inspired by neurobiology to make up what is referred to as a "neurosynaptic core" with integrated memory (replicated synapses), computation (replicated neurons) and communication (replicated axons).

IBM has two working prototype designs. Both cores were fabricated in 45 nm SOI-CMOS and contain 256 neurons. One core contains 262,144 programmable synapses and the other contains 65,536 learning synapses. The IBM team has successfully demonstrated simple applications like navigation, machine vision, pattern recognition, associative memory and classification.

IBM's overarching cognitive computing architecture is an on-chip network of light-weight cores, creating a single integrated system of hardware and software. This architecture represents a critical shift away from traditional von Neumann computing to a potentially more power-efficient architecture that has no set programming, integrates memory with processor, and mimics the brain's event-driven, distributed and parallel processing.

IBM's long-term goal is to build a chip system with ten billion neurons and hundred trillion synapses, while consuming merely one kilowatt of power and occupying less than two litres of volume.

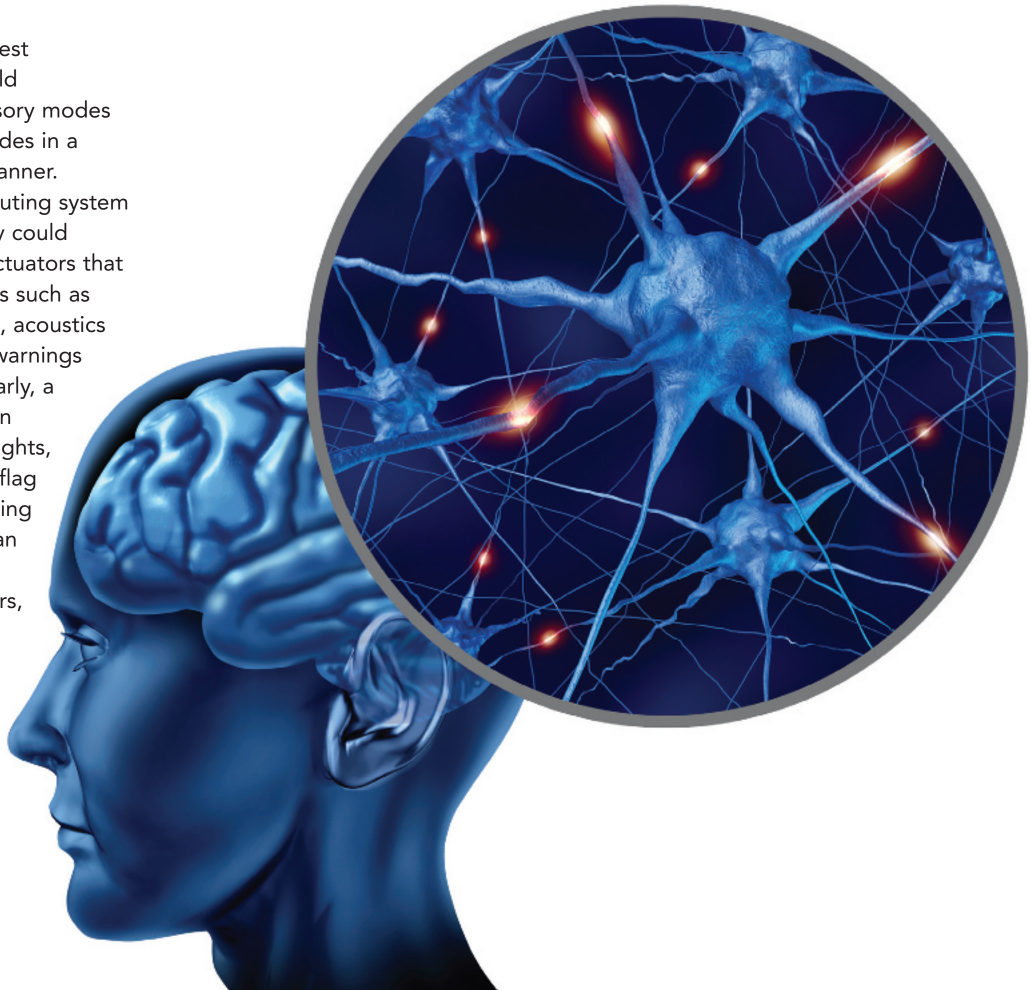
Future chips will be able to ingest information from complex, real-world environments through multiple sensory modes and act through multiple motor modes in a coordinated, context-dependent manner.

For example, a cognitive computing system monitoring the world's water supply could contain a network of sensors and actuators that constantly record and report metrics such as temperature, pressure, wave height, acoustics and ocean tide, and issue tsunami warnings based on its decision making. Similarly, a grocer stocking shelves could use an instrumented glove that monitors sights, smells, texture and temperature to flag bad or contaminated produce. Making sense of real-time input flowing at an ever-dizzying rate would be a Herculean task for today's computers, but would be natural for a brain-inspired system.

"Imagine traffic lights that can integrate sights, sounds and smells and flag unsafe intersections before disaster happens or imagine cognitive co-processors that turn servers, laptops, tablets, and phones into machines that can interact better with their environments," said Dr. Modha.

For Phase 2 of SyNAPSE, IBM has assembled a world-class multi-dimensional team of researchers and collaborators to achieve these ambitious goals. The team includes Columbia University; Cornell University; University of California, Merced; and University of Wisconsin, Madison.

IBM has a rich history in the area of artificial intelligence research going all the way back to 1956 when IBM performed the world's first large-scale (512 neuron) cortical simulation. Most recently, IBM Research scientists created Watson, an analytical computing system that specializes in understanding natural human language and provides specific answers to complex questions at rapid speeds. Watson represents a tremendous breakthrough in computers understanding natural language, "real language" that is not specially designed or encoded just for computers, but language that humans use to naturally capture and communicate knowledge.



Living in a material world

Manufacturers face a dilemma with the key to future technology laying with materials and their reticence to introduce new materials into their processes. **Dr. Geoff Irvine, Vice President, Marketing and Business Development and Xiaohong Chen, Market Manager, SAFC Hitech** discuss the importance of partnerships to realise the material possibilities whilst reducing interruption.

Following the challenging economic landscape in 2008 and 2009, 2010 saw positive signs of recovery in the semiconductor market, a trend which has continued in 2011. Materials continue to play a pivotal role in enabling advances in the global microelectronics and technology markets, not only in the silicon semiconductor space, but also in compound semiconductors and rapidly growing adjacent markets, including PV, solar and HBLEDs.

According to Linx Consulting[i] , between 2001 and 2010, the semiconductor materials market more than doubled in size, experiencing strong growth from $20.3 billion to $43 billion, with a CAGR of around 6.5%. The market demand for higher density memory devices has driven a critical need for new materials to enable the continued development of disruptive and novel chip processing technologies and manufacturing processes. This explosion of growth over the last decade mirrors the change in device scaling from geometrical scaling, which was 'de rigueur' in the three decades leading up to 2000, to the new era of equivalent scaling, expected to remain intact until at least 2014. During the past decade, the materials revolution enabled new processes and device structures that facilitated the continuation of Moore's Law which, in turn, saw the semiconductor industry see substantial growth, from approximately $200bn in 2000 to $304bn in 2010, according to KPMG. We saw a rapid expansion of new materials from the periodic table enabling innovations at the BEOL and FEOL, significant scaling of memory devices and the introduction of new type of semiconductor devices, such as non-volatile memory.

Partners in a material world

In this highly competitive market, the acceptance of new materials and the adoption of new deposition and delivery

techniques have seen intensive research and development continue as semiconductor companies and equipment manufacturers actively seek to tape out the next generation of devices. The scaling of semiconductor devices continues to move to smaller nodes at pace. At its May 2011 Investor Meeting, for example, Intel stated that it expects the 14nm node to be introduced to high volume manufacturing (HVM) in 2014. This type of aggressive timeline brings with it a new set of challenges throughout the supply chain, as the overriding goal is to ensure optimised device performance in ever smaller operating environments.

Challenges such as the increasingly dense packaging solutions required for the multichip modules found at the heart of today's multi-tasking smart devices are essentially making the design rules for these devices or components much more demanding. In addition, the physical limitations of devices and/or the manufacturing method, for example, migrating from CVD to ALD, are also driving the adoption and rate of material changes as integrations become more complex. It is therefore critical that the new materials and processes introduced are significant differentiators that not only improve functionality, but do so as an acceptable cost-benefit proposition.

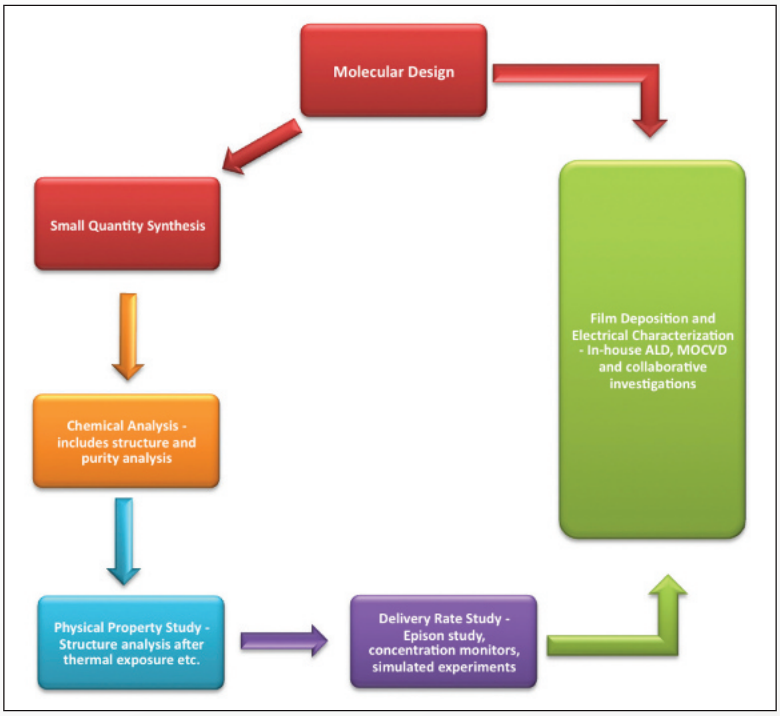
We are now seeing a growing emphasis on key strategic partnerships, with semiconductor manufacturers and tool manufacturers seeking to leverage the specific expertise of materials suppliers as the demand for custom materials solutions, using increasingly specialised materials, grows. From both a design and a manufacturing standpoint, and allied to a continued focus on cost of ownership (COO), deeper collaborations throughout the supply chain reflect the growing importance placed on highly functional device performance and process improvements. R&D, molecular design and test, the transport and delivery to the wafer of often volatile substances, and eventually scale up to HVM, the pooling of expert knowledge is essential if we are to continue to meet the challenges of manufacturing devices that are being custom tailored for integration with specific applications. Figure 1 shows the typical precursor design process undertaken by SAFC Hitech, which increasingly takes place within a deeply collaborative environment.

One of the main challenges facing materials providers is putting in place the most appropriate solution for migrating to new materials and in doing so achieve device performance, control cost of ownership and offer an acceptable price point. Currently, we are looking at around two thirds of the periodic table, if not more, for developing the advanced molecules used in silicon semiconductor manufacturing processes.

We are also looking at new molecules, innovative ways to produce them, new ways to test them, and to develop an understanding of their properties and their behavior on the surfaces where they are laid. This is one of the stages where the expertise of the materials supplier can really pay dividends and contribute to a lower COO.

For example, where we are depositing ZrO_2 film we have the option of using either a liquid or solid precursor. As it is significantly more cost-effective to purify a liquid to achieve the desired purity and quantity than it is to use a solid, engineers developing a ZrO_2 process can leverage the lower simply by using liquid in the vaporisation process. For process engineers, the development of the Zr oxide process using both precursors will essentially be the same. The customer presents the materials supplier with its need, to deposit Zr oxide. The supplier then has

Figure 1: SAFC Hitech's Typical Precursor Development Cycle



a choice of offering liquid or solid. If the process is developed, then the POR (Process of Record) is set.

Taking all of these developments into account, there are significant opportunities for companies that understand these new material operating environments and can provide these materials, specialised chemistries and processes that underpin the ongoing evolution of the semiconductor market.

Making new memories

With the emergence of new memory iterations there are accompanying opportunities for materials suppliers. Ultimately, of course, the success in the marketplace of memory materials will be tied to the types of memory that are in production and dominant in end user devices but, as the drive for increased device performance continues and the pace of materials adoption and precursor development intensifies, the resulting compacted timelines are placing added emphasis on collaborative research and development in the memory space.

The use of high-k layers has enabled the continued shrinkage of CMOS transistors and DRAM capacitors, allowing a larger number of devices per unit area and, in the case of CMOS, the continued following of Moore's law. However, limitations lie ahead very similar to those experienced when silicon-based materials started to reach their threshold. While these high-k materials are currently continuing to move forwards to replace older technologies, in all likelihood they themselves will not be used in their existing forms in, say, 15 to 20 years' time.

As we move beyond the 32nm node, the circuitry in a typical device becomes finer, and at the point DRAM, SRAM and NAND Flash will begin to reach their physical limitations in terms of their continued scaling, becoming increasingly expensive and difficult to manufacture. Critical then is the future integration of materials at the gate level and new material requirements of competing non-volatile memory technologies which are emerging to overcome the scaling limits of current memory technologies. These include PCM and a host of emerging memory iterations being evaluated by collectives such as the ITRS' Emerging Research Devices (ERD) and the Emerging Research Materials (ERM) Working Groups. Figure 2 illustrates the classification of memory technologies, where the prototypical classes are either in play or fairly imminent, with emerging areas being 'ones to watch.'

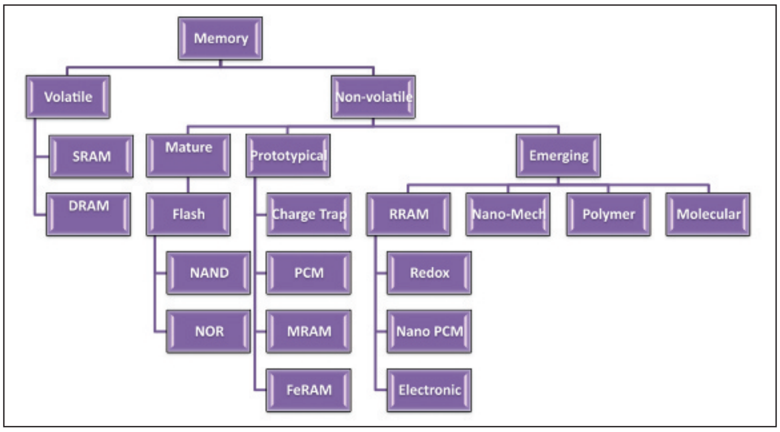
DRAM is not going to become obsolete overnight and, in the short-term at least, its market will remain significant and may even increase as the 32nm node rolls out to mass markets. However, having one eye on the future, as the semiconductor industry invariably does, and looking at the challenges facing DRAM beyond 32nm, there is an onus on manufacturers and materials suppliers to deliver on emerging memory options, processes and product categories through ongoing collaborative Research and Development efforts.

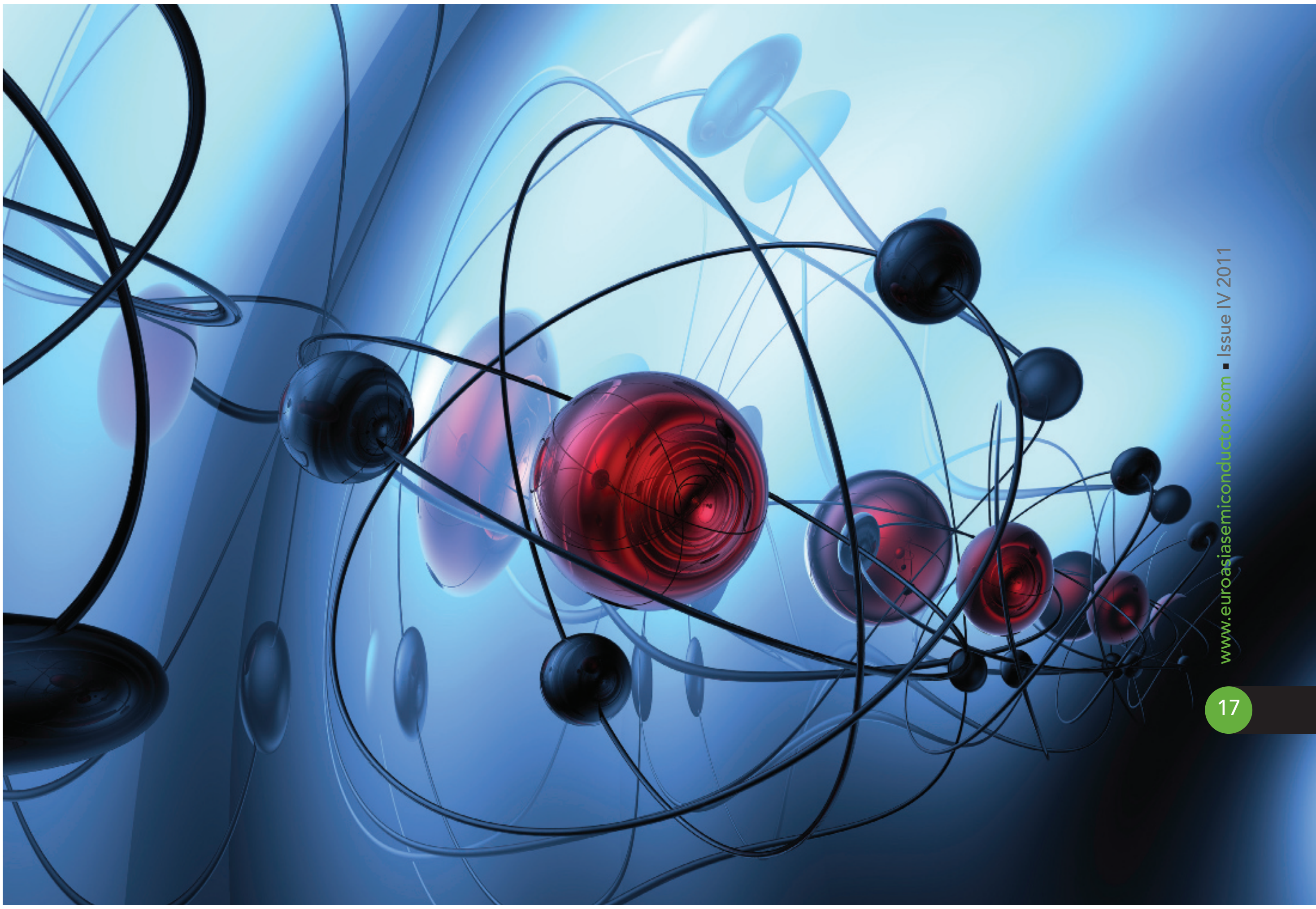
Speaking from a material supplier's perspective, SAFC Hitech has already developed an in-depth understanding of phase-change memory (PCM) and offers a portfolio of molecules developed in-house. As we see these materials moving into the mainstream with customers assessing their feasibility for thin film fabrication processes, we are constantly looking to evaluate what's next in memory. Currently, SAFC Hitech's high k materials are used in high capacitance dielectric layers for DRAM, CMOS, eDRAM and Flash architectures, and its precursors are increasingly being used in additional functional memory layers such as MRAM, ReRAM, FeRAM, and PCM memory architectures.

One of the main drivers of the development of new types of memory is mobile computing and data, which has seen the emergence of 'cloud' based technologies, with core programs not resident on devices but existing instead in vast data farms that can only be accessed via applications through user interfaces. Conventional DRAM memory technologies, which requires the re-writing of data several times per second, and the devices that house them, such as traditional spinning hard drives, are limited for such high volume cloud-based applications, as they consume a great deal of power and generate significant amounts of heat.

A number of technologies are potential

Figure 2: Memory Technology Classifications (courtesy of An Chen, Global Foundries)





contenders to eventually replace the memory architectures that are currently dominant. MRAM, for example, which stores data on thin film elements, is certainly being touted as a replacement for DRAM in certain applications, and although the technology is still being refined to offer the same performance as DRAM, it is already being used in niche applications.

Looking at ReRAM, the list of materials that are potentially viable are largely the same as those used for DRAM and their properties are already well-known, so there is an opportunity of assessing the suitability of already developed molecules than having to start from scratch to invent brand new ones.

Making use of chalcogenide glass, PCM works in ways similar to that of rewritable CDs or DVDs and has emerged as a more than a credible substitute for NAND. PCM manufacturers have claimed that it can be used not only as a significantly superior substitute for Flash memory but as a substitute for current DRAM applications as well.

Enabling the manufacturing of new types of memory presents its own set of significant challenges. MRAM, for example, uses new metal oxides and magnetic resistive layers, so materials suppliers are developing new chemistries that will remove residues from the manufacturing process without causing damage to the layers.

On the horizon?

At some point, it will be physically impossible to continue along the trajectory of Moore's Law. Many researchers are already looking beyond this horizon at new developments that could well take us beyond Moore's Law.

Referencing the ITRS' ERD and ERM Working Groups, in 2010 they assessed the potential and maturity of eight emerging research technologies and set certain parameters on which each technology would be assessed for future development, stating that "to be considered for increased focus, the

Making use of chalcogenide glass, PCM works in ways similar to that of rewritable CDs or DVDs and has emerged as a more than a credible substitute for NAND. PCM manufacturers have claimed that it can be used not only a significantly superior form of Flash memory but as a substitute for DRAM

memory technology needs to have demonstrated good performance with an understood storage mechanism and be scalable multiple generations beyond the 16nm technology generation.

"Further, it should be ready for manufacturing within the next five to 10 years… Following review and discussion, the ERD and ERM Work Groups recommended… that (Spintronics) STT-MRAM and Redox RAM receive additional focus in research and development to accelerate progress toward commercialization of one or both of these technologies.[ii]"

Spintronics, spin-transfer torque random access memory, or STT-RAM, offers lower power consumption and significantly improved scalability. Research into this technology, which has the potential to enable MRAM devices that combine low energy usage, significant device performance and reduce cost, has ramped up in the five or six years.

As work goes on to develop this technology, companies such as Hynix and Samsung (who purchased Grandis, one of the leaders in this industry sector, in August 2011), are committing resources to developmental work, although there are several challenges to overcome before this technology might be ready for commercial roll-out.

In terms of materials suitable for use in the development of STT-RAM, indium oxide, dosed with a small amount of chromium added to make it magnetic, is one potentially viable option. Other materials that could be considered include zinc and titanium oxides.

Redox-RAM is the term used for a wide variety of Metal Insulator Metal structures that share reduction/oxidation (redox) electrochemistry as central to changing their resistance state from low to high, or vice versa.

These technologies also offer significant benefits, such as excellent potential for scaling below 10nm, extremely fast read and write cycles (ideal for memory applications), low current usage, compatibility with existing CMOS materials and processes. However, a reliability model remains elusive, so work is again ongoing to fully evaluate this technology as a viable future option in the memory space.

Conclusion

"The only constant is change" wrote Heraclitus in 470BC. Today he would probably have worked in the semiconductor industry. The past decade has seen significant evolution within the semiconductor industry at both the materials level and in terms of the development of memory and in particular non-volatile memory devices. Device scaling continues to decrease while the demands put on these devices is increasing.

As a result, the materials used assume greater importance as performance enablers, presenting significant opportunities for electronic materials manufacturers, particularly relating to the areas of custom R&D and specialized molecule design.

To meet the challenges of moving to successive technology nodes while maintaining performance, optimising processes and controlling cost, we are seeing the ongoing development and importance of strategic collaborations throughout the supply chain. Hitting the performance/cost sweet spot remains one of the major challenges facing companies at the leading edge of electronic materials. To that end, materials suppliers must keep pace with a demanding business environment that calls for shorter times to HVM.

In terms of memory, manufacturers are looking beyond existing solutions and are weighing up viable alternatives, both in terms of technologies and materials that will enable continued shrinkage yet deliver the optimal performance required, not only by today's complex end user devices but by the applications that run on these platforms.

Looking beyond Moore's Law, it will be interesting to see if the challenges posed by technologies such as STT-RAM and Redox-RAM can be solved in an acceptable to all fashion that could herald the start of a new phase in microelectronics.

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1. 'Emerging Materials in Advanced Devices' - SMC 2011 - Mike Corbett, Linx Consulting

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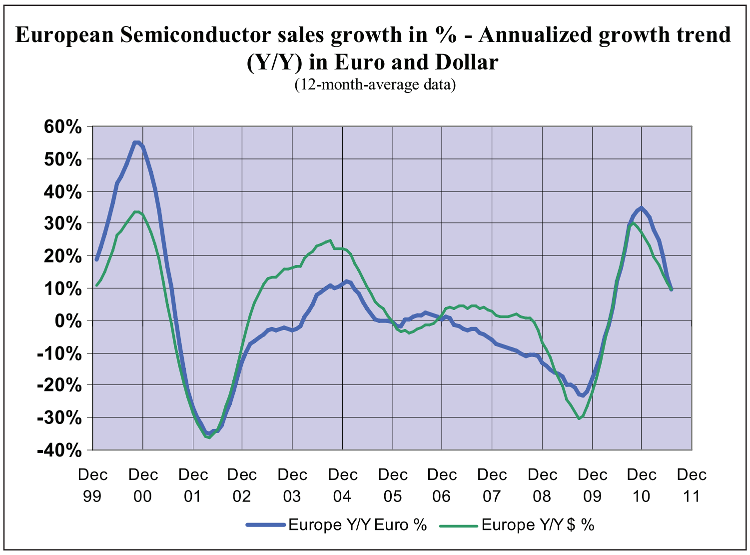
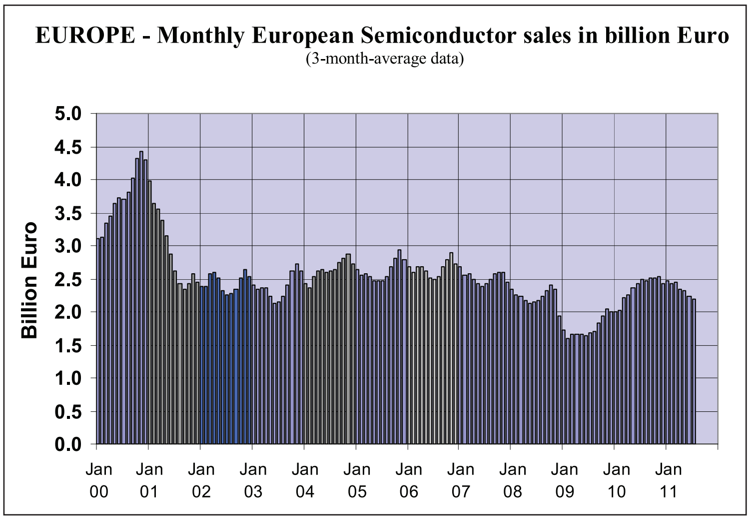
European stability

The most recent figures from the European Semiconductor Industry Association (ESIA) shows that European semiconductor sales are stable year-over-year





Sales on the European Semiconductor market were rather stable year-over-year in July, increasing at a growth rate of 0.7% compared to the same month last year, the World Semiconductor Trade Statistics (WSTS) reported yesterday. On a month-over-month basis, European sales decreased by 2.4 %.

All monthly sales numbers represent a three month moving average. Looking at specific product categories, total MOS micro - covering MOS microprocessor, MOS microcontroller and digital signal processors - showed positive growth in July.

Total logic also performed well, with in particular MOS logic ICs used for consumer equipment, for computers and for communications applications showing good growth rates.

Overall, European semiconductor sales in July 2011 amounted to US$ 3.131 billion. On a YTD basis semiconductor sales increased by 5.3% compared to the same period in the year 2010.

The exchange rate of the Euro compared to the US dollar has somewhat reduced its impact on the European sales picture in the last month. Measured in Euro, semiconductor sales were 2.138 billion Euros in July 2011, down 2.2% on the previous month and down 12.2% compared to the same month a year ago.

On a worldwide basis, semiconductor sales in July 2011 were US$ 24.850 billion, down 0.1% versus the previous month. This results in a decrease of 1.1% versus the same month in 2010.

All information kindly supplied by EECA-ESIA

Market data by region[1]

Market data for the 3 month moving average ending:								
Region	sales (in billions)		Month on Month growth		Year on Year growth		YTD growth	
	Jun 11	Jul 11	Jun 11	Jul 11	Jun 11	Jul 11	Jun 11	Jul 11
in $:								
Europe	3.210	3.131	-2.4%	-2.4%	4.1%	0.7%	6.5%	5.3%
Americas	4.702	4.636	1.6%	-1.4%	3.0%	-2.0%	10.5%	8.0%
Japan	3.305	3.467	-1.1%	4.9%	-11.8%	-10.3%	-6.2%	-7.4%
Asia Pacific	13.667	13.615	-2.3%	-0.4%	1.9%	1.5%	4.9%	4.1%
of which China	5.440	5.400	-1.5%	-0.7%	2.3%	0.5%	6.5%	5.2%
World	**24.883**	**24.850**	**-1.4%**	**-0.1%**	**0.3%**	**-1.1%**	**4.4%**	**3.2%**
In EURO:								
Europe	2.231	2.183	-3.4%	-2.2%	-8.0%	-12.2%	0.7%	-1.3%
Rate ($/Euro)	1.438	1.430	17.8%	12.2%	< Euro against $ versus prev. Year			

1) Unless otherwise indicated, all figures are 3-month-average data except YTD growth which is based on current month data.

Wireless wafer-like vibration sensor for diffusion furnaces

When a manufacturer has yield problems sometimes finding the cause can be as challenging as the solution. **Allyn Jackson, Field Application Engineer at CyberOptics Semiconductor** discusses how a wireless wafer-like vibration sensor helped a diffusion furnace team identify vibration sources and subsequently increase their yield.

A 200mm fab diffusion furnace group with a total of 13 tools was fighting low wafer yield for months. While some tools performed to standard, others were missing the mark, with four tools in particular experiencing low yields due to the following problems:

- Random broken wafers
- Scratched wafers
- Abnormally high wafer defect rates downstream
- Excessive particle counts

To resolve these issues, the diffusion team initially conducted various trouble shooting steps such as parts replacement, complicated and time-consuming partitioned particle checks, and various tool parameter adjustments. These randomly conducted, trial-and-error efforts, however, provided unverifiable or inconsistent results that contributed little to finding the primary cause of tool yield issues.

Next, the team sought to test a theory that differing and/or indiscriminate vibrations and/or misaligned tools for wafer handling leveling were affecting performance with some tools. Traditional wafer vibration and level test methods such as attaching wired accelerometers to wafers or running dummy wafers through a tool and listening with stethoscopes for abnormal noises proved difficult, inconsistent and ultimately inaccurate as such crude methods are not repeatable. The diffusion team wanted a more accurate, comprehensive and repeatable test method that could assess the whole tool while providing reliable data to quantify results with the ultimate goal of documenting and incorporating new maintenance procedures to prevent such problems in the future.

A wireless, wafer-like vibration sensor offered the capability to travel through tools to monitor three-axis accelerations and vibrations and transmit real-time vibration exposure data for analysis. By filtering out acceptable vibration frequencies produced by regular, slow-moving equipment or high-frequency noises between 1 to 200 Hz, the sensor could help identify vibration anomalies during wafer processing.

As the sensor operates in unison with its own vibration monitoring software, data could be viewed and manipulated to identify problems and predict equipment failures to improve process yield and cycle times.

Diffusion tool characterization goals

The fab chose to use the auto vibration sensor with an auto levelling sensor to characterize all 13 of its tools to determine if wafer handling and excessive vibrations were a contributing factor to these yield issues. A comprehensive test plan was formulated with the following primary goals:

- Establish a baseline levelling standard for all wafer transport or process positions in the tool. Of particular note were wafer

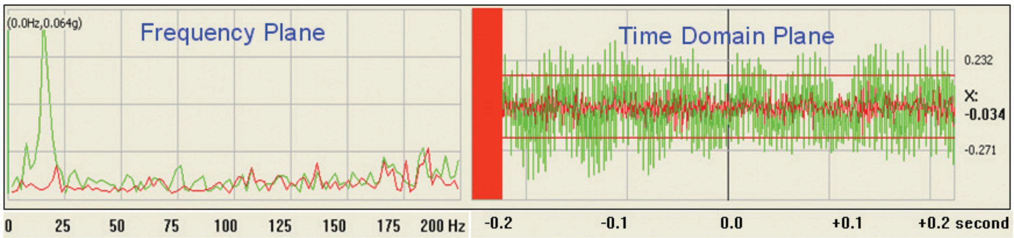


Figure 1

handling, storage cassettes and the setups inside the vertical furnace where access was particularly difficult.

- Identify wafer transport and process locations that do not meet the level standard and those that are level to standard to assure that all wafer handoffs and wafer processing are uniformly administered on all tools.
- Using the highest yield tool as the "golden reference", establish a baseline vibration signature for all wafer movements within the tool and use that baseline signature as a comparison reference for all similar moves on all other tools, with particular attention given to the lowest yield tools.
- Test all tools and identify locations where wafer movement does not conform to the established standard for vibration.
- In cases where wafer movements in "test" tools exceed the "reference" signature standards, determine the root cause of that excursion and correct it.
- White-paper or document as Best Known Method the newly established levelling and vibration test standards and schedule the levelling and vibration testing into the all ongoing routine tool PM activities.

Vibration characterization tool

Placed either in standard cassettes, storage cassettes or in wafer boats that typically hold 150 wafers, the wireless vibration sensor moved through the entire diffusion tool, monitoring three-axis accelerations and vibrations at all locations in the tool in which the wafer travelled. Using Bluetooth technology, the wireless sensor provided wireless real-time data on tool vibration as it moved through the process.

With companion software displaying data on a GUI, engineers were able to overlay vibration fingerprints and analyse vibration data. After carefully recording known good tool and using those golden move vibration signatures as a "reference" for all other tools, it was ultimately determined that there was no one specific cause, but rather many cumulative effects that contributed to poor yield in some tools in the diffusion department.

Results

Problem 1: Some robot moves exhibited excessive vibration.

Action: Perform routine maintenance such as lead-screw lubrication or identify and replace failing component.

Example 1 – Red trace reference signature of good wafer movement, green trace test signature: Shown above (Fig 1) are two overlaid vibration signatures of a stage move. Frequency is shown in the left plane and Time Domain on the right. The red trace is the reference signature and the green trace is the test signature. The two red lines and the red bar are the go no/go threshold.

Results show that the stage move on the test tool clearly failed, indicating possible defect sources and required maintenance. Also, note

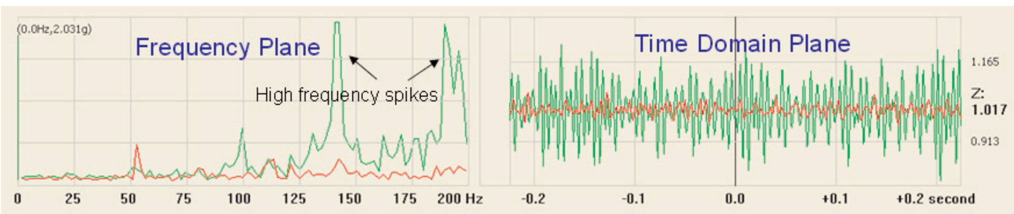


Figure 2

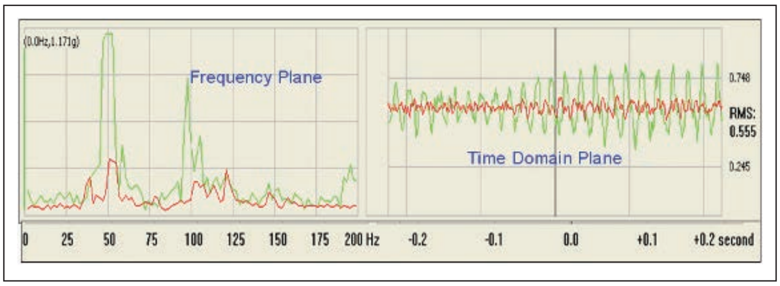


Figure 3

the low frequency spike around 15.6Hz. That is a common indicator of a slower motion source most likely requiring lubrication (failing higher speed components typically have higher frequency spikes).

Problem 2: Miscellaneous vibration sources such as passing carts, the carts themselves and the position of storage cassettes in relation to fans, expose wafers to varying degrees of vibration.

Action: Identify cause of vibration and take corrective action where necessary. For example, tools located close to busy aisles may require extra vibration damping or some tools fans may need to be retrofit with quieter fans.

Example 2 – Red trace tool fans in OFF position; green trace tool fans in ON position:
The effects of systems or events such as fans should not be overlooked when evaluating the total tool for defect causes.

In figure 2 the test signature in red shows Z axis wafer vibration when fans in storage areas fans are OFF. The green trace is the same storage cassette with the fans ON. When the cassettes are not leveled in a tilted back position, as shown in figure 1 above, the risk of “wafer walking” increased (wafers that move can be broken or scratched when the robot retrieves them).

Note that the Time Domain signatures look similar to those in figure 1. However, the Frequency signatures show spikes in the higher frequency range, indicating that the vibration sources originate from faster motions like failing ball-bearings.

Example 3 - Red trace tool not by busy aisle, green trace tool by busy aisle:
Some tools, due to their physical location such as next to a busy aisle with carts continually passing, will be exposed to more vibration than tools further away from busy aisles. In figure 3, the green trace shows a tool next to a high-traffic fab intersection and the red trace is of a tool away from the busy intersection. In this case, the tool next to the intersection was identified as needing additional vibration damping systems.

Results show that the stage move on the test tool clearly failed, indicating possible defect sources and required maintenance

Example 4a: Do the carts transporting wafers to and from the tool need vibration damping? Smooth cart transport to and from tools should not be over looked.

In figure 4a, the X, Y and Z axis as well as the RMS of the three are all displayed. Although the RED vibration-suppressed cart seems to show less vibration than the standard cart, especially in the Y axis, it is good practice to run statistical reports from the raw CSV file data of the vibration wafer outputs at 1000 times per second to quantify the vibration energy exposure.

Example 4b: Quantifying vibration “Test” and “Reference” vibration signatures:

In figure 4b, test and reference signatures shown in example 4a are compared for standard deviation using SPC reports provided with the vibration wafers software application. Although figure 4a visually depicts a general tendency for the enhanced cart (red trace) to be smoother than the standard cart (green trace), by applying statistical reporting to the raw CSV file format output, the actual difference is quantified.

This figure clearly quantifies that the standard deviation of the enhanced cart is measurably less in all three axis than that of the standard cart, thus proving that the vibration-suppressing retrofitted carts do offer greater vibration damping. (The vibration wafer software application comes with many SPC reports for advanced vibration analysis through multiple tests and reference signatures at one time.)

Problem 3: Stocker cassettes were not all leveled when tilted back, resulting in incidents of “wafer walking” caused by tool vibrations.

Action: Level all stocker cassettes tilting back 1mm

Example 5: For a comprehensive program in addressing wafer handling issues associated with excessive vibration, leveling wafer cassettes to established standards should be completed prior to conducting vibration analysis.

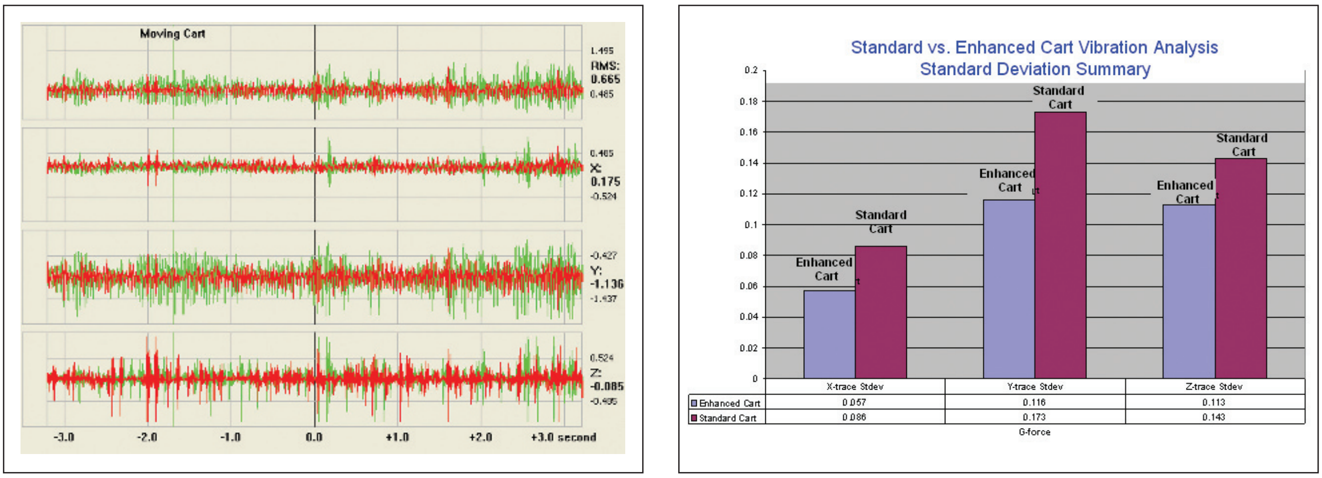


Figure 4a & 4b

Since it is impossible to completely eliminate all vibration in the storage cassettes, optimum inclination is tilted back 1mm to reduce "wafer walking". As the position of storage cassettes is often not an upright position when retrieved by the robot, it is important that levels are accurate. In this scenario, an auto leveling sensor, similar to the auto vibration sensor, was implemented to monitor level of storage cassettes against a set norm.

Leveling was also performed inside the difficult-to-access vertical furnace to assure that when wafers are being processed at 1000c+ degrees, they are at the proper inclination. Figure 5 shows that optimally levelled stockers, levelled with an automatice levelling system tilt back 1 degree to prevent 'wafer walking'.

Auto vibration sensor set new standards for vibration detection

Whenever a wafer is moved or something within the vicinity of the wafer moves, resulting vibrations can be a potential cause of defects. Typically only a few of the common sources of wafer vibrations such as robot arm bearings or lead-screw lubrication are investigated.

When comparing tools that should have identical yields, but one or more tools have abnormally high defects, investigation of the entire wafer path is key to quantify the full range of conditions to which the wafer is exposed.

The diffusion team did just that using the auto vibration sensor (AVS). Once the AVS identified multiple wafer defect causes that were previously overlooked or undetected, engineers at the 200 mm fab conducted a number of corrective actions that included:

- Routine maintenance such as lubrication, which was previously overlooked
- Replacement of failing or substandard parts before yield impact
- Service sub-par sub-systems such as noisy fans
- Where necessary, implement vibration damping systems such as on push-carts or tools near busy traffic areas
- Optimally level storage cassettes to reduce "wafer walking" and mishandling.
- Revise standard procedures to reduce wafer vibration where excessive vibration was identified
- Document new vibration and levelling wafer procedures for implementation into all future routine diffusion tool PMs

The AVS' data logging capabilities also allowed the fab to establish new preventative maintenance requirements and process control standards for both the tools and engineers that are now a part of Best Know Methods in preventive maintenance of tools. As a result, all 13 tools are providing yield at acceptable levels, including the four that were at sub-par levels.

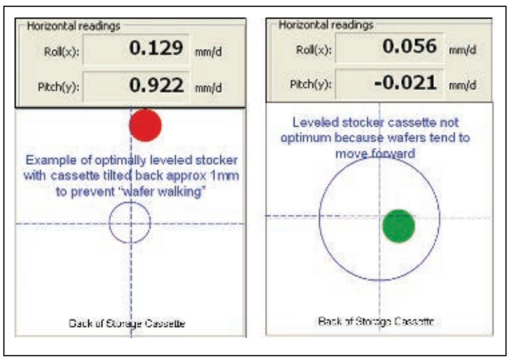
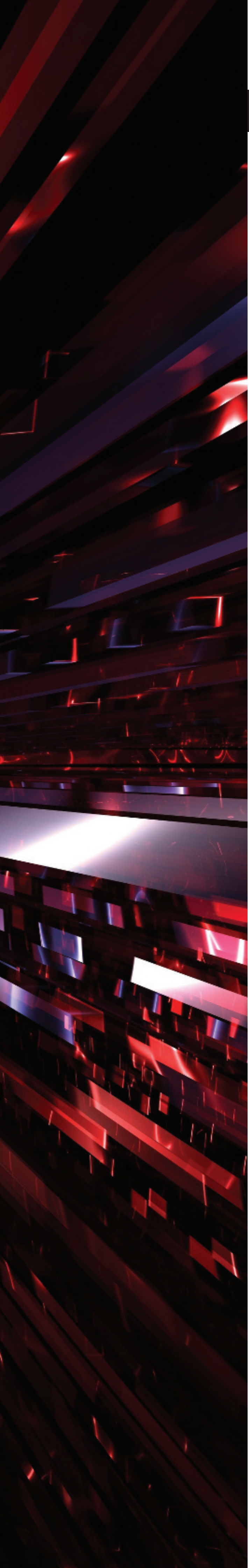


Figure 5



Broad spectrum analysis

Keithley Instruments recently launched an electrical characterization tool that provides a broad spectrum of applications across semiconductor manufacturing. David Ridsdale spoke to **Keithley's marketing director, Mark Cejer,** about the capability and application of the new tool.

Q Keithley has introduced a new tester for high end semiconductor activities such as LEDs, interconnects and high power semiconductors. Testing is an important part of manufacturing but many manufacturers see it as an annoying additive. However, an increasing complexity and lack of visual ability has seen such testing become more important. Do you think testing has moved from an added value to an enabling process for future needs?

A It's long past time for device manufacturers to start thinking about test as much more than "a necessary evil." The growing demand for higher efficiency semiconductors is driven in part by the push for more energy-efficient devices. One of the goals for end products that employ lots of power semiconductors, such as power supplies for servers, for example, must be reducing their energy consumption. When the power supply is in standby/off mode, leaky semiconductors in the inputs will waste a lot of electricity, especially when that leakage is multiplied by the number of power supplies in a big server farm. To improve energy efficiency, IC manufacturers are constantly exploring ways to create more efficient silicon devices, as well as those based on compound semiconductors like silicon carbide and gallium nitride, which are inherently more efficient than silicon. All of that means greater testing challenges: "more efficient" means materials and devices that are less leaky, "less leaky" means IC makers need to be able to characterize ever-lower leakage currents, which is especially challenging in production. Older instrumentation, designed for characterizing relatively leaky silicon, typically just is not up to the challenge. The ability to characterize power semiconductors with pulsed measurements is also critical to ensuring accuracy because pulsed measurements let you test using high current levels without creating the self-heating problems that would occur if you were sourcing high DC currents.

High brightness light emitting diodes (HBLEDs) also present some critical testing challenges. These devices are increasingly in demand for use in applications like backlighting displays, automotive headlamps, solid-state lighting that goes on buildings, and dozens of others. For these types of applications, the color of the light they output must be highly consistent from device to device because they're typically packaged with multiple LEDs in a module and multiple modules in a single end product. Any significant color variation is immediately obvious and would be unacceptable to the consumer. Ensuring high color consistency requires the ability to test these devices with extreme accuracy. Here, too, high throughput pulse testing is essential because HBLEDs are very susceptible to self-heating, which will affect the color of the light they output. And, of course, in production, test throughput is equally critical. And those are the big issues the Model 2651A High Power System SourceMeter instrument was designed to address.

Q Many companies highlight the generic capacities of their tools but with this tool Keithley have focused on the specialities. What motivates such a decision and what advantages does it provide the manufacturer?

A For some of our customers, all we have to say is "We've got a terrific new 50A SMU" and they'll know exactly how to use it in their applications. But for the rest, we feel that test vendors have a big responsibility to their customers to help them choose and use their products effectively. You're right—this product is designed to address a specific set of applications—but it's undoubtedly the fastest growing area of the semiconductor industry. Power semiconductors are used throughout more industries every year: in the auto industry for hybrid and electric vehicles, electric grid applications, solar and wind power generation, power supplies for PCs and consumer electronics, and many more. Just about every segment of the electronics industry and their downstream customers are using power semiconductors and HBLEDs in some way. And we want to serve all of them.

Q The three market areas this tool focuses on are all areas of the industry that are tipped to grow with mainstream lighting for LEDs, the growing needs for high power semiconductors and increasing complexity of interconnects. What sort of growth expectations does Keithley have for these markets?

A Industry analysts have indicated that the market segments we're targeting seem likely to produce double-digit growth over the next five years, so they are obviously growing significantly faster than other segments of the semiconductor industry. For example, a 2010 report from Lux

Research predicted that solar installations will rise at a compound annual growth rate of 23 percent between 2010 and 2015. Similarly, Global Industry Analysts have indicated that wind farm capacity will grow at 29 percent CAGR over the same period. JD Power and Associates is anticipating that the hybrid/electric cars market will grow by 27 percent CAGR from 2009 to 2015. The power semiconductors market is set to grow by 11 percent CAGR and LEDs by 16 percent. So it's pretty obvious that all the industries that depend on these components are poised to keep growing.

Q Test has become an increasing part of the manufacturing process but also an increasing part of the cost. In industries where margins are tight how does this tool help manufacturers? When they see specific tool requirements they assume that the cost will also be higher?

A Until recently, manufacturers of power semiconductors had to rely on what we call "big-iron" ATE functional testers. And those systems were pretty expensive—typically hundreds of thousands of dollars each. Even more important, those systems aren't really optimized to characterize modern power semiconductor materials and devices with their lower leakage currents and higher power levels. In contrast, the Model 2651A is designed for exactly those characterization challenges and costs about one-tenth as much. From a production test perspective, it not only lowers the cost of ownership dramatically but provides higher accuracy, better quality measurements without a loss of throughput. That's because the combination of the Test Script Processor (TSP®) embedded in the Model 2651A and the TSP-Link® virtual backplane that system integrators can use to link multiple instruments together makes it easy to scale a system as large as they need while ensuring high throughput. TSP makes embedded scripting and execution of commands possible, in contrast with line-by-line execution of commands over GPIB as in traditional instrumentation.

Q The area of industry Keithley is targeting crosses some intense research areas as well as the growing production needs. Do you have a strategy that enables cost of ownership at the research section and the ability to transfer to production stage with minimal disruption or added cost?

A Absolutely. The Model 2651A, and in fact, the entire Series 2600A System SourceMeter family, incorporates this strategy. For example, researchers often need to characterize a device very quickly by just taking a few measurements.

Series 2600A instruments have an embedded TSP Express software tool that allows researchers to perform common I-V tests quickly and easily without programming or installing software.

TSP Express, which is LXI compatible, runs from the instrument and is controlled via a web browser running on a PC connected to the instrument via an Ethernet cable. It has an intuitive user interface that resides on the instrument's built-in web page.

A user can just connect a laptop to the instrument with an Ethernet cable, open up a web browser on the laptop, type the instrument's IP address into the browser, and up comes the test application that's embedded in the instrument. And from there, the user can quickly point, click, run any of a number of tests, and download the resulting data to a .csv file or view it in graphical or tabular formats. TSP Express supports both basic and advanced tests, including nested step/sweeps, pulse sweeps, and custom sweeps for device characterization applications.

As useful as this software tool is, this is obviously not the approach for production test applications. For system-level applications, our TSP architecture is designed to simplify building high speed, multi-channel I V test systems of multiple instruments. The on-board microprocessor allows each Series 2600A instrument in the system to run its own test scripts, which can contain any sequence of routines that are executable by conventional programming languages.

That means the instrument can manage an entire test without sending readings back to a PC for decision-making, eliminating the delays caused by GPIB traffic congestion and greatly improving overall test times.

The TSP-Link bus allows system builders to connect multiple Series 2600A and other TSP instruments in a master-slave configuration so they behave as one integrated system. TSP-Link supports up to 32 units or 64 SMU channels per GPIB or IP address, so it's pretty easy to scale a system to match the requirements of an application. We also have built-in 500ns trigger controllers to ensure precise timing and tight channel synchronization of multi-instrument systems.

One of the big advantages of using the same instrument in the lab and on the production floor is measurement correlation. If manufacturing engineers discover a problem on the production floor, they can work with design engineers to track down the source of the problem much faster

Series 2600A instruments also provide a parallel testing capability that allows each instrument in the system to run its own complete test sequence, creating a fully multi-threaded test environment.

That means you can run as many tests in parallel as you have Series 2600A instruments in the system, which can really boost throughput dramatically. And when test requirements change, it's pretty simple to reconfigure a Series 2600A-based system via software without rewiring.

Obviously, one of the big advantages of using the same instrument in the lab and on the production floor is measurement correlation. If manufacturing engineers discover a problem on the production floor, they can work with design engineers to track down the source of the problem much faster, because they can scratch data correlation concerns off their list of "unknowns."

Q What are the key interconnect issues that this testing platform addresses? Can the tester deal with issues such as electromigration and what new perspectives will the manufacturer gain?

A With the ability to source and measure currents as high as 50A and the ability to resolve leakage currents as low as a picoamp, the Model 2651A offers the widest dynamic range of any SMU currently on the market. To make this possible, we put a lot of effort into developing specialized low resistance cabling and connectors to ensure our customers could make low noise measurements on any range. That specialized cabling is included with the product,

so users don't have to worry if their measurements are being compromised by noisy connections.

Q Temperature control at interconnect junctions is of concern for manufacturers of high end products. How does the new platform address the industry needs?

A To minimize the unwanted effects of device self-heating during testing, the Model 2651A supports pulsed measurements. A single Model 2651A can pulse up to 50A; two units can be combined using the TSP-Link bus to pulse up to 100A.

It can capture transient behavior such as changing thermal effects with one-microsecond per point (1MHz) sampling. The width of a sourced pulse can be programmed from 100 microseconds to DC and duty cycles from 1 percent to 100 percent are also programmable.

The Model 2651A provides a digitizing measurement mode that uses 18-bit A/Ds for characterizing transient behavior precisely. A separate integrating measurement mode, based on 22-bit A/Ds, provides the maximum measurement accuracy and repeatability.

For applications like studying the thermal impedance of power diodes and LEDs, characterizing the slope of the measured voltage at the top of the pulse is important. This capability is also useful for characterizing pulse amplitude flatness. The Model 2651A's high speed A/Ds simplify digitizing the top of the pulse accurately when the measurements are made synchronously with the source.

Q What are the key areas of power semiconductors that this platform addresses?

A Perhaps the most significant area is the enhanced efficiency of new materials and the testing challenges that come along with that greater efficiency. "More efficient" means that when the semiconductor is "on," it's really on and when it's "off," it's really off.

Because it is designed to source and measure pulses of up to 50A (or 100A if two are connected together) and measure voltages down to a microvolt, the Model 2651A offers the developers of new materials the ability to characterize the resistance from drain to source when the device is on (RDSon) with high accuracy. At the same time, manufacturers of these new materials are striving to minimize leakage current from drain to source when the device is "off"(IDSoff); with its one-picoamp current measurement resolution, the Model 2651A makes it possible to characterize this parameter with high confidence.

Q Keithley has a long history of test and measurement in the semiconductor and related industries. What are the key issues that Keithley sees facing the industry over the next few years as advanced and multiple device requirements are needed to meet roadmap intentions?

A Obviously, the demand for higher efficiency devices won't be going away. That means that not only will current manufacturers be experimenting with new materials but new companies will enter this segment of the market. Typically, when that happens, to meet the new manpower demands, less experienced people are going to be chasing more complicated technologies.

That obliges Keithley and other test vendors to keep producing products that are as simple as possible to use, so someone doesn't have be a test expert to start using them effectively. It also means we have to stay on top of providing applications support to get these new users up to speed quickly so they can find the products they need to do their jobs more efficiently. High accuracy products alone aren't enough—we have to continue making those products easy for our customers to use.

MARK A. CEJER is a marketing director for Keithley Instruments, Inc., Cleveland, Ohio, which is part of the Tektronix test and measurement portfolio. He joined Keithley in 1991. During his tenure, he has served in a variety of positions, including marketing engineer, product/marketing manager, regional sales manager, and business manager. In his work, he has helped define and launch a number of Keithley's most popular instruments, including many of the company's SourceMeter instruments, digital multimeters (DMMs), and datalogging products.He holds a BSEE from the University of Akron (Akron, Ohio) and an MBA from Case Western Reserve University (Cleveland, Ohio.)

Optimizing beyond expectations

Photolithography advances are continuing to enable high volume manufacturing of sub-22nm node features using argon fluoride (ArF) light sources. With the use of source-mask optimization (SMO), pixellated illumination schemes and computational lithography, the use of 193nm light continues to be extended to finer geometries. The light source contribution includes higher power to enable higher throughput, improved optical performance stability for tighter critical-dimension uniformity (CDU) and reduction of service events to increase system uptime. **Ted Cacouris, Ph.D discusses how Cymer** has been actively pursuing such light source advances on its latest ArF immersion light source, the XLR 600ix.

While Moore's Law continues to guide the semiconductor industry down an increasingly challenging photolithography path, the memory sector needs to accelerate the rate of device shrinkage beyond Moore's Law in order to counteract the rapid decline in average sales price (ASP) for each device node (Fig. 1).

While the technology continues to evolve to meet the requirements for smaller geometries (CD), the lithography tools continue to increase in complexity, driving costs up for outfitting a next-generation fab. Increasingly, the chip manufacturers look for ways to maximize the productivity of the process tools to leverage the growing capital investments. High wafer throughput and yield are the key drivers that enable the cost/bit to maintain pace with the market price pressures.

Process tool trends

Advanced ArF immersion scanners have been developed to continue increasing wafer throughput while improving overlay capability to enable double- and multi-patterning applications. For resolution enhancement, new freeform illumination optics are allowing designers to further extend SMO and push the limits of 193nm light. Newer resists that can achieve finer resolution are being contemplated, but require high exposure doses. These enhancements are further enabled by the light source contributions.

At the basic level, to increase efficiency, higher output power from the light source enables the use of higher exposure doses without compromising scanner throughput. Similarly, higher power can enable faster scanning speeds at the scanner for a given exposure dose, thus providing higher throughput. The Cymer XLR 600ix was designed with the basic premise of flexible power output in mind to deliver higher power when needed.

Excimer laser light sources were introduced for ArF immersion applications at a 60W power level (10mJ @6kHz). This level of power has been sufficient to supply scanners with enough light to operate at wafer throughputs on the order of 150 – 180wph under typical exposure conditions. However, if higher dose resists are used, the throughput may decrease, depending on illumination conditions. Higher power from the light source, therefore, can eliminate this constraint and enable high throughput.

One of the key challenges of delivering higher power from the light source is the availability of optic materials and coatings that can withstand the high energy present within the laser and not have a detrimental impact on component lifetime. Also, higher average power introduces more severe thermal effects, and in particular, thermal transients, when the light source keeps switching on and off as is typical during a wafer exposure sequence. Such thermal transients can affect the stability of the light if the optics and their surrounding components are not sufficiently immune to thermal effects. Through a multi-year development effort, Cymer has been able to introduce new CaF_2 optics and coatings that, combined with a robust architecture, achieve high stability in order to deliver 90W output power while maintaining tight optical performance specifications. The resultant platform, the XLR 600ix, incorporates Power Optics that lead to high stability as well

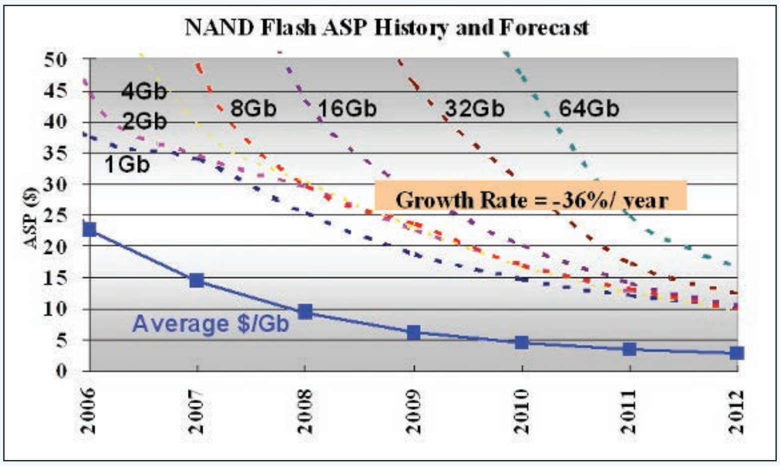


Figure 1 - Average sales price (ASP) of NAND devices over time

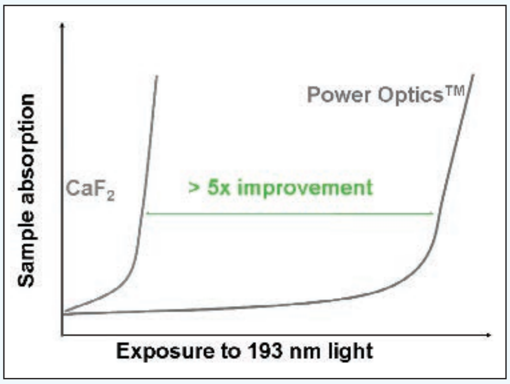


Figure 2 - High performance "Power Optics" tested under very high intensities in an accelerated life test show >5x improvement over conventional optics

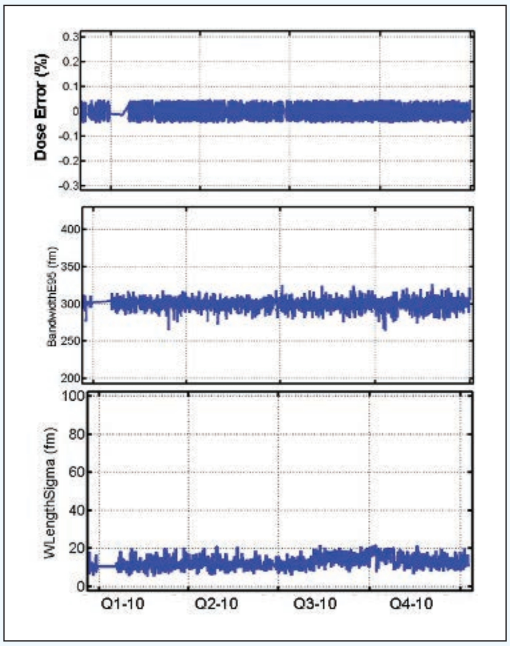


Figure 3 - Field data from a high volume fab showing stable operation over the course of one year while running at 90W power

as long optics life, as proven through accelerated lifetime testing (Fig. 2). Thus, both high performance and high availability can be achieved simultaneously using these new technologies.

Optical performance stability

In addition to a stable system design, key light source optical parameters such as energy, wavelength and bandwidth require sophisticated control systems to ensure consistentcy within wafer and within die CD uniformity. For a typical die, about 300 – 500 pulses of light are used, so the control systems in the light source have to ensure high pulse-to-pulse repeatability.

The control elements include high accuracy and high speed metrology to measure wavelength, bandwidth and energy for every pulse and fast processors and algorithms to drive actuators for closed-loop control. This combination results in very tight dose stability (<0.1%), low bandwidth variability (<30fm) and low wavelength variation (<20fm) under typical operating conditions and high, 90W output power (Fig. 3). Such high stability enables the very good CD uniformity and overlay performance that is required for sub 32nm node devices.

Furthermore, one of the elements that enables higher scanner throughput is the ability to increase scanning speed, which, in turn, results in fewer pulses per scan window (since the laser repetition rate is fixed at 6kHz). High pulse-to-pulse energy stability at high pulse energies enables the use of fewer pulses per scan window, reducing the reliance of pulse averaging that a large number of pulses would provide.

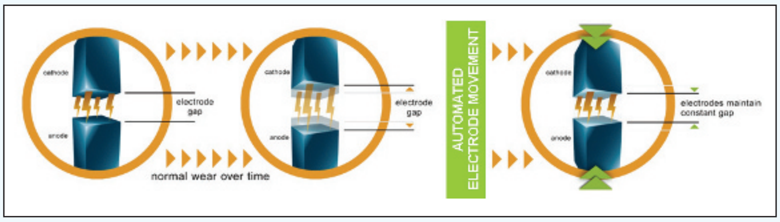


Figure 4 - Constant electrode gap concept introduced to improve discharge chamber performance and reduce frequency of service events

High uptime

While these performance advances improve the system capabilities, it is important to further improve overall system uptime and maximize the wafer productivity to keep the cost per wafer down. To this end, advances in key light source components that reduce the service frequency are equally important. Cymer has developed breakthrough technologies in the laser discharge chamber design that extend the time between service events. One of the key aging mechanisms of a laser discharge chamber is the erosion of the discharge electrodes that lead to a gradual increase in the gap between these electrodes.

Over time, this increasing electrode gap drives the need for a higher voltage to drive a discharge, until the voltage reaches an operating limit. The solution that Cymer implemented involves introducing movable electrodes to maintain a constant electrode gap (Fig. 4). While simple in concept, this solution has been elusive for many years: introducing movable parts in a discharge chamber without impacting other performance properties or system reliability. Maintaining a constant electrode gap has improved performance stability and resulted in fewer service events. This new chamber design has been implemented and field datahas confirmed an increase in system availability (Fig. 5).

Another common service event for excimer lasers is the periodic need to refresh the discharge chamber gas as it slowly degrades over time. Historically, one countermeasure to maintain a stable discharge over time has been to periodically feed new gas into the chamber in small quantities while the laser is firing so as not to interrupt production. This countermeasure has had limitations as gas byproducts from the discharge eventually reach concentrations that are high enough to perturb the system performance.

A gas refill with fresh gas has been necessary to enable continued operation, yet this gas refill requires interrupting production for about 20 minutes. The gas "life" is measured in terms of millions of pulses and for argon fluoride systems has typically been 100 million pulses (Mp) between refills. For reference, a typical wafer requires anywhere from 30,000 to 60,000 pulses to be fully exposed, so a high volume fab can reach 100Mp in as little as 24 hours.

To this end, Cymer has developed advanced gas management technologies to increase the gas life through more precise control algorithms that take into account actual operating conditions and thus reduce the frequency of refills. The first major step was a ten-fold increase in gas life, to 1 billion pulses (Bp) between refills, with a technology named "GLX" (for Gas Life eXtension), thereby reducing the refill frequency from once per day to once every 10 days in a high volume fab.

Further refinements of this technology led to extending it another factor of 2, resulting in a refill frequency of 2Bp. The net time savings over the course of a year has been on the order of more than 100 hours due to minimization of gas refill events. For an ArF immersion scanner running approximately 150 – 180 wafers per hour, this extra uptime has been very significant and has been rapidly adopted by the chipmakers. (Fig. 6) Further developments are under way to continue to reduce the need for refills and provide additional output from the scanner.

Conclusions

In summary, as ArF immersion lithography is extended with techniques that include double or multi-patterning, the role of the light source has increased in providing performance advances as well as reducing running costs to keep pace with chipmaker requirements. In addition to enabling higher power via the XLR 600ix platform, advances in optical performance stability and higher availability have continued to support the demands of high volume production at advanced device nodes.

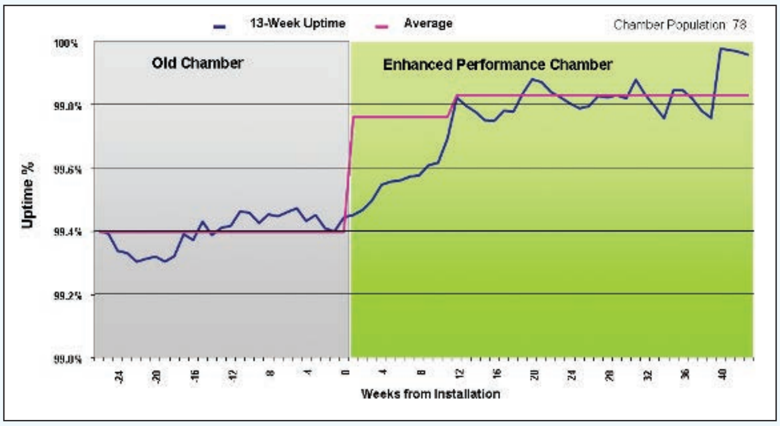


Figure 5 - Uptime improvement as a result of introducing the enhanced performance discharge chamber

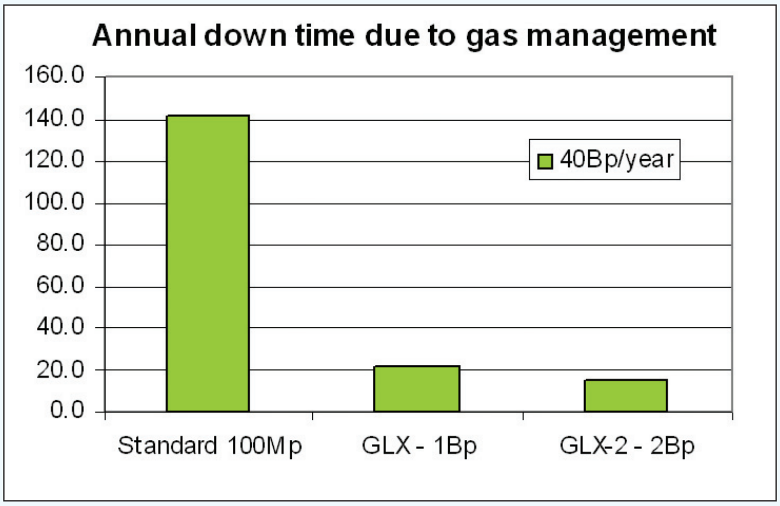


Figure 6. Improvements in gas management technology help reduce the frequency of gas refills and the associated system down time

As ArF immersion lithography is extended with techniques that include double or multi-patterning, the role of the light source has increased in providing performance advances as well as reducing running costs to keep pace with chipmaker requirements

Spectroscopic Ellipsometer SpecEL-2000-UV-VIS-NIR

THE SpecEl-2000-UV-VIS-NIR is a user-friendly, bench-top Thin Film measurement system utilising Spectroscopic Ellipsometry. Ideal for flat, semi-transparent samples such as wafers and glass plates, the Spec-El-2000 is designed to be an affordable, compact and convenient system, featuring simple placement of the sample and one button operation.

Spectroscopic ellipsometry measures relative changes in the phase and amplitude of the light instead of absolute intensity (reflectometry). This technique is therefore independent of any reference measurement and multiple parameters can be determined simultaneously. Measurements of thickness as well as refractive index (n) and absorbance (k) data for the wavelength range 300-1000nm are delivered within 7-13s.

Half the price of standard ellipsometry equipment, the Spec-El-2000-UV-VIS-NIR features an integrated broadband light source, guiding optics, a rotatable polarizer, the sample table, a second rotating polarizer (analyser), further optics and finally a miniaturized spectrometer with a CCD array as a detector. The incidence angle is nominally set to 70°, but can be customer specified to any angle between 65° and or 75°. The desktop footprint is extremely small (52 x 33 x 24cm).

Depending on the layer and substrate material, the SpecEl can detect layer thickness between 1nm and 10µm, and gives values for thickness accurate to 0.1nm. The system comes with a 32-bit Windows PC as standard, complete with powerful software offering a range of modelling possibilities such as Cauchy, OJL, Tauc-Lorentz, Drude, EMA and different types of oscillator. The software also stores specific measurement routines, reducing the tedium of repetitive measurements and easing integration.

The standard beam diameter is 400 – 1200 µm. Further options include reference wafers and 2D mapping accessories, with custom, multi-functional solutions available on request.

Equipment

Automation & Wafer Handling

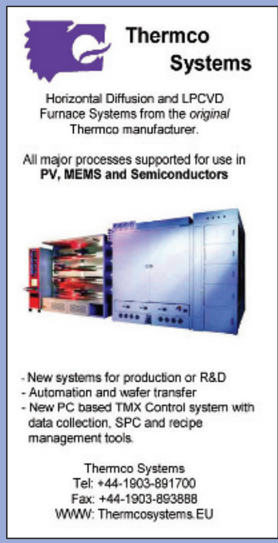
Connection Solutions

Furnaces

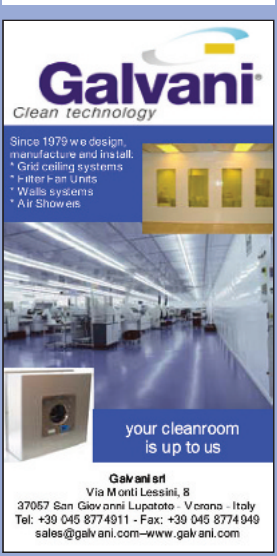
Furnaces

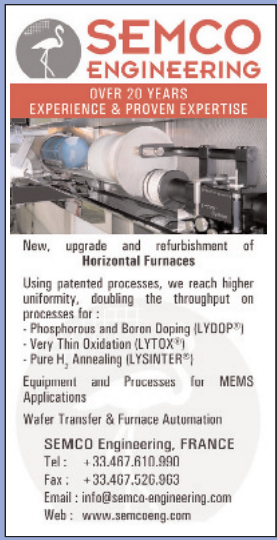
Chemical Pumps

Furnaces



Cleanrooms





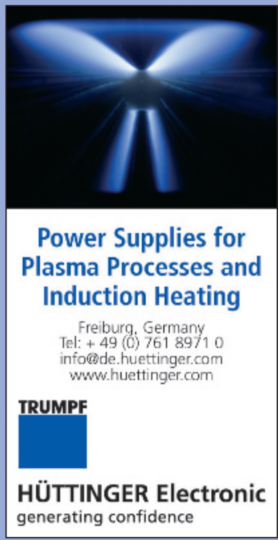
Furnaces Spares

Equipment

Gas Handling & MFC

Megasonic Cleaning Systems

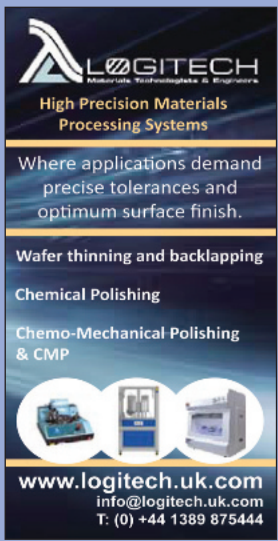
RF-/DC-/MF-Power Supplies

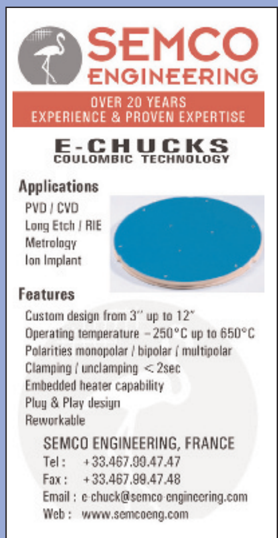


Semiconductor Equipment

Gas (High Purity) Process Control

Materials Processing



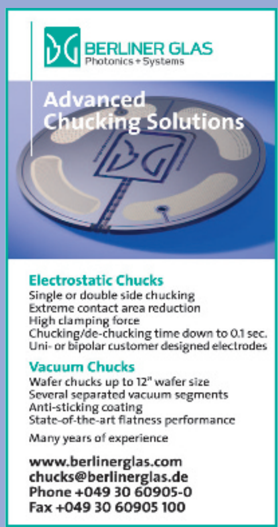


Service & Repair

Glove Boxes

Metrology Systems

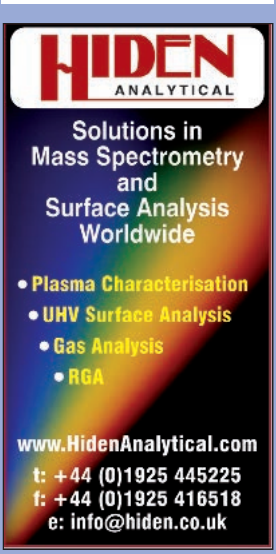
Semiconductor Equipment



Solder Rework

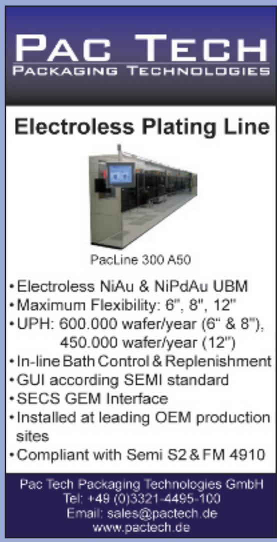
Equipment

Vacuum Equipment

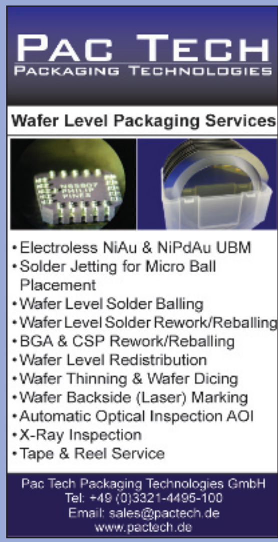


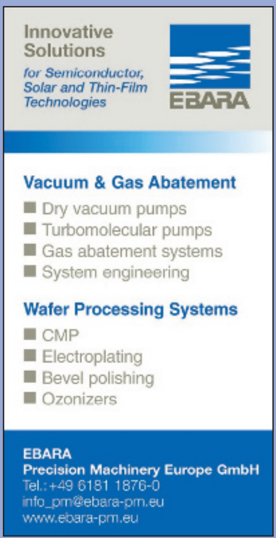
Vacuum Equipment

Wet Benches



Wafer Level Packaging





Valves / Gas Control

Wet Benches

Carbon Based Materials

Wet Benches

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Fabless funding continues

A report from the Global Semiconductor Association (GSA) shows that while semiconductor company funding declined the fabless sector had no such concerns with continued investor interest.

In July 2011, four semiconductor companies raised $81.6 million, down 46.8% from the $153.5 million raised in June 2011. However, funding deals increased 92.9% from the $42.3 million raised in July 2010.

The month-over-month (MoM) decrease was due to a smaller number of companies being funded in July 2011. The significant year-over-year (YoY) increase was largely due to companies in July 2010 not disclosing their deal values and companies reporting higher deal values in July 2011, with Bridge Semiconductor receiving a fifth round of funding valued at $60 million. The number of deals decreased by eight MoM and by three YoY.

In July, fabless companies were the only semiconductor companies funded. This marked the third month in 2011 that an IDM company was not funded. It was the second month that a semiconductor supplier was not funded. Two of the companies funded in July are U.S. based, while one is European and one in Israel.

The rise in public offerings and corporate acquisitions continue to keep a lid on VC investing. "Venture investment has held steady as companies either plot an exit or use creative financing strategies like government grants, corporate leasing or project financing to fuel growth," said Jessica Canning, global research director for Dow Jones VentureSource.

IPO Activity

For the second consecutive month, zero semiconductor companies priced. However, July saw two semiconductor companies file for an initial public offering. Semiconductor and clean energy technology platform company Intermolecular announced that it had filed a registration statement with the SEC for a proposed initial public offering. Morgan Stanley, J.P. Morgan Securities and Barclays Capital will act as joint book-running managers for the offering with Pacific Crest Securities LLC and Needham & Company, LLC as co-managers.

Cirtek Electronics, which has been in business for more than 25 years, provides turnkey solutions that include package design and development for semiconductor devices. BDO Capital and Investment Corp is the underwriter for the offer. This filing marks the second IPO in the Philippines this year.

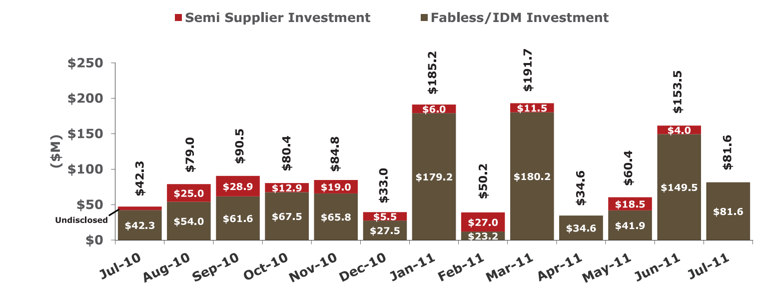
According to findings from Merrill DataSite, the second half of 2011 is expected to be flat or weaker when compared with the first half.

"Increased IPO transaction volume throughout the first half of 2011 is a direct result of increased confidence in our country's economy," said Ed Bifulk, president of the Merrill DataSite virtual data room business at Merrill. "As we move into the second half of the year, however, the number of IPO transactions may decrease, depending upon the economy, as well as the actions of many highly valued Internet companies and investor demand."

M&A Activity

In July 2011, the number of semiconductor mergers and acquisitions (M&As) announced (i.e., M&As of entire fabless, IDM and semiconductor supplier companies, not sectors/product lines or foundry facilities) increased by three MoM and one YoY. The number of deals that included a fabless or IDM company increased by three MoM and remained the same YoY.

The number of semiconductor supplier deals remained the same MoM and increased by one YoY. According to Smith and Associates' MarketWatch Central, the semiconductor and electronics industry is forecast to experience continued revenue growth during 2011, making an increase in M&A activity throughout the remainder of the year nearly certain.

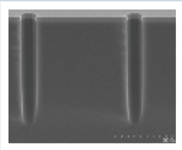


Source: GSA; Financial terms were not disclosed for a number of funding deals; For detailed funding data see downloadable Excel spreadsheet.

Solid State Equipment LLC

ADVANCED PACKAGING
SINGLE WAFER
WET PROCESSING

TSV RESIST STRIP AND CLEAN



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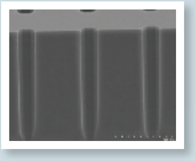

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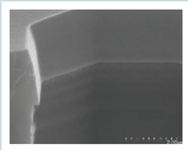

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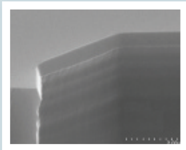

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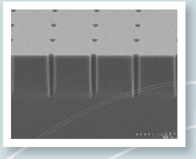
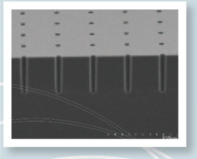
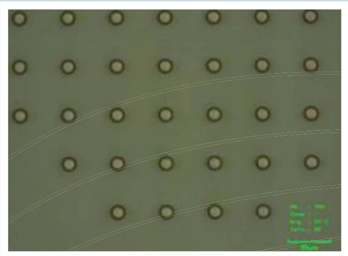


As received – post DRIE



After SSEC Cleaning

Si ETCH TO REVEAL Cu TSV



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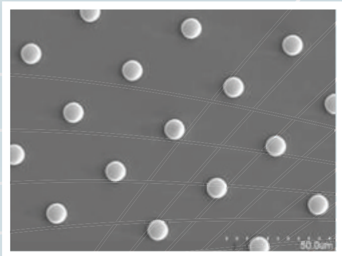
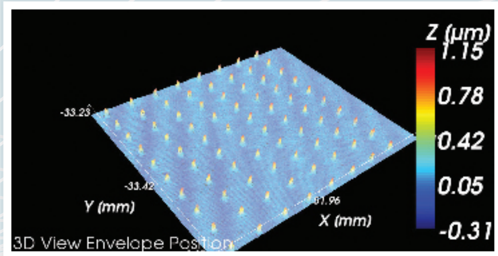
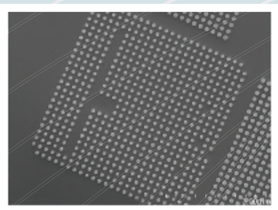


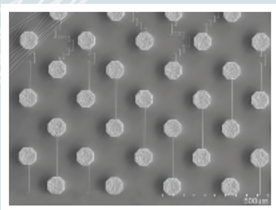
SEM

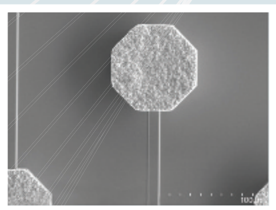


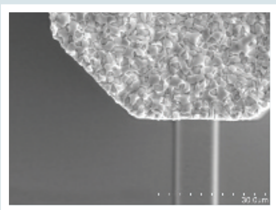
ISIS 3D

DRY FILM STRIP

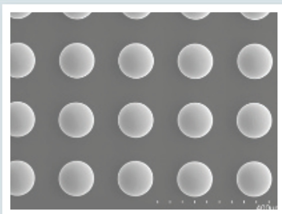


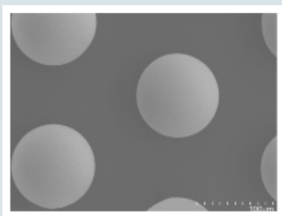




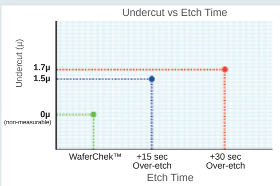


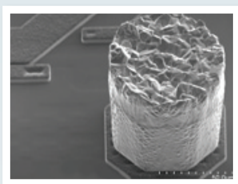
FLUX CLEANING



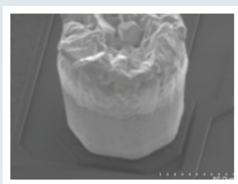


UBM AND RDL METAL ETCH





Before Etch



After Etch

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ADVANCED PACKAGING SINGLE WAFER WET PROCESSING