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Dynamic changes

The semiconductor industry dynamics continue to change and not always in the most expected way. In fact viewing the industry as a monolithic concern is becoming less relevant as new opportunites arise ensuring more markets allowing for success or failure in a sub-market completely independent of the global movement.

These changes make is extrememly difficult for investors and financial watchers who like to rely on safe over arching figures that direct their aspirations and goals for the foreseeable future. In reality overall industry figures tell you very little about the dynamics and more about potential share price reactions. The financial community, many of whom have trouble seeing beyond a global picture, have difficulty drilling down to the individual growing opportunities for the industry. A quick look at financials reveals one example where the differences for DRAM manufacturers as opposed to the overall industry provides a different financial picture.

These dynamics affect everyone, including yours truly and the time has come for EuroAsia Semiconductor to once again respond to the market change as it has successfully done for over thirty years. The last time I changed the magazine was in response to the reduction of European manufacturing efforts and the growth of Asian manufacturing. Now the industry has bcome more global and although the core industry may be smaller than it once once, the growth in opportunities is a continual expansion allowing all companies along the value chain to consolidate their positions or develop entirely new markets created by the innovation the industry has always fostered.

Of course not all industry challenging events occur due to market forces as we were all reminded with the sudden passing of Micron CEO, Steve Appleton. His style and approach was not to everyone's liking but there is no doubt his aggressive approach ensured the USA maintained some manufacturing outside of Intel and IBM and his tenacious attitude to competition ensured that the memory market was never controlled by a monopoly of one (or two) companies. His passing has left a hole in the industry and will impact the memory market drastically unless the USA finds another strong individual not afraid to take the fight to the competition.

I hope everyone is looking forward to the changes as much as we are and although we say goodbye to this particular name, the new look will carry the title through for another thirty years and counting.

David Ridsdale
Editor-in-Chief

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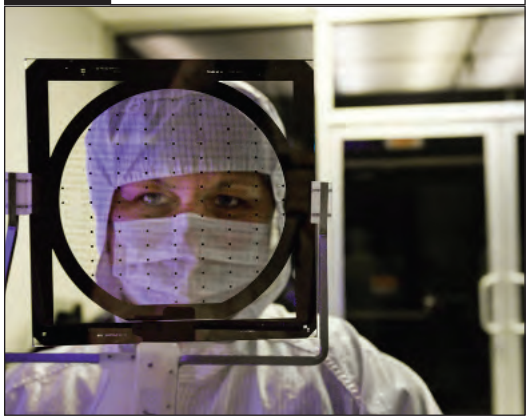

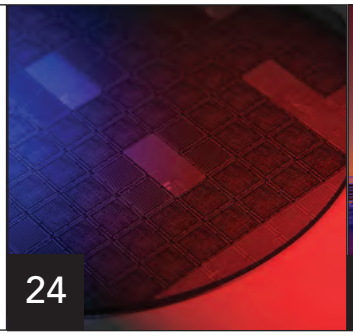

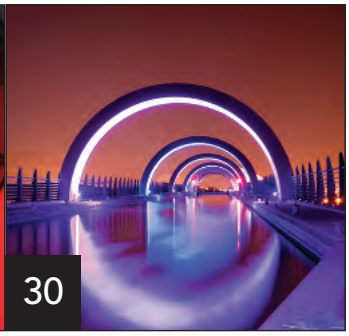

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Record breaking 2011

December 2011			
Billions			
Month-to-Month Sales			
Market	Last Month	Current Month	% Change
Americas	4.59	4.36	-4.9%
Europe	3.03	2.78	-8.2%
Japan	3.82	3.59	-5.9%
Asia Pacific	13.79	13.10	-5.0%
Total	**25.22**	**23.83**	**-5.5%**
Year-to-Year Sales			
Market	Last Year	Current Month	% Change
Americas	4.57	4.36	-4.6%
Europe	3.30	2.78	-15.8%
Japan	3.97	3.59	-9.5%
Asia Pacific	13.31	13.10	-1.6%
Total	**25.15**	**23.83**	**-5.3%**
Three-Month-Moving Average Sales			
Market	Jul /Aug /Sep	Oct /Nov /Dec	% Change
Americas	4.61	4.36	-5.4%
Europe	3.13	2.78	-11.3%
Japan	3.80	3.59	-5.4%
Asia Pacific	14.27	13.10	-8.2%
Total	**25.81**	**23.83**	**-7.7%**

THE SEMICONDUCTOR INDUSTRY ASSOCIATION (SIA) announced that worldwide semiconductor sales for 2011 reached a record $299.5 billion, a year-on-year increase of 0.4 percent from the $298.3 billion recorded in 2010. Worldwide semiconductor sales in December amounted to $23.8 billion, a decrease of 5.5 percent from the month prior. Fourth quarter sales of $71.5 billion represent a 7.7 percent decline from the immediate prior quarter, and a 5.3 percent decrease over the same period in 2010.

"Between the natural disasters in Japan and Thailand and the overall impact of a weak global economy, 2011 presented a number of challenges for the semiconductor industry. Despite these setbacks the industry showed resiliency and posted year-on-year growth with record-breaking revenues for 2011," said Brian Toohey, president, Semiconductor Industry Association.

In 2011 the industry saw strong demand in several areas; specifically the optoelectronic, sensor and actuator, and microprocessor markets showed solid year over year growth. Lamps and image sensors drove growth in the optoelectronic market to $23.1B, a 6.4% increase. Optoelectronic applications bring energy efficiency and low cost in a wide range of products including mobile devices and cameras.

Sensors and actuators, currently the smallest semiconductor market segment showed the highest year over year growth at 15.5% to $8.0B in 2011. Sensor technology which can be used to convert temperature, pressure or acceleration into electrical signals is growing as an application in consumer electronics, medical devices and automotive systems to improve safety and efficiency. An area of continued growth for sensors is in the application of MEMS, or microelectromechanical systems which are increasingly included in smartphones, tablets, digital cameras, and numerous other consumer electronic products.

MOS Microprocessors, part of the integrated circuit category, which are predominantly used in PCs and other devices that need processing capabilities also experienced year-over-year growth, with an increase of 7.5 percent in revenue to $65.2B making it the second largest semiconductor market segment for 2011, behind Logic. Strong demand in the enterprise computing segment drove microprocessor sales.

In 2012 the industry is expected to experience recovery due to demand across a broad range of end market segments combined with the delayed sales impact from the supply chain disruptions in the second half of 2011. Several large semiconductor companies announced plans for new facilities and new R&D projects that will serve to fuel the industry's long-term growth expectations.

Soitec acquisition completion

SOITEC announced the successful completion of its acquisition of all of the outstanding shares composing the capital of Altatech Semiconductor S.A., a French company located in Montbonnot Saint Martin near Grenoble (« Altatech »), as announced at the end of 2011.

The final purchase price was set to 15 million Euros. The acquisition was financed partly in cash and partly using Soitec stock, purchased by BNP Paribas Exane on the market under the share buy-back program approved by the shareholders during the combined ordinary and extraordinary meetings held on June 24, 2011. Selling shareholders are bound by certain holding requirements for the portion of the purchase price to be paid in Soitec stock.This acquisition will ensure Soitec a strategic access to specific equipments necessary to deliver its light-emitting diode (LED) strategy as well as to support Soitec's new Plug&Sun™ stand-alone mini solar tracker system manufacturing ramp up.

Altatech Semiconductor was a privately held French company located in Montbonnot-Saint-Martin near Grenoble, France. Based on its advanced knowledge and experience in high-tech semiconductor production systems, Altatech, created in 2004 by a group of semiconductor professionals, currently develops highly efficient, cost-effective technologies and equipments for new applications in emerging markets.

Slow growth expected for 2012

WITH global economic prospects remaining uncertain and semiconductor inventory not moving quickly enough to stimulate new production, the worldwide chip market is expected to suffer a slow year in 2012 marked by sluggish growth. Semiconductor industry revenue in 2012 is expected to reach $323.2 billion, up a slight 3.3 percent from last year's revenue of $312.8 billion, according to an IHS iSuppli Global Manufacturing Market Tracker report.

While expansion this year is expected to be better than the paltry 1.25 percent increase of 2011, the overall picture could brighten considerably if the United States and the rest of the world recover in 2013. Under such a scenario, growth from 2013 to 2015 will average between a more encouraging 6.6 to 7.9 percent, as shown in the figure below, with total semiconductor revenue by 2015 rising to some $397.7 billion.

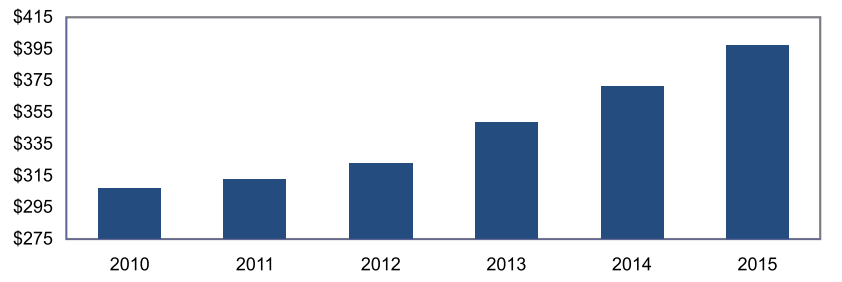
"Much of the weak performance in both 2011 and this year can be attributed to external circumstances over which the semiconductor industry has no control—the ambiguous state of the global economy, along with assorted troubles in the world's major markets of the United States, Europe, Japan and China," said Len Jelinek, director and chief analyst of semiconductor manufacturing research at IHS. "And because the world economy is not in a strong-enough position to drive growth, the semiconductor business is coming under pressure."

Consumer spending is also a key factor determining conditions in the chip market. Although consumer spending lowered the level of inventory of electronic devices and other items incorporating semiconductors during the 2011 holiday season, the reduction was insufficient to re-energize chip demand to replenish stockpiles. Worse, a deliberate decrease in manufacturing run rates by companies in the third quarter of 2011 proved unable to bring inventory down to levels that would have fired up additional orders and increased factory run rates. As a result, demand for manufacturers will remain depressed until the Q2 of 2012.

IHS iSuppli Figure: Worldwide Semiconductor Industry Revenue Forecast (Billions of US Dollars)

	2010	2011	2012	2013	2014	2015
Billions of US Dollars	$307.0	$312.8	$323.2	$348.7	$371.5	$397.7

Source: IHS iSuppli Research, January 2012



Source: IHS iSuppli Research, January 2012

Such developments will have a ripple effect throughout the industry. For instance, because factory utilization will not recover until the middle of 2012, the integrated device manufacturers (IDM) that both design and manufacture semiconductors in-house will experience even greater stress to simply maintain the viability of underperforming factories. And with current manufacturing capacity deemed acceptable for meeting demand, most capital expenditures to boost efficiency within the industry likely will be pushed out to 2013.

The most beleaguered semiconductor segment will be the memory space, especially in dynamic random access memory (DRAM), with revenue projected to decline to 16.1 percent in 2012 on top of a 26.8 percent fall in 2011. And a once-energetic performer in 2011—NAND flash—will see less rosy prospects this year because of additional capacity coming on to meet a surge of demand for the memory in devices like mobile handsets and media tablets.

In contrast, a strong market revenue driver this year will be the wireless communication segment, spurred by media tablets, smartphones and industrial electronics. For the semiconductor industry to revitalize, however, it is imperative that the core PC and peripheral markets experience a significant increase in demand, IHS believes.

The first half of 2012 is almost certain to be a challenging period for the industry, with negative growth being forecast for the historically slow first-quarter season. The industry will begin to rebound in the second quarter and then go on to a strong third quarter, as is normal for the business.

Foundries dedicated to manufacturing semiconductors as their main activity will continue to outperform the industry, while IDMs will have lower growth, especially as they have abdicated manufacturing in leading-edge technology—where the high margins are—to the foundries. The advice is for IDMs not to sit by idly and allow fabless or foundry companies to control leading-edge design or production on their own.

with current manufacturing capacity deemed acceptable for meeting demand, most capital expenditures to boost efficiency within the industry likely will be pushed out to 2013

DRAM merger would change industry

A POSSIBLE merger between Micron Technology and Elpida Memories has the potential to redraw the competitive landscape of the dynamic random access memory (DRAM) space, yielding a new No. 2 player that could challenge Samsung Electronics leadership. A union would catapult the consolidated entity to 2nd place in the global DRAM market, with a combined capacity of 374,000 wafer starts per month.

The newly merged company would have a 28 % share of DRAM manufacturing capacity, placing it just behind leader Samsung Electronics currently with a 33% share. On their own, Elpida and Micron usually place in the No. 3 and No. 4 spots, respectively. The reconfigured DRAM terrain also would mean that Hynix Semiconductor falls to third place.

Media and industry speculation currently poses the possibility of Micron taking over Elpida, or of Elpida coming to some sort of arrangement with its rival. But before such a Trans-Pacific marriage can proceed between the leading U.S. memory player and the chief Japanese DRAM producer, both Micron and Elpida would have to face down a number of potent challenges, Howard pointed out.

The first and largest, is Elpida's debt. At the end of the third quarter last year, Elpida owed $4 billion in outstanding obligations. And although the DRAM industry is familiar with large amounts of debt because fabs can be extremely expensive to build and often require debt to finance, Micron is decidedly debt averse. A second daunting challenge is the strong yen, the currency in which approximately 60 percent of Elpida's wafers in Japan is denominated.

A third possible challenge could be Micron's ongoing partnership with Nanya Technology. There could be covenants in the agreement between Micron and Nanya that could sour any chance of a possible deal between Micron and Elpida. And in an unexpected development, the Feb. 3 death of Micron CEO Steve Appleton in an experimental airplane crash could complicate matters and delay consolidation, especially since Appleton was a known advocate for consolidation and was likely a driver behind any possible deal.

For Elpida, a key advantage would be greater access to the premium customer segments that Micron serves. In the third quarter, Elpida DRAM commanded an average selling price of $0.70 per gigabyte, compared to an enviable, near-double rate for Micron at $1.34 per gigabyte. Micron, clearly, is serving a different customer group that Elpida simply would love to get its hands on, IHS believes.

But while Elpida would gain access to Micron's specialty customers in a merger, Micron also would be able to reach Elpida's mobile DRAM buyers. Elpida shipped 18.4 percent of mobile bits in the third quarter, compared to only 5.3 percent for Micron. And with mobile DRAM now accounting for about 15 percent of the total DRAM market, such leverage for Micron would constitute an unqualified boost and help expand its overall revenue.

Surging DRAM concerns

ALREADY besieged by low demand and bleak growth prospects, the market for dynamic random access memory (DRAM) is encountering yet another dispiriting obstacle—an alarming rise in inventory that threatens to further sink the industry. In contrast to the overall semiconductor industry, where days of inventory declined slightly in the third quarter of 2011, DRAM stockpiles increased dramatically, according to an IHS iSuppli DRAM Market Brief.

The IHS iSuppli DRAM Inventory Index in the third quarter of 2011 stood at 12.8 weeks, as presented in the figure attached. This represents a sharp 31 percent increase from 9.8 weeks in the second quarter of 2011, and more than double the 6.1 weeks seen during the first quarter of 2010, which marked a recent low point for DRAM inventory. It also is significantly higher than the long-term quarterly average of 9.2 weeks.

The DRAM Inventory Index measures the inventory value at the end of a quarter against the sales for the quarter. The index accounts for DRAM inventory held by the memory suppliers themselves, and not by DRAM buyers. A rise in the Inventory Index value means that there is more inventory being held by DRAM producers, putting downward pressure on chip prices.

"The surge in inventory exacerbates the travails of the steadily deteriorating DRAM market," said Clifford Leimbach, analyst for memory demand forecasting at IHS. "DRAM suppliers are suffering from a multitude of market-depressing factors including the lack of worldwide demand, the arrival of new applications needing less DRAM, and operating systems that do not require an incremental increase in DRAM as previous versions did."

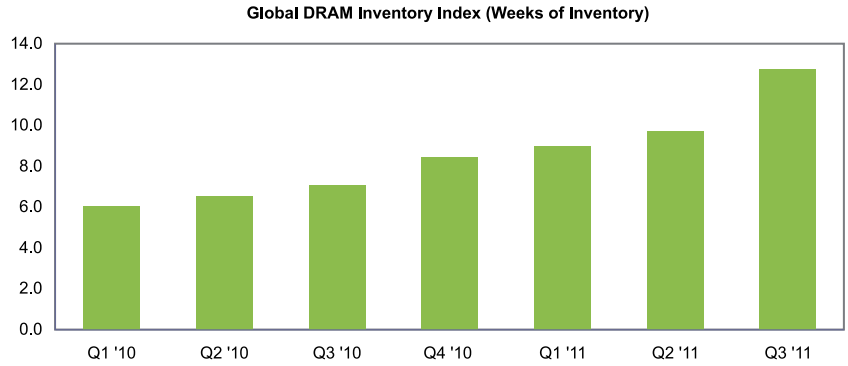
The new applications include tablets, which employ lower densities of DRAM and are slowing sales growth for traditional notebook PCs.

The financial difficulties of a number of DRAM players also have prevented capital expenditure investments on their part in more cost-effective processes, which could have improved the profitability of the companies. This is because newer DRAM chips manufactured using the most advanced process node technology yield higher profit margins, compared to lower margins seen from previous-generation chips that are newly produced or that have been sitting in inventory. With companies already suffering from razor-thin profits or even losses, the disparity between old and new DRAM chips becomes even more pronounced.

IHS iSuppli Figure: Global DRAM Inventory Index (Weeks of Inventory)

	Q1 '10	Q2 '10	Q3 '10	Q4 '10	Q1 '11	Q2 '11	Q3 '11
Weeks of Inventory	6.1	6.5	7.1	8.5	9.0	9.8	12.8

Source: IHS iSuppli January 2012



Source: IHS iSuppli January 2012

The worrisome spike in the inventory index in the third quarter is reminiscent of the last DRAM oversupply situation in 2008, which coincided with the worldwide economic recession at that time. But while the circumstances from the past are recurring on some level at the present, they also are different in many ways.

For instance, the last upheaval occurred over a drawn-out period lasting nine quarters, while the level today from trough to current high has taken only six quarters. Also, the present peak is already higher than all of the data points in the previous cycle save for one—the previous apex, reached in the first quarter of 2009—and there is every possibility that this cycle could surpass the last, IHS believes. Because DRAM is a cyclical market, such distressing patterns during what should be the traditional peak sales season are not comforting to producers of the memory type. And given the decidedly uncertain state of the world economy, the DRAM inventory index could well continue to rise for a few more quarters, worsening an already bad situation within the space. In line with the gloomy state of the market, IHS is estimating that DRAM revenue slid to slightly more than $6 billion in the fourth quarter of 2011, down 11 percent from the third.

Furthermore, it appears unlikely that the downward trend on operating profits will subside—which means that there will be little respite for the many DRAM companies already operating at, or below, cash costs. All told, the historical trajectory illustrates that the worst is yet to come.

"Should expectations arise that the economy might be headed for improvement—the belief alone is sufficient—things could rapidly improve," Leimbach said. "An example of heightened expectations very quickly reversing the downward path of the DRAM market occurred in 2009, when the Inventory Index recovered from a beleaguered 14 weeks to a desirable six weeks in the space of just three quarters."

To be sure, the prospect of a bright future would bring a dramatic turnaround and some much-needed relief for the DRAM industry. But as it currently stands—and unfortunately for the industry—there is little cause for optimism.

2011 was a record year

GLOBAL sales of semiconductor grew for the second-consecutive year following the 2009 downturn, reaching a record of $299.5 billion in 2011, the World Semiconductor Trade Statistics reported yesterday.

This represents an increase of 0.4 % compared to the $298.3 billion reported in 2010.

In 2011, most of the major semiconductor product categories showed strong growth year-over-year. In particular total discrete, opto & sensors grew by 8.3% and MOS microprocessors grew by 7.5% compared to 2010.

The relatively low growth of total semiconductor sales was mainly driven by the development of DRAMs, which decreased significantly. Most of the other categories showed an average to above average development.

In December, worldwide sales were $23.8 billion, resulting in a decline of 5.5 % compared to the previous month. A sequential decline in December reflects normal seasonal patterns. European semiconductor sales amounted to US$ 2.779 billion.

On a total year basis European semiconductor sales reached in 2011 a value of 37.391 billion $ resulting in a decrease of 1.7% versus the year 2010.

The exchange rate of the Euro compared to the US dollar has continued to have an impact on the European sales picture in the last month. Measured in Euro, semiconductor sales were 2.061 billion Euros in December 2011, down 6.7% on the previous month and down 15.2% versus the same month a year ago.

On a total year basis semiconductor sales reached in 2011 a value of 26.871 billion Euro which represented a decrease of 6.5% versus the year 2010.

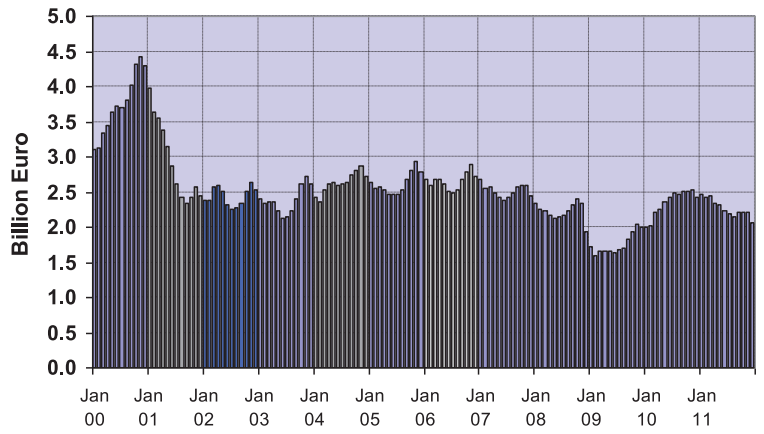
All data kindly provided by EECA-ESIA.

Market data by region[1]

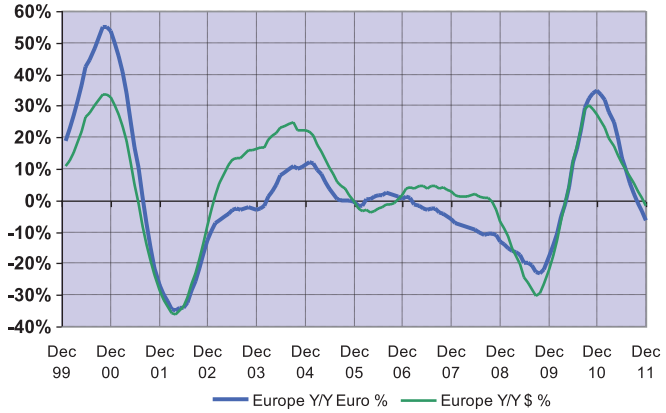
Market data for the 3 month moving average ending:								
Region	sales (in billions)		Month on Month growth		Year on Year growth		YTD growth	
	Nov 11	Dec 11	Nov 11	Dec 11	Nov 11	Dec 11	Nov 11	Dec 11
in $:								
Europe	3.026	2.779	-1.8%	-8.2%	-11.5%	-15.8%	-0.5%	-1.7%
Americas	4.585	4.361	-1.8%	-4.9%	-2.5%	-4.6%	3.1%	2.8%
Japan	3.818	3.591	-1.7%	-5.9%	-8.2%	-9.5%	-7.9%	-7.9%
Asia Pacific	13.790	13.101	-2.7%	-5.0%	1.1%	-1.6%	3.0%	2.5%
of which China	5.567	5.273	-8.2%	-5.3%	0.5%	-1.7%	5.2%	4.8%
World	**25.219**	**23.833**	**-2.3%**	**-5.5%**	**-2.7%**	**-5.3%**	**0.9%**	**0.4%**
In EURO:								
Europe	2.209	2.061	-0.2%	-6.7%	-12.8%	-15.2%	-5.7%	-6.5%
Rate ($/Euro)	1.359	1.318	-0.8%	-0.2%	< Euro against $ versus prev. Year			

1) Unless otherwise indicated, all figures are 3-month-average data except YTD growth which is based on current month data.

EUROPE - Monthly European Semiconductor sales in billion Euro
(3-month-average data)



European Semiconductor sales growth in % - Annualized growth trend (Y/Y) in Euro and Dollar
(12-month-average data)



Market needs

Semiconductor manufacturing consists of a wide and varied food chain with different companies, products and services all contributing to the quality end result. The industry has also seen a rapid change in market dynamics around the world with geographical shifting of markets and manufacturing. All companies along the value chain need to take responsibility for their input and output into the manufacturing process. **Neil Lavender Jones, President of Edwards Asia Pacific** discusses the company's recent approach for Asian success with an environmentally-responsible manufacturing approach to the industry needs.

The rapid growth of manufacturing has improved the economic prospects of many in Asia's vast population; however the benefits have not come without costs, particularly in the negative impacts of manufacturing operations on the environment. Although government regulation is essential to guaranteeing a level playing field - and many governments in the region have taken strong regulatory positions - in the end, manufacturers must find ways to mitigate negative environmental effects that also allow them to compete successfully in the marketplace. Edwards is committed at all levels to providing manufacturing solutions that are both economically viable and environmentally responsible, from the products we make, to the manufacturing facilities we use to make them. We hope that our newest facility, recently opened in Korea, not only demonstrates this level of our commitment to environmentally-responsible manufacturing, but may also provide

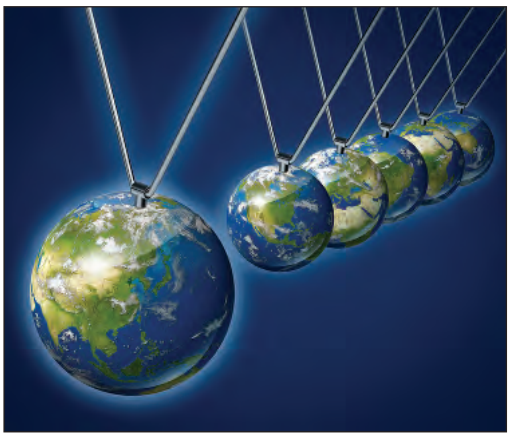
a model for manufacturing operations that achieve both economic and environmental goals.

Edwards is a global company with major manufacturing operations in many countries around the world. We have had a manufacturing presence for some time in Asia, with major operations in Korea, Japan and China. Like other global companies, the recent growth in Asia has given us good reason to locate new facilities there, close to our customers and key markets. Last year, nearly 60 percent of our business was in Asia. When it came time to expand our capacity for dry vacuum pumps, Korea, where we already had an assembly operation for pumps used by makers of flat panel displays, was a strong contender. When we selected Korea as the location of the new operation, we also committed to creating a facility that would incorporate all of our best practices and technology for environmentally-responsible manufacturing.

The new plant has 25,000 square meters of floor space and the capacity to produce 25,000 pumps annually. To ensure a stable manufacturing environment, the facility is "closed door" with the interior temperature controlled to within 2°C. The building itself is of double wall construction with an insulating air gap. Double reflective windows reflect energy from the exterior in summer and interior in winter.

Most interior lighting is high-efficient LED based, with extensive use of "task lighting" that provides light only where it is needed. Air compressors, used extensively in our operations, incorporate energy-efficient variable speed drives. Water is heated by solar energy. Comprehensive recycling is designed to meet the goal of zero landfill waste. Paint and finishing processes use materials that cure at low temperature to reduce energy consumption by hot air dryers. All cleaning is water based and 95 percent of the water used is recycled.

Of course quality is not sacrificed. The latest, 5-axis CNC milling tools are capable of creating the complex three dimensional shapes required by our pumps in a single operation. Advanced coordinate measuring tools enable those tools to manufacture parts with high precision. A lean manufacturing workflow minimizes unnecessary movement of people, parts and tools. Unidirectional flow, from materials in to finished products out, reduces opportunities for contamination. Kanbans and just-in-time scheduling keep parts inventories at a minimum. All products are fully tested and all parts are fully traceable.



Remanufacturing is also an important component of our overall strategy. Smaller remanufacturing facilities are distributed throughout the region, currently in Taiwan, China, Singapore, Korea and India. These facilities reflect the same emphasis on lean manufacturing practices, product quality and environmental responsibility. Remanufactured products undergo the same stringent assembly and test procedures applied to new products. Remanufacturing is essentially a recycling program for our own products. It reduces waste that would otherwise be created by scrapping old pumps and reduces cost to our customers - recycled pumps are less costly than new ones. Equally important, the network of recycling facilities brings us closer to our customers and builds local technical expertise that improves support.

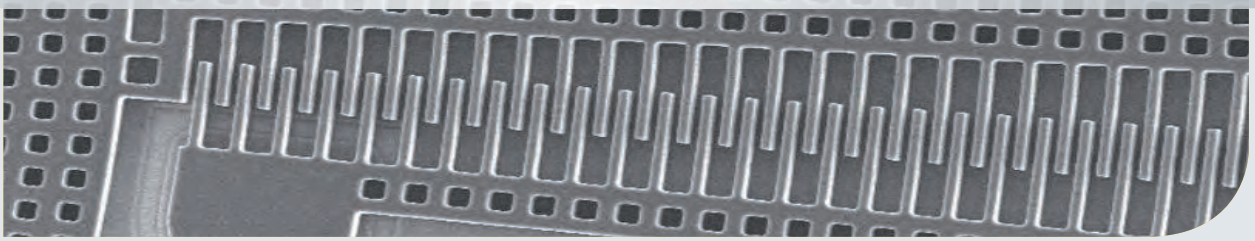
By investing in modern manufacturing facilities close to customer base we not only enhance the quality of our products and support, we also ensure viability of Edwards as a global company, benefitting our customers and employees around the world, and at home. For example, the dramatic growth in our Asian markets is a primary driver in our current plans for a new research and development facility in the UK. Ultimately, we believe we are all best served by a company footprint that encompasses both the worldwide distribution of our customers and markets and the historical distribution of our core expertise.

Edwards takes very seriously its responsibilities to its customers, its workforce, and to the global environment. Rather than conflict we see opportunity in the challenge to serve the shared interests of all our constituencies.

The new plant has 25,000 square meters of floor space and the capacity to produce 25,000 pumps annually

siconnex
customized solutions

APPLICATIONS



PRODUCE 200 ACID

BATCH SPRAY ACID PROCESSOR

- Metal Etch (Al, Ti, TiW, Pt,...)
- Oxide Etch
- SPM Resist Strip
- SicOzone™ Resist Strip
  (Positive Resists, Negative Resists)
- Clean

PRODUCE 200 SOLVENT

BATCH SPRAY SOLVENT PROCESSOR

- Resist Strip
  (Positive Resists, Negative Resists)
- Polymer Removal
- Resist Ash Residue Removal
- Clean

VERTICAL 200 SOLVENT

SINGLE WAFER SPRAY SOLVENT PROCESSOR

- Metal Lift Off
- Resist Strip
- Polymer Removal
- Megasonic/High Pressure Clean

wetspray expert™

www.siconnex.com

The enhanced approach for metal lift off processes

Siconnex is a equipment manufacturer for the semiconductor and related industry with a focus on wet batch and single wafer spray. Siconnex systems provide small footprints, high safety, full automation and improved throughput. Here they outline product advantages impacting the MEMS industry.

SINGLE WAFER SOLVENT applications are becoming more relevant for the MEMS industry. As a consequence Siconnex has expanded its activities and now offers Metal Lift Off, Resist Strip and Polymer Removal processes on the Siconnex Vertical 200 platform.

The process head on the Siconnex Vertical 200 platform is especially designed to run solvent applications such as Metal Lift Off, Resist Strip and Polymer Removal. The Substrate Face-Down Technology eliminates the risk of wafer contamination. Dry wafer handling throughout the system minimizes maintenance. Up to 6 process modules are arranged in a stacked chamber design, keeping the footprint (with integrated chemical conditioning system) smaller than 4m^2. Based on this configuration a typical Lift-Off application achieves a throughput of 125wph.

Wafer sizes up to 8-inch are processed in this system.

Advantages

InSitu Lift-Off Chamber

Compared to other available systems on the market, the Siconnex Vertical 200 SOLVENT has an on the Siconnex Vertical 200 platform enabling the tool to perform both steps in one chamber, a complete soaking process as well as the final High-Pressure Lift-Off cycle. The soaking step is done by utilizing dedicated spray nozzles, up to a pressure of approximately 2 bar. Using the mechanical force of this stream, the soaking time can be reduced by over 75%. The subsequent High-Pressure step eliminates residues and cleans the surface completely. The required pressure (up to 150 bar) can be adjusted in the recipe.

Substrate Face-Down Technology

Wafers are loaded face-down into the process chamber, where they are held by a vacuum chuck. A N2-Purge completely protects the wafer backside from splash-backs caused by the high pressure step.

Due to Substrate Face-Down Technology, all residues will be kept away from the wafer surface by gravity. In addition, this technology prevents the wafer from scratches caused by metal residues.

Process Qualification

Siconnex qualifies all processes in its laboratory in Salzburg. The cleanroom is equipped with all Siconnex systems being offered to the industry – Produce 200 Acid for batch spray wafer acid applications, Produce 200 Solvent for batch spray wafer solvent applications and Vertical 200 Solvent for single wafer solvent applications.

Currently, more than 50 000 wafers were processed in the Vertical 200 Solvent to develop and qualify Metal Lift Off, Resist Strip and Polymer Removal processes. Upcoming laboratory activities are the qualification of contactless handling (Bernoulli chuck) and the development of the Vertical 200 Acid for single wafer acid tasks.

Siconnex – Wet Spray Expert

Founded in 2002, Siconnex is headquartered in Salzburg/Hof, Austria, and operates via a customer support network, with subsidiaries in France, Malaysia and Taiwan.

Siconnex provides surface preparation equipment and processes, including wet batch wafer spray and single wafer spray systems for MEMS, III-V Semiconductor, Wireless, Power, Energy Harvesting, WLP, Data Storage and Logic industries.

Global business practises

The semiconductor industry is truly a global market place and for many new companies in the sector there is a minefield of knowledge required in building associates and relationships in foreign markets. **Jackson Wood, corporate business manager of MSR eCustoms,** takes a look at what to be wary of when building a global presence and asks how well do you know your customers?

Doing business in a global economy can be a challenge. As the marketplace grows, it is critical to ensure your business partners are not subject to restrictions. While opportunities abound, some companies practice due diligence and others just go ahead and hope things fall into place smoothly.

Although it may sound simple, a major element of diligence is to Know Your Customer (KYC). Commonly referred to by bank regulation and financial institutions, KYC is the due diligence that they and other regulated companies must perform to identify clients and gather pertinent business information. It usually takes the form of an internal policy used to conform to a customer identification program mandated by the Bank Secrecy Act (BSA) and the USA PATRIOT Act.

Many international jurisdictions take their cues from the U.S. to form their own similar version. The policy of knowing your customer is becoming more important on a global scale, to prevent identity theft fraud, money laundering and terrorist financing. It's important to implement these types of procedures in your company to ensure you, your agents, consultants or distributors are in anti-bribery compliance.

Who to look out for

So how does one make the connection between knowing the customers they do business with and bribery? Although they are called slightly varying names in different countries, there are prominent public figures generally known as a Politically Exposed Person (PEP) or Foreign Official. These people,

due to their position and influence, are a higher risk for possible bribery and corruption. The Financial Action Task Force on Money Laundering (FATF) also includes the immediate family members or publically known individuals that are close personal or professional associates of the PEP in their definitions.

While there is no global definition for the term, most countries have based their own definitions of the FATF. The anti-bribery provision of the Foreign Corrupt Practices Act (FCPA) "makes it unlawful for a U.S. person, and certain foreign issuers of securities, to make a corrupt payment to a foreign official for the purpose of obtaining or retaining business for or with, or directing business to, any person." The penalties for violation are severe. Criminal penalties could include fines up to $2,000,000, and individuals including officers, directors, stockholders, employees or agents could be fined up to $100,000 and imprisonment up to 5 years. Without proper screening procedures, it is possible to engage in business with someone who is considered a PEP, putting you and your company at risk of violating the law.

What to look out for/Money Laundering

Without participating in due diligence practices, it could be possibly to accidently bribe a PEP or Foreign Official when engaging in business with a new country, or a new company. The bribing of public officials is considered money laundering under the expanded definition in the USA PATRIOT Act. An approximation by the International Monetary Fund estimates between 2% and 5% of global gross domestic product as laundered money, financing criminal enterprises and terrorism. Money laundering has been a criminal offense in the U.S. since the Money Laundering Control Act of 1986, however anti money laundering (AML) guidelines came into prominence after the September 11, 2001 attacks. Many countries worldwide have initiated their own Money Laundering legislation. The United Kingdom, and many other European countries have based their regulations direct on the EU directive 91/308/EEC, 2001/97/EC and 2005/60/EC, preventing the use of financial institutions for the purpose of money laundering and terrorist financing. The easiest way to ensure you company doesn't contribute to money laundering is to Know Your Customer by screening potential companies and individuals to do business with.

Usually when we think of globally exporting items, we visualize shipping docks loaded with containers ready to be sent across the ocean. However many companies may be currently exporting items without even realizing they are violating export controls.

Export Controls

Usually when we think of globally exporting items, we visualize shipping docks loaded with containers ready to be sent across the ocean. However many companies may be currently exporting items without even realizing they are violating export controls. The U.S. holds strict export regulations under the Export Administration Regulations (EAR), which regulate export and re-export of commercial items.

Under the EAR, many forms of communication such as a set of schematics sent via e-mail, or software downloaded from an internet site are both considered an export. Even if the item is only leaving temporarily, or is a gift, it is still considered an export. To confuse

There are lists issued by various government agencies globally that are a compilation of restricted or denied parties. While the thought of comparing your potential customer against dozens of lists sounds tedious and time consuming, there are service providers who can filter the names you provide, flag suspicious names and classify them according to risk

matters even further, the release of technology to a foreign national in the U.S. is considered a "deemed export" and is subject to EAR as well.

Fortunately not every product requires commerce export licenses, however the responsibility lies on the exporter to determine whether they need a license or not. License requirements depend on a variety of factors including what you are exporting and its' purpose, where it's being exported to, and who will receive the item. The main factor in determining if an export license is needed is whether the item has a specific Export Control Classification Number (ECCN). All of the ECCN's are listed in the Commerce Control List (CCL) which is divided into 10 broad categories, of which each is then further subdivided into five product groups. The 'where' and 'who' tie back into the 'Know Your Customer' guidance on dealing with embargoed countries or restricted parties.

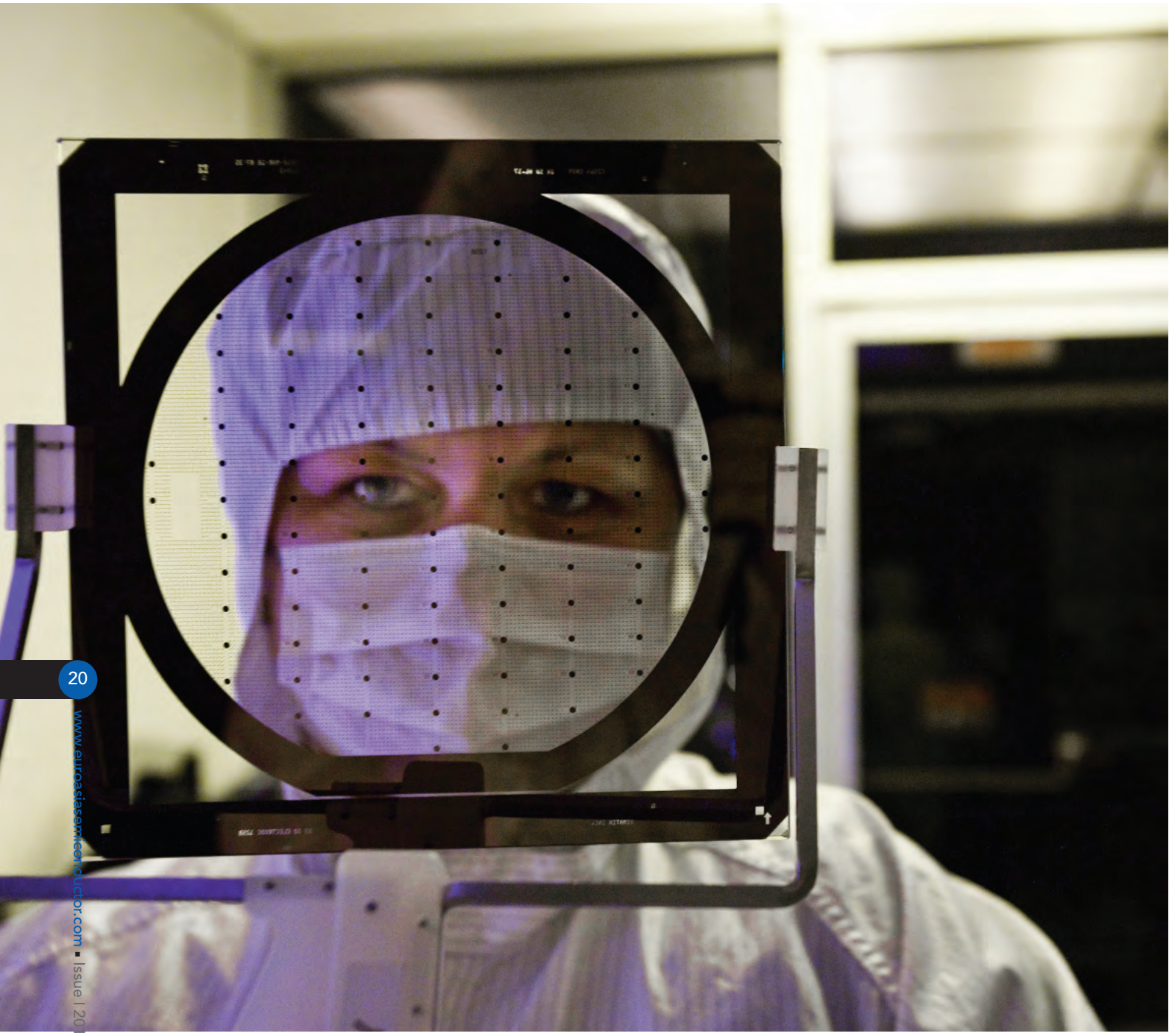
How to look out for you

There are lists issued by various government agencies globally that are a compilation of restricted or denied parties. While the thought of comparing your potential customer against dozens of lists sounds tedious and time consuming, there are service providers who can filter the names you provide, flag suspicious names and classify them according to risk.

They can also inform you if the company you are interested in doing business is located within a country that is hostile or if there are trade sanctions against it. The U.S. and E.U. share sanctions against several countries including Iran and North Korea. The United Nations also lists several countries under embargo. Some embargoed countries are allowed commercial goods, while other have much stricter restrictions. The best way to qualify potential business prospects is to compare it to the assembled lists. While it may not always be illegal to conduct business with these countries, a special license may be required to do so.

Enhanced due diligence practices ensure that your company and your executives are protected from the law. Under the Sarbanes-Oxley Act, U.S. companies need to have strong internal controls at every level of the organization to ensure the highest degree of financial accuracy and accountability. As the company is ultimately held responsible for compliance it makes the most sense for corporate chiefs to directly oversee internal procedures rather than outsource, or rely on third parties.

All these practices tie back to one simple premise: Know Your Customer. By participating in this modest diligence exercise, companies can ensure that they are protecting themselves and their country.



Choosing the right **photomask**

Anyone involved in the IC manufacturing industry is well aware of the cost that photomasks bring to the bottom line of a project. Large manufacturing ventures are well versed in their needs but the ever expanding smaller and fabless ventures may not have the knowledge for what suits them. **Gordon Hughes, CAD Systems Development Manager at Compugraphics International** provides an outline for manufacturers on how to specify a photomask.

There are a small number of IDM's and Foundries that order hundreds and even thousands of photomasks every year. Such users are pretty knowledgeable about the criteria used to select the right photomask. However,there are thousands of other mask users who may only order a few photomasks a year and don't have the time or resource to figure it all out. This article is aimed at them.

They will want to order a photomask which is not over specified and thus unnecessarily expensive. Most are using 1x projection lithography systems. Once they are ready to order their photomasks they should consider the substrate choice options. The article examines the pros and cons of these options, setting out the technical differences between them. Then the question arises of how tightly the dimensions on the photomask need to be controlled. The article will give guidance on what sort of cd control is easy, medium and hard, with an explanation of why tight CD control is inevitably more expensive. The article will cover the same ground for overlay control and defectivity.

Furthermore there is the question of who to order this photomask from. The article will provide an overview of the options, ranging from global semiconductor manufacturing companies to university run R&D departments, sometimes used to make masks. There are many benefits in going to dedicated photomask producers and this article will explain why. As the larger photomask manufacturers are already geared up to provide masks to a specified standard and quality, it need not be a more expensive option.

A photomask represents a complex piece of engineering, the result of a manufacturing process with many process steps and options. As a result, when a customer orders their first photomask they are presented with a very large number of questions often using terminology which the user will not be familiar with. This article will attempt to demystify the process. There are three significant components which make up the complete photomask order.

The first of these is a file that defines the geometrical data which is to be exposed on the photomask. In the mainstream semiconductor industry this will usually be one of three data formats, Calma GDSII Stream (often abbreviated to any one of these three names) , OASIS (a modern, more compact, data representation) or MEBES (the machine specific format used by the Etec photomask writing systems). Smaller customers have a large number of possible formats for defining their geometry; two common ones are Caltech Intermediate Format (CIF) and AutoCAD DXF. If you are not using one of the main-stream formats, an important aspect to bear in mind is the need to define geometry which defines areas, rather than constructs such as Line and Arc which produce nice pictures, but are not always easy to convert to exposed regions of a photomask. It is preferable to use one of the three main-stream data formats if possible, as these are less ambiguous about what the geometry represents than some of the other formats.

Technical description

The final aspect of a photomask order is the commercial aspects of the order. A typical flow for smaller customers is to provide either sample or actual geometrical data to allow a quotation to be generated, which is then followed up a purchase order.

Within the technical requirements, there are a number of different categories of information required. In summary these are:

- The physical materials required – size and type of glass
- The size and acceptable tolerances of the minimum features
- Any requirements for registration and overlay
- The inspection criteria for acceptable defectivity levels

The information provided in these categories will dictate which of a range of photomask writing and inspection tools will be used, and dictate the cost. As a general rule, the larger the size of glass, the smaller the features, the tighter the tolerances and the more critical the defect levels, the more advanced tools must be used and the greater the cost.

The most common sizes of glass are 4", 5", 6" 7", 9" and 14" square photomasks designed for use with 3", 4", 5", 6", 8" and 12" wafer sizes. As the size gets larger the thickness also tends to get larger, ranging from 0.06" to 0.25". For historical reasons, photomask sizes are normally specified in inches, even though the features on them are normally expressed in microns/nanometres. The size required is dictated by the capabilities of the equipment that the photomask will be used on. Most photomasks ordered by smaller customers are for 1X contact or alignment systems, so the photomask needs to be slightly larger than the

As a general rule, the larger the size of glass, the smaller the features, the tighter the tolerances and the more critical the defect levels, the more advanced tools must be used and the greater the cost

wafer size to allow for handling and titling. Such photomasks are often described as master photomasks, and can either be used directly or can be used to make contact print copy photomasks. The alternative is to manufacture photomasks called Reticles when stepper or scanner technology is used, where each reticle will typically be 5" or 6" in size and the features will be 2X, 2.5X, 4X, 5X, 10X the size required on the final silicon wafer. The requirements may also include the need for one or two pellicles to be attached. A pellicle protects the surface of the photomask and also moves any particles on the pellicle surface out of the focal plane of the system using the photomask.

The minimum feature size that appears on the photomask will dictate which exposure system needs to be used to write it. Most writing systems have a number of different writing modes, and the mode determines the minimum feature size which can be exposed, as well as the typical tolerance which can be achieved. Commercial manufacturers are making hundreds of photomasks per week and maintaining SPC data about the key aspects of their process equipment so will have a good understanding of their process capabilities.

For the semiconductor industry, most photomasks will have CD tolerances of less than 0.25 microns, so any requirement which is slacker than this can be ordered on the basis of the SPC results. Where machines are being used as part of a research environment, or are cheaper photo plotters rather than the laser/ebeam based writing systems used in merchant photomask manufacturers, there is likely to be more process variation between photomasks.

Photomasks can also be checked for the positional accuracy of feature placement within the photomask, either by comparing the overlay of the photomask with another photomask or by comparing points measured from the photomask to a standard grid. Any photomask being produced for the semiconductor industry will typically have registration and overlay results better than 0.25 microns, and for most non-semiconductor applications SPC results can be

used for the mask qualification. It is also important to note the difference in thermal expansion coefficient between quartz and soda lime glass, with quartz glass being an order of magnitude better. For soda lime, a 10C change in temperature results in a 1um expansion over a 4" distance. If soda lime glass is being used, it is useful to advise the photomask manufacturer of the temperature at which the photomask will be used, as this can be compensated for as the photomask is written. If the temperature is likely to vary while the mask is in use, or if the mask is being used with a deeper UV wavelength (i-line or lower) then quartz material should always be used.

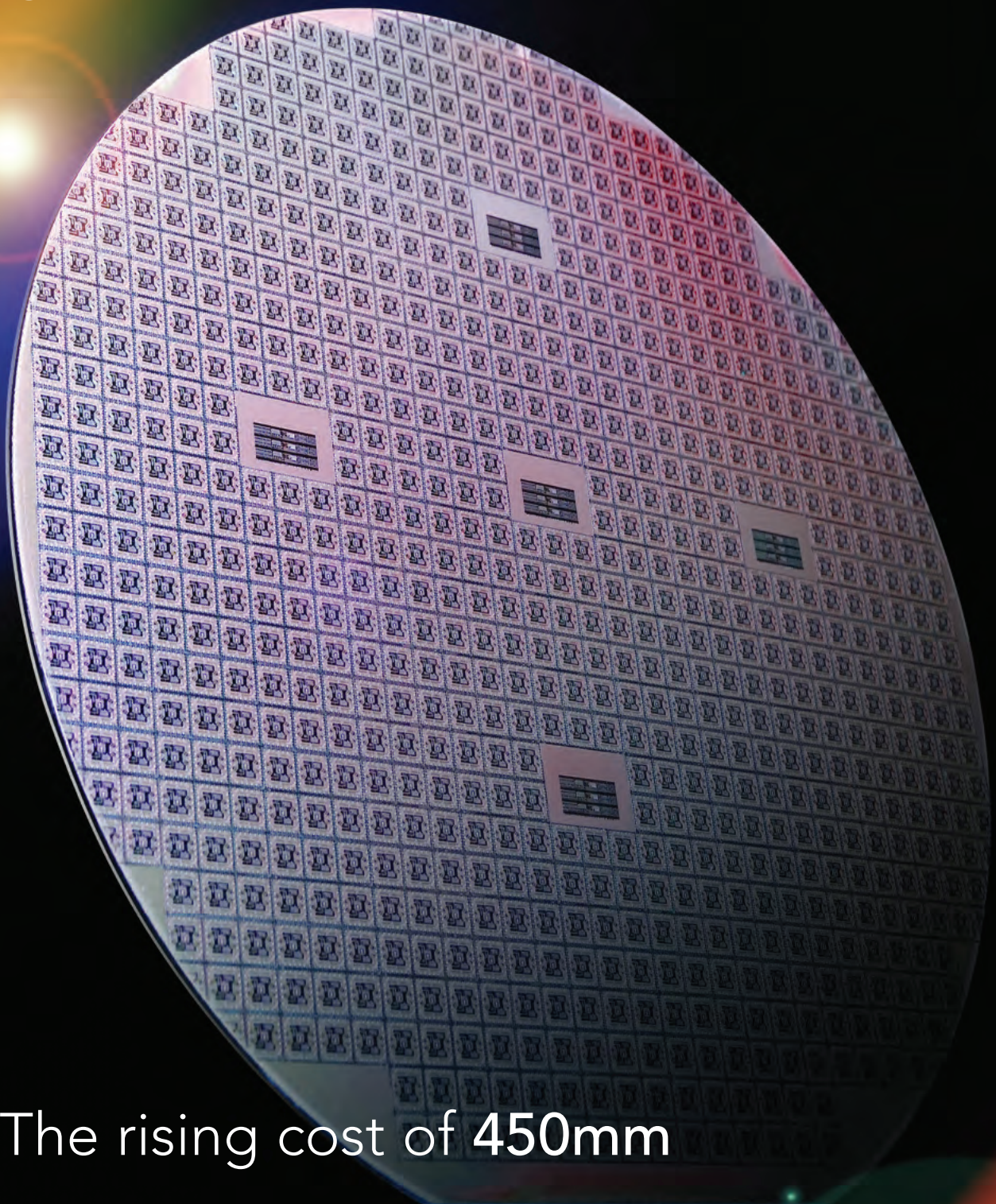
There is no such thing as a defect free photomask. The question is: at what level of detail do you want to inspect the mask? At some, possibly sub-micron level, there will always be some defects caused by imperfections in the photomask blank, the coating or the development and etching process. In the case of reticles or 1X photomasks with no repeating patterns, a typical defect specification would be "zero defects greater than x microns". In the case of advanced photomasks "x" might be hundreds of nanometres, and for semiconductor photomasks "x" will usually be 1 micron or less. If there are repeating patterns, then the mask defectivity is usually expressed as being a maximum acceptable level of "y" defects per square "unit" at "z" microns, where "y" is the number of allowable defects, "z" is a defect size in microns, and "unit" is typically "cm" or "inch". (e.g. 1 defect per square inch at 1 micron). In some causes it is also desirable to use both a defect density specification and a maximum allowable defect size, e.g. 1 defect per square inch at 1 micron and 0 defects > 5um. Any defects detected outside of this specification can either be repaired or the photomask rejected and rewritten. If there is a repeated pattern, and the mask is only being used for development or research purposed, the existence of small numbers of defects may be non-critical. If this is the case the customer can request no defect inspection, and thus save the cost associated with a significant process step. Again ordering photomasks with no inspection is most practical when you are using a major photomask manufacturer where the SPC can show that all of their masks are being manufactured to very low levels of defectivity.

It can also be very useful to advise the photomask manufacturer what type of technology the mask will be used for. Examples are optical wave guide masks where high resolution when writing the mask is important in achieving smooth curved features; or surface acoustic wave devices where any breaks or bridges in the fingers can cause fatal device errors. Larger manufacturers will already be familiar with many similar issues, based on the extensive experience of their workforce.

Once all of the technical information has been assembled, there are a number of methods for passing it on for manufacture. For many smaller customers, the instruction to apply the photomask manufacturer's standards may be sufficient (although some items such as mask titles, tone required and a minimum feature size are always required). Larger manufacturers offer online ordering systems which can capture the data required in a user friendly manner. If ordering large quantities of masks, standards such as the SEMI P10 format can be used, but the software effort required to generate this data is probably hard to justify for smaller customers.

Getting the photomasks you desire is never a trivial task, but some consideration to the requirements and qualification options required can pay dividends in achieving cheaper and reliable photomasks.

Gordon Hughes is the CAD Systems Manager at the Compugraphics International Glenrothes site. He graduated with a BSc in Computer Science from Edinburgh University. Following graduation, continued to work for Edinburgh University developing and supporting their CAD tools that were used as part of an MSc course. He then joined Lattice Logic (subsequently) European Silicon Structures where he developed the Shapesmith software for the processing of mask data. He has been responsible for the CAD and Data Processing systems within Compugraphics for over 20 years, pursuing his interest in automation of the data processing and customer requirements from order forms and specifications.



The rising cost of **450mm**

The semiconductor industry was once well used to transitioning along technology nodes. Moore's Law provided the parameters of expectation guiding companies along the shrinkage path. That was until 300mm and the financial and industry fall out from that nodular move is still felt throughout the industry. Now 450mm is on the table and the recent SEMICON Europa saw an international event on the matter. **Tom Morrow of SEMI** outlines the details of the event.

In the most complete, public discussion to date on the scope and character of the 450 mm wafer transition, representatives of SEMATECH, policy-makers from the European Commission, industry consortia, and technology suppliers met to discuss the implications of 450 mm transition at SEMICON Europa on October 13-14, in Dresden, Germany. Among the highlights of the 2-day session was the 450 transition price tag estimated by speakers at $25-$40 billion, much of it centered at the Global 450 Consortium (G450C), perhaps with little room for other industry consortia or non-G450C participants.

According to Tom Jefferson, 450 program manager at SEMATECH, by mid-2013 to early 2014, a complete 450 mm production line will be established in New York containing 50 different tool types. The objective of the pilot line will be to develop data to support the purchase of production-line tools and it is unlikely that non-participants in G450C will be favorably considered for 450 production lines. According to many speakers, like the case with 200 mm tools during the 300 mm transition, when 450 mm reaches production, significant 300 mm development will cease.

What 450mm Means for Europe and 300mm

The 450mm Progress Review at SEMICON Europa was organized by Lothar Pfitzner, Fraunhofer IISB, and included sessions on R&D and Planning, Facilities, Silicon and Metrology, FEOL Equipment and Automation, and Technology and Device Issues. Georg Kelm, head of the European Commission's Nanoelectronics sector, discussed the preliminary results of a draft study, due by year's end, which seeks to clarify policy options and support considerations for the European semiconductor industry. Preliminary conclusions of the study claim that once 450mm enters full production, further 300mm node development will cease for tool suppliers due to limited resources and poor return on investment. Some equipment suppliers may choose to stay off 450mm and focus on specialty development on 300mm platforms, but the 8nm node is likely to be the 450mm equivalent of 65nm's '300mm only' moment. Furthermore, the "Post CMOS" era will likely be exclusively on 450mm wafers.

Once 450mm is fully developed, spare capacity in 300mm will emerge, encouraging a migration from 200 mm production, impacting the viability and competitiveness of both 200 mm and 300 mm fabs in Europe and the world. In 15-20 years, even low volume, mature technologies in MEMS, power and analog could migrate to 450 mm fabs.

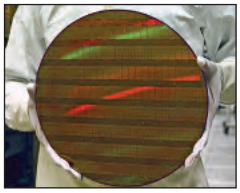
How the EU chooses to support the semiconductor industry through the coming years is being evaluated by the study, industry players and policymakers throughout the region. There are clear divergences of interests across the industry: European IC manufacturers are currently not planning 450 mm investments; many equipment and materials suppliers see an opportunity, but many suppliers see the 450 R&D draw threatening long-term profitability and current customers. Similarly, European consortia and R&D organizations see both an opportunity and a threat as—unlike current 300 mm process development which occurs at multiple locations around the globe—near-term 450 development seems likely to be exclusively conducted at the G450C site in New York.

Kelm acknowledged the prominence of different views on government support for More-Than Moore, and More Moore programs and the challenges 450 will make on current semiconductor and high-tech policy. With $2-3 billion necessary for a stake in a 450 development fab capability, it is unclear whether both wafer size transition, next node scaling, new transistor technology, and 3D IC could be simultaneously be funded. With 450 demanding such a large resource commitment, it is also unclear how semiconductor industry support will fare among all European Key Enabling Technologies (biotechnology, advanced materials, photonics, etc.).

Michel Brillouet, Senior Advisor, CEA-LETI, who estimated the total cost for 450 wafer size conversion to reach as high as $40 billion, summarized the EU options: help develop 450 and forget all More-than-Moore projects; forget 450 and concentrate on other process technologies such as 3D, EUV, etc; and support R&D by equipment and material suppliers without a European production or pilot development lab.

Effective Migration: Affordable and On-Time?

Hans Lebon, VP Fab & Process Step Development at IMEC, began his presentation with the statement that "wafer size transition



Other presentations during the 2-day program addressed many unique fab, tool and technology requirements for larger wafers. These presentations demonstrated that while pilot plans are sharpening, considerable work has yet to be completed

accelerates industry consolidation." Estimating the cost of the transition at $25 billion, Lebon said the 300 mm wafer size transition "wasn't cost effective." One of the ways to manage costs will be through "fewer equipment platforms." Imec is still trying to formulate a role in 450, and claimed there "still was a long journey to go."

Tom Jefferson from SEMATECH, however, sees a clear timeline, schedule and participation process in place for 450. He stated that over 40 companies are participating in the program, defects per wafer have been reduced from more than 3000 to less than 200, and that effective SEMI standards have been developed to enable development.

Jefferson reiterated the key details of the September announcement that IBM, Intel, TSMC, GlobalFoundries, and Samsung, along with the College of Nanoscale Science and Engineering, University of Albany, State University of New York, have committed $4.4 billion to next-generation chip research, including 450 mm wafer processing. How much of the announced $4.4 billion was already-committed IBM money for other (non-450) advanced chip design and technology development was not verified. The new fab site has been prepared and walls are going up on the fast-track project. Nanoimprint technology from EV Group will be used as the "stopgap measure" in lieu of a workable EUV solution.

On Day 2 of the Session, Jefferson returned to clarify that the pilot line will include 50 types of tools, many with more than one supplier contributing. The goal of the pilot line will be to develop a database that will be used to support production tool purchasing. Participants in the program will benefit from access to patterned and non-patterned wafers, shared metrology and Multi Application Carriers (MACs), shared consortium staff resources, data sharing, and "financially leveraged business partnerships" with consortium partners. Suppliers who do not participate in the program will be lower on the priority for access to test wafers. The impression left was that not participating in the program will lower the probability of participation in production line rollouts by consortium partners.

Jefferson also clarified the intercept point of the pilot line. The consortium is expected to have different intercept points for logic and DRAM, but the "expectation should be for 10 nm and beyond," and the timing for the second half of 2013-early 2014.

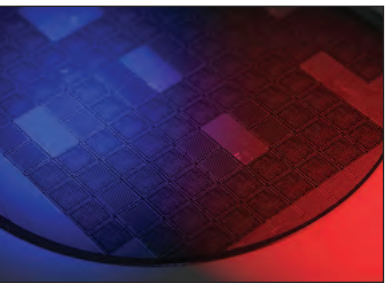
New Requirements for 450 Fabs

Other presentations during the 2-day program addressed many unique fab, tool and technology requirements for larger wafers. These diverse presentations demonstrated that while 450 mm pilot plans are sharpening around firm schedules and requirements, considerable engineering and science work has yet to be completed.

Peter Csatary, Head of Group Technologies, M+W Group, highlighted utility, construction, material handling requirements for a 450 fab. Ines Stolberg, Manager Strategic Marketing Litho, Vistec, discussed their concept for a direct write, variable beam (rather than single beam) approach to maskless lithography. Guilhem Delpu from Recif discussed work being funded by the EU on improving vibration, cleanliness and substrate affects on wafer handling.

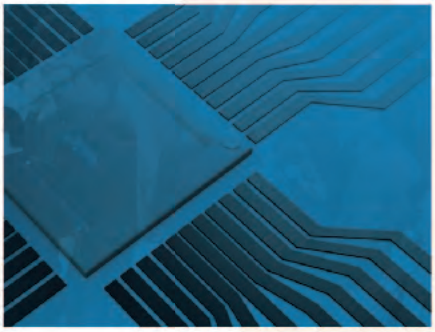
Geert van der Zalm of Bosch Rexroth also discussed alternative material handling approaches and control strategies for 450 mm wafers to manage vibration with heavier loads and longer arms. "We may need to rethink tool architecture, such as using inverted linear motor to enable inline vacuum transport that has been proven useful in the solar industry."

Results from another European funded project on etch process development illustrated the challenges in 450 mm process development. Mike Cooke from Oxford Instruments indicated the first tests on 450 PECVD SiO2 processing have so far yielded only a 4.2% uniformity across all points. In induction coupled etch plasma, a +/- 10% uniformity across a 450 wafer has been achieved (half of the non-uniformity at the wafer edge), that according to Cooke was "not good enough, but a useful start."



SEMI EXPOSITIONS

SEMICONDUCTORS • SOLAR/PV
LEDS • MEMS • FPD
PLASTIC ELECTRONICS
EMERGING MARKETS



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SEMICON West 2012
July 10-12
Moscone Center, San Francisco, California
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SOLARCON India 2012
September 3-5
Bangalore, India
www.solarconindia.org

SEMICON Taiwan 2012
September 5-7
TWTC Nangang Hall, Taipei, Taiwan
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PV Taiwan 2012
October 3-5
TWTC Hall 1, Taipei, Taiwan,
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SEMICON Europa 2012
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Wet Benches

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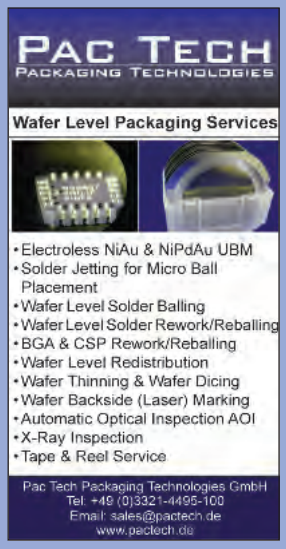

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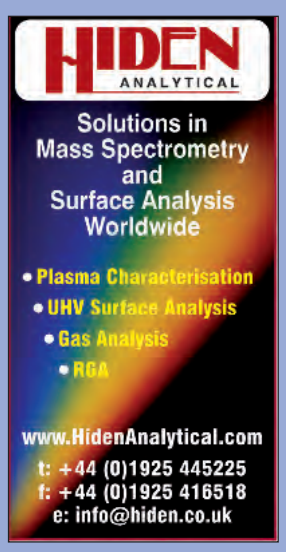

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Scottish semiconductor success

While much of the semiconductor industry focuses on global figures revealing overall slow growth there is always bright spots of innovation and success. Scotland's Semi Scenic is an excellent regional example after it doubled sales in semiconductor market in 2011.

In an exceptional year, semiconductor company Semi Scenic, one of the emerging success stories in the Scottish electronics sector, has more than doubled its sales and nearly trebled its operating profit. As the industry globally has experienced a period of growth over the year the sector continues to be extremely competitive. Along with the rapidly increasing push in the Asian Semiconductor manufacturing market towards localisation, the East Kilbride firm's achievement in turning in such healthy figures is even more remarkable.

Semi Scenic, based in the Lanarkshire town's Scottish Enterprise Technology Park, posted turnover for the year to February 2011 of £3.3M, up from £1.5M for the same period last year. Operating profits rose to £725k, up from £270k.

Chief executive Don Nicolson said: "This is a very cyclical industry and our ability to adjust quickly to rapid changes in demand, without compromising on quality, has enabled us to maintain a respectable growth rate. Utilising our technical capabilities to supply a global market has been critical as almost 90% of our revenue came from exports. "

Semi Scenic, which is recognised by major US-based multi-national Lam Research as its preferred legacy etch system refurbishment provider in Europe, employs a 20-strong team of experienced engineers from East Kilbride.

It operates a dedicated facility for supplying refurbished semiconductor systems globally, as well as providing engineering support services at customer sites throughout Europe. Its approach is to provide licensed high-quality support within the semiconductor sector at competitive prices.

Mr. Nicolson added: "Growth in the semiconductor industry resumed over the course of the year although enthusiasm is currently muted at best as consumer spending remains fragile in the most important markets.

"Against that background, the team at Semi Scenic remains one of Scottish engineering's success stories and is to be commended for its continuing dedication and professionalism. We are confident that growth will be maintained in the current year and with that in mind hope to move to a larger facility in the next 6 to 12 months."

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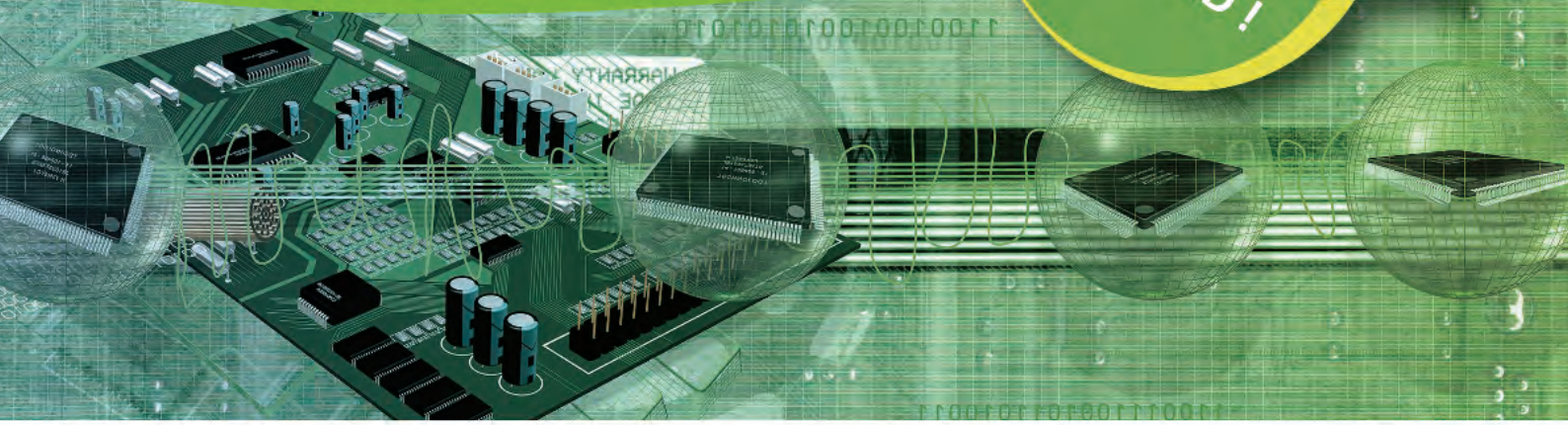

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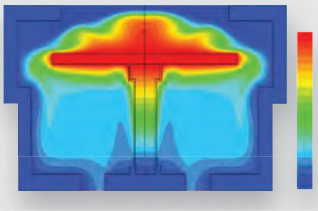

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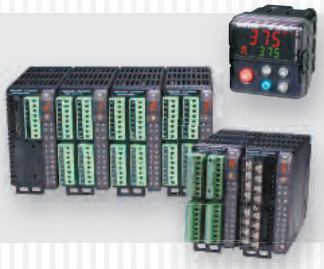

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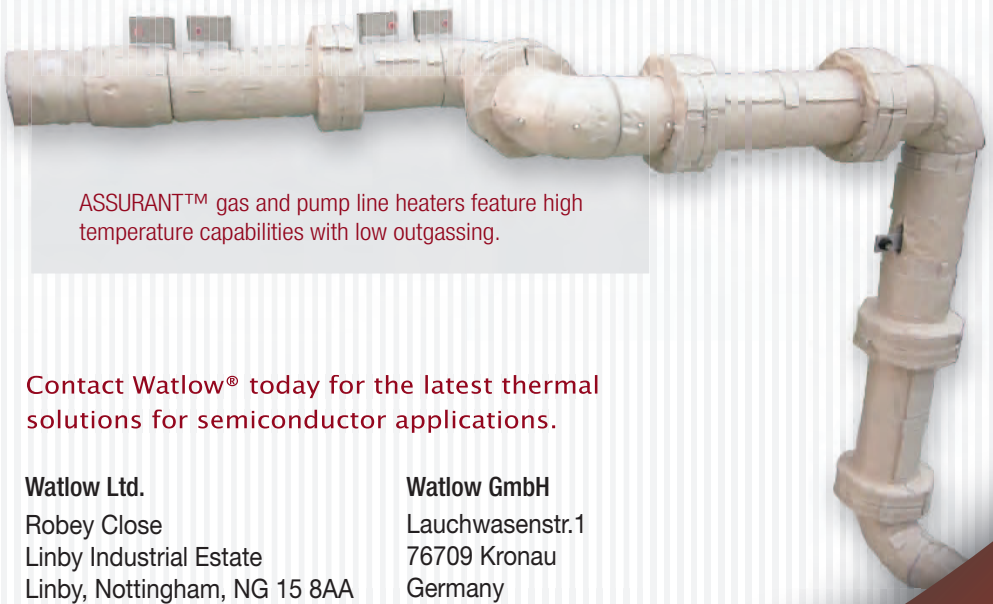

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