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Measurement
Choosing a source measurement unit instrument

Moisture control
Exponential growth in expectations

Manufacturing
Novel 3D integration process flow

News review
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Industry's First Analogue 3-axis, High-g MEMS Accelerometer

EPIGAN

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EpiGaN's power electronic opportunities

An Angel Business Communications publication

Volume 34 Issue II 2012

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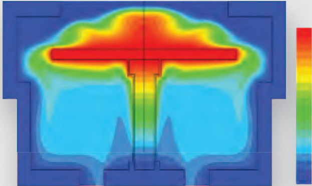

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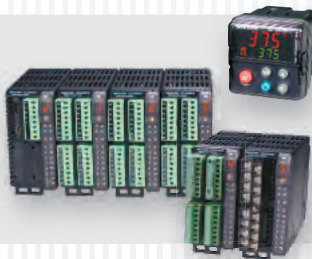

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EuroAsia Semiconductor is now Silicon Semiconductor - a natural evolution

It is with great pleasure that the publishers of EuroAsia Semiconductor announce an evolution in our stable of technology titles. EuroAsia Semiconductor is now Silicon Semiconductor and will make an even greater global impact than ever before.

The semiconductor value chain has gone through enormous change over the last decade as consolidation in a maturing market leaves the global industry with less players and fewer options, as it strives to maintain the scaling innovations of the last half a century. Semiconductors continue to be the major engine for the modern technological world and the next few years will see industry challenges that will redefine the future of technology. Critics have warned semiconductor manufacturers that they are reaching the physical limitations of manufacturing and the industry now faces technical challenges moving beyond 32nm manufacturing. To compound the looming lithographic limits, the wheels have been set in motion to bring in 450mm wafers to maintain the scaling desires of manufacturers. After a few steady years the top players appear to be entering a new phase of competition which is manifesting in a positive increase in expenditure for research, development and manufacturing.

Silicon Semiconductor will be the new name for our title reflecting the simple reality of the innovative engineering and manufacturing that defines this global industry. The semiconductor sector is tipped for strong growth over the next few years and Silicon Semiconductor will be the key information portal for the world's silicon semiconductor community. The new title also brings together our stable of titles, with our sister publication Compound Semiconductor covering manufacturing on compound material substrates.

Silicon Semiconductor will follow the manufacturing trends, industry opportunities and market announcements to provide the decision making information our reader's need to do a difficult job in a challenging industry. Silicon Semiconductor will provide exclusive content on the manufacturing issues affecting the industry wherever in the world it may be. With so many industry challenges on the horizon it is more important than ever to gain a worldwide perspective. Silicon Semiconductor will be a catalyst for a truly global community.

The changing nature of the semiconductor industry has seen geographical changes in the way the global industry is represented both in manufacturing and market place. The current trend sees a great deal of activity continue to migrate to the Asia Pacific region creating new challenges for industry players but no continent stands alone in a global community. On the contrary, some of the strongest innovation continues to emanate from Europe and North America. The semiconductor industry of today may have changed drastically but it is still a growing industry with 2011 seeing tool and materials suppliers reach the 300 billion dollar mark. The industry still continues to grow at a double figure average and the volatility is better managed by fewer players.

All these changes impact the entire value chain and that includes information providers in the sector. Silicon Semiconductor intends to be the key communication platform for the industry moving towards a new future.

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Editor-in-Chief

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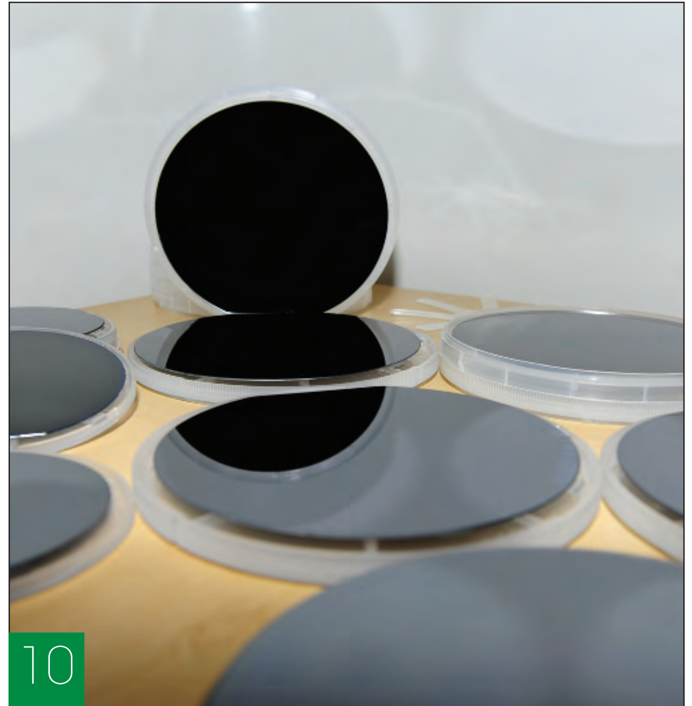
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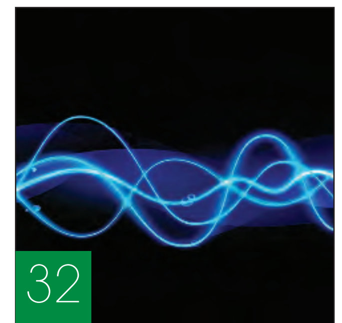
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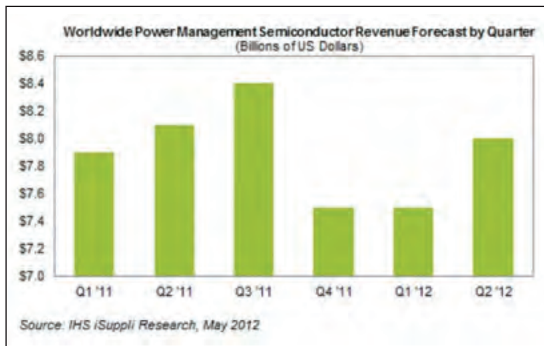
Bellwether market for power management semiconductor chips rebounds

AFTER a drastic decline in the last three months of 2011, the market for power management semiconductors recovered somewhat at the beginning of 2012. The last quarter has seen even better growth, driven primarily by an expansion in the consumer and industrial sectors.



According to the "IHS iSuppli Power Management Tracker" report, revenue for power management semiconductors will reach $8.0 billion in the second quarter, up 6.7 % from $7.5 billion in the first quarter.

IHS believes this increase is the first palpable sign of growth since industry revenue plunged sharply at the end of last year. The market had enjoyed seven straight quarters of growth until the fourth quarter of 2011, when sequential revenue plummeted by a sizable 10.7 %, as shown in the figure below.

However, the market has been on the mend since then, posting flat revenue at the start of the year but not declining further. The projected increase for the second quarter is also expected to continue in the second half of this year. IHS says total power management semiconductor revenue for 2012 is expected to reach $32.8 billion, up 2.8 % from $31.9 billion last year. And although conditions this year will be weaker compared to the strong growth of 2009 and 2010, at least no losses are projected on a yearly basis in 2012. "Power management semiconductors are employed in a broad range of products, with devices ranging from computers, to cell phones, to energy systems all requiring management of their electrical supplies," says Marijana Vukicevic, senior principal analyst for power management at IHS.

"The rising emphasis on portable electronic devices, including the booming sales of media tablets and smartphones, is highlighting the importance of power management semiconductors, which are essential for achieving the heat dissipation, weight and size requirements for such products."

IHS notes that due to seasonality variations, the power management market usually experiences a decline in the fourth quarter of each year. However, the scale of the contraction in the fourth quarter last year was a serious indication of an especially depressed market for these semiconductors.

Several conditions had conspired to bring about the decline. Including, the disruption to manufacturing after the Japan earthquake-tsunami disaster in March and then the heavy floods in Thailand during October. A worldwide slowdown in consumer spending and a pullback in many government-run and supported programs also made matters worse. So, by the end of last year, a decline in growth had been experienced by almost all power management semiconductor markets.

Now though, growth is expected to continue in another area where power management semiconductors have been strong. This is in the industrial electronics and alternative energy (covering wind, solar and geothermal applications) markets.

Jury award $123 million against Mitsubishi

A SILICON VALLEY jury has found Mitsubishi Electric & Electronics USA, Inc. guilty of violating an April 2001 non-disclosure agreement with a small technology company, Grail Semiconductor, Inc. The case involved pioneering technology for a unique memory chip design sold by Mitsubishi's sister company Renesas Electronics Corporation of Tokyo, Japan.

After a three week trial and 4 days of deliberation, the 12 person jury found that Mitsubishi had illegally used and disclosed Grail's confidential technical information for an inductive-capacitive memory chip to its affiliate Mitsubishi-Japan and to the jointly-owned Japanese company, Renesas, awarding $123,898,889 in damages to Grail. Renesas is one of the world's largest manufacturers of memory chips with annual sales topping $8 billion.

The two Renesas products at issue in the case are its SUPER SRAM (also known as Advanced Low Power SRAM) and it's embedded MONOS-FLASH microcontroller units (MCU's). Annual sales of the two product families exceed $4 billion.

"This is a great victory for the little guy against companies like Mitsubishi and Renesas, who, in this case, decided to simply take technology rather than pay for it" said Raymond P. Niro of Niro, Haller & Niro, lead trial counsel in the case.

Attorney's fees and prejudgment interest could be added to the $123,898,889 judgment. "We feel vindicated" said Ron Hofer, CEO of Grail: "the real impact of this case could be a possible injunction against the Mitsubishi companies and Renesas prohibiting use of our technology." Grail also has a separate suit against Renesas for patent infringement pending in Federal Court in San Francisco.

Intel invests over $40m to push innovation

INTEL is to invest more than $40 million over the next five years in a worldwide network of university research communities known as Intel Collaborative Research Institutes" (ICRI).

The ICRI program is based on the U.S.-based Intel Science and Technology Centres (ISTCs), and will bring together experts from academia and industry to help explore and invent in the next generation of semiconductor technologies.

"The new Intel Collaborative Research Institute program underscores our commitment to establishing and funding collaborative university research to fuel global innovation in key areas and help address some of today's most challenging problems," says Justin Rattner, chief technology officer at Intel.

"Forming a multidisciplinary community of Intel, faculty and graduate student researchers from around the world will lead to fundamental breakthroughs in some of the most difficult and vexing areas of computing technology," he adds.

The three ICRIs will collaborate with their own multi-university communities and other ICRIs, as well as the U.S.-based ISTCs.

Two previously established centres are being incorporated into the ICRI program. These are the Intel Visual Computing Institute (Saarland University) and the Intel-NTU Connected Context Computing Centre (National Taiwan University).

Each institute will specialise in a particular area and use its research to focus on the unique environments within its region, country and area of research.

The three new ICRIs include the ICRI for Sustainable Connected Cities based in the United Kingdom. This joint collaboration between Intel, Imperial College London and University College London aims to address challenging social, economic and environmental problems of city life with computing technology. Using London as a test bed, the scientists will explore technologies to make cities more aware and adaptive by harnessing real-time user and city infrastructure data.

Through a city urban cloud platform, the city managers could perform real-time city optimisations such as predicting the effects of extreme weather events on the city's water and energy supplies. This is expected to result in the delivery of near-real-time information to citizens through citywide displays and mobile applications.

One of the other collaborators is the ICRI for Secure Computing, Germany. At this Institute, Intel and the Technische Universität Darmstadt will explore ways to advance the trustworthiness of mobile and embedded devices and ecosystems.

In the development of secure, car-to-device communications for added driver safety, using new approaches to secure mobile commerce, and a better understanding of privacy and its various implementations. By grounding the research in the needs of future users, the institute will then research software and hardware to enable robust systems suited to these applications.

The final institute, the ICRI for Computational Intelligence is based in Israel. It is a partnership between the Technion-Israel Institute of Technology in Haifa and the Hebrew University in Jerusalem. The ICRI will explore ways to enable computing systems to augment human capabilities in a wide array of complex tasks.

Large assembly and test facility select Rudolph to meet demand

Rudolph Technologies, Inc., has announced that a large OSAT (outsourced semiconductor assembly and test) company has placed orders for 14 NSX Series 320 Inspection Systems. The NSX Systems, scheduled for Q2 2012 installation, will be used for inspection in multiple steps during wafer-level chip-scale packaging (WLCSP) processes.

Nathan Little, vice president and general manager of Rudolph's Inspection Business, stated, "As confirmed by our strong order book for this new tool, packaging and test houses want to take advantage of the latest-generation inspection equipment to maximize throughput and productivity.

The NSX320 System performs defect inspection, 2D bump metrology and acquires on-the-fly defect images for maximum productivity and flexibility. In addition, WLCSP requires flexibility for handling substrates in a variety of formats while collecting detailed defect and 2D metrology information during the inspection process; the NSX320 System incorporates whole wafer and film frame handling solutions to address this requirement."

The NSX320 System was selected after a competitive evaluation for its high speed and efficient, easy-to-use operating procedures, which delivered the highest productivity and lowest cost-of-ownership of all the tools considered.

"This order is evidence of the leading position the NSX320 Inspection System has established in the rapidly growing market for back-end inspection," Little added. "Rudolph's R&D investments in technology-leading products and the history we have with our back-end customers give us the ability to respond to the changing requirements in this important market segment."

Apple & Samsung Standalone

THE good news is that the smartphone market grew by a decent 44.4% year over year in the last quarter, according to market research company Forward Concepts.

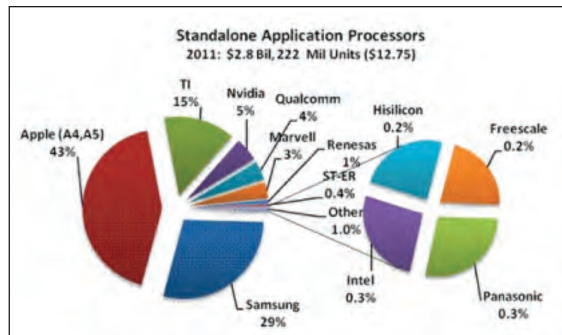
On the down side, the firm's annual market research report, "Cellular Handset & Tablet Chip Markets '12," says that smartphone Q1 2012 shipments also declined to only 6.9% over the previous quarter.

Global sales of mobile phones (budget, midrange, feature and smartphones) to end users reached 379 million units in the first quarter of 2012, a 9% decline from the first quarter of 2011.

High smartphone demand continued to drive mobile device market growth, reaching 139 million units in the first quarter of 2012, a hefty 37% of the global cell phone market.

And Apple and Samsung, raised their combined share in the smartphone market to 45.7%, up from 30% in the first quarter of 2011, widening their lead over Nokia , which saw its smartphone market share drop to a mere 8.6%.

In the first quarter of 2012, Apple iPADs achieved a 59.3% share of the media tablet market, including the sub-$199 Amazon Kindle and Barnes & Noble Nook.



Also, Apple's multimode LTE "iPAD3" has enabled the company to offer the iPAD2 at lower prices, causing a decline in Android tablet shipments.

E-reader manufacturers shipped only 1.4 million units in the first quarter of 2012, down from 4.2 million units shipped in the final quarter of 2011.

According to the principal author of the report, Carter L. Horney, "Global sales of mobile devices declined in Q1 more than expected due to a slowdown in demand from the emerging regions. All vendors were impacted at different levels; however, Chinese white-box vendors suffered the most with bloated inventories."
Among the top 10 cellphone vendors, Nokia, Samsung and Apple topped 2011 unit shipments while Chinese suppliers Huawei, ZTE and TCL also moved into the top ten.

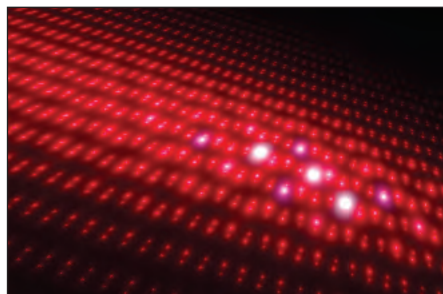
In terms of revenue, Apple led over Samsung and Nokia in the smartphone market. But Samsung beat Nokia in overall cell phone unit shipments in Q1/2012, with Apple taking 3rd place.

Although Baseband chips of several types constitute the largest non-memory cell phone chip market at $15.9 billion for 2011, there are other multi-billion-dollar cell phone chip markets. These include $5.5 billion for power management units, $3.7 billion for RF transceivers, $3.6 billion for RF power amplifiers, $2.9 billion for image sensors, $2.8 billion for standalone application processors, and $2.7 billion for touch-screen controllers.

CMOS based process revealed

X-FAB SILICON FOUNDRIES has unveiled the XU035, a new CMOS-based process for ultra-high-voltage (UHV) consumer applications. These include AC LED lighting, chargers with no-load power consumption and other power conversion and control applications.

The new XU035 process provides low specific On-resistance for 700V power devices and is claimed to enable the most cost-effective solutions for consumer applications.



X-FAB says its cost-competitive process architecture and comprehensive design support enables first-time-right designs, enabling fast time to market. The new XU035 process includes multiple cost-effective features such as a single poly and single 5V gate oxide architecture, 8-inch bulk starting material, optional third routing and power metals and optional MIM capacitors. It also includes a depletion transistor and a high-resistive poly module. X-FAB says that depending on the process module combination chosen , the total mask count range of 13 to 18 is the foundry industry's lowest.

Besides the 700V N&PMOS, DMOS and depletion transistors with RDSON as low as 15Ω mm^2 and 20V and 40V devices with floating high-side capabilities, XU035 process users can select from a wide spectrum of analogue passive devices . These include UHV resistors, MOS and MIM capacitors and protection diodes The XU035 platform comes with comprehensive X-FAB design support including PDKs for all major design environments, precise Spectre and H-Spice models, digital libraries and 2kV ESD support. Commenting on the XU035 process for mass-market applications, X-FAB's Technical Marketing Manager Volker Herbig says, "Government regulation and increasing energy pricing mean that energy conservation is becoming an important aspect in the daily lives of people around the world."

"Our new XU035 process enables our customers to compete effectively in energy-efficiency applications like LED lighting and phone chargers that require ultra-low standby power. It provides the most cost-effective process for targeting the vast high-volume consumer space, where price and time to market are primary considerations."

The XU035 process will be available for tape-ins of prototypes and risk production in June 2012.

Industry's First Analogue 3-axis, High-g MEMS Accelerometer

Analog Devices, Inc. (ADI) has revealed what it claims is the industry's first commercially available analogue, 3-axis, high-g MEMS accelerometer.

The ADXL377 measures acceleration of high-impact events resulting from shock and vibration, within a range of ± 200 g with no signal saturation.

This measurement range, combined with an analogue output that continuously captures impact data, makes the ADXL377 a good sensor for contact sports where the detection of concussive forces can reveal indictors of Traumatic Brain Injury (TBI).

With a bandwidth of 1600Hz, the ADXL377 is also suited for use in industrial equipment where shock levels must be closely monitored. The accelerometer also eliminates the need for alignment and the placement of orthogonal sensors, which significantly simplifies design. ADI says the board space required is reduced by up to five times compared to typical solutions requiring multiple, single-axis accelerometers. The ADXL377 has also been designed for incorporation into the IZOD 2012 INDYCAR Series driver impact safety system. INDYCAR worked in closely with Analog Devices at the ADXL377 product definition phase.

The resulting device allowed INDYCAR to upgrade the sensors located in its communications earpieces, which are used to measure driver impacts triggered by collisions during practice, time trials and during races, according to Jeff Horton, director of engineering for INDYCAR.

"The new Analog Devices ADXL377 3-axis accelerometer is going to be a great addition to our ear sensor program," says Horton.

"Not only will the smaller size greatly reduce the manufacturing time needed to place the components into the custom ear moulds that we make for each of the drivers, it also will allow us to place the accelerometer closer to the ear canal opening which should help with the coupling of the accelerometer to the driver's head for a more accurate reading. In the past we had to use three separate ICs in each ear to obtain the same amount of data."

"With TBI now a serious medical concern in many facets of life, from athletes and workers to military personnel, ADI is helping customers design smaller, more accurate and simpler impact systems," adds Mark Martin, vice president and general manager, MEMS/Sensors group, Analog Devices.

"Because so many of these applications require extreme mobility, the ability to eliminate orthogonal sensors while simultaneously lowering energy consumption means that these battery-operated devices can run longer between charges."

Renesas electronics and TSMC collaborate

RENESAS ELECTRONICS CORPORATION and TSMC have announced that they have signed an agreement to extend their microcontroller (MCU) technology collaboration to 40 nanometer (nm) embedded flash (eFlash) process technology for manufacturing MCU products used in next-generation automotive and consumer applications such as home appliances.

Renesas previously agreed to outsource MCUs to TSMC using 90nm eFlash process technology. Under the 40nm MCU collaboration, Renesas will outsource MCU production at 40nm and future technologies.

Renesas and TSMC will collaborate to lead in advanced technologies for MCU platform and production by combining Renesas' MONOS (Metal-Oxide-Nitride-Oxide-Silicon) technology supporting both high reliability and high speed, and high-quality technical support with TSMC's advanced CMOS process technologies and flexible production capacity.

Furthermore, by making the MONOS process platform available to other semiconductor suppliers around the world (including fabless companies and IDMs), Renesas and TSMC aim to set up an ecosystem and further widen the customer base.

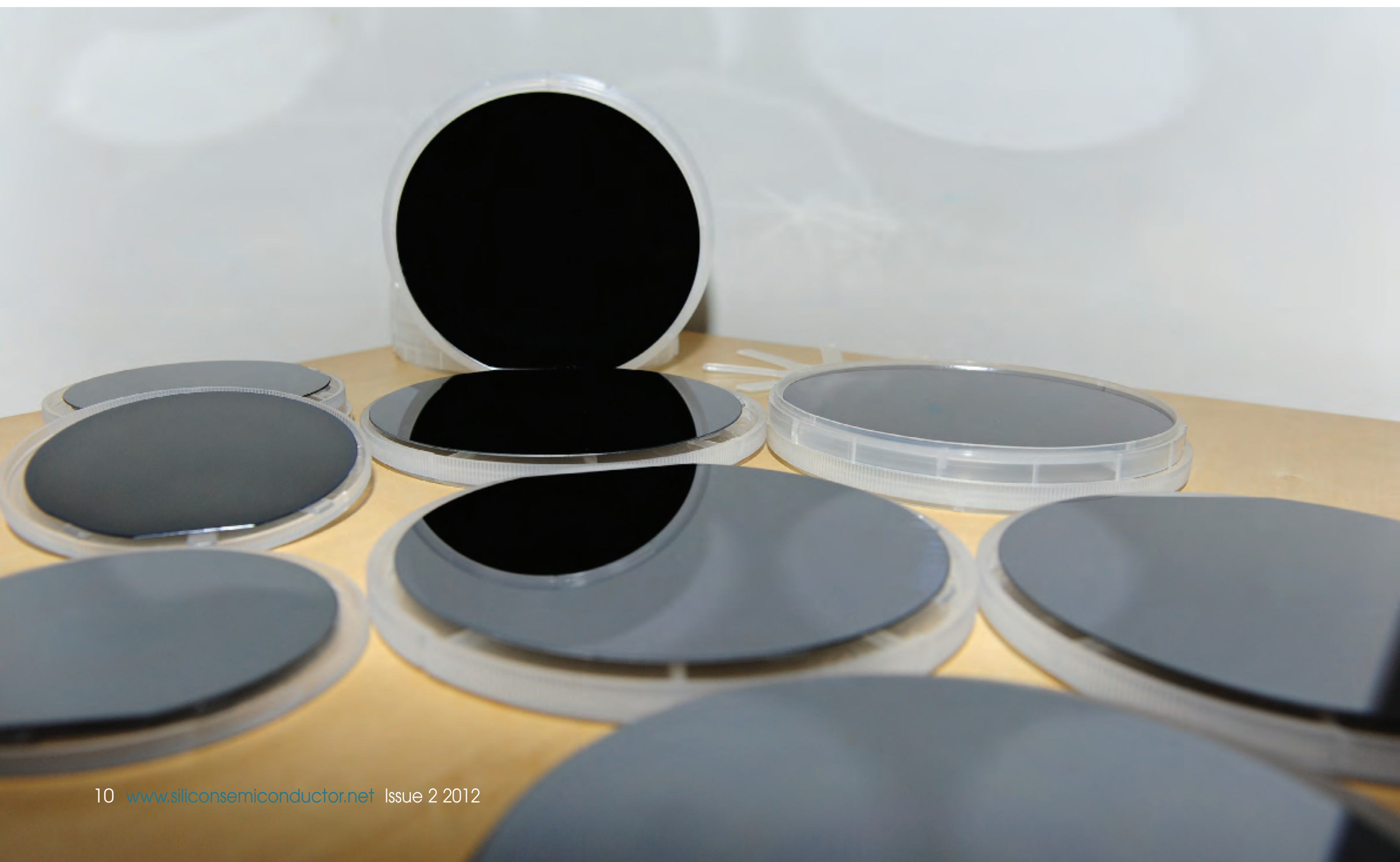
"In order for us to achieve further global growth, we are confident that TSMC will provide us with significant benefits in accelerated time-to-volume production and maximum flexibility in addressing the volatile fluctuation of the market demand," said Shinichi Iwamoto, Senior Vice President of Renesas Electronics Corporation. "Based on what we have learned from the Great East Japan Earthquake last year, which brought major impacts to several of our manufacturing sites and our customers businesses, we have been accelerating the construction of the "fab network" as part of the company's business continuity plan (BCP). By integrating both companies' world-leading technologies through this collaboration, we will construct a supply structure which secures consistent supply for our customers and also drive the market as a leading MCU supplier aiming to set up an ecosystem for MCUs."

"Renesas is one of the leaders in the MCU market and the collaboration will help deliver the performance Renesas needs for new production introduction with the level of quality and reliability its customers have come to expect," said Jason Chen, Senior Vice President of Worldwide Sales and Marketing at TSMC.

Founded in 2010 as a spin-off from Belgian research centre Imec, EpiGaN has become a key player in GaN-on-Si semiconductors. Thanks to its wide bandgap, combined with other performance features, GaN shows superior efficiency at high voltages. This is paving the way for replacing conventional silicon power semiconductors by GaN HEMTs (high-electron mobility transistor) Such GaN devices will enable more efficient power converters, power supplies, motor drives, solar inverters and transport systems – all with a smaller environmental footprint.
Just last month, on May 23, EpiGaN officially opened its new volume production facility at the Research Campus Hasselt (RCH) in Belgium, located in the busy European high-tech triangle Eindhoven-Leuven-Aachen. This campus offers the framework for cleanroom facilities as required for the production of GaN-on-Si.

EpiGaN Creating the Future

Compound semiconductors have long been touted as a disruptive force to traditional semiconductor manufacturing but have often ended up with niche markets as superior speeds have not been matched with cost differences. The last decade has seen a surge in compound semiconductor potential and here we profile a new company that quickly developed a reputation for power electronics based on Gallium Nitride (GaN) and become an integral part of European research efforts.



EpiGaN is currently offering state-of-the-art GaN epitaxial layers deposited crack-free, on Si up to 150 mm or, for specific applications, on SiC. Wafer diameters of 200mm are under development. The availability of large wafers to be processed in existing Si CMOS fabs explains how GaN-on-silicon technology excels at combining affordability with great performance.

The Promise of GaN

With its superior properties, GaN promises to be a suitable material for power switching devices operating at significantly higher frequencies without suffering from major losses. This is due to the drastically lower on-state resistance of GaN power transistors, combined with considerably reduced in/output capacitances. The higher switching frequency substantially reduces the volume of accompanying passive components such as inductors, current transformers and capacitors.

Thus, in the future, the volume of power systems will be smaller and they will be more lightweight. In the long run, GaN power electronics will combine these significantly improved operational properties with lower costs. The efficiency of present systems is largely limited by the active components used.

To accelerate the progress on this future-oriented, energy-saving power technology, the EU has established a three-year research project, called “HiPoSwitch”. EpiGaN is substantially participating in the effort.

HiPoSwitch has a total budget of 5.6 million euros. To this, the EU is contributing about 3.6 million Euros. Eight European program partners are covering the complete value chain, from academic research and development (Ferdinand-Braun-Institute, Leibniz-Institute fuer Hoechstfrequenztechnik, Slovak Academy of Sciences, Vienna University of Technology; University of Padua, to industrial application (AIXTRON SE, Artesyn Austria, EpiGaN, and Infineon Technologies Austria. The objective is to make GaN power transistors and 200mm GaN-on-silicon substrates commercially available and marketable world-wide. HiPoSwitch is coordinated by the Berlin-based Ferdinand-Braun-Institute.

The European Space Agency (ESA) has also invested significant levels of funding in establishing a European value chain of space worthy GaN-devices, in particular within the GREAT2 project. Today, they also support EpiGaN in the establishment of a European GaN material source through a three years contract, aiming at material production both either RF or High Voltage applications for space suppliers.

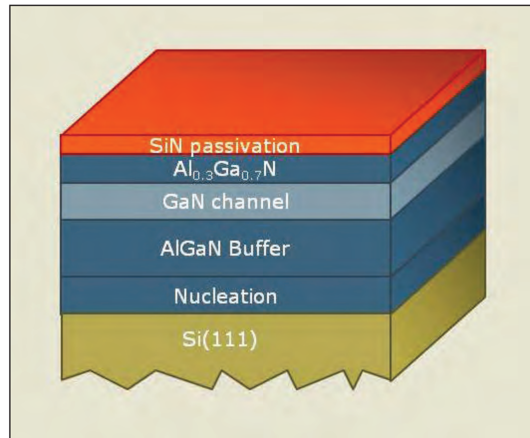


Fig 1: 150 mm and 4-inch GaN-on-silicon epiwafers

All these efforts cater to the promise that transistors based on GaN-on-silicon could grab a major share of the power device market. Converting their potential into success hinges on scaling production to the handling large wafer sizes and employing appropriate passivation techniques - according to EpiGaN founders Marianne Germain, Joff Derluyn and Stefan Degroote.

There is a tremendous opportunity, the EpiGan founders say, for realising substantial reductions in energy losses associated with AC/DC and DC/DC conversion. If a new generation of electronic devices can combine higher power levels with lower switching losses at higher operating frequencies, they will boost the efficiency of power systems, while trimming their size and weight.

EpiGaN: Making Nitrides Affordable

As wide band gap semiconductors GaN-on-silicon devices belong to a superior class of materials: One of their biggest advantages is their high breakdown voltage, which stems from a field strength that is an order of magnitude higher than that of silicon. Due to the high carrier mobility and concentration associated with the two-dimensional electron gas (2DEG) of the AlGaN/GaN heterostructure, nitride devices in switching applications also combine a low on-resistance with high switching speed. Their wide band gap properties enable them to operate at high temperatures.

Development of nitride power devices has been underway for more than a decade, and their progress has enabled today’s switching devices to outperform their silicon rivals. In the performance stakes at very high voltages (>1200V), SiC is a tougher opponent, but GaN more than holds its own. GaN-on-silicon is the most cost-efficient wide-band-gap technology. It has developed to a point where it is feasible to deposit advanced

The European Space Agency (ESA) has also invested significant levels of funding in establishing a European value chain of space worthy GaN-devices, in particular within the GREAT2 project

heterostructures on silicon substrates up to 150mm in diameter. In the near future this growth process will be extended to 200mm silicon. There is also an opportunity to develop process compatibility with standard CMOS technology. This would open the door to further cost reduction by enabling these wafers to be put through lines at 200mm silicon labs operating around the globe.

No wonder that GaN power electronics technology is lately attracting increasing interest. But no one is yet to deliver the real commercial breakthrough - a reliable device operating at 600V. One of the challenges is to establish a compound semiconductor technology in a field where silicon dominates, and many potential users have been scarred by the experience of SiC. Although the performance of SiC diodes is attractive for power converter manufacturers, they are too pricey. In addition, until recently these diodes could not be paired with SiC transistors - which is detrimental to the uptake of this first-on-the-market wide band gap solution.

Another reason behind the lack of a commercially attractive and reliable 600V and above device is that it is tough to manufacture GaN-on-silicon epitaxial structures, which are the starting point for making power electronics.

This is the challenge that EpiGaN has set out to master. The company was formed as a spin-off from the large international nano-electronics research centre located in Leuven, Belgium. EpiGaN is built on its founders' expertise developed at Imec, where they were involved in GaN research since 2001. Some of their key successes include the world's first low-sheet-resistivity, 150 mm HEMT structures in 2006, and the first GaN-on-silicon 200 mm epi-wafers, a feat achieved in partnership with the MOCVD toolmaker Aixtron.

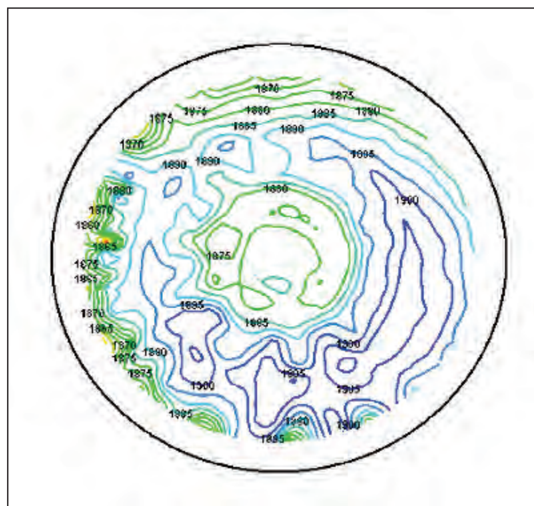


Fig 2: SiN/AlN/GaN heterostructure

EpiGaN's approach differs from that of several other players, which employ SiC as the substrate for their nitride devices. EpiGaN focuses on GaN-on-silicon, due to its cost advantage. Initially, the company developed material for RF devices (such as epi-wafers for RF applications). However, given the strengths of GaN-on-silicon for power electronics, it was obvious to switch target the potentially lucrative power semiconductor market.

The commercial prospects of GaN on silicon have attracted a strong investor group, among them Robert Bosch Venture Capital, Capricorn Cleantech fund and LRM. These investments have been used to set-up the plant for producing GaN epi-wafers by MOCVD, which was started up in May 2012.

Taking out the Strain

EpiGaN's epitaxial growth process tackles the grid strain that arises when GaN is deposited on silicon. The two materials show different crystalline properties and thermal expansion coefficients. Left unchecked, this can lead to unchecked strain in the epi-layer and substrate that can ultimately cause the wafer to bow and even crack.

Carefully managing this strain yields wafers suitable for passing through regular silicon processing lines. EpiGaN now manufactures 150mm epi-wafers with a bow well below 50μm - typically 20 to 30μm, depending on wafer specs. Uniformity, in terms of standard deviation of either layer thickness or electrical characteristic, is typically better than 3 percent.

Stress engineering certainly is a challenging aspect of forming GaN-on-Si. An even more challenging issue is passivation of surface states. As a piezoelectric material GaN has an excellent high-electron concentration associated with high electron mobility - obtained without extra doping.

But there is a significant price to pay: an extreme sensitivity governing device characteristics, such as current density and threshold voltage on the filling of those surface states, which have a density comparable to that found in the channel. If passivation is poor, the device's dynamic behaviour suffers. To combat this so-called dispersion problem, devices must be processed in a carefully controlled manner using high-quality epi-wafers, because this leads to optimized buffers and controlled surface states.

Uncontrolled charging or discharging of these

surface states - which can be modified during processing and device operation - can severely degrade the dynamic properties of the device. To prevent this EpiGan deposits a unique in-situ SiN capping layer, which is grown by MOCVD as part of the epitaxy process on top of HEMT epi-wafers. The interface between this capping layer and the top nitride surface is incredibly smooth, and it enables perfect passivation of surface states (Figure 1).

The capping layer can properly control the filling of the surface states during device operation. It is believed that SiN can provide enough charge to neutralize the surface charge of the AlGaN barrier layer so that its surface potential no longer contributes to 2DEG depletion. In addition, the SiN layer aids device stability at elevated temperatures.

The in-situ deposited SiN films can also lead to drastic reduction of the channel resistance, This enables adjusting the top part of the FET so that it can meet particular device specifications. GaN FETs are lateral devices, and optimizing their performance demands a trimming of conduction losses. This means that, for switching applications, aluminium-rich barriers are preferred in a typical AlGaN/GaN structure, because it yields a higher piezoelectric field, higher current density and lower specific on-resistance.

One of the major benefits of the SiN cap layer is that it enables higher aluminium concentration without any significant material degradation. This is not the case in transistor structures with an uncapped or GaN-capped AlGaN/GaN 2DEG, where relaxation of the strained top AlGaN layer typically prevents the obtention of a low channel resistivity.

For the SiN/AIN/AlGaN design detailed in Figure 2, sheet resistance falls to 235Ω/· with EpiGaN passivation technology. In this structure, Hall measurements indicate that the electron sheet concentration is 2.15 x 10^{11} cm^{-2} and electron mobility is 1,250 cm^2/Vs. These are very promising values and they enable the fabrication of devices with high transconductance, even when the gate length is relatively large. They highlight the potential of this device for high-frequency operation.

The neutralization of surface charges provided by the SiN layer also unlocks the door to an innovative approach for making enhancement-mode devices. This form of transistor, which is required for power converters, can be made by combining a thin AlGaN barrier layer with local removal of SiN under the gate. By offering a very smooth, clean and uniform protecting surface for active layers, the use of in-situ SiN also enhances the controllability of the device manufacture , further to reduce the cross-contamination potential issues when using a III-V material in a Si CMOS fab. The excellent uniformity of the in-situ SiN layer is shown on Figure 3.

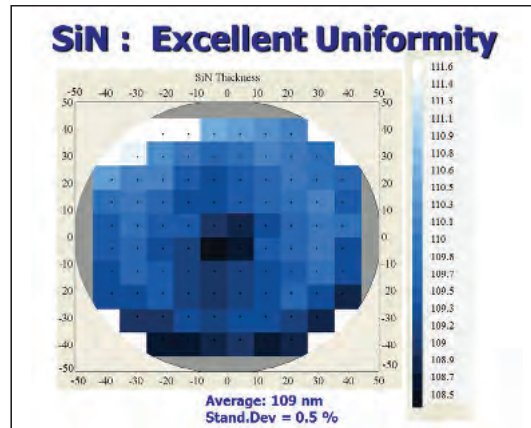


Fig 3: The uniformity of the in-situ SiN layer

From 600 V to 1.2 kV

Today EpiGaN is able to manufacture GaN-on-silicon wafers with a breakdown voltage above 600V and a very low leakage current. But this is by no means the upper limit for the breakdown voltage of these devices. Recent work has yielded FETs with a breakdown above 2kV.

GaN can already be used to make power products in the 30 to 200V and 600V range, and it will not be long before variants operating at 1,200V can be added to the list. This will pave the way for the replacement of two silicon MOSFETs with a single GaN HEMT - a move that will trim the cost and weight of power converters. To make this happen, EpiGaN is focusing on the development of 1,200V epi-wafers on 150mm silicon.

Future products based on this process will complement the existing range of 4-inch and 150-mm epi-wafers for high-voltage and/or high-frequency applications. The production capacity for these products is currently being ramped up at the new Hasselt facility. In parallel, manufacturing processes for 200mm GaN epi-wafers are being developed.

Although today the demand for these larger epi-wafers is weaker than that for those with diameters of 150mm or less, larger sizes will spur a cost reduction and enable GaN to deliver success in a field where, until now, no compound semiconductor has seriously challenged silicon.

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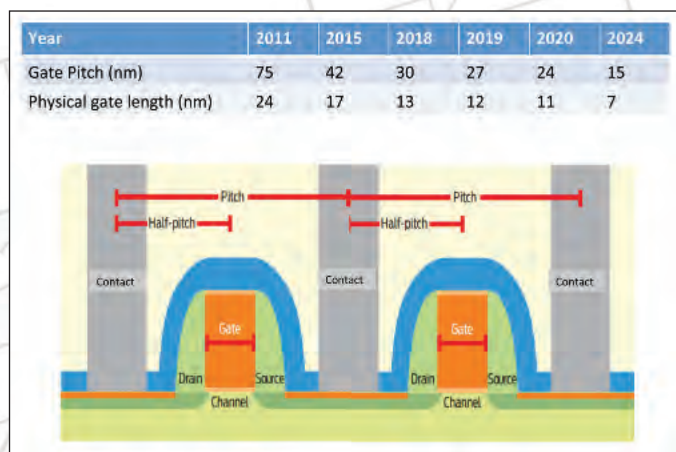
Today EpiGaN is able to manufacture GaN-on-silicon wafers with a breakdown voltage above 600V and a very low leakage current

III-Vs and the silicon roadmap

Silicon foundries could switch production from silicon MOSFETs to those based on III-Vs and germanium by the end of this decade. Making this transition is far from trivial, but progress is being made in gate dielectrics, contact resistance, peak current flow and material quality. **Richard Stevenson reports.**

Time and time again, critics have claimed that there will soon come an end to the shrinking of silicon transistors to smaller dimensions. Some have argued that photo-lithography cannot extend beyond optical wavelengths – but tools have been built that can do just that; others have warned that electrons cannot zip about fast enough when transistors reach the nanoscale – but adding a little strain into the material has put that issue to bed; while others have pointed out that high leakage currents will put an end to device scaling – but this issue has not been a show-stopper, thanks to a switch from silicon dioxide to high-*k* dielectrics, such as hafnium dioxide.

Today, claims that the days of the silicon transistor are numbered are still being made – and there's a good chance that this time the critics could well be right. That's because this belief is not just held by those outside the silicon industry, but also some within it:



Year	2011	2015	2018	2019	2020	2024
Gate Pitch (nm)	75	42	30	27	24	15
Physical gate length (nm)	24	17	13	12	11	7

Figure 1. According to the ITRS roadmap, between 2011 and 2024 reductions in gate pitch will be more rapid than those in gate length

Alternatives to silicon are now on the International Technology Roadmap for Semiconductors (ITRS), with III-Vs and germanium predicted to make an impact at the 11 nm node that could be rolled out in 2015.

Iain Thayne from the University of Glasgow, UK, explained the reason for the potential invasion of these new materials into silicon lines at the recent CS Europe conference in Frankfurt, Germany. Thayne, whose efforts at developing III-V transistors initially focused on RF and millimetre-wave front-end applications, argued that compound semiconductors must be introduced to maintain performance as dimensions are reduced.

"Increasing the density of transistors in silicon leads to heating, which will soon approach an air-conditioning limit," said Thayne. He explained that preventing over-heating in the circuits that will be built with tomorrow's transistors requires a reduction in the voltage of the power supply, but no compromise in performance. The only way to satisfy these conditions is to replace silicon transistors with those based on III-Vs and germanium.

He also pointed out that scaling efforts are focused on increasing the density of transistors. Although every new node has a shorter gate length, it also has a reduction in gate pitch, which is scaled even more aggressively (see Figure 1).

Sceptics within the silicon industry have argued that III-Vs will never be suitable for logic circuits, because the drive currents produced by this class of transistor are not high enough, due to the low densities of states associated with compound semiconductors. But Thayne's colleague Asen Asenov has spotted fundamental flaws in this argument: Although the low density of states in III-Vs leads to a lower effective capacitance, these materials combine a high mobility with a low mass, resulting in the injection of carriers with high velocities and increased 'ballisticity'. What's more, the lower density of states means that

carriers are injected with a higher velocity, thanks to their higher energy; and due to superior mobility, these materials can trim access resistance and thereby boost the efficiency of gate modulation.

Material attributes

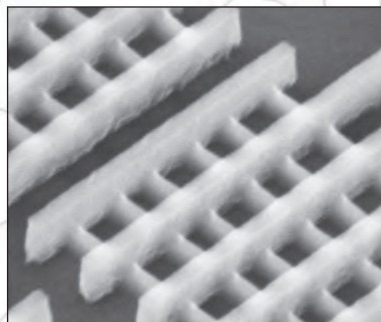
To optimise III-V MOSFETs, developers must select a material that combines a high carrier velocity with the potential to yield a device with a low operating voltage. According to Thayne, as gate pitch decreases from 75 nm to 15 nm (the value expected in 2024), channel concentration may decrease from 8.5 x 10^{12} cm^{-2} to 5.1 x 10^{12} cm^{-2} while the carrier velocity will increase from 1.3 x 10^5 ms^{-1} to 3.5 x 10^5 ms^{-1}. The most promising materials for meeting those requirements are alloys of InGaAs, and work from MIT suggests that $In_{0.7}Ga_{0.3}As$ channels can produce injection velocities above 3 x 10^5 ms^{-1} at gate lengths below 20 nm.

Thayne discussed additional requirements for the introduction of III-V MOSFETs for logic applications. He said that transistors will need to have a sub-threshold swing of 75 mV/decade so that they could be turned-off easily, and they will probably need to be built with a non-planar architecture, such as the 'Ivy Gate' tri-gate structure employed by Intel for the manufacture of transistors at the 22 nm node. In addition, due to scaling, source and drain dimensions will have to be just a few nanometres, which could lead to an unwanted hike in contact resistance.

The Glasgow team, which has been involved in both the European Dual Logic programme and efforts led by the Semiconductor Research Corporation Non-Classical CMOS Research Center, has focused its efforts in three directions: Gate stack improvements, resolving issues related to the scaling of source and drain contacts, and the development of silicon compatible process flows for III-V MOSFETs.

Efforts have centred on a flatband architecture MOSFET (see Figure 2). This is similar to a HEMT, according to Thayne, because there is delta-doping in a high bandgap material, leading to the transfer of electrons to a low bandgap channel where they create a high-mobility, two-dimensional electron gas. If a high work-function gate metal is formed on top of the dielectric, depletion occurs, driving the device into an off-state at zero bias. Forward biasing of the gate repopulates the channel with carriers.

This MOSFET architecture is claimed to have two key strengths: Immunity to short-channel effects, due to a high bandgap lower barrier; and high mobility, thanks to a combination of no doping in the channel, low interface roughness scattering and a low resistance of the source and drain extension access regions.



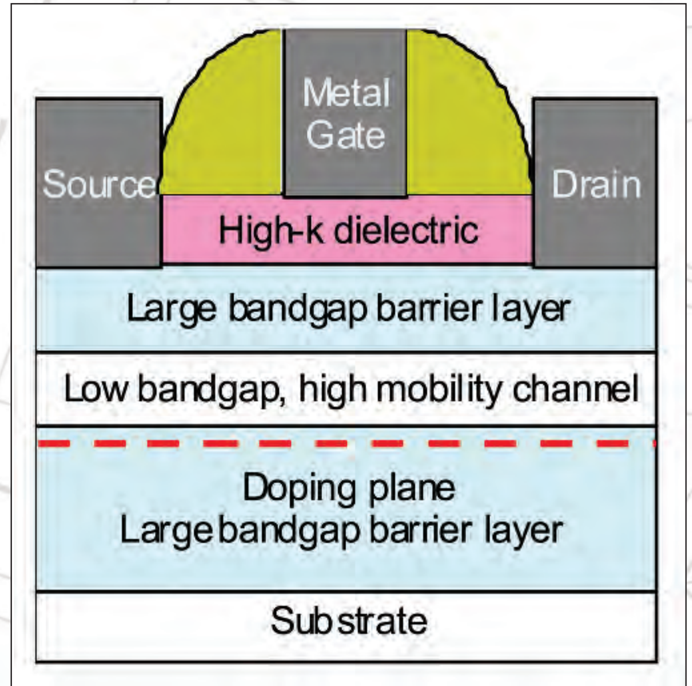


Figure 2. Ian Thayne's group at the University of Glasgow, UK, has developed III-V MOSFETs with a flatband architecture

When the team started developing III-V MOSFETs at the beginning of the previous decade, efforts were partly devoted to establishing a good gate stack. Initially they employed a Veeco Gen III dual chamber MBE system to grow III-V layers by MBE on a semi-insulating GaAs substrate, before transferring the sample under vacuum to a second chamber, where they added a Ga_20 template and a GdGaO layer. The flatband III-V MOSFETs fabricated from these wafers produced mobilities in excess of 5000 cm^2 $V^{-1}s^{-1}$ at sheet carrier densities above 2 x 10^{12} cm^{-2}, and transistors with a 1 μm gate length had a transconductance of 357 $\mu S/\mu m$ and a sub-threshold swing of 68 mV/decade.

To increase injection velocity, the researchers switched to $In_{0.53}Ga_{0.47}As$ channels and Al_2O_3 dielectrics, which were deposited by a 60-cycle atomic layer deposition process. The benefits of this new structure included gains in mobility – at an electron density of 2 x 10^{12} cm^{-2} mobility topped 6000 cm^2 $V^{-1}s^{-1}$.

For surface-channel transistors with a 1 μm gate and a 2.5 nm-thick Al_2O_3 dielectric, transconductance hit 432 $\mu S/\mu m$, but the sub-threshold swing reached 150 mV/decade.

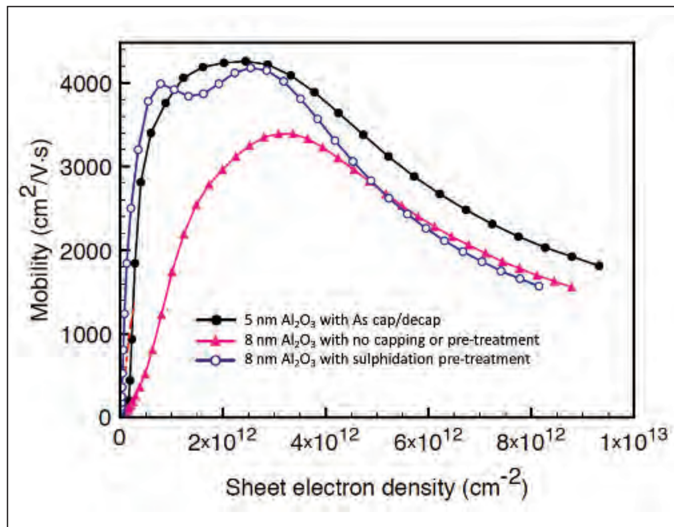


Figure 3. A sulphidation process developed by researchers at the Tyndall Institute can offset most of the degradation in mobility resulting from the removal of an arsenic cap. This is a promising result for non-planar transistors, which will not have pristine interfaces

Intel's move from planar transistors to three-dimensional varaints points the way to production of non-planar devices, which will not have pristine interfaces. To consider the implications of this trend, Thayne, in partnership with Paul McIntyre at Stanford and Paul Hurley at the Tyndall Institute, has looked at the impact of various treatments of transistor performance.

The team compared three wafers. Two of them were removed from the MBE chamber after the growth of III-V materials: A gate dielectric was added to one wafer without any intermediate surface treatment, so air-exposed oxides were likely to be present in the dielectric-semiconductor interface; and a optimised sulphidation treatment was applied to the other prior to deposition of the high-*k* dielectric. The third wafer had as arsenic cap deposited in the MBE chamber to prevent oxidation in air. This cap was removed in the atomic layer deposition tool at Stanford, enabling the gate deposition on a pristine surface. Measurements of the mobility of MOSFETs made from these wafers reveals that it is possible to produce interfaces as good as those on pristine surfaces if a sulphidation process is performed (see Figure 3).

The second issue that Thayne and his co-workers have investigated is the fabrication of low resistance source and drain contacts with dimensions of just a few nanometres. The ITRS roadmap dictates that as gate pitch is reduced from 75 nm in 2011 to just 15 nm in 2024, source and drain contacts must be trimmed from 21 nm to 2 nm, while source and drain resistances are cut from 160 Ωμm to 110 Ωμm.

'Traditional' approaches will not succeed – experiments and simulations reveal that contact resistance rises rapidly when the contact size enters the nanoscale. Several groups have recently developed different approaches for overcoming this problem, including that from Glasgow, which has turned to NiInAs to fabricate an ultra-low resistance, shallow, metallic source-drain. According to Thayne, this is the first source-drain technology that can meet the most aggressive ITRS specification for the 12 nm technology node, which corresponds to a gate pitch of 27 nm.

The third strand of research at the Nanoelectronics Research Centre is the development of approaches for forming fully self-aligned III-V MOSFETs with silicon compatible process flows. The team has pioneered two different designs: 'Gate first' and 'replacement gate' architectures. The former has been used to form $In_{0.3}Ga_{0.7}As$ flatband MOSFETs with a GaO/GaGdO dielectric stack and a 100 nm gate length. These transistors exhibit a peak drain current of 250 μA/μm, transconductance of 150 μS/μm and a sub-threshold swing of 150 mV/decade. Sub-threshold swing falls to 130 mV/decade with the replacement gate architecture, which has a modest on-state performance due to a very high access resistance of 18 kΩμm. This issue can be addressed by improving the source drain anneal, which is needed to supress material diffusion in very small devices.

Into the third dimension

One team that is following Intel's lead and taking III-V MOSFETs into the third-dimension is Peide Ye's group from Purdue University. Ye detailed an evolution path for FETs, which begins with a bulk III-V planar architecture and ends with a III-V gate-all-around HFET (see Figure 4). His team have recently fabricated the latter structure, which is built on InP substrates and features a *p*-doped InGaAs channel, or multiple channels, wrapped in a 10 nm-thick layer of Al_2O_3 and a thicker layer of WN (see Figure 5 for details). Devices with 4 parallel channels, a 50 nm gate length and a 30 nm fin width produce a very low gate leakage, a peak

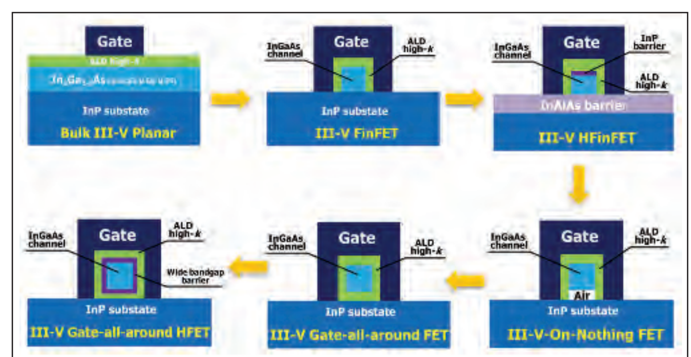


Figure 4. According to Peide Ye from Purdue University, III-V MOSFETs have evolved from planar structures to those that wrap a dielectric right around the channel

The second issue that Thayne and his co-workers have investigated is the fabrication of low resistance source and drain contacts with dimensions of just a few nanometres. The ITRS roadmap dictates that as gate pitch is reduced from 75 nm in 2011 to just 15 nm in 2024

current of 1170 μA/μm and a sub-threshold swing of 150 mV/decade.

These devices have several promising attributes for making an impact on the ITRS roadmap. Reductions in gate length result in an increase in current and transconductance, and the transistors appear to be immune from short channel effects. What's more, reductions in the dimensions of the nanowire channels lead to a hike in current flow, thanks to quantum confinement.

Recently, Ye has had a paper accepted for publication in *Electronics Letters* that details these findings. He and his team found that the current increased by 40 percent when nanowire widths were reduced from 50 nm to 30 nm, while mobility and transconductance increased by 34 percent and just over 20 percent, respectively.

To understand why thinning of the nanowires has lead to an increase in current – this is the opposite of what one would expect – the team simulated device behaviour using Sentaurus Device, a tool made by Synopsys. Simulations revealed that nanowires operate in the volume inversion regime, which means that the electron density reduces at the edges of the nanowire and increases in its inner region. Electrons can then, on average, travel faster through the channel because it is increasingly likely that these chage carriers are away from the interface, where scattering impedes progress. Simulations suggest that the proportion of electrons in the middle of the wire increases as its dimensions are reduced, with a very promising electron density profile reached for a width of 10 nm.

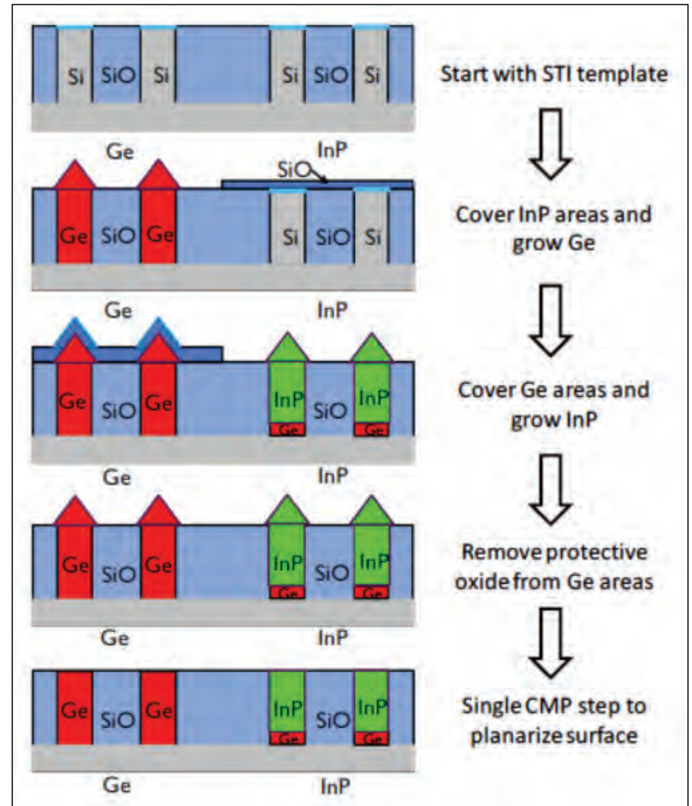


Figure 6. Researchers at imec are developing processes to unite germanium and III-V transistors on a silicon substrate

Building on silicon

If compound semiconductor MOSFETs are to move into production, they must be made on large diameter silicon substrates. Forming high quality germanium and III-V transistors on silicon is tricky, due to differences in lattice constants and crystal structures, but progress in this direction is being made by Matty Caymax's group at imec, Belgium. At CS Europe Caymax detailed efforts to form high-quality germanium and III-V devices on silicon, the latter achieved using trenches with a cup-shaped bottom (more details can be found at *imec prepares the ground for III-V transistors on silicon*, Compound Semiconductor March 2011 p.12). This approach (see Figure 6) eliminates anti-phase domains that lead to device shorting. "The best result that we have right now is a defect density of 2 x 10^8 cm^{-2}," said Caymax. "This is not sufficient – we have to work to get a lower dislocation density."

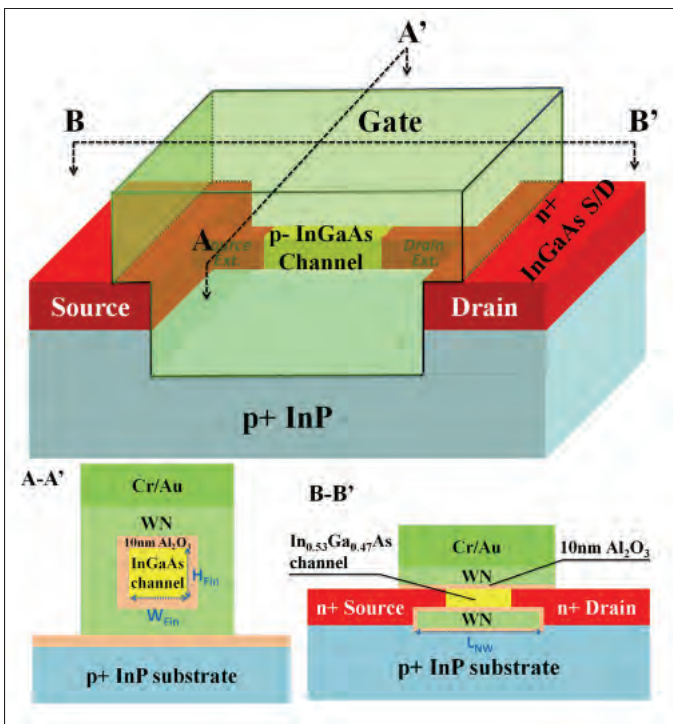


Figure 5. Peide Ye's group at Purdue University have pioneered the III-V gate-all-around FET. Transistors that they have built so far feature a gate length of 50-120 nm, a fin width of either 30 nm or 50 nm, and 1, 4, 9 or 19 parallel wires with a length of 150-200 nm and an Al_2O_3 dielectric with a thickness of 10 nm

Transistors made recently suffer from a high junction leakage. To investigate the origin of this leakage, the team have carried out atom probe tomography, a technique that has revealed that some atoms are located in places where they should not be: Some germanium is found in InP, and some indium and phosphorous atoms are located in germanium and the underlying silicon substrate.

Caymax's team, like those headed by Ye and Thayne, still has work to do to help III-Vs to make an impact in future logic applications. But the results to date are promising, showing ways to overcome many tough hurdles, and it seems that when silicon CMOS finally runs out of steam in a few years' time, compound semiconductors will be there to pick up the pieces.

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Lithography process control enhancements using advanced light source metrology

As ArF immersion lithography is extended with multi-patterning techniques, improved process control is required to ensure stable and repeatable performance. Nakgeuon Seong, Omar Zurita, Joshua Thornes, Yookeun Won, Slava Rokitski, Bernd Burfeindt, from Cymer Inc. describes how the addition of on-board beam metrology on the light source along with data analysis tools can provide an additional process control dimension.

Multiple lasers in the field were monitored after installing a new on-board metrology product called SmartPulse. We found that changes in beam parameters can be significantly reduced at major module service events when new service procedures and on-board metrology were used, while significant beam parameter shift and illumination pupil changes were observed when on-board metrology was not available at service events, causing lengthy scanner illumination pupil recalibration.

SmartPulse software from Cymer Inc. was used to monitor the variation of light source performance parameters, including critical beam parameters, at wafer level resolution.

The monitoring and control of process parameters at the process tool level has been used to improve process stability without increasing direct off-line wafer metrology, enabling fast wafer turn-around time and fab capital cost reduction. We have identified the need to provide process monitoring capability with higher resolution and additional process parameters at the light source level to complement monitoring at the litho cell (scanner and track).

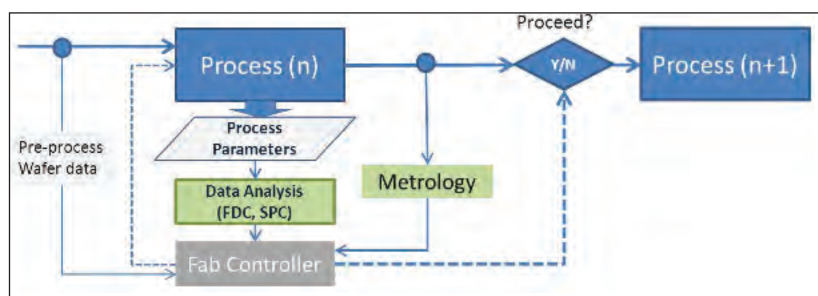


Figure 1. Concept diagram of process control utilizing equipment process parameters

Process monitoring and control improvement

As the use of ArF immersion lithography processes for most critical layer patterning has continued for multiple technology generations, each lithographic imaging solution has become highly optimized for specific patterns to be printed. Use of different imaging solutions for different device patterns also drives different levels of control for process variables. For example, highly optimized SMO (source mask optimization) imaging solutions require tighter control of the illumination pupil than simple SDP (Spacer double pattering) with dipole illumination. Very high throughput lithography patterning processes were implemented to reduce the cost of multiple patterning processes, which are commonly used for memory device production.

It has been recognized that smaller pattern size and lower k1 imaging processes at the latest technology nodes drive tighter control of more process performance parameters of lithography tools than at previous nodes. Process parameter monitoring and control for the process tools has been adopted as a way of reducing process errors and improving process control, and minimizing added metrology capital costs.(Figure 1.)

Laser parameter monitoring

Light sources for lithography have previously relied on three major metrics to determine if the quality of the light produced meets requirements for wafer production: center wavelength, bandwidth and energy.

The importance of monitoring and controlling light source bandwidth was previously reported on various papers and improvements to the laser were delivered over time. Lately a software solution has been developed for improved monitoring, reporting and analysis capabilities. The software correlates laser optical parameters, such as bandwidth, wavelength and energy, to the wafer level.

In addition to the optical parameters of the light source, the need for beam parameter monitoring and control was recognized when noticeable changes of illumination pupil images were sometimes reported after laser service events requiring laser beam alignment (Figure 2.)

Illumination pupil changes can induce changes of wafer CD, which is a significant issue for current lithography processes since the stability of the illumination pupil is one of the most critical parameters for OPC (optical proximity correction) stability. When an illumination pupil change was observed, it triggered, in most cases, a lengthy scanner illumination recalibration process, which can cause several hours of production down time.

In general, laser beam parameters are measured and characterized with off-line field service tools after the laser service events. Off-line beam metrology does not provide beam parameter information before the service event, cannot be used as an absolute reference (due to insertion and removal) and cannot provide real-time information during normal operation of the laser. Therefore new on-board metrology was developed to enable real-time measurement of beam parameters with high accuracy and with a fixed reference point.

On-board laser metrology

Advanced, on-board beam parameter metrology is offered as an upgrade to Cymer's industry leading XL light source platform. This upgrade adds new capability to the platform by providing a new metrology system with significantly expanded in-situ metrology capabilities.

This expands the existing metrology on the XL platform to make available to the chipmaker beam parameter measurements in addition to the already available data on energy, wavelength and bandwidth.

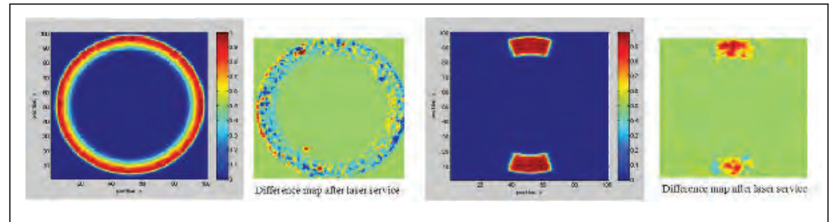


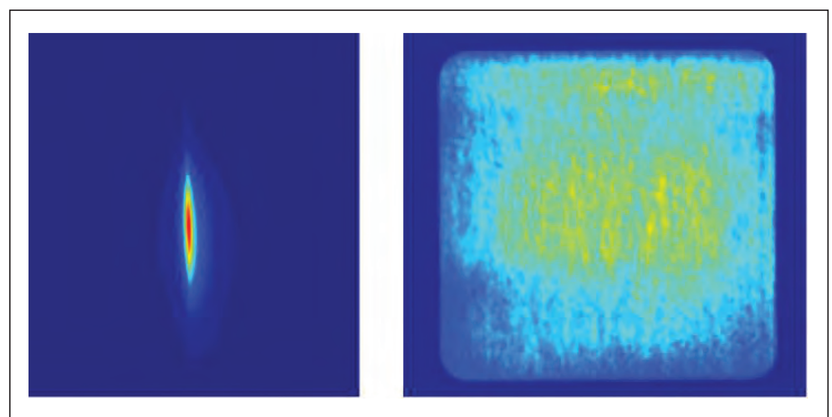
Figure 2. Two examples of illumination pupil change after laser service events

The first of these new capabilities is in-situ 2D imaging of the light source beam. This system obtains both near-field and far-field images of the light source (Figure 3) simultaneously. These images are used both qualitatively to provide additional information about the light source and quantitatively to derive standard beam parameter metrics, such as divergence and energy density. The on-board beam parameter metrology also includes pointing measurements which are absolutely referenced to the interface between scanner and light source. Lastly, polarization ratio is also constantly measured by the metrology unit.

The on-board local controller processes data from the metrology unit into high resolution data that characterizes the light source performance. This data can be monitored by chipmakers to understand potential wafer variability. Cymer's new light source parameter monitoring software, SmartPulse, was developed for efficient monitoring of light source performance parameters with built in statistical analysis and warning capabilities. It performs data monitoring, reporting and analysis of light source performance parameters including the on-board beam parameter metrology data.

It provides wafer level resolution data enabling direct correlation of wafer performance to light source parameters to support improved process control and yield. The product is also capable of alarming for any excursion of the monitored parameters from preset limits.

Figure 3: Color image of far field (left) and near field (right) of XL light source obtained with on-board beam metrology



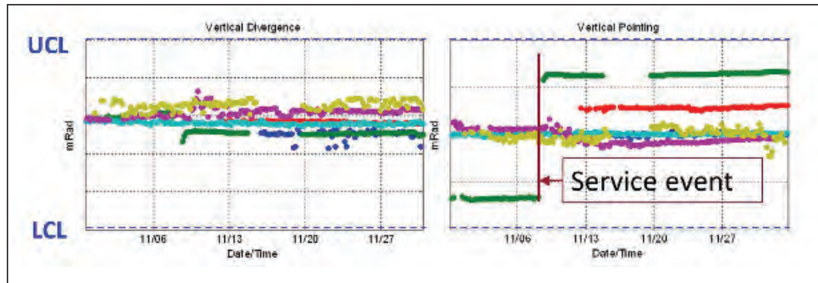


Figure 4: Long term (one month) data of measured beam parameters from six field installed tools

Field application data of on-board metrology

Multiple on-board metrology modules were installed in the field and monitored for several months. Long term drift of all beam parameters was minimal and local variation depended on the operation conditions of each tool, due to product type and tool utilization. The local variation was reduced after laser modules were replaced and the laser performance optimized. In general the scale of local variation was within an acceptable range compared to control requirements. In one case, a significant shift of vertical pointing was observed on a tool after a module exchange service and the shift exceeding the allowed limit value. It would not have been recognized if the new on-board beam parameter metrology had not been installed on the tool (Figure4). Total variation of beam parameters can be maintained well within control requirements if any shift at service events is reduced by using the new on-board beam parameter metrology for continuous beam parameter monitoring to a fixed reference point.

When the measured data was filtered for 30 to 40 percent duty cycle operation, which represents typical wafer exposure operation, excluding maintenance and calibration events, the local variation was reduced by about 40%. SmartPulse captures light source performance parameters during wafer exposure operation only to maximize the correlation of wafer CD performance to recorded light source performance parameters. Two service events were compared to understand the impact of service on beam parameters. At Service A in Figure 5, no attempt was made to use measured on-board beam parameter metrology and resulted in unacceptable shifts in one beam parameter (vertical pointing). A shift in the illumination pupil was also confirmed. When an improved procedure was used with the new on-board beam parameter metrology tool, the change in the beam parameter was minimized to within normal local variation levels (Service B at Figure 5.)

The results showed that the change in light source beam parameters during light source service events can be significantly reduced by using the new on-board beam parameter metrology tool and an improved service procedure. The reduced change of beam parameter at each service event will minimize the change of illumination pupil, with the possibility of reducing required scanner illumination recalibration procedure, resulting in improved lithography tool availability for wafer production.

Summary

A new on-board metrology module, which measures beam parameters of the light source in real-time, and SmartPulse light source parameter monitoring software, were introduced by Cymer to improve process stability, especially proximity effect for OPC stability.

Real-time monitoring of light source performance parameters during wafer exposures will enable a correlation with CD performance on the wafers as well as laser health status. The new on-board beam parameter metrology can be used to minimize the change of beam parameters to avoid lengthy illuminator pupil calibration after light source service by using an improved service procedure.

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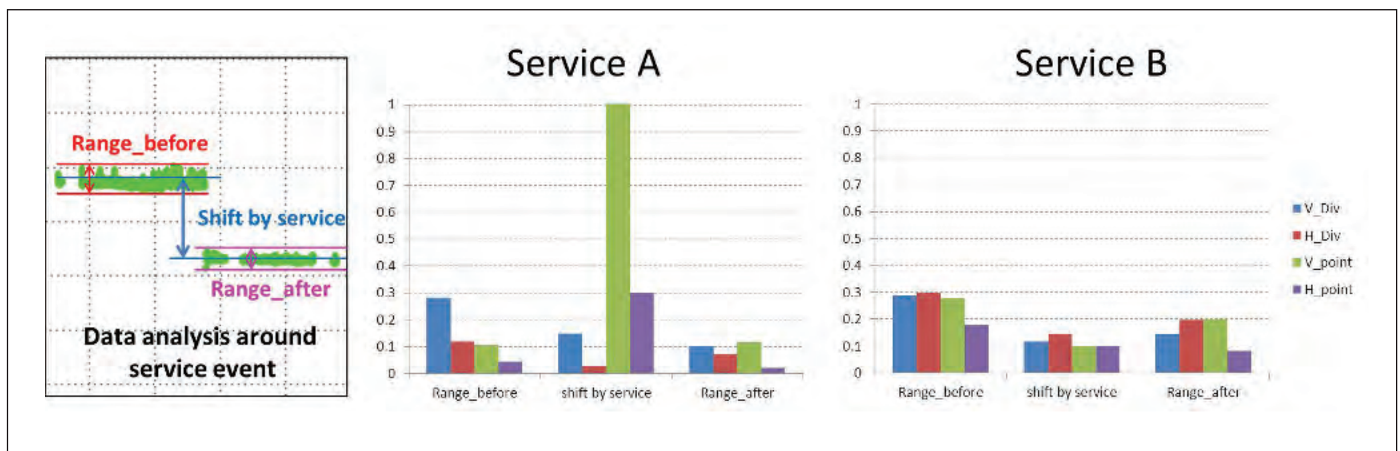

Figure 5: Comparison of beam parameter variation surrounding laser service events

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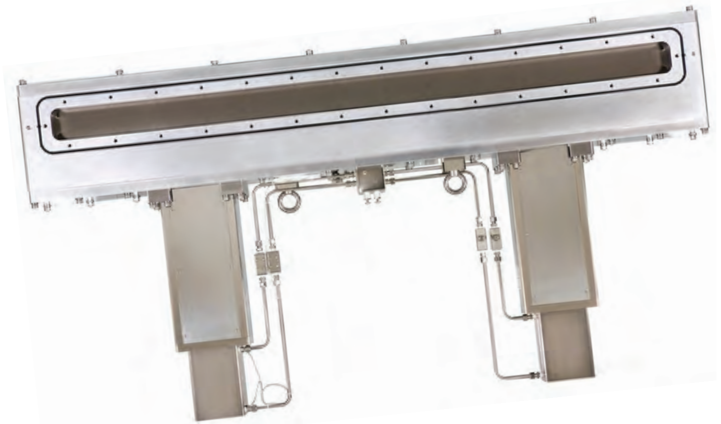

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Choosing a source measurement unit instrument

A source measurement unit (SMU) instrument integrates the capabilities of a precision power supply (PPS) with those of a high-performance digital multimeter (DMM) in a single instrument. The high performance architecture allows using them as pulse generators, as waveform generators, and as automated current-voltage (I-V) characterization systems. **Mark A. Cejer, Marketing Director & Lishan Weng, Applications Engineer, Keithley Instruments, Inc discusses the benefits offered.**

The real benefit of SMU instruments for test and measurement applications comes from their ability to source and measure signals simultaneously. When compared with using separate instruments to handle each function, SMUs' simultaneous operation provides for faster test times, simplified connections, improved accuracy, less complex programming, and a lower cost of ownership (COO). Their tight integration lets them protect the device under test (DUT) from damage due to accidental overloads, thermal runaway, and other dangers. It also makes SMU instruments ideal for characterizing and testing semiconductors and other non-linear devices and materials.

SMU vs. Power Supply

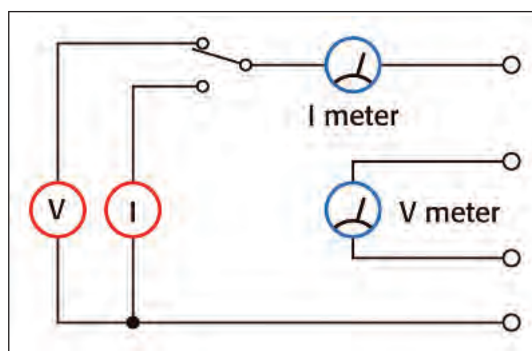


Figure 1. Basic SMU instrument topology

Given that an SMU instrument integrates the functions of a power supply with a digital multimeter, how exactly does the performance of an SMU's source differ from that of a typical power supply?

- Greater speed and precision: SMUs are optimized for both speed and precision, so they can offer significantly faster rise times and much lower measurement uncertainty than power supplies. SMUs' settling times are measured in microseconds compared to the milliseconds that power supplies require to settle on their programmed value. Similarly, an SMU's measurement uncertainty is measured in nanoamps vs. microamps for typical power supplies.
- Wider operating range and better resolution: Because of their outstanding low current capability, SMUs typically offer much wider operating ranges with greater resolution than power supplies, so they are suitable for a wider range of test and measurement applications.
- Four-quadrant rather than two-quadrant operation: As illustrated in Figure 2, a typical power supply can only source voltage and/or current. In other words, it provides only two-quadrant operation (in quadrants I and III), but an SMU can provide full four-quadrant operation because it's capable of sourcing and sinking power, acting as both power supply and an

electronic load. During source or sink operation, the SMU can simultaneously measure voltage, current, and resistance. This operating flexibility can be especially valuable when characterizing batteries, solar cells, or other energy generating devices.

- Built-in sweep capabilities: The various sweep capabilities SMUs offer can simplify programming a test's source, delay, and measure characteristics, significantly boosting testing productivity. All sweeps can be configured for single-event or continuous operation to simplify the process of capturing the data needed to characterize and test a wide range of devices. Sweeps can also be used in conjunction with other throughput-enhancing features like Hi-Lo limit inspection and digital I/O control to create high speed production test systems.
  - A fixed level sweep outputs a single level of voltage or current with multiple measurements his is typically done to bias or stress devices. Various types of fixed level sweeps can be generated, depending on the needs of the application.
  - Pulsed sweeps are often used to limit the amount of power that goes into a material sample or device over time and to minimize self-heating effects that could otherwise damage semiconductors and light emitting diodes (LEDs), experimental materials such as graphene, or other fragile nanotechnology-based devices.
  - Custom sweeps simplify creating application- specific waveforms.

SMU vs. DMM

Because of its built-in sourcing capabilities, an SMU can minimize overall measurement uncertainty in many applications. The first diagram in Figure 3 shows the basic voltmeter configuration for the SMU. Here, the built-in current source can be used to offset or suppress any system-level leakage currents (such as cable noise) that could cause unwanted errors in voltage measurement applications.

For current measurements, the SMU's built-in source and "feedback ammeter" design works together to keep voltage burden low, and enable low current measurements to subpicoamp levels. DMMs do not have the built-in source, and typically have "shunt ammeter" designs that typically limit low current capabilities to microamp or nanoamp levels.

Finally, for resistance measurements, the SMU architecture offers full flexibility over the amount of current or voltage sourced to the DUT. DMMs have fixed current source values that are dependent on the range being used to measure resistance. SMUs offer fully programmable source values for measuring resistance. This can be valuable for protecting DUTs or for measuring extra high or extra low resistances. For high resistance measurements, the source voltage method is preferred; for low resistance measurements, the source current method is best. Some SMUs have a six-wire ohms feature that "guards out" the effects of unwanted parallel resistance paths in the circuit.

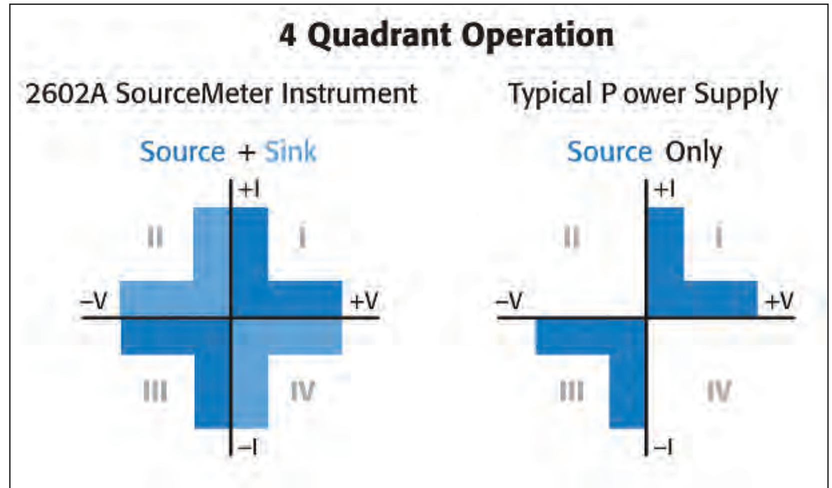


Figure 2. A power supply (right) offers only two-quadrant operation; an SMU instrument (left) can source and sink power in all four quadrants

SMU Measurement Terminology

One of the first considerations in choosing an SMU instrument must be the quality of the measurements it produces. Poor measurement integrity can cause those using the data produced to draw incorrect conclusions about the performance of a given DUT. In R&D, this can mean an imperfect understanding of a device's operating parameters, leading to unnecessary rework and costly time-to-market delays. In production test, inaccurate measurements can result in rejection of good parts (false failures) or acceptance of bad ones, either of which can cause poor yields, customer dissatisfaction, and other problems.

When considering an SMU instrument's measurement integrity, keep several key terms in mind: accuracy, repeatability or stability, resolution,

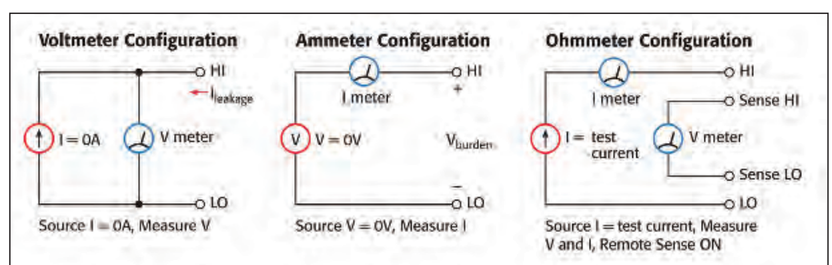
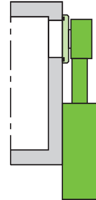


Figure 3. SMU voltmeter, ammeter, and ohmmeter configurations

Transfer Gates

Door



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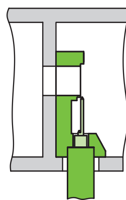
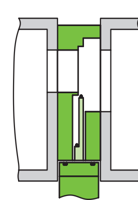


Valve



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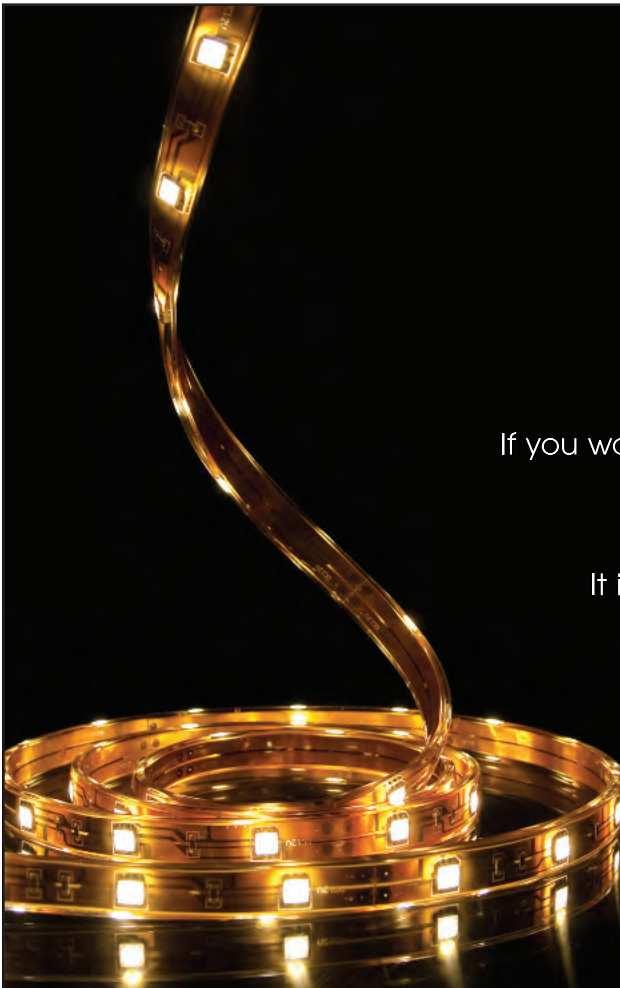

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sensitivity, and integration time.

Accuracy is defined as the closeness of agreement between the result of a measurement and its true value or accepted standard value. Imagine you are shooting arrows at a target: the accuracy of your shots would be defined by how close the arrows come to the bullseye.

Repeatability refers to the closeness of agreement between successive measurements carried out under the same conditions. Although repeatability is not typically specified on an instrument's datasheet, it can usually be easily determined during an instrument demonstration or evaluation. Figure 4 illustrates the concepts of accuracy vs. repeatability.

Resolution is defined as the smallest portion of the signal that can be observed. The resolution of an instrument is determined by the number of digits it can display on the front panel or send to a PC over the communication bus. This can often be changed by pressing a front panel button or by sending a programming command to the instrument. In Figure 5, the user is toggling between 4½, 5½, and 6½ digits on the display and has just selected the 6½-digit display.

An SMU instrument's usable maximum resolution depends on its overall accuracy and the resolution of its analog-to-digital converter (ADC). For example, no one would produce a 6½-digit instrument with an 8-bit ADC and 5% accuracy because most of the digits being displayed would be meaningless. In general, however, the higher the resolution is, the higher the bit count on the ADC and the higher the accuracy will be.

The sensitivity of a measurement is the smallest change in the measured signal that can be detected. The ultimate sensitivity of an instrument depends both on its maximum resolution and its lowest measurement range. For example, a 6½-digit

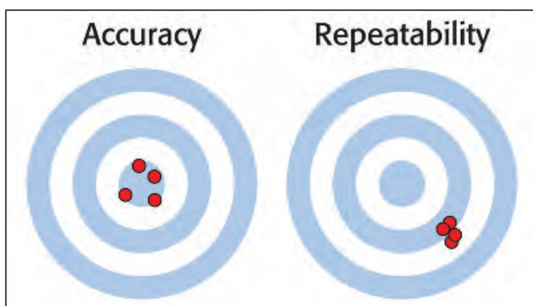

Figure 4. In the target on the left, the shooter had high accuracy but poor repeatability. The target on the right shows high repeatability but poor accuracy

Figure 5. Adjusting an SMU instrument's resolution

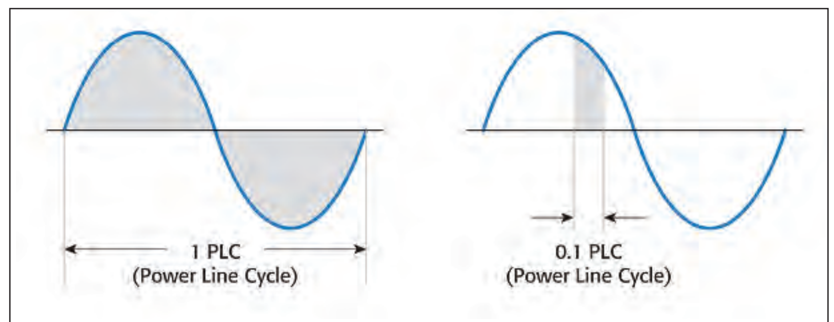

Figure 6. ADC integration time comparison (NPLC)

SMU with a bottom range of 1µA would have 1pA sensitivity. However, depending on that instrument's accuracy, that sensitivity might not be particularly useful.

Measurement instruments employ either (or both) of two basic types of analog-to-digital converters: integrating ADCs and digitizing ADCs. In general, an integrating ADC will offer higher accuracy because it cancels out the unwanted effects of AC noise from the power line.

The instrument's integration rate, which is specified in NPLC (Number of Power Line Cycles), is adjustable. To reject AC noise, the NPLC must be equal to or greater than 1. Integrating the measurement over multiple power line cycles will reject this noise still further and thereby provide a more accurate measurement. However, this noise rejection capability comes at the expense of reading speed; one power line cycle takes 16.7ms at 60Hz or 20ms at 50Hz. Setting the NPLC to a fraction of a line cycle will provide faster measurements at the expense of more noise or lower accuracy (Figure 6).

That means the reading rate and measurement speed of a highly accurate instrument like an SMU are determined by its NPLC setting. However, an ADC's reading rate is only one of many factors that affects an SMU instrument's true speed; other factors that can affect overall throughput include function and range change times, trigger in and out times, settling times, and program execution times.

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Key Considerations for Selecting an SMU Instrument

When evaluating a specific SMU instrument for a specific application, it's essential to consider:

- System-level speed/throughput
- Source resolution vs. stability
- Measurement settling time, offset error, noise
- Cabling and connections

Let's examine each of these characteristics.

- System-level speed or throughput. In other words, how quickly can you get a final measurement or set of measurements (such as a suite of current vs. voltage parameters) back to the PC controller? For example, let's consider a typical diode or LED test, which will consist of three measurements—forward voltage, reverse voltage, and reverse current—each of which is typically compared to upper and lower limits. The part is considered "bad" if any one parameter fails. The objective is to test this part as quickly as possible without sacrificing accuracy in order to minimize the cost of test.

The challenge is that all the source and measure values are different. Although the readings/second spec is important, a range or function change must occur before a reading can be taken. This type of test isn't about taking multiple readings of the same value repeatedly; it's about taking single-point measurements at different source/measure levels. Therefore, the speed of the ADC (the NPLC spec) alone won't be a good indication of how quickly the instrument can test this part. One should also consider a variety of other operating parameters, including trigger in time, range change time, function change time, source settling time, trigger out time, and command transfer, processing, and execution time.

Figure 7 shows a comparison of the actual test results from a Keithley Series 2600A System SourceMeter instrument with that of another brand of SMU instrument. The data shows the number of diodes tested per second, so the higher the number the higher the speed. This is a true measure of test throughput.

Recall that the larger the NPLC is, the more accurate the measurement will be (corresponding to lower speed). Note how reducing the NPLC setting to less than 0.1 NPLC does not make a significant difference in overall test time per part. In typical applications in which multiple parameters are being tested, the speed of other characteristics, such as range or function change time, triggering time, bus communication time, or program execution time, start to dominate. Even at 1 NPLC, these other characteristics, if not optimized by the SMU instrument manufacturer, can have a big impact on overall test throughput. The Keithley Series 2600A System SourceMeter instrument in this example can test more than twice as many parts per second at 1 NPLC; therefore, it has more than 100% faster throughput than the other SMU instrument while maintaining optimum accuracy.

Although range and function change times are important, it's also possible to obtain major breakthroughs in system throughput by embedding then executing the majority of the test program within the SMU instrument itself. This eliminates most of the communications bus traffic, speeds up triggering, and optimizes command processing time. Using this type of feature is a major reason an SMU instrument running at 0.1 NPLC can be as much as four times faster and much more accurate than an SMU running at 0.00048 NPLC in real-world applications.

Keithley's Series 2600A System SourceMeter instruments employ a feature known as Test Script Processing, or TSP technology. TSP technology optimizes command transfer, command processing, and command execution times by embedding the actual test program (or script) into the instrument's non-volatile memory. However, TSP technology

	1 NPLC	0.1 NPLC	0.01 NPLC	0.001 NPLC	0.00048 NPLC
Non-Keithley SMU instrument	6.1	8.1	8.2	8.2	8.2
Keithley Series 2600A	13.3	33.2	37.8	38.2	N/A
	Most accurate ←				→ Least accurate

Figure 7. Test results: parts per second

	Programming Resolution 20V Range
Non-Keithley 6½-digit SMU instrument	10 µV
Keithley Series 2400	500 µV

Figure 8. Programming resolution based on specification sheet

Source Value – 10.001 V	Source Readback Displayed Value (pk-pk of variation)	Actual Measured Value of Source Output (pk-pk of variation)
Non-Keithley 6½-digit SMU instrument	0.0 µV	438.7 µV
Keithley Series 2400	30.0 µV	42.9 µV

Figure 9. Actual output stability

goes far beyond simply storing and executing a sequence of standard SCPI commands. TSP technology is based on Lua, a powerful BASIC-like scripting language. Functions like "do" loops, variables, If-Then-Else statements, and more are all supported in Lua. Therefore, TSP scripts are just as powerful as traditional test programs residing in PCs but have the advantage of actually being embedded in the instrument to optimize overall test speed.
◆ An SMU instrument's sourcing resolution and output stability are also key to its overall performance. Let's look at the relationship between source resolution and output stability.

When evaluating the performance of an SMU instrument's source, it's important to look beyond the spec sheet and the instrument's source

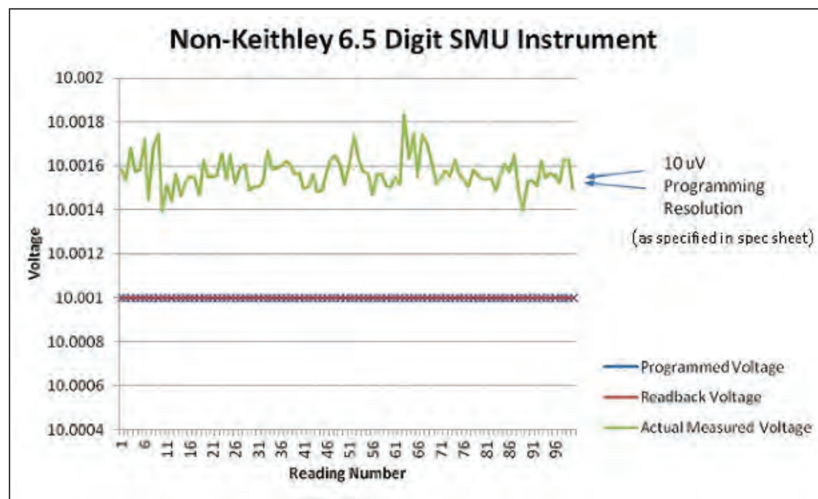

Figure 10a. Actual source performance: programming resolution vs. stability for non-Keithley 6?-digit SMU

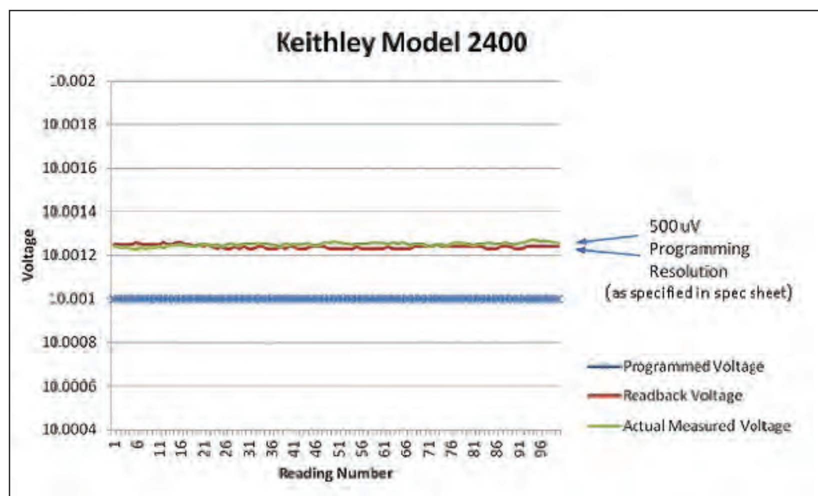

Figure 10b. Actual source performance: programming resolution vs. stability for Keithley Model 2400 SourceMeter instrument

readback display. The source's actual output performance may be very different from its specified resolution or from its displayed value, which may require instrument specifiers to do their own testing to verify it.

Based solely on an SMU instrument's spec sheet, one might conclude that the SMU instrument with the greatest programming resolution is the most accurate. The programming resolution determines the output's "fineness" of adjustment. In Figure 8, note that the non-Keithley SMU offers 50 times greater programming resolution than the Model 2400 SourceMeter instrument.

Furthermore, based on the SMU's "source readback" value displayed on the front panel or over the bus (Figure 9), one might conclude that the SMU showing readback values closest to the programmed values is the most stable and therefore the better choice. In this example, note that the non-Keithley SMU shows 0μV of peak-to-peak variation when sourcing a 10.001V signal, while the Model 2400 shows 30μV.

However, the picture changes dramatically when we measure the actual source output using a separate instrument. To obtain the data in the right-most column of Figure 9, we chose Keithley's Model 2002 8?-digit digital multimeter to measure the source output of each SMU directly. The Model 2002 is one of the most accurate DMMs available on the market and is used by many calibration labs, which makes it a good choice for high accuracy applications of this type.

To view the stability of the source outputs, we made 100 measurements using the Model 2002 at 10 NPLC to ensure maximum accuracy. We observed that the non-Keithley 6½-digit SM (Figure 10a) actually has almost 0.5mV peak-to-peak variation when sourcing a 10.001V signal. This is very different from the 0μV variation its source readback display indicates. In addition, this error is more than 40 times greater than the 10μV programming resolution. The Keithley Model 2400 SourceMeter instrument (Figure 10b) actually has more than 10 times better output stability than the non-Keithley 6½-digit SMU (42.9μV vs. 438.7μV).

For the non-Keithley SMU, note that the readback voltage is exactly the same as the programmed voltage. However, the actual measured voltage is quite different from the readback voltage or the programmed voltage. The SMU readback indicates the output voltage to be exactly 10.001V; in reality, the output voltage is somewhere between 10.0014V and 10.0018V. This is a significant amount of error

that the user would not normally see indicated on the SMU display. In addition, the fineness of adjustment of the programming resolution (10µV) is overwhelmed by the inherent error of the source, so this level of resolution is unrealizable.

In contrast, for the Keithley Model 2400 SourceMeter instrument, note that the readback voltage closely tracks the actual voltage measured at the output terminals. You'll also see that the readback voltage differs from the programmed voltage. One would expect to see a difference, given the source's accuracy specs. These kinds of results should give you confidence that the voltage actually being delivered to the DUT is that which is expected. In addition, with the Model 2400, the source error does not overwhelm the programming resolution, as it does for the non-Keithley SMU. That means users can have the confidence to take full advantage of the fineness of adjustment of the programming resolution.

As this comparison shows, an SMU instrument's programming resolution specification is not a good indication of its stability and overall performance. It also shows that the source readback results can be highly questionable. Therefore, when evaluating an SMU for your application, be sure to do some testing for yourself.

- *Measurement settling time,* offset error, and noise can have a big impact on an SMU instrument's performance, particularly in low current applications. The example illustrated in Figure 11 shows the results of two SMU instruments sourcing 200V with nothing connected to the input terminals while measuring the resulting current using each instrument's built-in ammeter feature. This comparison offers a good indication of each instrument's fundamental low current performance, and it's an easy test to recreate on the test bench.

Note that the non-Keithley 6½-digit SMU (the blue line) settles to its specified offset error of 50pA in about four seconds. The "bumpiness" of the data curve indicates measurement noise. In contrast, the Keithley Model 2636A (the red line) settles to its specified offset error of 0.12pA (120fA) in about half a second.

The smooth data curve indicates a distinct lack of measurement noise. So, based on the data, it's obvious the Model 2636A will deliver a better measurement faster. In fact, at the point when the Model 2636A is settled and capable of providing in-spec sub-picoamp measurements, the non-Keithley SMU still has nanoamp-level errors. In addition, if you were to take a series of measurements over

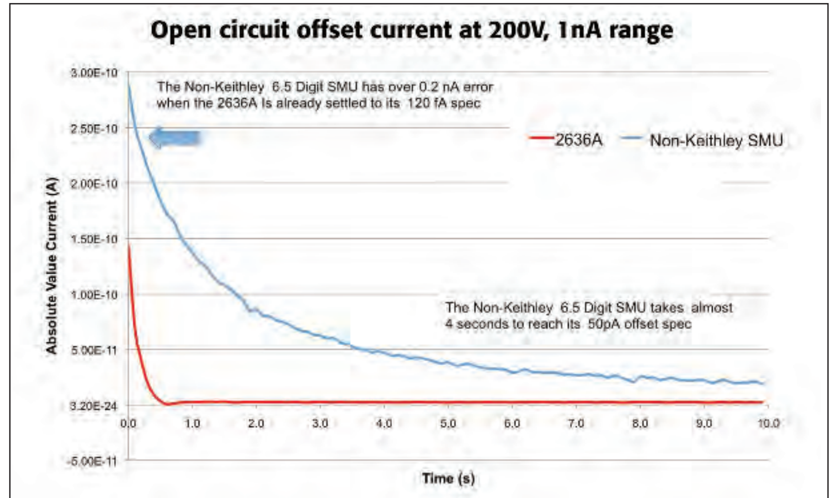

Figure 11. Comparison of measurement settling time, offset error, and noise

time, the Model 2636A would provide more consistent results due to its fast, flat, and noise-free settling.

Note that, in either case, when measuring low current, the settling times drive overall test time. This is due to R-C time constants inherent in the overall architectural design of any SMU instrument. Therefore, an ADC running at sub-line cycle integration (for example, at 0.001 NPLC) won't provide a faster measurement. Low current performance is very important for many semiconductor and optoelectronic applications, as well as in materials research applications such as nanoscale devices, graphene, etc. To understand the true measurement performance of an SMU instrument, it's important to look beyond "headline" terms like 6½ digits or 10fA resolution. Figure 12 offers another comparison of the low current performance of the Model 2636A with the non-Keithley 6½-digit SMU.

Figure 12. It's important to understand the difference between an SMU instrument's actual measurement performance and its "headline" specifications. The table lists specifications from the data sheet; the diagram explains the offset accuracy.

The non-Keithley SMU is specified as having 6½ digits and 10fA resolution. However, a closer look at the manufacturer's specs shows that its bottom current range is 10nA and its offset accuracy is 50pA. The total accuracy of most instruments is calculated as the gain accuracy plus offset accuracy. Gain accuracy is typically given in % of signal, and offset accuracy is usually a fixed amount. The Model 2636A is specified as having 1fA resolution. The spec table in Figure 12 shows that it has a 100pA range and 120fA of offset

SMU	Lowest range	Total accuracy*	Resolution
Non-Keithley	10nA	±(0.10% + 50pA)	10fA
Keithley 2636A	100pA	±(0.15% + 120fA)	1fA

*Total accuracy = Gain accuracy (%) + Offset accuracy

Lowest Current Range	nA	pA	fA
Non-Keithley 6.5 Digit SMU:	10	050	00x
Keithley 2636A		100	120

Offset Accuracy Spec

Figure 13. Cable and connection considerations

accuracy. Obviously, although both the Keithley and non-Keithley SMU instruments can appear similar when looking at the "headline" specs, the Model 2636A actually has 400 times better offset accuracy, so it has much better sensitivity, and is capable of far more accurate low current measurements.

- Cabling. Using triaxial cables rather than the more common coaxial cables is essential to achieving optimal low current measurement performance. Triaxial cables have an extra shield that coaxial ones don't, which ensures lower current leakage, better R-C time constant response, and greater noise immunity. In addition, the better R-C response allows for faster settling when measuring higher levels of current.

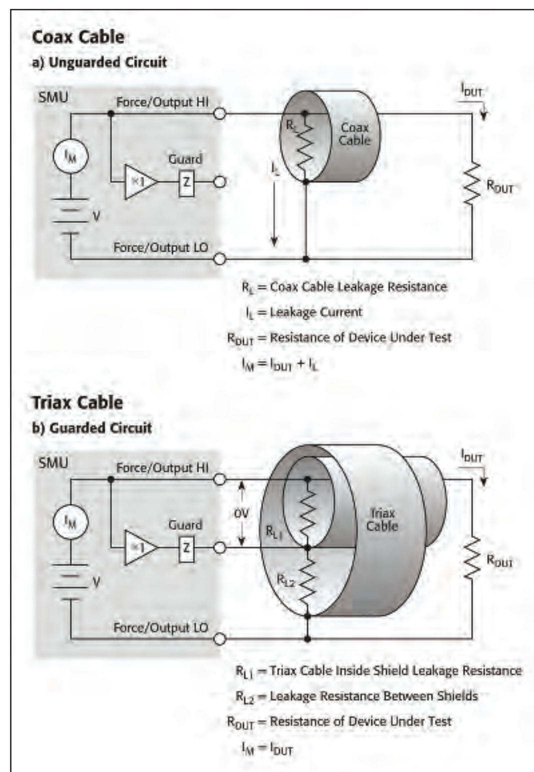

Figure 13 illustrates how a triaxial cable works with the SMU instrument's driven guard to prevent the leakage resistance of the cable from degrading the low current measurements. In the circuit on the top, the leakage resistance of the coaxial cable is in parallel with the device under test, creating an unwanted leakage current. This leakage current will degrade low current measurements.

In the circuit on the bottom, the inside shield of the triaxial cable is connected to the guard terminal of the SMU instrument. Now this shield is driven by the SMU's unity-gain, low impedance amplifier (Guard). The difference in potential between the Force/Output Hi terminal and the Guard terminal is nearly 0V, so the leakage current is eliminated.

Due to their high level of performance, triaxial cables can be expensive, so when specifying your final test configuration or comparing price quotations from various manufacturers, make certain they are included with the SMU instrument.

If they are considered an optional accessory instead, you could be in for a costly surprise. In addition, some SMU instruments require optional adapters to convert more common input connectors, like banana jacks, to use triaxial cables.

Again, be sure to understand and specify your cabling carefully, because it can easily add more than $2000 to the total cost of an SMU instrument.

Conclusion

The integrity of the measurements an SMU instrument produces must always be a primary selection consideration. Poor measurement integrity can produce costly errors in both R&D and production test applications, leading to expensive rework, time-to-market delays, poor yields, customer dissatisfaction, and other problems.

A careful evaluation of an SMU's accuracy, repeatability, resolution, sensitivity, and integration time is critical. Other key considerations when selecting an SMU instrument include system-level throughput, source stability, measurement settling time, offset error, and noise, and finally, cabling and connection issues.

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Orders of magnitude: Addressing the semiconductor industry's exponential needs

Peter Berg, Bernt Meßtechnik GmbH and Fred Conroy, Tiger Optics LLC review the progress made in the last 10 years.

Tiger Optics reduced the lower detection limits (LDL) by a factor of ten times (10x) or more when compared to existing on-line moisture analyzer technologies such as the electrolytic process using Faraday's Law or the quartz-crystal microbalance (QCM). Not only did the MTO-1000 offer lower detection limits; it also provided the user with an absolute measurement that did not require the use of zero or span gases. The semiconductor industry took heed. In its fabrication plants, the margin of success can hinge on the purity of required gases.

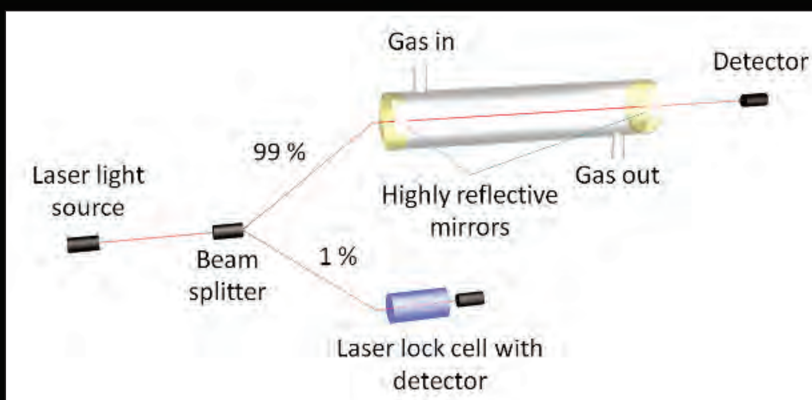
Moisture Measurement via Ring-down Spectroscopy

The Tiger Optics' core technology is based on continuous wave cavity ring-down spectroscopy (CW-CRDS). The measurement principle is shown in Figure 1. A laser beam in the near-infrared (NIR) realm is coupled to a measurement cell, with parallel, highly reflective mirrors at either end. The dielectric coating of the mirrors reflects more than 99.999 percent of the light within a specific, rather narrow, frequency band. The small amount of light that passes through the mirror at the far end of the measurement cell is captured by a detector, which measures its remaining intensity. The gas stream to be analyzed flows continuously through the measurement cell.

The measurement process starts with the continuous-wave (CW) laser energizing the cell until the light energy reaches a threshold value. The laser is then shut off for a fraction of a second. The laser beam travels back and forth between the mirrors within the measurement cell, for a total path length of close to 30 kilometers. The laser light's intensity level follows a decreasing exponential function until the energy is exhausted (a "ring down"). The determination of the concentration of moisture is based on the time required for the light to die.

CW CRDS provides an "absolute" measurement via the Beer-Lambert Law, so no zero gas is required. The zero portion of the measurement is determined by intentionally tuning the laser to a frequency at which moisture does not absorb light. Figure 2 shows the water vapor spectrum in the wavelength range of 1391 to 1393 nm. In the wide region marked "τZero – Abklingzeit/Ring-down time," there is no absorption of light by the moisture present in the gas stream. The associated ring-down time of 86 microseconds is solely caused by the loss of light from the measurement cell. The laser is then tuned to the wavelength of a known absorption peak of the water vapor spectrum (marked "τPeak H2O-Band" in Figure 2). The shorter measured ring-down time of 29 microseconds is due to moisture absorbing a portion of the light. When the τZero

Figure 1: Tiger Optics CW-CRDS Schematic

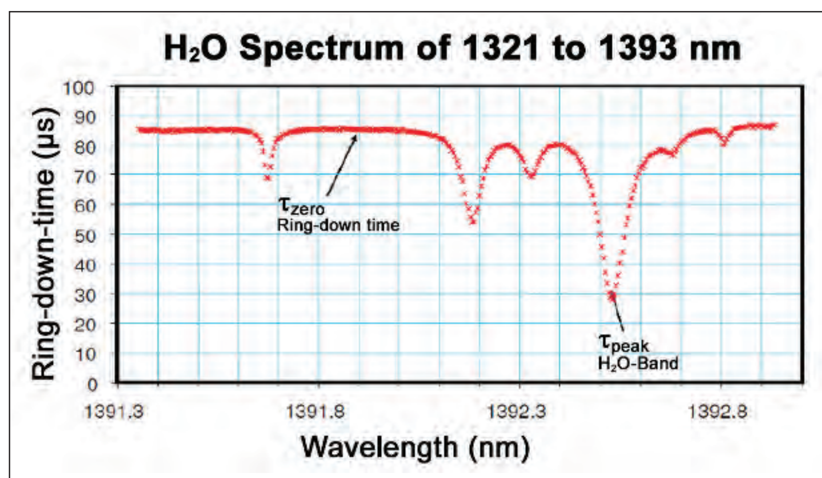


and τPeak ring-down times are entered into the formula of the Beer-Lambert Law, the result is the moisture concentration. This time-based measurement contrasts with other laser-based measurement techniques relying on hard-to-control factors such as differences in light intensity, rendering them “relative” techniques, requiring external calibration.

While a true zero measurement is insured by capturing the ring-down time off-peak, the on-peak performance is verified via a reference cell. A small fraction of the laser light is diverted through a reference cell that contains a small amount of the analyte in question.

When the laser is exactly on peak, the amount of light reaching a detector at the far end of the reference cell is minimal. If the intensity begins to increase (indicating a drift from the correct wavelength), the laser is adjusted by changing the supplied current until the intensity is again at a minimum. This “laser locking” ensures that the proper τPeak wavelength is being used and eliminates any long-term drift that continues to plague other technologies. While the underlying science is relatively complex, the instruments are very simple to operate. All of the calculations are performed by the system’s software and the concentration is continuously updated on the touch-screen display. Tiger analyzers are effortless to install and do not require the use of calibration gases or null gases. Once the system is taken out of the crate, measurements on a dry gas can be taken in just a matter of minutes.

Figure 2: Laser Trace3 vs LaserTrace Moisture Specifications



	LaserTrace3		LaserTrace	
H2O	LDL	Sensitivity	LDL	Sensitivity
In Argon	150 ppt	75 ppt	300 ppt	150 ppt
In Helium	100 ppt	50 ppt	200 ppt	100 ppt
In Hydrogen	250 ppt	125 ppt	500 ppt	250 ppt
In Nitrogen	250 ppt	125 ppt	500 ppt	250 ppt
In Oxygen	300 ppt	150 ppt	300 ppt	150 ppt

Tiger’s Reach

Since 2001, Tiger’s R&D team has developed a variety of analyzer versions from its CW-CRDS technology. These include the LaserTrace family, HALO family, Tiger-i (for ambient and environmental contaminants), ALOHA-H2O (for UHP ammonia), and Prismatic. Each platform addresses specific market needs. Foremost on Tiger’s agenda: anticipating the requirements of the semiconductor industry, with its ever-decreasing line geometries coupled with increasing wafer sizes. No instrument maker is more attuned to a fabrication plant’s constant need for gas purity analyzers with lower LDLs, reduced cost of ownership (COO), and increased uptime.

Accordingly, Tiger introduced its LaserTrace system in 2003. The platform provides users with a modular product line that allows for the monitoring of their bulk gases (Ar, He, H2, N2, O2) to sub-ppb levels for moisture, oxygen, methane, and other analytes. By 2008, the LaserTrace+ system was able to provide users with an LDL as low as 200 ppt (depending upon the gas matrix). The LaserTrace has become the company’s most popular product family, with nearly 500 systems in use worldwide.

The EURAMET 1002 Study

The absolute nature of the CW-CRDS technology is heralded not only by industrial users, but by the scientific community as well. Throughout the world, national metrology institutes (NMIs) have established their own methods of generating precise levels of moisture to develop and compare standards and to perform vital calibration processes in their own country or region.

As each NMI’s moisture generator is large and of complex design, it has not been feasible to ship these generators around the globe for comparison studies. The NMIs needed a portable, absolute measurement technique that could be shipped from one institute to another to perform the analysis. Enter Tiger Optics.

Using two Tiger instruments, the European Association of National Metrology Institutes (EURAMET) recently completed an international study of different moisture generating techniques from four (4) NMIsii. The participants included the National Institute of Standards and Technology (NIST, USA), National Metrology Institute of Japan (NMIJ, Japan), National Physical Laboratory (NPL,

UK), and Physikalisch-Technische Bundesanstalt (PTB, Germany). The multi-year, multinational study determined that the deviation of Tiger's LaserTrace analyzer was less than two percent (2%) over the three (3) year period in the entire range of 10 ppb – 2 ppm.

LaserTrace 3

While the semiconductor industry has long relied on the LaserTrace system for absolute measurements, shrinking geometries on the wafer have resulted in even tighter controls being placed on the purity of gases used in the semiconductor manufacturing process. As some fabs set alarm limits for moisture as low as 500 ppt, the semiconductor industry is now requiring even lower LDLs. Once again, Tiger Optics has responded to the industry's needs.

At Semicon West 2011, Tiger Optics introduced the LaserTrace 3, for which the LDLs of most contaminants and gas matrices have been cut in half. For moisture in helium, the LDL is now an astonishingly low 100 ppt (Figure 3). The achievement is one of the reasons that the Tiger Optics' LaserTrace 3 won the prestigious Golden Gas Award for 2012 from Gases and Instrumentation International Magazine in the Gas Analysis and Detection category.

In addition to the dramatic reduction in the LDL, the engineering team at Tiger Optics has increased the speed of response for a multi-channel LaserTrace 3 by a factor of more than 2.5x. The end user can be assured that the LaserTrace 3 will display updated moisture concentrations on each channel every two seconds. This dramatic improvement in the LDL and the speed of response is the result of a tremendous amount of work on both the hardware and the software of the system. In keeping with Tiger's philosophy of focusing on the needs of the customer, existing LaserTrace users are able to upgrade the hardware and the software of their systems to achieve the performance of the LaserTrace 3.

LaserTrace 3x

While the LaserTrace 3 (coupled with the associated moisture and/or oxygen, etc. measurement cells) is focused on measuring the contamination levels of the bulk gases as they enter the fab, the LaserTrace 3 platform is also utilized to monitor the moisture levels in the exhaust gases of low temperature epitaxial process tools from manufacturers such as Applied Materials, Inc., and ASM International N.V.

> I'm a great believer in particularly being alert to changes that change something, anything, by an order of magnitude
>
> Andrew Grove, former CEO, Intel Corporation

In order to perform the required moisture measurements at pressure levels down to 50 torr (or below), Tiger uses a reduced-pressure or Epi sensor. Initially, the industry needed only two Epi sensors to be coupled to a single LaserTrace 3 electronics module so that the exhausts from a two-chamber epi system could be monitored independently. Subsequent requests to also monitor the moisture levels within the transfer chamber required a redesign of the electronics module.

According, Tiger Optics developed its LaserTrace 3x, to permit monitoring the transfer chamber at reduced pressures while also monitoring each of the tool's epi exhausts. Tool owners can monitor for moisture in these critical areas after preventive maintenance is performed on the tool. The result is that the tool can now be brought back on-line when the moisture levels are low enough to insure that the product will not be impacted due to moisture contamination. The savings from the reduced downtime of the tool, along with a reduction in the number of wafers that might need to be scrapped due to moisture contamination, is sure to bring about a high return on investment (ROI).

Working in Tandem

The semiconductor industry, having set the goal to produce 14nm nodes and 450mm wafers by 2015, can only intensify its strenuous efforts to control the quality of the inputs and the manufacturing process itself. With the LaserTrace 3 insuring the quality of the input gases and the LaserTrace 3x insuring the quality of the process, the hard-working fabs may continue to score—by orders of magnitude—improvements upon previous generations of product.

Fig 3

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Novel 3D integration process flow: backside 'soft' via reveal

Imec has been working on a via-middle through-Si-via (TSV) approach to 3D stacking. This method is new to industry as it allows for a 'reveal' of TSV contacts by using a Si-etch process.

In the new 3D integration flow, a TSV contact is buried in the wafer during front-side processing. After completion of the wafer processing, the wafer is thinned and the bottom side of the TSV contacts are 'revealed' in order to contact to a next layer of a 3D stack.

This process is novel to IC manufacturing and has to be performed with great care, in order not to damage the devices. In the past year, great progress has been made with respect to the wafer-support system for handling 300mm wafers, thinned down to 50μm thickness. A total thickness variation (TTV) of the thinned wafer of less than 2μm has been achieved. Key step in this process is the bonding of the device wafer to a carrier wafer, prior to wafer thinning, by using a temporary adhesive. This material is stable during the subsequent process steps, but still allows for room temperature debonding of the thinned wafer upon completion of backside processing.

After wafer thinning, the backsides of the TSVs are successfully 'revealed' using a Si-etch process. Both wet and dry processes can be used. Chemical mechanical polishing (CMP) of the Cu/Si surface is not used as it results in a high risk of contamination and has a high cost-of-ownership. An effective via reveal process has been obtained using wet etching, exposing the TSVs uniformly on the wafer backside. In this stage, the TSV nails are still protected by their barrier and liner layers. The next step in the backside process consists of applying a backside passivation layer (this avoids Cu diffusion in the thin Si wafer) and selective opening of the liner layers on the TSV. This is achieved using a maskless, self-aligned dry etch-process.

After this 'soft' via reveal process, further interconnect layers and bump interconnects can be processed on the wafer backside. The process is then completed by debonding the thin wafer from the carrier wafer and transferring the thin wafer to a dicing tape. This step can now be performed at room temperature. This process flow was successfully applied to a 300mm diameter wafer with active high-k/metal gate CMOS circuits.

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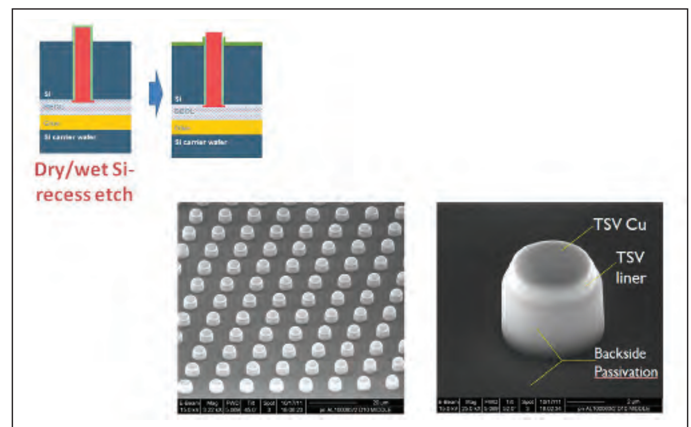
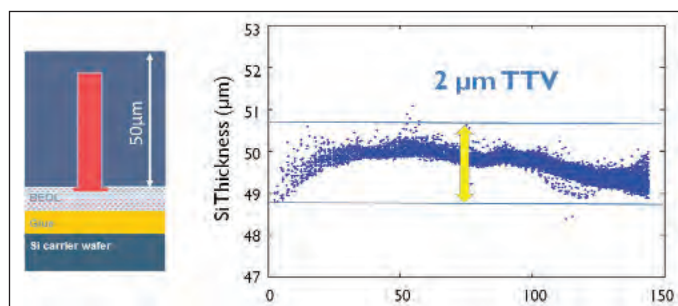
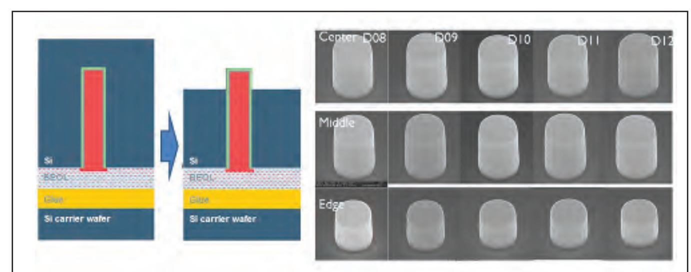


The 'soft' via reveal process with Si3N4 backside passivation.



Wafers are thinned down to 50µm thickness, with a total thickness variation of less than 2µm



Backside 'soft via reveal' process

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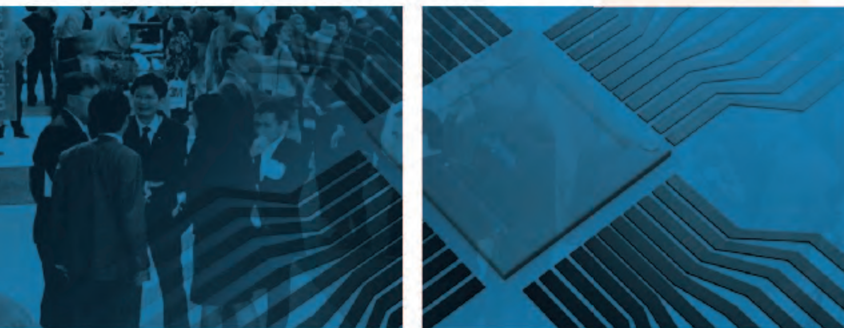

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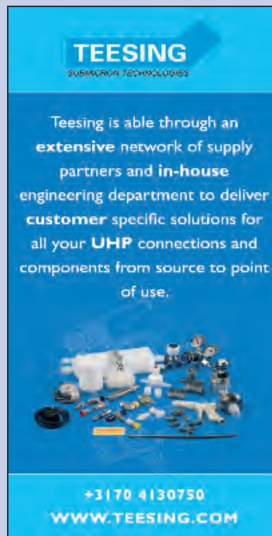

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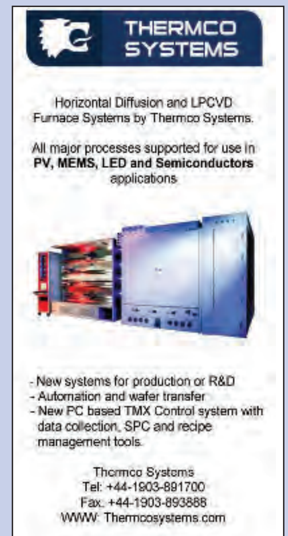

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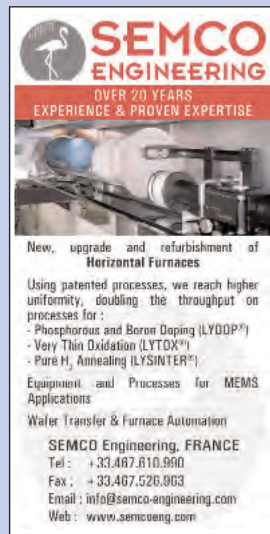

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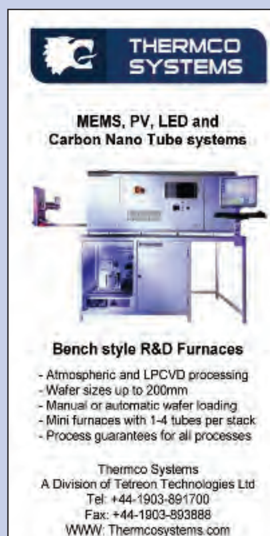

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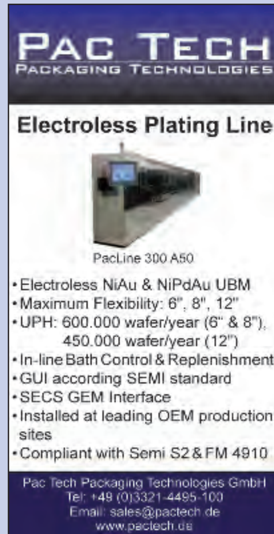

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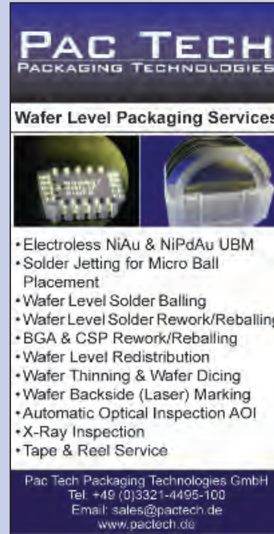

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