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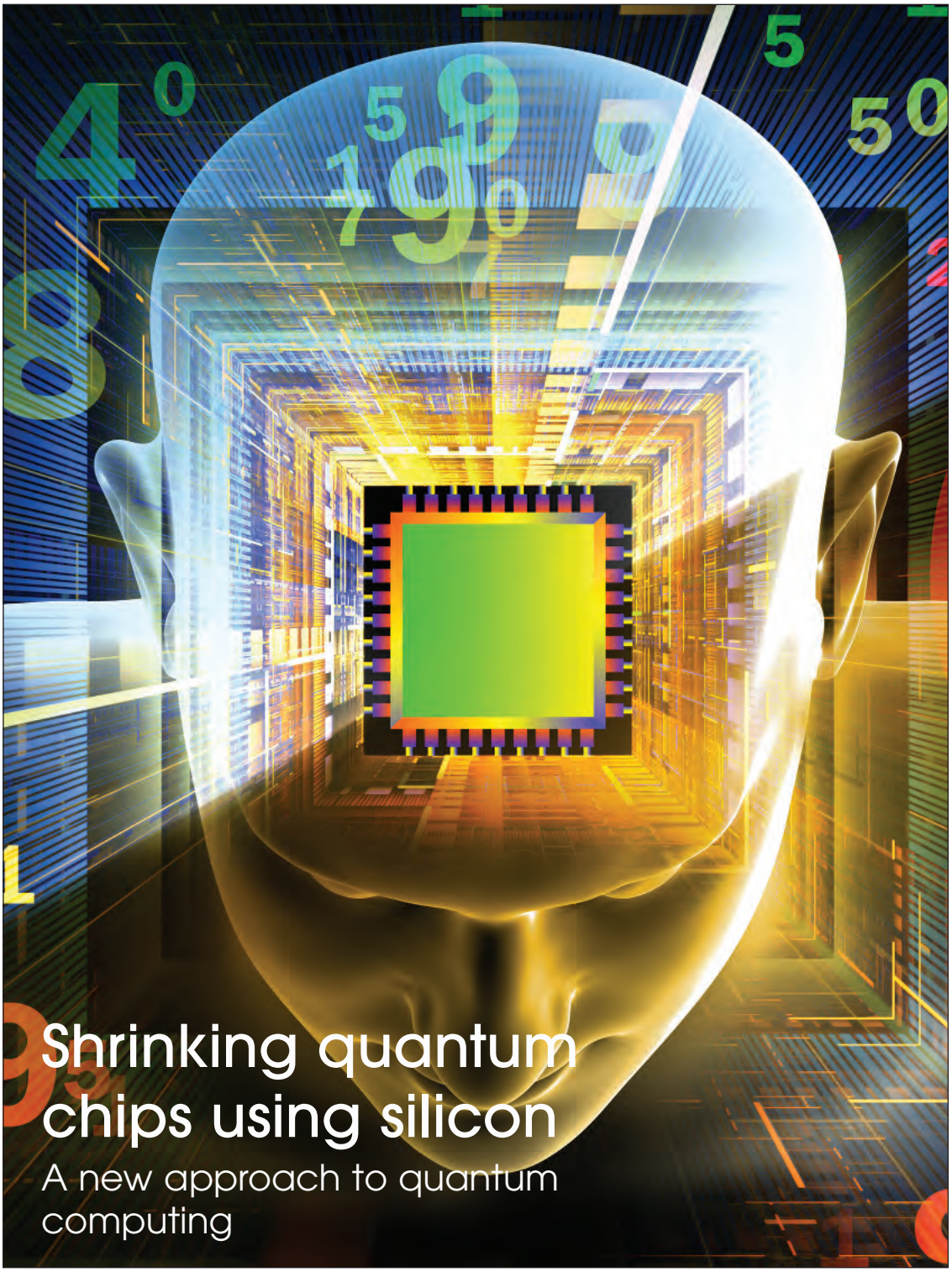

Shrinking quantum chips using silicon

A new approach to quantum computing

An Angel Business Communications publication

Volume 34 Issue 4 2012

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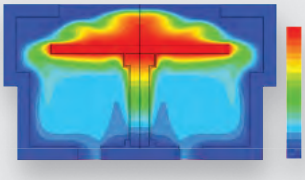

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Volume 34 Issue 4

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Silicon Semiconductor is published four times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/€158 pa (UK & Europe), $138.00 pa (air mail), $198 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication.

US mailing information: Silicon Semiconductor (ISSN 1096-598X) is published four times a year for a subscription of $198 by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. Periodicals postage paid at Rahway, NJ. POSTMASTER: send address changes to: Silicon Semiconductor, c/o Mercury International Ltd, 365 Blair Road, Avenel, NJ 07001

Printed by: Pensord Press. © Copyright 2012.
ISSN 2050-7798 (Print)
ISSN 2050-7801 (Online)

450mm Wafer Transition: a challenging disruptive technology format that opens up new opportunities and risks in semiconductors

THE TRANSITION to manufacturing semiconductors on larger wafers continues to be one of the hottest topics under discussion in the industry. Some chipmakers have committed to advancing the transition. Intel announced that its D1X fab in Oregon and Fab 42 in Arizona will be 450mm compatible. TSMC recently updated their outlook and plans to have 450mm pilot lines by 2016-2017, with volume production in 2018. IMEC has well-established programs focused on the challenges posed by manufacturing with 450mm wafers and the University of Albany's College of Nanoscale Science and Engineering (CNSE) is expanding facilities to encompass 450mm tool development and other related R&D programs. The Global 450 Consortium (G450C), which was announced one year ago, provides a collaborative framework for GLOBALFOUNDRIES, IBM, Intel, Samsung and TSMC to jointly manage 450mm technology development within the CNSE infrastructure.

The 450mm wafer transition represents a significant industry inflection. While the top 3 chip makers have deep pockets and will heavily invest into the new format, the equipment industry needs to reinvent their business models to finance the enormous development costs associated with the new wafer size.

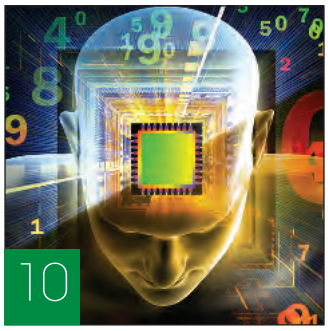
ASML, the largest equipment maker and provider of critical lithography technology, has allowed chip makers to get a stake in their company in order to co-finance the 450mm development. This is understandable as ASML also has to undertake the enormous financial burden of developing new EUV lithography tools. It would not be surprising to see similar new "deals" to mitigate the financial risk for the supply-chain.

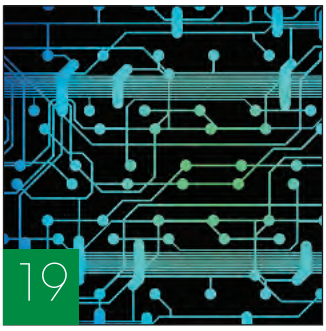
The question remains what will be the impact on the other semiconductor device segments in the "More than Moore" arena? How much "More Moore" is needed to remain competitive there? Clearly, 450mm is not currently a priority for a variety of customer specific applications such as in automotive, analog mixed signal, power devices, MEMS, etc. Nevertheless, some higher volume products might also be attracted by the 450mm community sooner or later. Therefore, most within semiconductor ecosystem are necessarily paying attention to – and planning for, the eventual wafer size transition as it will have widespread implications for those that make the transition as well as those that wait. For its part, SEMI is facilitating the development of industry standards and the flow of information throughout the supply chain with the launch of 450 Central (www.semi.org/450), a web-based information service to help the semiconductor industry efficiently transition to 450mm-ready solutions and keep the industry informed of important news and perspectives on 450mm wafer processing.

By Heinz Kundert,
President SEMI Europe

Volume 34 Issue 4

industry & technology





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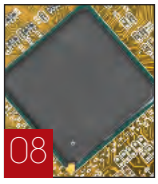


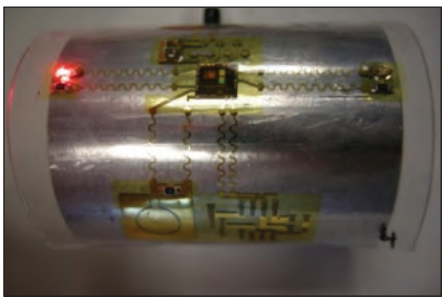
imec: electronics stretches like skin

RESEARCH institute imec has integrated an ultra-thin, flexible chip with bendable and stretchable interconnects into a package that adapts dynamically to curving and bending surfaces.

The resulting circuitry can be embedded in medical and lifestyle applications where user comfort and unobtrusiveness is key, such as wearable health monitors or smart clothing.

At the 2012 ESTC conference (Electronics System Integration Technology Conference) in Amsterdam, the researchers will present their results and showcase their latest demonstrations. Today, most electronic appliances are rigid and mechanically flexible. A growing number of applications, however, require electronics that dynamically adapt to curving and bending surfaces.

For example, biomedical systems such as unobtrusive, wearable health monitors (e.g. electrocardiogram or temperature sensors), advanced surgical tools, or consumer electronics such as mobile phones embedded in smart textiles are needed.



Imec's associated lab at the University of Ghent has pioneered this technology and is inviting industrial partners to join the R&D program.

For the demonstration, the researchers thinned a commercially available microcontroller down to 30μm, preserving the electrical performance and functionality. This die was then embedded in a slim polyimide package (40-50μm thick).

Next, this ultrathin chip was integrated with stretchable electrical wiring. These were realised by patterning polyimide-supported meandering horseshoe-shaped wires, a technology developed and optimised at the lab.

Finally, the package was embedded in an elastomeric substrate, e.g. polydimethylsiloxane (PDMS). In this substrate, the conductors behave as two dimensional springs, enabling greater flexibility while preserving conductivity.

"Future electronic circuitry will stretch and bend like rubber or skin while preserving its conductivity," says Jan Vanfleteren, responsible for the research on flexible and stretchable electronics at imec's Ghent lab.

"This breakthrough achievement demonstrates that flexible Ultra-Thin Chip Packages (UTCP) can be integrated with stretchable wiring, paving the way toward fully flexible applications. We anticipate the first appliances will be used in intelligent clothing, with medical applications following later. Once commercial products are introduced, I expect to see clothing with signalisation by using LEDs and sensors to track movements."

This research is supported by the Agency for Innovation by Science and Technology in Flanders (IWT) through the SBO-BrainSTAR project.

Fujitsu shifts LSI facilities to J-Devices

FUJITSU SEMICONDUCTOR LIMITED will transfer ownership of its Large Scale Integration (LSI) assembly and test facilities belonging to its fully owned subsidiary, Fujitsu Integrated Microtechnology Limited (FIM), to J-Devices Corporation.

The objective of the agreement is for the two companies to build a long-term, mutually beneficial strategic partnership in the semiconductor manufacturing business.

It is expected that a conclusive agreement will be signed and the transaction completed by the end of this year. Fujitsu Semiconductor has been striving to enhance its business foundation and improve corporate management by pursuing a unique "fab-lite" business model, as announced in 2009. As part of these efforts, the company has been optimising its manufacturing resources in accordance with changes in the economic and business environment.

As one of Japan's largest independent companies devoted to semiconductor assembly and test operations for customers, J-Devices believes that, to further expand its business, it must be cost-competitive with business rivals based outside of Japan. To that end, J-Devices believes it is of the utmost importance to extend the scale of its operations.

The ownership transfer of the assembly and test facilities, therefore, is in line with the business objectives and views of both Fujitsu Semiconductor and J-Devices, leading to the signing of the agreement. By the end of this year, ownership of FIM's Miyagi Plant and Aizu Plant is scheduled to be transferred to J-Devices, which will then take over the operation of these manufacturing facilities.

All employees of the two plants are expected to be transferred to J-Devices. In addition, FIM plans a staged transfer of equipment from its Kyushu Plant to J-

Devices facilities also located in Kyushu, and ultimately will transfer all of its manufacturing capability. After the transfer is complete, the manufacturing currently conducted at FIM's Kyushu Plant will take place with the same standards for quality at J-Devices' facilities. Employees of FIM's Kyushu Plant are scheduled to be transferred to J-Devices or reassigned within the Fujitsu Group.

The products that are currently being manufactured at the assembly and test facilities to be transferred will be produced by J-Devices and will continue to be supplied to customers through Fujitsu Semiconductor.

Veeco IBD system slashes defects

SEMATECH, a global semiconductor consortium that conducts research and development to advance chip manufacturing, has recently achieved a major breakthrough using Veeco's NEXUS Low Defect Density Ion Beam Deposition (LDD IBD) System to significantly reduce defects from multi-layer deposition of mask blanks used for extreme ultraviolet lithography (EUVL).

Frank Goodwin, Manager of SEMATECH's Mask Blank Defect Reduction program, stated, "EUVL requires a low defect density reflective mask blank, which is considered to be one of the top two critical technology gaps for commercialisation of the technology. Veeco's world-class IBD technology was a major catalyst in helping us to demonstrate low defect levels for the deposition of critical films, and meet the 22 nm defect requirements for EUV mask blanks."

Vivek Vohra, Veeco's Vice President and General Manager, Veeco Ion Beam Equipment, added, "Veeco's NEXUS LDD IBD System has continuously demonstrated the ability to provide low defect density deposition and precise control, which are required to accelerate the development of mask blanks used for extreme ultraviolet EUV, bringing that technology a step closer to high-volume manufacturing. We congratulate the research team at SEMATECH for reaching this milestone and for achieving it on our production-proven system."

Ion beam deposition tools are used in the fabrication of EUV masks. The nanometre-scale patterns on masks are projected onto a semiconductor wafer to define a chip. A single mask may be used to print over 6 million chips during its life, requiring strict mask defect control.
Advanced-technology EUV masks are

used to define chips with smaller geometries, which results in improved power and performance as required for an increasing number of mobile devices. Veeco says its IBD products enable high film quality, featuring extremely low particulate deposition and precise control of optical properties for single or multi-layer processes, two critical factors for producing advanced EUV photomasks.

Samsung invest in Voltaix to advance semiconductor technology

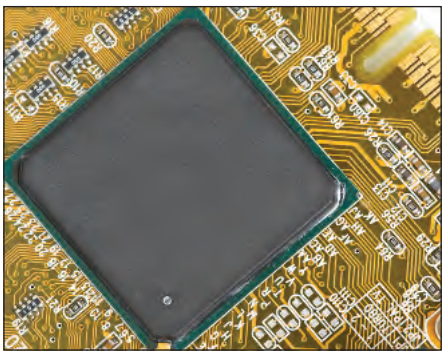
VOLTAIX, a provider of materials that enhance the performance of semiconductor chips and other electronic devices has secured growth financing from Samsung Venture Investment Corporation (SVIC), the global investment arm of Samsung.

Both companies have remained tight-lipped about the amount invested. Voltaix manufactures electronic chemicals and gases used in semiconductor manufacturing processes at major integrated circuit fabs worldwide.

"The financing from SVIC will enable us to continue building our worldwide infrastructure and will further accelerate our new product pipeline development activities," says Peter Smith, CEO of Voltaix.

"We believe our materials innovations will help drive new device architectures and manufacturing technologies to high volume manufacturing," Smith adds.

Dong-Su Kim, SVIC Senior Investment Director notes, "The increasing demand for novel gases and materials in electronics fabrication has attracted our



attention. Based on our analysis of the future demand and the players in the space, we found Voltaix to be the leader and are quite excited about our equity investment."

The firm manufactures specialty materials that enhance the performance and manufacturability of semiconductors. Voltaix produces specialty materials that enhance the performance and manufacturability of semiconductors.

The firm specialises in a number of areas. These include enhancing advanced DRAM computer memory, strained silicon for high speed logic computer chips (CPUs) and copper-enabling low-K dielectrics for logic and memory chips.

Foundry selects Adept robots

ADEPT TECHNOLOGY, INC. has deployed an initial batch of mobile robots to a major semiconductor manufacturer for the automated transport of semiconductor pods.

"Adept is very pleased to have begun introducing mobile technology to the semiconductor and cleantech space through this initial production deployment with such a large and respected client," said Rush LaSelle, vp and general manager of mobile robots. The use of automated guided vehicles (AGVs) has been explored by semiconductor fabs for decades, but such robots have so far not been utilised very much. This is mainly down to the inherent nature of traditional AGVs which have lacked navigational flexibility and ease of installation. Adept's indoor navigation technology and small platforms function well within crowded environments and allow for non-disruptive installation in sensitive facilities. Adept's newly released SPC-4200 and SPH-2200 transporters are used to carry pods from one machine tool to another (intra-bay loading) and between various process areas within the fab (inter-bay transfer). The pods are enclosed in plastic boxes that encase a set of semiconductor wafers

SEMI equipment spending plummets 13 percent

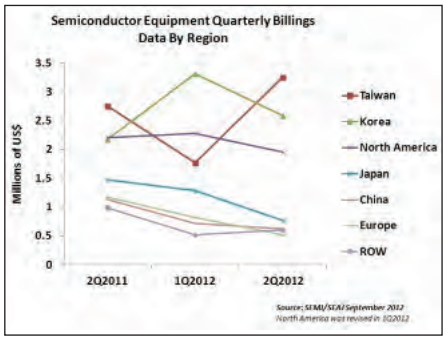
SEMI has reported that worldwide semiconductor manufacturing equipment billings reached US$ 10.34 billion in the second quarter of 2012.

The billings figure is 4 percent lower than the first quarter of 2012 and 13 percent lower than the same quarter a year ago.

The data was gathered jointly with the Semiconductor Equipment Association of Japan (SEAJ) from over 100 global equipment companies that provide data on a monthly basis.

Global semiconductor equipment bookings were $9.70 billion in the second quarter of 2012. The figure is 10 percent lower than the same quarter a year ago and 4 percent lower than the bookings figure for the first quarter of 2012.

The quarterly billings data by region in millions of U.S. dollars is shown in the



graph above and shows that apart from the rest of the world (ROW), Taiwan was the only country to increase spending on semiconductor equipment in the second quarter this year as compared to Q1 2012.

Year-over-year, Japan and China cut their spending from Q2 2011 to Q2 2012 by 48 percent and 44 percent, respectively while Europe slashed its spending by a massive 56 percent.

Creating a low-noise chip-based optical wavelength converter

Researchers from the NIST Centre for Nanoscale Science and Technology have demonstrated a low-noise device for changing the wavelength of light using nanofabricated waveguides created on a silicon-based platform using standard planar fabrication technology.

Optical wavelength conversion is an important resource for applications in both classical and quantum information processing; it can connect physical systems operating at different wavelengths, and facilitate improved light detection by converting light to wavelengths for which highly sensitive detectors are available.

However, for many such applications the conversion process must not introduce additional noise.

Now researchers at NIST have demonstrated noise-free wavelength conversion using silicon nitride (SiN) waveguides fabricated on a silicon substrate. These waveguides were designed based on electromagnetic simulations to determine an appropriate device geometry for a process called four-wave-mixing Bragg scattering, where an input signal field is converted to an output field whose frequency is shifted from the original by an amount equal to the difference in the frequencies of two applied pump fields.

Measurements show conversion efficiencies in these devices as high as a few percent, approaching the levels needed for some applications, and with no excess noise added during the conversion process. These new noise-free frequency converters are dramatically smaller than the nonlinear crystals and optical fibres used in previous work (by several orders of magnitude), and can be created in arrays and integrated with other on-chip devices using scalable silicon-based fabrication methods.

The scientists say that in the future, they will focus on increasing the conversion efficiency levels by optimising the waveguide geometry and incorporating the waveguides into optical resonators.

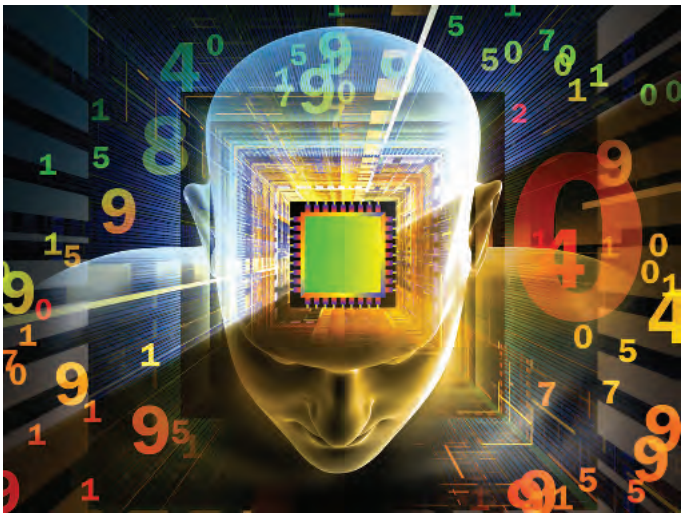
Foundries boost 2012 spend

SEMI's World Fab Forecast database indicates that the total fab spending for equipment needed to ramp fabs, upgrade technology nodes, and expand or change wafer size could increase 16.7 percent in 2013 to reach a new record high of $42.7 billion.

The estimate includes new equipment, used equipment, or in-house equipment but excludes test assembly and packaging equipment.
The latest edition of the forecast lists over 1,150 based facilities and includes 850 silicon based plants, with 76 facilities starting production this year and in the near future. Since the previous publication in May 2012, SEMI analysts have added 296 fabs to more than 230 facilities, into the database. This includes 244 silicon fabs. Semiconductor manufacturing foundries were significant drivers of fab equipment spending in 2012 with over $10 billion combined investment. Their dominance is expected to continue with approximately $10 billion additional equipment spending in 2013. In 2012, the Americas dominated fab construction. From 2010 to 2012, over $6 billion will be spent on fab construction projects in this region, led by Intel, Samsung, Globalfoundries, and Micron. Most of these construction projects will be completed by the end of 2012. No immediate new fab projects in the Americas are anticipated, resulting in projected investment for 2013 construction to drop below $500 million from almost $3 billion in 2012. The situation is set to change In 2013, however, with most fab construction expected occur in Taiwan, China, and Korea. Samsung has begun an aggressive conversion of up to four existing Memory lines to System Large Scale Integration (LSI). A transition from Flash to System LSI is difficult; some drop in capacity in Memory is expected, but the company is expected to compensate by building a new fab for Memory, in Xian, China, with a whopping investment of $7 billion. The fab is expected to begin construction in mid-September 2012. Other increases in fab construction investment will come from SMIC's new fab in Beijing, and TSMC and UMC fab projects in Taiwan.

Shrinking quantum chips using silicon

A research team led by scientists from the University Of Bristol, UK, has developed a new approach to quantum computing that they say could lead to the mass-manufacture of new quantum technologies.



Scientists from University of Bristol, UK, Centre for Quantum Photonics have developed a silicon chip that will pave the way to the mass-manufacture of tiny quantum chips.

The announcement was made at the launch of the 2012 British Science Festival in September. Conventional semiconductor technology is largely based on crystalline silicon which is an indirect bandgap semiconductor. This means it is inefficient at emitting light compared to materials such as gallium arsenide and indium phosphide, which have a direct bandgap. These latter materials are compound semiconductors and are widely used in optoelectronics.

Now that optoelectronics is becoming increasingly important for information and communication technologies, there is a need to develop optoelectronic devices that can be integrated with standard microelectronics. The leap from using glass-based circuits to silicon-based circuits is significant because fabricating quantum circuits in silicon has the major advantage of being compatible with modern microelectronics. Ultimately the researchers believe this technology could be integrated with conventional microelectronic circuits, and could one day allow the development of hybrid conventional or quantum microprocessors.

Now the research team led by the University of Bristol has developed quantum chips from silicon. However, unlike conventional silicon chips that work by controlling electrical current, these circuits manipulate single particles of light (photons) to perform calculations.

These circuits exploit strange quantum mechanical effects such as superposition (the ability for a particle to be in two places at once) and entanglement (strong correlations between particles that would be nonsensical in our everyday world). The technology developed uses the same manufacturing techniques as conventional microelectronics, and could be economically scaled for mass-manufacture. These new circuits are compatible with existing optical fibre infrastructure and are ready to be deployed directly with the internet.

Mark Thompson, Deputy Director of the Centre for Quantum Photonics in the University's Schools of Physics and Electrical & Electronic Engineering, said, "Using silicon to manipulate light, we have made circuits over 1000 times smaller than current glass-based technologies. It will be possible to mass-produce this kind of chip using standard microelectronic techniques, and the much smaller size means it can be incorporated in to technology and devices that would not previously have been compatible with glass chips. This is very much the start of a new field of quantum-engineering, where state-of-the-art micro-chip manufacturing techniques are used to develop new quantum technologies and will eventually realise quantum computers that will help us understand the most complex scientific problems," he continued.

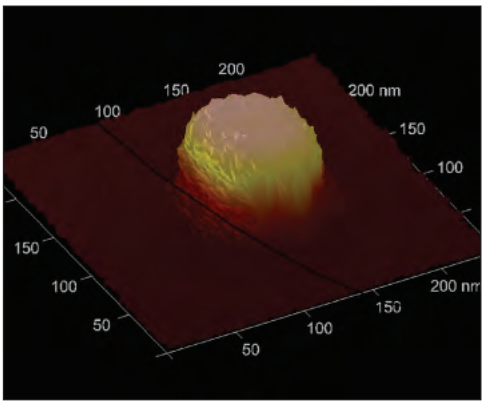
Along with recent demonstrations from the Bristol research group and other groups showing on-chip generation of photonics qubits and results from the US showing on-chip detection of single photons, the Bristol-lead research team now believes that all the key components are in place to realise a fully functioning quantum processor - a powerful type of computer that uses quantum bits (qubits) rather than the conventional bits used in today's computers.

Quantum computers will have unprecedented computational power for tasks including search engines and the design of new materials and pharmaceuticals. This work, carried out with collaborators including Heriot-Watt University in Scotland and Delft University in the Netherlands, is an essential step towards the miniaturisations of quantum technologies.

How IBM & GLOBALFOUNDARIES improve computer chips

A refined method developed at the National Institute of Standards and Technology (NIST) for measuring nanometre-sized objects may help computer manufacturers more effectively size up the myriad tiny switches packed onto chips' surfaces.

The process, which makes use of multiple measuring instruments and statistical techniques, is already drawing attention from the semiconductor industry. According to NIST scientist Richard Silver, "IBM and GLOBALFOUNDRIES have already begun developing the technique since we first described it at a 2009 conference, and they are improving their measurements using this hybrid approach."



The image above, showing a tiny silicon pillar measuring less than 100 nm along any of its sides, is the sort of computer chip feature that manufacturers can now measure more precisely with NIST's hybrid metrology method. This information can reduce the nagging uncertainties that have long plagued industry's measurement efforts.

Nothing in life is certain except maybe death and taxes, but in the world of computer chip manufacturing, uncertainty is a particularly annoying issue, especially when measuring features smaller than a few dozen nanometres. Precision and accuracy are essential to controlling a complex and expensive manufacturing process to ensure the final chips actually work.

But features on modern chips are so tiny that optical microscopes cannot make them out directly. Metrologists have to use indirect methods, like "scatterometry" to deduce their shape from sampling the pattern light creates as it scatters off the features' edges. When this isn't enough, there's atomic force microscopy (AFM). It's expensive and slow, but it can give distinct measurements of the height and width of a nanoscale object while light scattering occasionally has trouble distinguishing between them.

Even with these measurement techniques, however, there's always a nagging margin of error. "Maybe scatterometry tells you the width of an object is 40 nanometres, but it's plus or minus three nanometres, a relatively large variance," says NIST scientist Richard Silver. "Making things worse, the total uncertainty usually increases when measurement techniques are combined, making our vision even hazier."

What the NIST team needed was a more precise yet less expensive method of measuring what sits on a chip, and their answer has turned out to be a combination of scanning techniques and statistical analysis. They first created a library of simulated data based on typical chip feature dimensions to which they can compare their actual measurements, made with AFM, scatterometry and other means.

A complex statistical analysis of library values is then compared with actual measurements to extract valid measurement values, but this is often at a cost of high uncertainty. But NIST statistician Nien Fan Zhang found an elegant way to use a statistical method called Bayesian analysis to incorporate a few key additional measured values from other tools into the library model before performing the comparison.

In doing so, the team was able to reduce the uncertainty in some of the measurements, lowering them by more than a factor of three in some cases. This approach is expected to be essential when measuring complex three-dimensional transistors 16 nm in size or smaller in the near future.

The math wizardry is a little counter-intuitive. "In essence, if you've got a really small uncertainty in your AFM measurement but a big one in your optical measurements, the final uncertainty will end up even smaller than either of them," says Silver.

The hybrid method has been described in detail in the paper, "Improving optical measurement uncertainty with combined multitool metrology using a Bayesian approach," by N.F. Zhang et al, in Applied Optics, Vol. 51, No. 25. Sept. 1, 2012. DOI: http://dx.doi.org/10.1364/AO.51.006196

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Event Schedule

Programs and Events: 8-11 October 2012
Exhibits: 9-11 October 2012
Messe Dresden, Germany

	Exhibition Register now online!	TechARENA 1 Free Participation - Hall 1	TechARENA 2 Free Participation - Hall 2	Conferences MEMS, Test, Packaging
Monday **8 October**				**International MEMS/MST Industry Forum** New Dynamics in the MEMS Industry
Tuesday **9 October**	**Exhibition** 10:00 – 17:00 **Show Floor Highlights:** - Science Park - Secondary Equipment and Services Pavilion - MEMS, Test and Packaging Pavilion - PE2012 Exhibition	**New Materials Session** **MEMS** Exhibitor Presentations **Advanced Process Control (APC) and Manufacturing**	**Packaging Session** Exhibitor Presentations **PE 2012** Exhibitor Presentations **Secondary Equipment and Technology Session**	**International MEMS/MST Industry Forum** New Dynamics in the MEMS Industry **Advanced Packaging Manufacturing Conference** Packaging Solutions for the New Technologies
Wednesday **10 October**	**Exhibition** 10:00 – 17:00 **Show Floor Highlights:** - Science Park - Secondary Equipment and Services Pavilion - MEMS, Test and Packaging Pavilion - PE2012 Exhibition	**Test** Exhibitor Presentations **Market Briefing** **Metrology, Process Control, Automation and Software**	**Workshop on Equipment Assessment & Equipment Performance Improvements** **IC Industry Awards** by SiS SILICON SEMICONDUCTOR Silicon2012 Semiconductor industryawards	**Advanced Packaging Manufacturing Conference** Packaging Solutions for the New Technologies **14th European Manufacturing Test Conference (EMTC)** Overcoming New Test Challenges through Cooperation and Innovation
Thursday **11 October**	**Exhibition** 10:00 – 16:00 **Show Floor Highlights:** - Science Park - Secondary Equipment and Services Pavilion - MEMS, Test and Packaging Pavilion - PE2012 Exhibition	**3D IC Session**	**Lithography Session** **LED / SSL Session**	**14th European Manufacturing Test Conference (EMTC)** Overcoming New Test Challenges through Cooperation and Innovation

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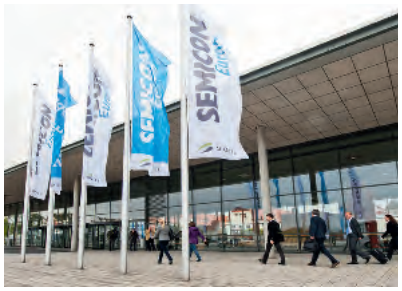

Conferences

MEMS, Test, Packaging

International MEMS/MST Industry Forum
New Dynamics in the MEMS Industry

International MEMS/MST Industry Forum
New Dynamics in the MEMS Industry

Advanced Packaging Manufacturing Conference
Packaging Solutions for the New Technologies

Advanced Packaging Manufacturing Conference
Packaging Solutions for the New Technologies

14th European Manufacturing Test Conference (EMTC)
Overcoming New Test Challenges through Cooperation and Innovation

14th European Manufacturing Test Conference (EMTC)
Overcoming New Test Challenges through Cooperation and Innovation

Semiconductors

16th Fab Managers Forum
Networking Evening

16th Fab Managers Forum
Conference

SPECTARIS-Forum
Trends in Semiconductor Processing and Market Environment for the Photonics Industry (organized by SPECTARIS)

450mm Session
Progress in 450mm

450mm Session
Progress in 450mm

Exec. Programs

Business & Market

Press Conference

6th Executive Summit and Reception

SAXONY! - Get Together

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Making Ring Oscillator Measurements

In the world of CMOS wafer parametric testing, the ring oscillator is one of the more important test structures because its test data helps confirm that logic gates are meeting their speed design criteria. Dave Rose, Senior Staff Engineer, Keithley Instruments, Inc discusses techniques for testing these devices using automated parametric testers.

A growing number of semiconductor fabs are incorporating ring oscillators into their overall process control monitoring test structures. Frequency measurements on ring oscillator structures are used to determine gate propagation delay, one of the critical parameters that determine how quickly a digital circuit can operate. Every logic gate has input capacitance, so no device can switch instantaneously because the input capacitance limits the speed at which a gate can switch. However, this gate propagation delay is too short for most test equipment to measure directly, so test systems measure oscillation frequency instead and the gate propagation delay is calculated from this frequency measurement.

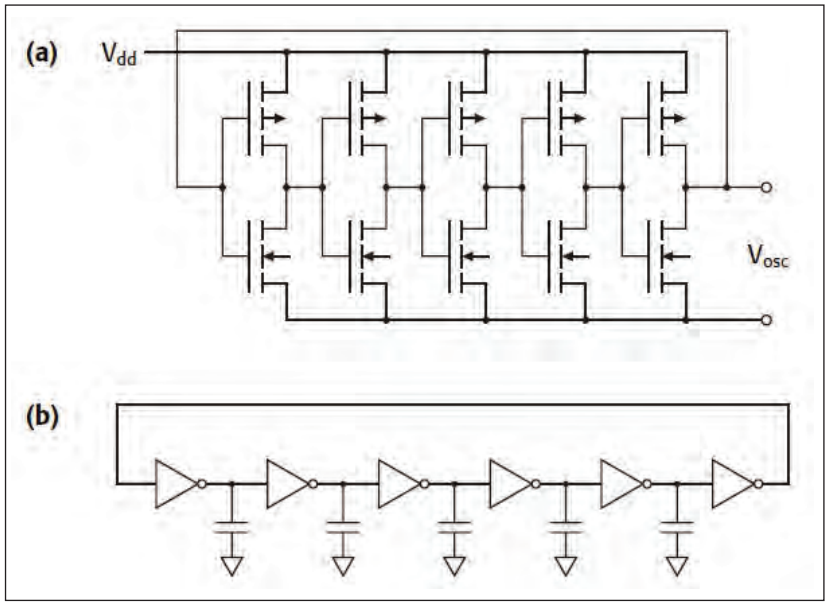

Figure 1. Schematic (a) and block diagram (b) representation of a CMOS ring oscillator (without trigger or buffer stage)

In a CMOS fabrication process, a ring oscillator test structure is typically designed and constructed with an odd number of inverter stages. Rather than cell libraries or gates, a ring oscillator test structure is usually constructed from transistors in order to ensure an accurate representation of the parameters of interest.

The structure is designed to be as compact as possible to ensure that its performance is dominated by the transistors rather than by the interconnects. The device channel length of the transistors is usually the minimum length that the process design rules will support.

Figure 1a is a high-level schematic view of a typical ring oscillator circuit; Figure 1b is a block diagram of a ring oscillator.

The ring oscillator shown in Figure 1a (like all ring oscillators) consists of an odd number of inverter stages. The input can consist of a 2-input NAND gate that can serve as an externally controlled trigger. Once triggered, the ring oscillator will free-run at a frequency that's dependent on the propagation delay between the stages.

Because the ring oscillator will natively oscillate at a frequency much higher than a typical parametric test system can measure directly, the output of the test structure is usually isolated with a buffer (in order to deal with the effects of test system capacitance) and its output signal divided using a

D-type flip-flop by a factor of 256 (or as high as 1024 for processes 0.25_m or smaller). The measured frequency (after the signal is divided) is typically on the order of 1-50MHz.

Given that the oscillation frequency is what's being measured but the propagation delay is the actual parameter of interest, the next step is to calculate the propagation delay from the frequency measurement using this equation:

$$t_{delay} = \frac{1}{2nf_{osc}}$$

where: *n* is the number of inverter stages and fosc is the measured frequency of oscillation

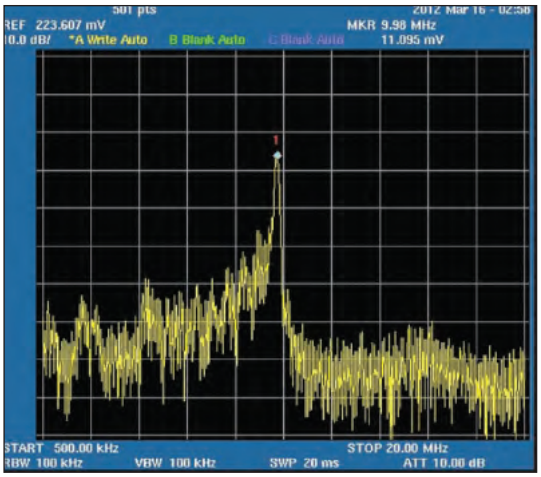

Figure 2. Ring oscillator signal spectrum through the S530 switch matrix

Measurement considerations

Parametric test systems have always been optimized to perform accurate, low-level DC measurements. However, AC performance for these systems is also important for supporting C-V measurement, pulse generation, and frequency analysis of ring oscillator structures.

The Model S530 Parametric Test System, for example, has been designed to provide high accuracy DC measurements over a broad dynamic range and with an AC signal bandwidth of 20-30MHz. A frequency counter is often thought of as the best instrument for measuring frequency.

However, given that frequency counters count crossings (through zero, etc.), they can often produce erroneous readings in situations where the signal has to be extracted from a noisy AC environment. That's why frequency measurements are often best performed using a spectrum analyzer or an oscilloscope using spectrum analysis techniques.

Spectrum analyzers operate by converting a signal from the time domain to the frequency domain using Fourier analysis. Each frequency in the signal's spectrum is plotted versus its signal amplitude (Figure 2). That means, in a noisy signal environment, the signal of interest is often the one with the highest amplitude. Of course, in some instances, even spectrum analysis fails, such as when the amplitude of the signal of interest is below the noise floor of the system.

Frequency Measurement Software

Like many frequency measurement solutions, the S530's frequency measurement option supports a variety of measurement commands:

ring_max	Detects the frequency with the highest amplitude.
ring_ref	Detects the frequency that is closest to the specified reference frequency.
ring_Icc	Detects the 5 frequencies whose amplitudes are larger than the specified threshold.
ring_meas	Determines the ring oscillator frequency and amplitude.
freq_init	Initializes the oscilloscope card to its default state.
freq_setup	Sets the start frequency and end frequency of the scan as well as the resolution bandwidth.
freq_measure	Measures the frequency and amplitude of the strongest signal.
freq_measure_next	Measures the frequency and amplitude of the next strongest signal as compared to the measurement returned by the freq_measure command.
freq_detect_peaks	Returns the frequencies and amplitude of the specified number of peaks.
freq_selftest	Places the oscilloscope card in self-test mode and returns the status.

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This is another situation in which a spectrum analyzer will produce more accurate readings than a frequency counter because the amplitude of the frequency of oscillation will usually stand out despite these distortions

In applications outside the general-purpose parametric test environment, test system designers strive to ensure that the impedances of the DUT, transmission lines, and measurement equipment are matched and that there are no open signal paths, thereby minimizing the major causes of AC signal distortion: insertion loss and reflections. However, this is not always possible to accomplish in a DC parametric test environment.

This is another situation in which a spectrum analyzer will produce more accurate readings than a frequency counter because the amplitude of the frequency of oscillation will usually stand out despite these distortions.

Frequency measurement hardware

Some parametric testers, including the S530 Parametric Test System, support characterizing ring oscillators using a frequency measurement option. For the S530, this measurement option is oscilloscope-based and connects to an instrument port on the system's switch matrix, just like the system's source measurement units (SMUs), C-V unit, pulse generator units, and digital multimeter (DMM.) Once connected to the switch matrix, the frequency measurements can be switched to any one of the matrix's DUT pins.

The instrument driver for the frequency measurement option measures the frequency of a ring oscillator signal by using Fourier analysis to convert the signal from the time domain to the frequency domain. The various software commands return the measurement in the form of pairs of results, corresponding to the frequency and amplitude of the strongest signals. The S530's frequency measurement option can accurately measure AC signals with signal levels above 25mVp-p and frequencies up to 20MHz.

Ring oscillator measurement example

To illustrate the process of making a ring oscillator measurement, let's begin by assuming a ring oscillator like the one shown in Figure 3. The freq _ init, freq _ setup, and freq _ measure commands described previously provide one way to measure the ring oscillator frequency and signal amplitude. For the purposes of this example, let's assume that

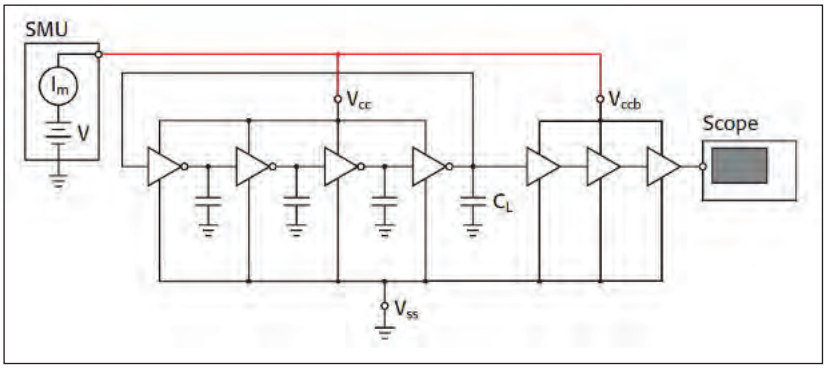


Figure 3. Generalized CMOS ring oscillator

For this example, the following seven-command S530 test sequence could be used to perform this measurement:

vss _ pin = 1 vcc _ pin = 2 vccb _ pin = 3 output _ pin = 4	Defines the DUT pins.
vcc = 5.0	Defines the voltages required to power and trigger the ring oscillator.
conpin(SMU1, vcc _ pin, vccb _ pin, 0) conpin(vss _ pin, GND, 0) conpin(SCP1A, output _ pin, 0)	Makes the connections to the DUT.
forcev(SMU1, vcc)	Powers the device and triggers the oscillation.
init _ status = freq _ init()	Initializes the oscilloscope card. This command is always required to use the scope card!
setup _ status = freq _ setup(0e6, 15e6, 1e6)	Defines the frequency scan and resolution bandwidth. Because the oscillator frequency is 10MHz, it's essential to make sure that it is within the scan boundaries. In this case, the start frequency is set to 0Hz, the end frequency to 15MHz, and the resolution bandwidth (or scan resolution) to 1MHz. This would give a frequency measurement that is accurate to 1MHz.
meas _ status = freq _ measure(frequency, level)	Performs the measurement and returns the frequency (in Hz) and amplitude (in Vp-p) of the strongest signal found.

the ring oscillator frequency is 10MHz and that its Vss, Vcc, Vccb, and output pads are connected to pins 1, 2, 3, and 4 respectively. Let's further assume this device requires 5V to power it and 5V to trigger the oscillation.

This article has offered a number of techniques useful for performing ring oscillator measurements with a frequency measurement tool.

The ring _ max command listed previously offers a simpler approach to performing this same measurement:

vss _ pin = 1 vcc _ pin = 2 vccb _ pin = 3 output _ pin = 4	Defines the DUT pins.
vcc = 5.0	Defines the voltages required to power and trigger the ring oscillator.
meas _ status = ring _ max(vcc _ pin, vccb _ pin, vss _ pin, output _ pin, vcc, 10e6, 0.5, 25e-3, frequency, level, meas _ status)	Performs the measurement and returns the frequency (in Hz) and amplitude (in Vp-p) of the strongest signal found. The ring _ max command simplifies things a bit. Although most of the arguments are self-explanatory when compared to the previous example, the 6th, 7th, and 8th arguments (...10e6, 0.5, 25e-3...) require some explanation: ● 10e6 is the expected frequency of oscillation. ● 0.5 is the measurement tolerance. This parameter tells the function how to know that it has measured the desired frequency. The measurement stops when the following condition is met: $\frac{f_{meas} - f_{expected}}{f_{expected}} < tollerance$ ● 25e-3 is the minimum acceptable signal level in Vp-p.

Vacuum pump selection for advanced chip packaging

Today, advanced semiconductor packaging techniques are employed that move beyond simple wire bonding of a single die. Stacked dies, flip chips, and recently, more frequent employment of redistribution layer (RDL) wiring are commonplace to convert nanometer scale dimensions to ones more easily measured in fractions of a millimeter. Michael S. Boger, Global Market Sector Manager for Edwards, discusses.

With greater complexity in packaging, the number of bonding pads has, likewise, increased significantly. Further complexity is added with the introduction of interposers to act as a virtual breadboard for multiple dies in a single package – colloquially, a 2.5D device. In a few years, true 3D will be a reality with the stacking of homogeneous or heterogeneous dies. The trend to increasing complexity and 3D processing can be considered one of the "More than Moore" trends referenced in the International Technology Roadmap for Semiconductors. This trend is shown pictorially in Figure 1.

Growing challenges due to packaging topology selection are associated with greater use of vacuum-based processing tools. For example, flip-chip packaging can make use of physical vapor deposition (PVD) vacuum processing equipment to deposit the under-bump metals (UBM) used as the bonding locations for the solder bumps.

When RDL wiring, which can also be deposited via PVD or electrochemical deposition, is added, dielectric deposition is required to insulate the metal traces. This dielectric could be chosen from a number of different materials. In particular, polyimide appears to find some level of popularity.

If, as forecasted, silicon interposers find more use in advanced packaging, a full suite of interconnect–producing, vacuum-based processing equipment will be required to create the package-enabling through-silicon-vias (TSVs) and dual-Damascene wiring (depending on the number of wiring levels).

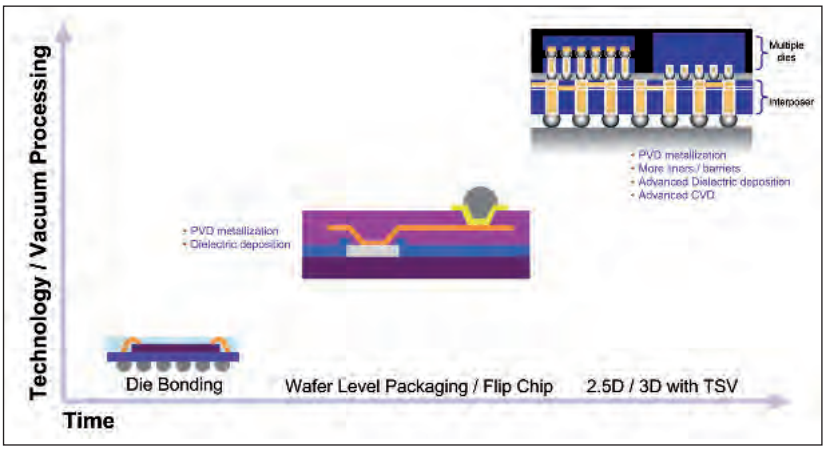


Figure 1. Increased complexity in packaging will require greater user of vacuum-based processing tools

The feature sizes of the circuitry are orders of magnitude larger than today's smallest transistor sizes, but the reliable manufacture of such features will require semiconductor processing knowledge. With full 3D packaging technology, greater skill will be required, as well as a potential division of labor related to device manufacturing and packaging.

In particular, for both 2.5D and 3D technology, the questions are: will independent device makers (IDMs) and foundries do the packaging themselves? Will out-source assembly and test (OSAT) companies stretch their technology portfolio to include more vacuum processing? Or, will all of the work go to an independent third party as part of an intellectual property protection strategy, especially when chips from different vendors are used in a single package? Today, no one business or technology model prevails. From a vacuum company perspective, one conclusion can be derived: more and more vacuum processing equipment will be required in the packaging factory, and the packaging factory managers are likely to be less experienced with that equipment than those same managers of an IDM or foundry.

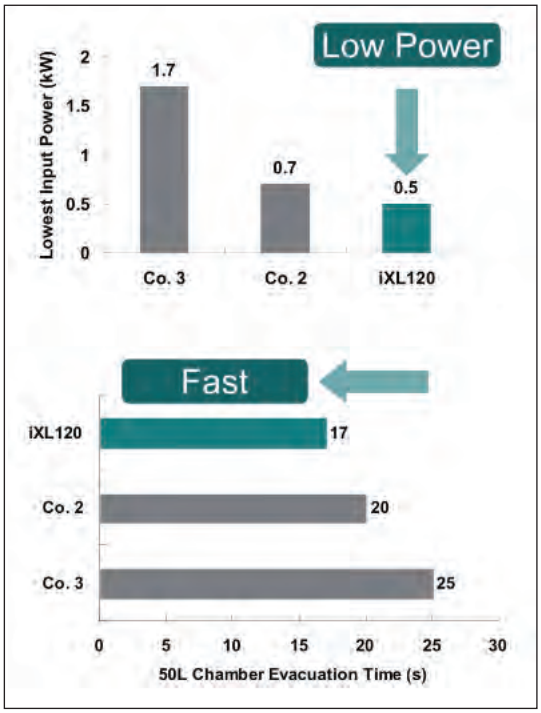


Figure 2a. Performance comparison of similarly classed load-lock pumps for use with with vacuum processing tools

To minimize operating costs in an advanced packaging factory, it is helpful to take advantage of the advancements in vacuum product technology. For example, new vacuum pumps dedicated to load-lock or light duty processing are incredibly compact with low consumption of utilities. Figure 2 shows an example of such a light duty pump (the iXL120 from Edwards, which is well suited for PVD processing tools) and how it compares to other similar products in the market. The iXL120 consumes only 500 Watt of input power at a 700 Torr exhaust pressure. It can also evacuate a 50 liter vacuum chamber in only 17 seconds, a distinct advantage for improving processing tool throughput.

More vacuum pumps will be required for other processes likely to be introduced into packaging factories for 2.5D and 3D processing, such as chemical vapor deposition (CVD) of dielectrics and deep reactive ion etch (DRIE). DRIE, in particular, poses particular challenges related to thermal management of the pump and all associated piping to ensure high reliability and a long time between pump services. Experience with best known methods related to pump reliability counts if down-time is to be minimized.

As the complexity of processing increases, so will the number of vacuum pumps in the factory. As a company's size increases, the number of factories will also increase, especially since packaging tends to be geographically close to where the wafers are being manufactured. In order to maximize operational efficiency, it can be financially advantageous to monitor vacuum pump performance to prevent unplanned maintenance and scrapping of wafers.

Vacuum pumps provided by leading manufacturers generally have on-board data monitoring capability and an ability for connection to a network where a database server is running to monitor and capture data. With good network design, vacuum pump data can be made easily available within a company's intranet for monitoring purposes. Especially when fault prediction algorithms are employed, savings related to implementing a computer monitoring system add up quickly.

Figure 2b. iXL120 Vacuum Pump

Consider the assumptions shown in Table 1. Using the assumptions given, it can be seen that routine checks would cost a company $60,833 (€47,388.91) per year. If the data is analyzed and discussed, it can cost $10,920 (€8,506.68) per year. The higher costs come from an unplanned event that results in lost production. If five unplanned events occur per year, and it is assumed $1,000 (€779.00) can be earned per wafer, the unplanned events can add up to $1,000,000 (€779,000.00) of loss production per year excluding the cost of any lost wafers.

Although the price per wafer that can be earned varies greatly by product produced, even a value of $500 (€389.50) per wafer still results in a significant savings if computer monitoring can reduce the amount of unplanned downtime. Evidence suggests that making use of on-board monitoring capability within leading edge vacuum pumps can only be beneficial. In order to realize these benefits, it is important to select vacuum pumps, such as turbo-molecular pumps, from a single vendor to ensure seamless connection to a dedicated monitoring system.

Item	Assumption
Number of pumps	100
Periodic checks	
Routine pump check	5 min / pump
Service person's wage	$20 / hr (€15.58)
Cost for checks	$60,833 / year (€47,388.91)
Data review and analysis	
Analysis time	2 hr / week
Collation / summary	1 hr / week
Analyst wage	$70 / hr (€54.53)
Cost for analysis	$10,920 / year (€8,506.68)
Pump replacement analysis	
Time to replace	2 hr
Tool preparation time	2 hr
Unplanned times	5 / year
Downtime per year	20 hr / year
Process tool & wafer price	
Tool throughput	50 wafer / hr
Price per wafer earned	$1,000 (€779.00)

Table 1. Model Assumptions

In conclusion, advances in semiconductor packaging are happening today. Tomorrow, greater complexity involving semiconductor vacuum-based processing will pose a challenge. Using advanced vacuum products from experienced companies will help reduce operational costs, especially if features built-in to the products can be used to advantage.

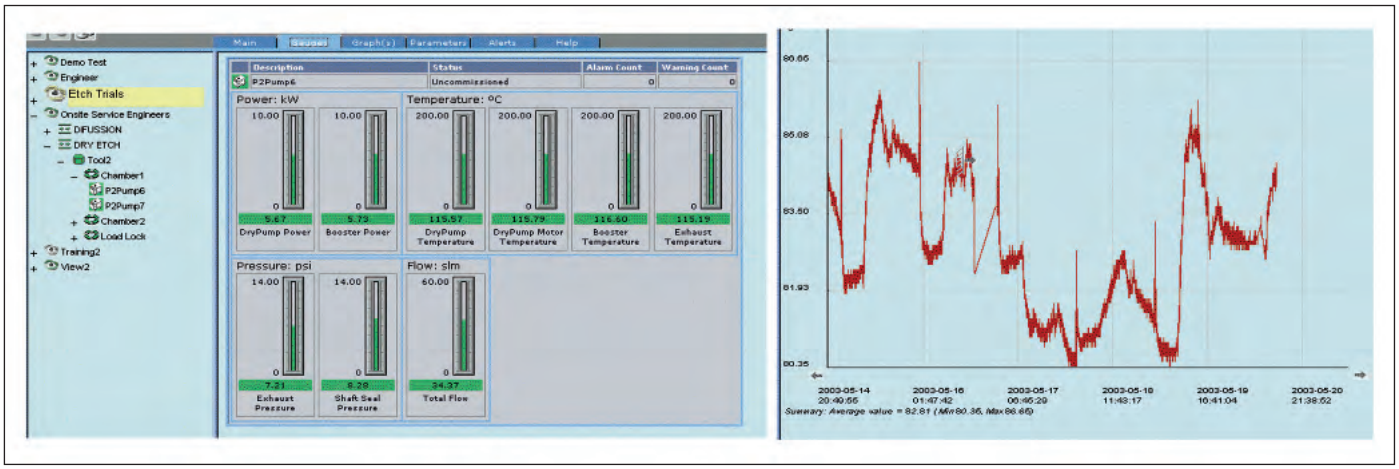


Figure 3 (a) Example of Edwards Fabworks equipment monitoring scheme. (b) Example of data monitoring used for predictive failure analysis

SEMICON Europa: A marketplace for visionaries

In a few weeks Europe's largest and most important show for the semiconductor manufacturing industry will start. It's the marketplace that promotes the sharing of knowledge and ideas, brings together manufacturers and suppliers, creates standards and enables all participants to think outside the box.

SEMICON Europa 2012 and Plastics Electronics 2012 will provide unique opportunities for companies. Now integrated with SEMICON Europa is the 8th Plastics Electronics Exhibition and Conference (PE2012). It will also take place from 9 – 11 October at Messe Dresden.

The mission of PE2012 is to bring together experts, research institutions, manufacturers, investors, suppliers and other industry stakeholders to accelerate plastic electronics from the laboratory to the large-scale, high volume production.

More than 350 exhibitors from over 20 countries are expected at the combined SEMICON Europa and Plastic Electronics events, which also feature over 210 industry leaders speaking on a wide range of topics.

The 16th European Fab Managers Forum, a comprehensive two-day event, covers issues and topics focused on improving

manufacturing productivity and extending the life of existing FABs through new technologies and markets. The topic this year: “Cost Reduction and Continuous Improvement by using IT Tools”.

The International MEMS/MST Forum will focus on “New Dynamics in the MEMS Industry”. The forum is an exceptional platform for exhibitors and visitors to explore the MEMS industry supply chain.

The 450mm Session is covering the latest state of introducing, planning and R&D for 450mm. The session includes all major initiatives as well as the progress which was made during the last years.
The Advanced Packaging Conference will present “Packaging Solutions for the New Technologies”. The conference will give the opportunity to learn more about most important microelectronics applications developments which enable novel, advanced packaging solutions to be the key drivers in system integration of electronic devices. The 14th European Manufacturing Test Conference (EMTC) is presenting “Overcoming New Test Challenges through Cooperation and Innovation”. The Conference will present an interesting mix of topics in the broad area of testing semiconductor devices.

SEMICON Europa remains the largest industry event in Europe focusing on technologies and solutions for advanced microelectronics manufacturing including semiconductors, MEMS, printed and plastic electronics, power electronics, and other emerging and related electronics markets. “SEMICON Europa is the heart and soul of the microelectronics industry in Europe,” says Heinz Kundert, president of SEMI Europe. “It is the place where the entire industry gathers – suppliers, technologists, executives, and purchasing agents – to learn, network, and understand the developments of technology and trends that shape and drive microelectronics innovation.”

Plastic Electronics offers new opportunities
After many years of research and development efforts around the global, plastic electronics is reaching the momentum of commercialization in areas such as for displays, lighting, photovoltaics and integrated smart systems. The Plastic Electronics 2012 Conference and Exhibitions in Dresden will be focused on challenges and opportunities for manufacturing these applications and products for the mass consumer markets. It is the single and sole event to focus on issues related to manufacturing of these challenging new applications and products and will bring together the stakeholders for this new emerging industry in a single setting. The conference will present a line-up of over 90 expert views for top-level professionals in the field, whereas the exhibition will be the market place to meet about 100 materials suppliers, tooling vendors and integrators of PE systems and solutions.

The Plenary Session, a comprehensive three-day event, covers issues and topics focused on technologies and markets. The keynote-speakers are:

Barry Young, Managing Director, OLED Association is presenting the “Market Forecast”. He addresses issues as the development of industry standards for OLED display and lighting, promotion of the technology and the resolution of industry-wide technical issues.

Thibaud Le Seguillon, CEO of Heliatek will speak about: “Future Applications: Roll-to-roll Vacuum Deposition of Small Molecules – The Right Choice”. Heliatek GmbH, a global leader in high-end solar PV technology, is about to start production of its worldwide unique organic solar films. The solar films will be produced in a low temperature roll-to-roll process in which small molecules (oligomers) are vacuum deposited onto inexpensive plastic substrate. The presentation will inform about the progress on ramping up Heliatek’s vacuum based roll-to-roll production and the production process in general.

Luisa Torsi, Professor, Università degli Studi di Bari “Aldo Moro”. She focuses on “Technology: Ultra Sensitive Label Free Bio-electronic OFET Sensors”. She is the 2010 E. H. Merck prize winner for Analytical Science, being the first women to be awarded with this prize. Her main research interests are in the fields of functional materials/nanostructures and electronic

Integrated Smart Systems is the new buzzword for a innovative class of applications and products which are expected to arise. Manufacturing, processing and tooling issues will be at the focus of attention of the event and in line with applications and products entering the end-user markets. Attending the event will be challenging and rewarding to anyone exploring the opportunities of this emerging and promising technology!

devices for chemical and biological sensing. Ho Kyoon Chung, Chair Professor and Director, Samsung SMD OLED Center, Sungkyunkwan University will do the motivational speech on the third day. His topic: "Challenges of AMOLED TV and Plastic AMOLED". AMOLED technology has been successfully commercialized for the high resolution mobile displays and is now poised to enter the new markets such as large size TV's and plastic AMOLED. However, there are still many challenges for commercialization, which is related to the cost of manufacturing. This talk will discuss these challenges and propose innovative ideas to overcome the cost issues.

The Plastic Electronics Conference and Exhibition will consider all major aspects of the industry. It is the best forum to meet with other professionals with the same interests, both from research and industry.

SEMICON Europa has ever been a marketplace for visionaries for many years. Organic and plastic electronics are an entirely new area of technology. "This combination fits very well", says Ed van den Kieboom, Chairman of the Plastic Electronics Special Interest Group. "The two events offer visitors as well as exhibitors great synergies and opportunities. No other event combines the two disciplines under one roof like the SEMICON Europa in Dresden, Germany. Topics like 'Smart System Integrations' touch both traditional semiconductors and new technologies emerging from plastic electronics."

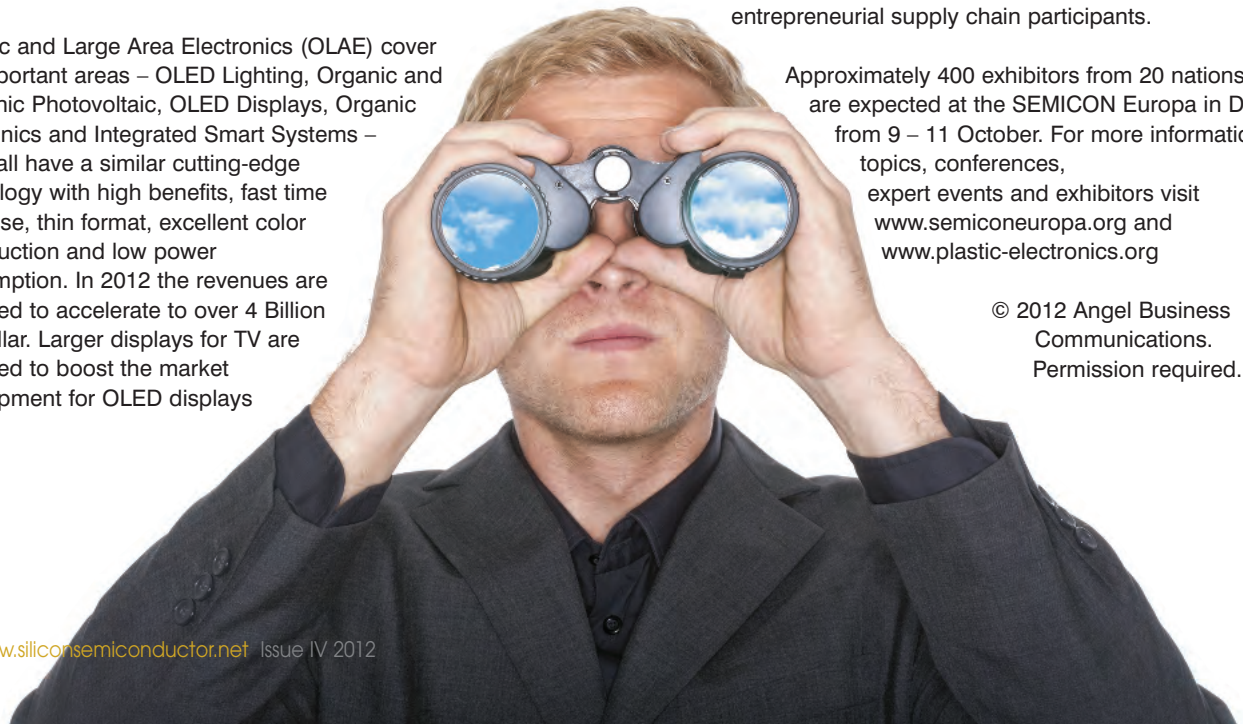
Organic and Large Area Electronics (OLAE) cover five important areas – OLED Lighting, Organic and Inorganic Photovoltaic, OLED Displays, Organic Electronics and Integrated Smart Systems – which all have a similar cutting-edge technology with high benefits, fast time response, thin format, excellent color reproduction and low power consumption. In 2012 the revenues are expected to accelerate to over 4 Billion US-Dollar. Larger displays for TV are expected to boost the market development for OLED displays and are expected to reach worldwide revenues of over 20 Billion US-Dollar in 2015.

The world market for flexible and organic PV is currently estimated at about 2.6 Billion US-Dollar. According to the market research company Nanomarkets, the market for thin film and organic photovoltaics will grow worldwide up to 7.5 Billion US-Dollar in 2015. It is generally expected that roll-to-roll manufacturing of flexible PV, partly done by soluble printing will become economically feasible for grid-linked application once efficiencies of 10% at cell level will be passed.

Integrated Smart Systems is the new buzzword for a innovative class of applications and products which are expected to arise. Manufacturing, processing and tooling issues will be at the focus of attention of the event and in line with applications and products entering the end-user markets. Attending the event will be challenging and rewarding to anyone exploring the opportunities of this emerging and promising technology!

SEMICON Europa and Plastic Electronics Exhibition and Conference offer a unique proposition for visitors and exhibitors. The two segments have much in common, sharing basic technologies, equipment, materials, and services. For existing members and customers, many topics touch on both traditional semiconductors and new technologies emerging from plastic electronics. Synergistic opportunities exist for enterprising and entrepreneurial supply chain participants.

Approximately 400 exhibitors from 20 nations are expected at the SEMICON Europa in Dresden from 9 – 11 October. For more information on topics, conferences, expert events and exhibitors visit www.semiconeuropa.org and www.plastic-electronics.org



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Future Trends in PCB Production

What key trends will shape the future of PCB production? John Cunningham, Chief Chemist, Rainbow Technology Systems Ltd has identified some key drivers that are universal to the electronic sector and looks to answer this broad, yet complex question.

When Rainbow Technology embarked on a journey six years ago to develop a new method of PCB production, the following factors were taken into account:

- All manufacturers want to cut costs without compromising quality.
- All manufacturers want to improve yields and reduce wastage and reject rates.
- There is an overriding pressure to make processes greener. This not only means the use of more environmentally friendly materials but also making every effort possible to reduce energy consumption in the manufacturing process.
- Features are becoming increasingly smaller therefore there is a greater demand for fine line circuitry than ever before.

The result was the Rainbow Processing Unit – an automated PCB production unit incorporating coating, imaging and developing in one compact enclosure.

Traditional PCB production

The process for producing PCBs has changed little in the past 50 years. There have been incremental improvements in quality and efficiency but nothing revolutionary. At present PCB manufacturing equipment requires a substantial capital investment as it must be housed in a clean room environment and the machinery takes up considerable amounts of space. The process starts with either laminating the copper boards with dry film protected with Mylar™ or roller coating with a solvent-based coating which is then passed through a hot air or infrared oven to remove the solvent and leave a dry film. Due to long drying times, often in a horizontal position, debris can get on to the panel which can lead to occlusions later in the imaging process These dry film or coated panels are then transported under yellow light to the imaging unit.

Imaging is carried out with an off-contact process using collimated light, which at present can only achieve imagining down to 50 microns.
The imaged panel is then transported (again in yellow light) to the developing station where the 20-25 microns of film or coating spend 1-2 minutes being developed before storage or forwarding to

the etching line. When it comes to fine line detail (under 50 microns) the most common methods employed are Laser Direct Imaging (LDI) or units incorporating a Digital Mirror Device (DMD). Both of these methods use imaging units which require the copper panels to be coated with a dry film laminate or a wet solvent-based photoimageable resist.

Both methods require considerable space for the laminating or coating lines and consume a lot of power as there require drying ovens (from 20kW to 70kW), laminators (averaging 20kW) and collimated UV light sources for the imaging process (averaging 20kW).

Resist

The first area Rainbow looked at was the type of resist commonly used. Traditionally dry film is used however it has a number of drawbacks. To obtain fine detail the dry film is very thin in the order of 12-15 microns, it is difficult to handle does not conform easily to the surface of the copper and has a tendency to delaminate particularly when printing fine detail. It is also applied laminated with heated rollers prior to imaging which can lead to stress forces building with in the copper panel.

We therefore looked to develop a special wet resist which could be applied wet to the panel surface and squeezed into all the contours of the copper substrate thereby greatly improving surface conformity and subsequent adhesion. As the coating is 100% solids and solvent free it does not need to be pre-dried. The resist is cured using UV LED light and any unexposed resist is simply washed off as it remains in its liquid state.

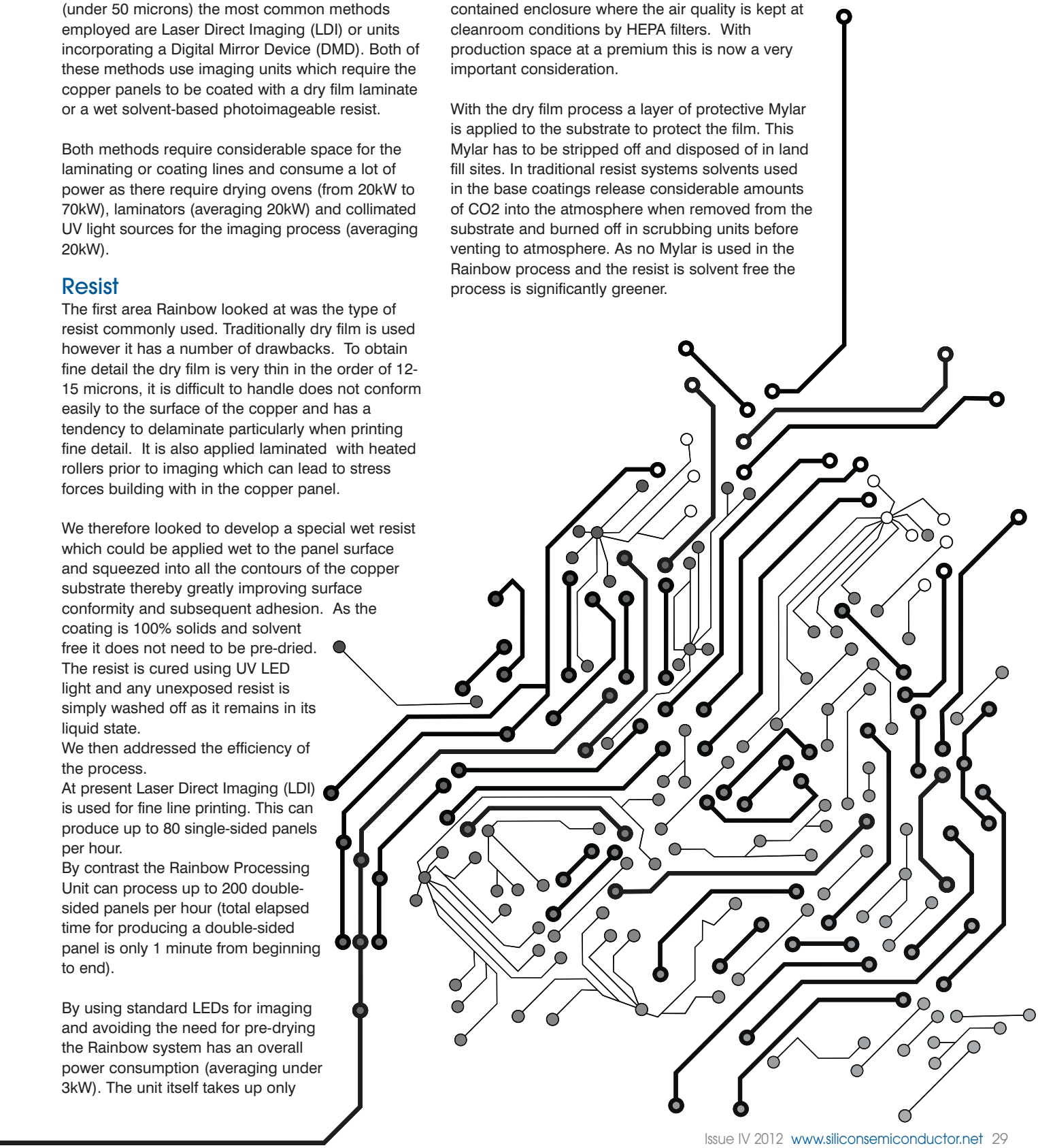
We then addressed the efficiency of the process.

At present Laser Direct Imaging (LDI) is used for fine line printing. This can produce up to 80 single-sided panels per hour.

By contrast the Rainbow Processing Unit can process up to 200 double-sided panels per hour (total elapsed time for producing a double-sided panel is only 1 minute from beginning to end).

By using standard LEDs for imaging and avoiding the need for pre-drying the Rainbow system has an overall power consumption (averaging under 3kW). The unit itself takes up only 12sq m of floor space and is in its own self-contained enclosure where the air quality is kept at cleanroom conditions by HEPA filters. With production space at a premium this is now a very important consideration.

With the dry film process a layer of protective Mylar is applied to the substrate to protect the film. This Mylar has to be stripped off and disposed of in land fill sites. In traditional resist systems solvents used in the base coatings release considerable amounts of CO_2 into the atmosphere when removed from the substrate and burned off in scrubbing units before venting to atmosphere. As no Mylar is used in the Rainbow process and the resist is solvent free the process is significantly greener.



Traditional methods of PCB are changing in line with manufacturers demands for greater efficiency, finer line circuitry and a greener approach to production. Companies such as Rainbow Technology Systems are developing new processes to meet these demands and produce the next generation of PCB imaging equipment

Maximum yields

All manufacturers are striving for maximum yields and minimum waste. The Rainbow System has been designed using optics which has a collimation of only six degree half angle. As there is only a nine-second gap between the coating and imaging stages and the panel in a vertical orientation this offers less opportunity for debris to attach itself to the wet resist.

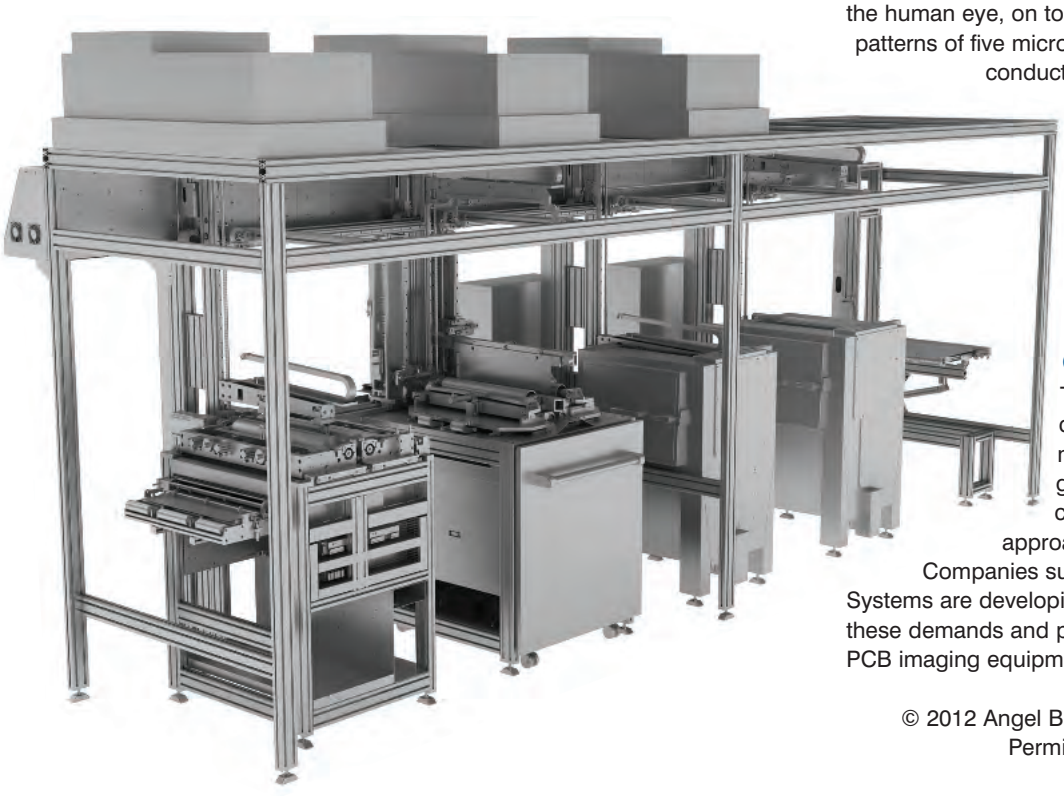
Particles which trapped in the cured resist will be transported on with the panel or if present in the wet resist will either slide off the protective layer on the phototool or again move forward with the panel and be removed in the developer and so repeat errors are unusual.

Given this and the fact that the whole process is almost entirely automated it should lead to higher yields. As the panels come out ready for etching there is no need to transport or store them in yellow light (to prevent premature curing from UV light in the atmosphere). One of our aims in developing the system is to give a new lease of life to standard photo tools without the costly maintenance connected with LDI. Very little heat is generated by the process so the issue of heat distortion of the photo tool is avoided.

Standard silver halide photo tools are used and a special three-micron coating is applied using Rainbow's Panda Coater to protect the tool from moisture and chemical attack from the resist. Photo tools take under two minutes to changeover using a self-locating cart system

Touchscreen production

Although we designed the Rainbow Process primarily for PCB production there has been interest in applying the technology in other areas most notably touchscreen displays. The process can be used to print very fine conductive tracks, invisible to the human eye, on to a clear substrate. Grid patterns of five microns by 300-pitch offer more conductivity than ITO or conductive polymers and offering much closer track and gap configurations (down to 10 micron spacing) designers will have more scope to incorporate additional features and functionality into the touch screen.



Conclusion

Traditional methods of PCB are changing in line with manufacturers demands for greater efficiency, finer line circuitry and a greener approach to production. Companies such as Rainbow Technology Systems are developing new processes to meet these demands and produce the next generation of PCB imaging equipment.

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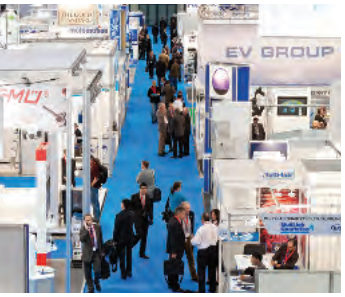

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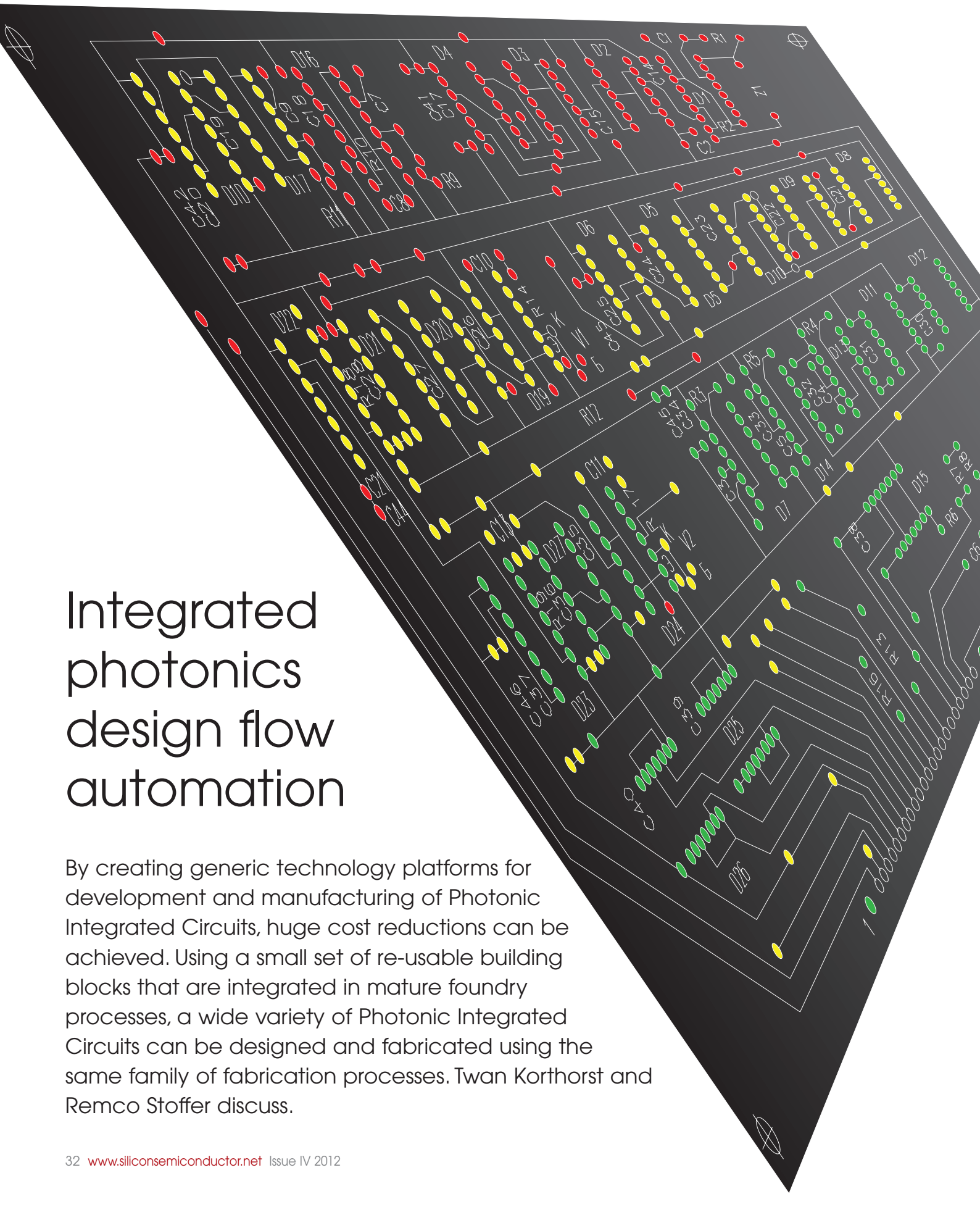

Integrated photonics design flow automation

By creating generic technology platforms for development and manufacturing of Photonic Integrated Circuits, huge cost reductions can be achieved. Using a small set of re-usable building blocks that are integrated in mature foundry processes, a wide variety of Photonic Integrated Circuits can be designed and fabricated using the same family of fabrication processes. Twan Korthorst and Remco Stoffer discuss.

Stable fabrication and integration technologies decrease the cost price and development time of photonic integrated components without sustaining a loss on the performance of the photonic component. Instead of optimising the fabrication technology for every single application, the product design is adapted to the capabilities of available, mature, high performance fabrication processes. To create stable processes right tools are needed, such as software for layout, simulation and fabrication execution and methods such as in-line and off-line quality testing. Next step is to collect the information from the fabrication processes and translate this into standard building blocks for the photonic integrated circuit, given a particular fabrication process flow.

Integrated Product Creation Process

Underpinning the whole "generic manufacturing" concept is the information flow between different abstraction levels and the different stages of product and process development. When system engineers, design engineers and process engineers work together to design both the product and, when required, fabrication processes, it is known as the integrated product creation process (iPCP figure 1). The designer's consideration of design for manufacturability, cost, reliability and maintainability is the starting point for an integrated product development.

The iPCP concept has been implemented by developing dedicated Design Kits for various fabrication technologies, amongst others silicon photonics. PhoeniX Design Kits contain all relevant information for designers in order to create a photonic integrated device or circuit within the capabilities of the fabrication processes. Users benefit from this by having immediate access to mature and proven building blocks, ensuring functional devices. Furthermore, recurring costs are avoided by streamlining the discussions amongst designers and engineers at the foundry. The knowledge of the product creation process will be utilised into the Design Kits through standard design software, which assists to avoid that designers repeatedly build libraries for same technologies. The main content of these Design Kits are the building blocks containing geometrical information, parameters, boundaries, design rules, IP-rights, simulation settings, mask information, version, etc. By reusing validated definitions for multiple applications and designs, the quality of the information used by the designers increases considerably.

Photonics Design Automation

In the electronics industry, the use of 'Electronics Design Automation' (EDA) is wide-spread. A foundry offers an extensive set of building blocks (BBs), which a designer can use to create a complex device. The BBs and their combination are guaranteed to work as expected if the given design rules are respected. Software supports each step in the design process, from physical analysis to layout, and flags any design rule violation before the final design is shipped to the foundry. Furthermore, simulation tools are integrated in, or link directly into, the EDA environment and assist the designer in his work.

In the field of integrated photonics, such advanced design kits have not been available until recently. A number of European companies and institutions has worked together to set up a Photonics Design Automation (PDA) tool-set. Just like in EDA, photonic foundries define a number of building blocks, which are implemented in software tools ranging from mask layout through physical and circuit simulators. The circuit simulator is able to call

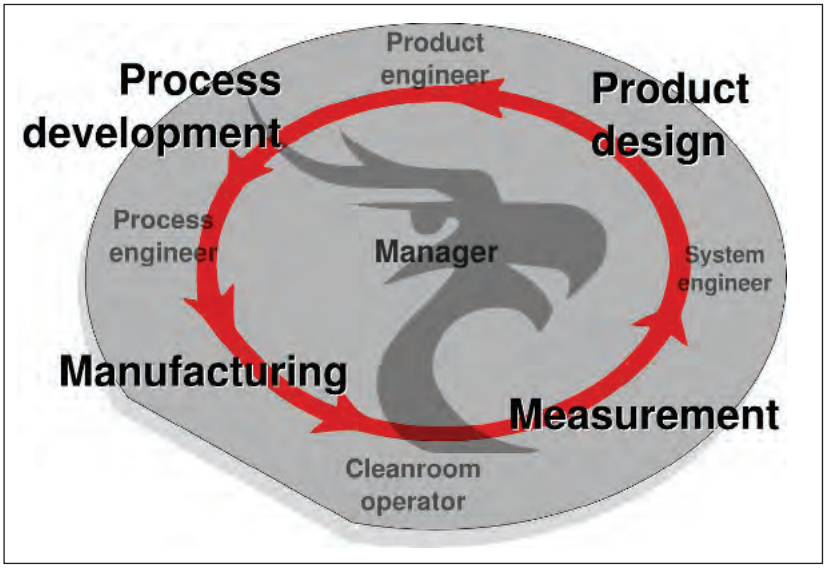

Figure 1: Integrated Product Creation Process

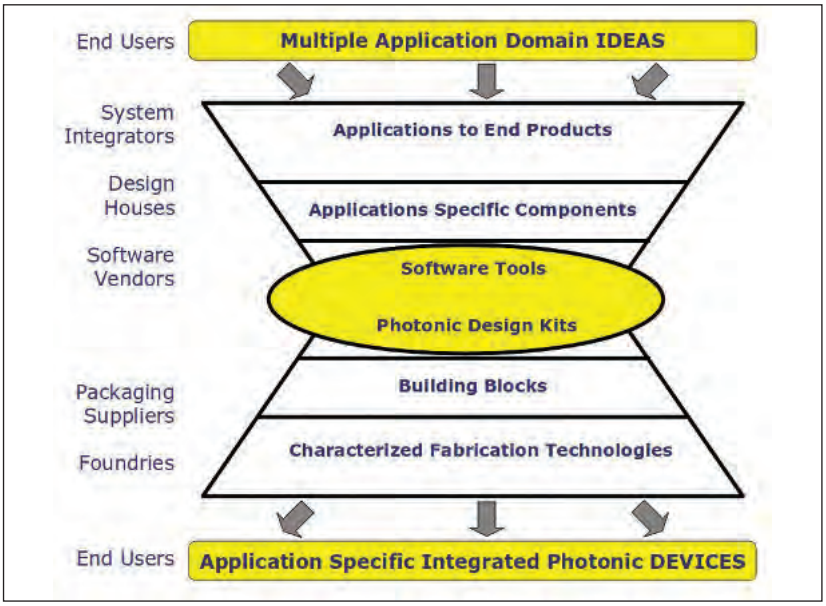

Figure 2: Photonics Design Automation as central pivot point in the supply chain

the physical simulation software, or query a building block directly, in order to quickly simulate the response of a device. Furthermore, it can call the mask layout software to export the circuit design into a physical mask layout.

Since building blocks of one foundry can be similar to those of other foundries, many designs will be transferable from one foundry to another with only minor changes to the layout (due to differences in BB sizes and port locations), however with significant changes to the mask layers (due to differences in technologies and process flows).

Design flow

A designer of a PIC (Photonic Integrated Circuit), who wants to have his design realized by a foundry, typically starts his design by modelling it in a circuit simulator [1]. In the circuit simulator, one designs an optical circuit by placing building blocks from the foundry library with their properties into the circuit layout. The designer does not focus on how exactly a building block is implemented; the foundry rather specifies the input / output ports and, possibly in conjunction with physical layer simulators [2, 3], the wavelength dependent scattering matrix (S-matrix) of the block. By clicking together a circuit and specifying its input and outputs, the designer can very quickly calculate the spectral response of the complete device. He can then optimize it for better functionality or for better robustness with respect to fabrication technology tolerances.

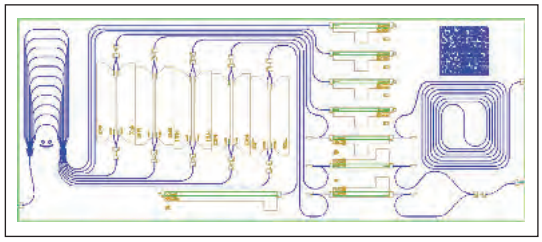

Figure 3: Mask design with bounding boxes for IP licensed building blocks

Once a satisfactory design has been created in the circuit design tool, it can be transferred, via the PDA framework, to the mask layout software [4]. The user specifies a chip type available in the foundry and (if packaging options are available) a package. Such a combination of chip type and package defines the locations of the optical and electrical input and output ports.

In the mask layout software the designer can adjust the exact layout of his design to optimize for space constraints and to make sure all connections (both optical and RF or DC electrical connections) are correct.

In the layout environment, the designer might only be allowed to see the outline of the foundry-defined building blocks. A foundry can protect its IP by just exposing a bounding box and the locations and dimensions of access waveguides and connections for electrical signals, as shown by the private building blocks in Figure 3.

When the designer is satisfied with his mask layout, he exports it to a mask file. This process involves automatic post processing on the mask layers that are defined by the foundry; for example, a waveguide on the final mask might have to be a little wider than designed to correct for under etch, or a final mask layer might have to be a local inversion of the designed waveguide.

During this foundry specific automatic mask export process, the software performs design rule checks (DRC) on both the logical and mask layer levels. An example of a logical check is the radius of curvature of a waveguide, while an example of a mask layer check is whether a metallization layer and a waveguide layer overlap – or are closer than a given distance to each other.

Since the designer has no knowledge of the inner workings of a private building block, the mask files that are produced will be incomplete as the IP-protected building blocks are left open. The export process also generates a list of the used building blocks and their exact locations in the layout.

When the foundry receives designs created with the developed design environment, for example for a Multi Project Wafer run, it assembles all the mask files from the users into one reticle or mask set.

Furthermore, it uses the building block information supplied by the users to fill in the private building blocks in all designs with its own proprietary mask

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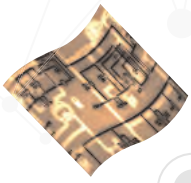

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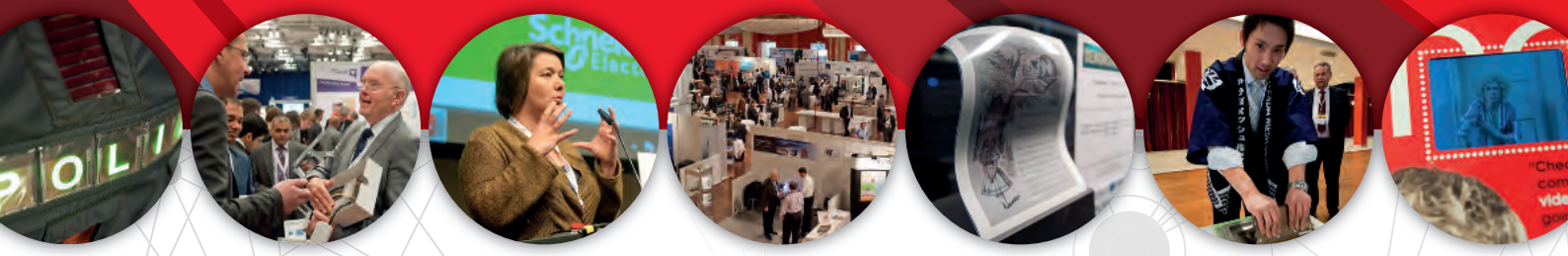

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data. After this final mask assembly, the reticles or masks can be created.

Multi Project Wafer runs

By sharing the costs for the fabrication, the reticles or masks and the set-up and use of the design environment in Multi Project Wafer (MPW) runs, the access barrier to photonic integration technology can be brought down.

The amount of offered MPW runs has increased considerably over the last period of time and these results in a steep increase in the amount of research and development activities in the field of integrated photonics. Moreover, the increase of the number of fabricated wafers with a same process flow creates more stable manufacturing processes to further drive down the costs by an increased yield.

The design flow as described in this paper has been applied successfully within a number of MPW runs [5, 6, 7]. During the past six months, runs in Indium Phosphide [9, 10, 11], TriPleX [7] and silicon photonics [12, 13] have been executed on the developed design platform and more than 50 different designs have been successfully implemented for six different foundries and two packaging providers [14, 15].

Future outlook

A set of re-usable building blocks that is available in stable and mature (commercial) foundry processes leads to huge cost reductions. This opens up the application of photonics integration technologies to a much larger public. Instead of optimizing the fabrication technology for every specific application, the product design will be adapted to the capabilities of available, mature, high performance fabrication processes. The presented PDA environment plays a central role (see Figure 1) in the whole product and value chain from concept application to material, through design to manufacturing.

Further, this developed framework can be used by both companies and institutes to promote internal collaboration and information exchange between designers and with process engineers. The developed PDA framework is open to other parties creating their own plug-ins and building blocks. For example, two different Arrayed Waveguide Grating plug-ins, for designing wavelength filters, have been created by third parties [11, 16] and are actively used in the mentioned MPW runs designs.

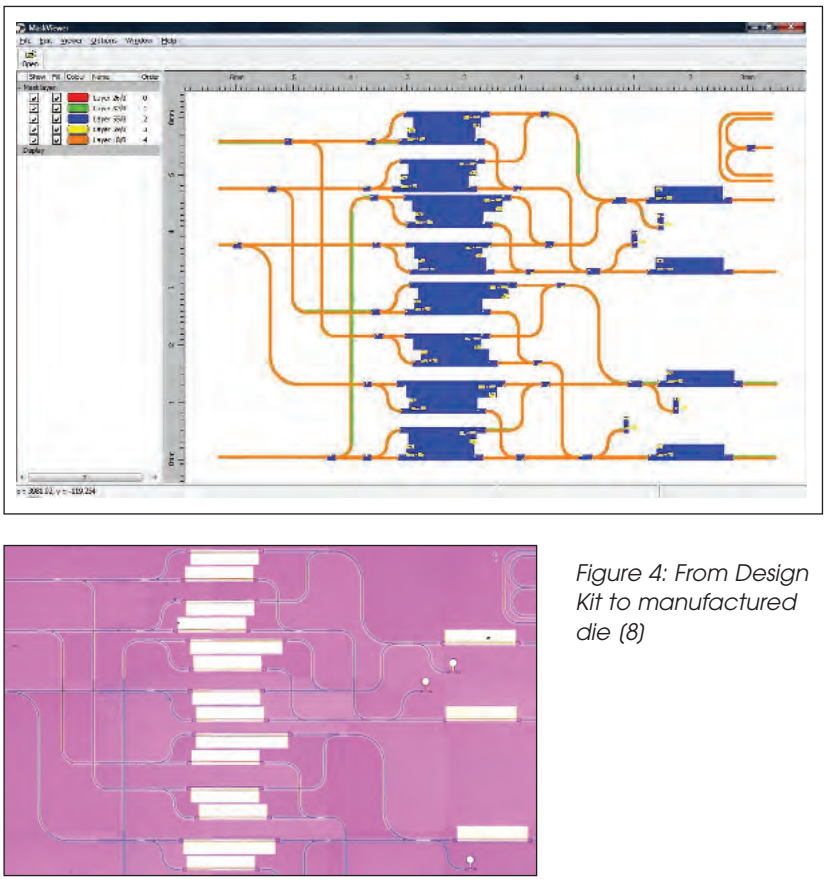

Figure 4: From Design Kit to manufactured die (8)

References

(1) *Aspic: photonic circuit design and simulation tool*
(2) *FieldDesigner: advanced modesolver, including T/O, E/O, 3D Ring Resonator and Active Material modules*
(3) *OptoDesigner: propagation simulator, includes BPM, FDTD, BEP/EME, Zone and FAST technology*
(4) *MaskEngineer: object oriented and parametric layout solution*
(5) *InP MPW brokering organisation: JePPIX - http://www.jeppix.eu*
(6) *SOI MPW brokering organisation: ePIXfab - http://www.epixfab.eu*
(7) *TriPleX foundry partner: LioniX (Netherlands) - http://www.lionixbv.com*
(8) *European project EuroPIC - http://europic.jeppix.eu*
(9) *InP foundry partner: Oclaro (UK) - http://www.oclaro.com*
(10) *InP foundry partner: FhG-HHI (Germany) - www.hhi.fraunhofer.de*
(11) *InP foundry partner: Technical University Eindhoven (Netherlands) - http://w3/ele.tue.nl/oed*
(12) *Silicon photonics foundry partner: CEA-Leti (France) - www.leti.fr*
(13) *Silicon photonics foundry partner: IMEC (Belgium) - www.imec.be*
(14) *Packaging partner: CIP (UK) - http://www.ciphotonics.com*
(15) *Packaging partner: Linkra (Italy) - http://www.linkra.it*
(16) *Design house: Bright Photonics (Netherlands) - www.brightphotonics.eu*

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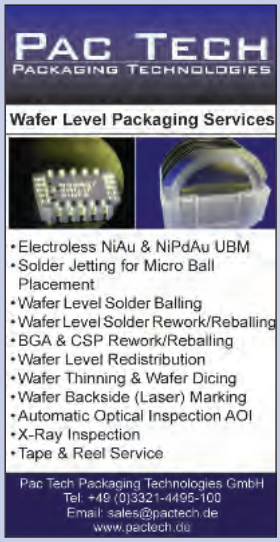

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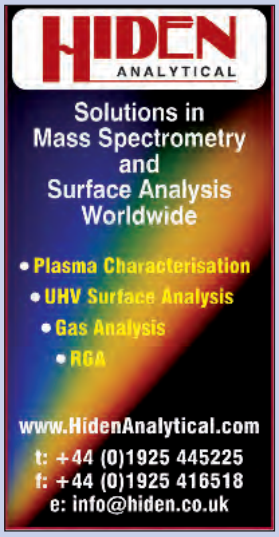

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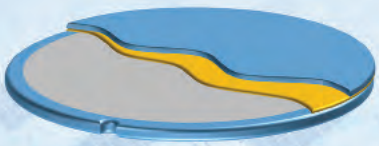

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