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Spray coating fundamentals

Unlocking the potential of diamond

Rewriting the book on cleanroom installation

Defect inspection challenges and solutions for ultra-thin SOI

Black silicon solar cell efficiency

Enhancing silicon-based batteries

Overcoming Moore's Law with carbon nanotubes

Resist processing modules in the latest generation EVG150 high-volume coater / developer

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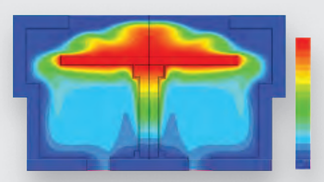

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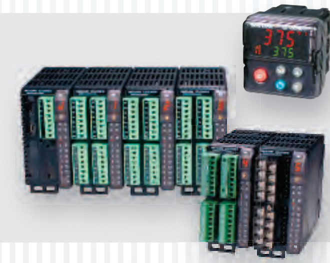

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More than Moore technologies will be essential for 450-mm wafers

AS THE SEMICONDUCTOR INDUSTRY moves ever closer to the 450-mm wafer transition, much has been made about how the cost and readiness of scaling to smaller nodes is inextricably linked to the next wafer size transition. Yet increasingly, the key differentiators for many of today's consumer electronic products – in particular, mobile products such as smart phones and tablets – are coming from "More Than Moore" enabled devices. Examples include MEMS-based motion sensors, image sensors with backside illumination and wafer-level manufactured optics, smaller form factor frequency filters, power devices and higher-quality microphones.

In most cases, these devices have several process steps in common – such as permanent wafer bonding, temporary bonding and debonding, double-sided lithography, deep silicon etching and related through-silicon metallization processes – that would not exist in a pure CMOS scaling environment. This is because for decades CMOS scaling has been driven by shrinks through improved front-end lithography, and based on that history more severe architectural changes were simply not required.

On the other hand, these process steps are key enablers for next-generation device architectures like 3D ICs and wafer-level packaging. This is important to note since the continuation of Moore's Law by conventional CMOS scaling (device shrinks through advanced lithography) is becoming more and more challenging and requires monumental capital investments, already on the order of billions of euros. However, 3D IC with through silicon via (TSV) interconnects provides a complementary path to Moore's Law – enabling an increasing amount of functionality and capability to be integrated into a device or package through vertical stacking, which minimizes footprint. Recent announcements from leading image sensor and memory manufacturers show that 3D ICs are finally moving into high-volume manufacturing, thereby making "More Than Moore" a reality.

How could these innovative process steps be adopted within a few years in a fully automated 300-mm fab environment?

At EV Group, pioneering such technologies for initially small market segments, like MEMS and compound semiconductors, has essentially helped enable More Than Moore process development to be carried out for more than 20 years. As a result, the manufacturing lessons learned from that experience have successfully scaled to today's 300-mm manufacturing. The examples of backside illuminated CMOS image sensors and 3D integrated FPGAs show 3D implementation in 300-mm volume fabs. Other applications, such as DRAM and logic are currently in pilot-line volume and well on their way to volume production.

Once these applications are established in 300-mm mainstream semiconductor manufacturing, adoption at 450 mm is no longer a "Moore's Law" or "More than Moore" question. It is expected that the economics of moving to larger wafers and the smaller device footprints associated with 3D-IC architectures will render wafer-level processing an even more favourable approach compared to single die processing. Naturally, wafer stacking technologies and "wafer-level back end" processing will play a significantly larger role as well. Today, IDMs and foundries focus on 450 mm and next-generation front-end lithography while others focus on developing 3D IC. At 450 mm, the industry will come together. In short, 3D-IC processes have arrived and are here to stay.

Paul Lindner
Executive Technology Director
EV Group

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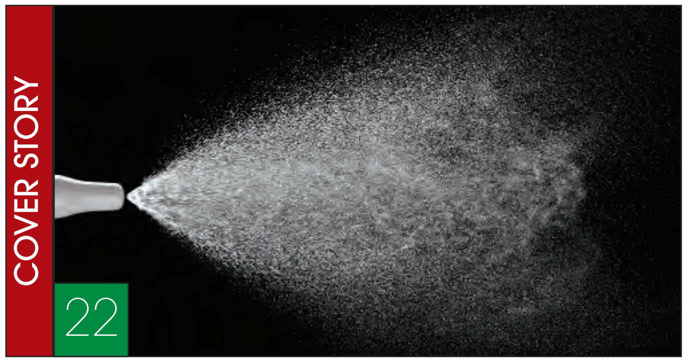
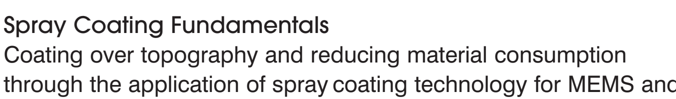
industry & technology





Spray Coating Fundamentals
Coating over topography and reducing material consumption through the application of spray coating technology for MEMS and 3DICs.

Unlocking the potential of diamond
Diamond is a very successful material, a source of power and an object of beauty. For semiconductor devices, thermal issues are a primary consideration, while for MEMS devices, the chemical and physical properties of diamond have enabled new devices to yield hitherto unseen performance levels, which silicon cannot deliver.

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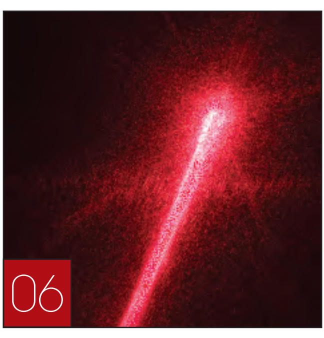

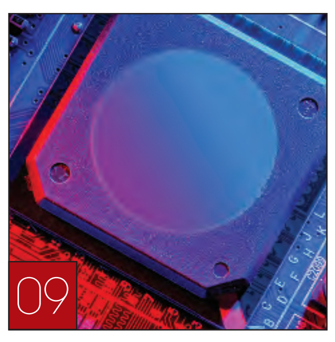

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Cover art designed by Mitch Gaynor

Rewriting the book on cleanroom insulation
Cleanrooms in pharmaceutical and semiconductor industries are adopting a new “slimmer” insulation that can reduce cleanroom size requirements and eliminate downtime costs.

Defect inspection challenges and solutions for ultra-thin SOI
What are the challenges for ultra-thin SOI inspection using a laser light scattering system? Using an unpatterned DUV inspector, KLA-Tencor Corp consider the impact of reflectivity on haze and minimum threshold, the required sensitivity for 28nm and beyond SOI inspection.

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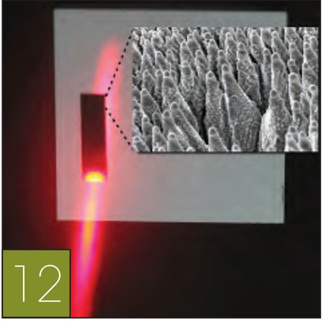
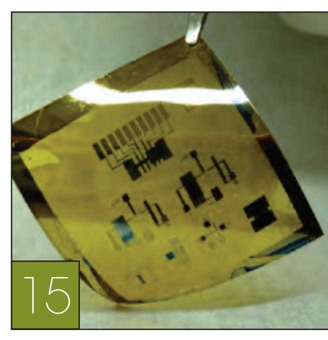
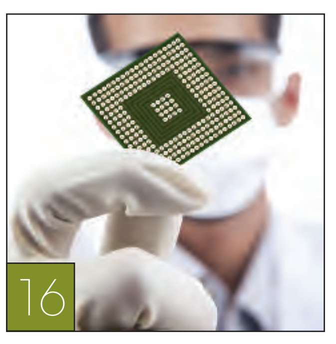






Semiconductor market to pick up 9 percent In 2013

SEPTEMBER WSTS data shows the 3Q 2012 semiconductor market increased 1.8 percent from 2Q 2012. According to market research firm, Semiconductor Intelligence, the year 2012 semiconductor market will certainly show a decline. The fourth quarter of 2012 would need to grow 11 percent to result in positive growth for 2012.

The outlook for key semiconductor companies points to a 4Q 2012 roughly flat with 3Q 2012.

Guidance for 4Q 2012 varies widely, from double digit declines for TI and Infineon to a 20 percent increase for Qualcomm. Most companies expect a flat to down 4Q 2012. The companies generally expect weak end market demand in 4Q, with the possible exception of mobile communications. Semiconductor Intelligence is forecasting the 4Q 2012 semiconductor market will be up 0.5 percent from 3Q 2012, driving a 2.5 percent decline for year 2012.

So what's the outlook for 2013?

The overall economic outlook is uncertain. The latest forecast from the International Monetary Fund (IMF) calls for worldwide GDP growth of 3.6 percent in 2013, a slight improvement from 3.3 percent in 2012. The advanced economies are expected to grow 1.5 percent in 2013, up from 1.3 percent in 2012.

The IMF expects the Euro Zone to begin a slow recovery from the downturn caused by the debt crisis. Emerging and developing economies will be the major growth drivers with 5.6 percent growth in 2013.

China GDP growth should increase slightly in 2013 after slowing in 2011 and 2012. Semiconductor Intelligence has developed a forecast model based on GDP. Since semiconductors are at the low end of the electronics food chain, the market tends to follow the acceleration or deceleration of GDP growth rather than the rate of GDP growth. The 0.3 percentage point acceleration in GDP growth from 2012 to 2013 indicates 2013 semiconductor market growth of around 8 percent to 10 percent.

The electronics market outlook is mixed. Business and consumer spending on PCs is weak. However smartphones and media tablets are continuing to show healthy growth. Inventory adjustments are being made in the semiconductor supply chain.

The semiconductor market should turn up quickly when end demand picks up. Based on these factors, Semiconductor Intelligence is forecasting 9 percent growth in the semiconductor market in 2013.

Imec revolutionises KLA-Tencor's Lithography e-beam tool

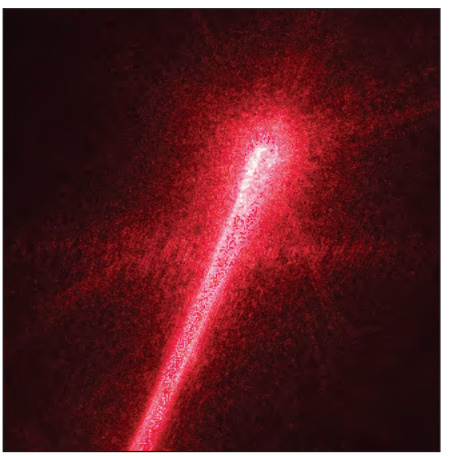
IMEC has designed and fabricated an electrostatic micro-lens (lenslet) array for KLA-Tencor's anticipated Reflective Electron Beam Lithography (REBL) tool.

The REBL technology potentially enables a high throughput e-beam writing process for maskless lithography. The lenslet array is a key component for the parallelisation of the e-beam writing process.

Functionality of the lenslet chip was demonstrated in KLA-Tencor's REBL e-beam column. The lenslet consists of a densely packed array of 4μm deep cylindrical holes with a 1.4μm diameter and top spacing of only 200nm. The electron beam entering the lenslet holes is focused through a set of 4 ring electrodes.

The ring electrodes can be tuned to focus the electron beams by applying static voltages up to 50V on the ring electrodes. The bottom of each hole consists of a small metal plate that can be switched by a CMOS circuitry below, either reflecting or absorbing the incoming electrons.

In this way, the incoming electron beam is split into 1 million smaller beamlets, a strategy designed to enable higher throughput for the e-beam writing process through parallelisation.



And through its alliances, imec can also offer a path to transfer the technology to a foundry for volume production.

The CMORE toolbox contains a wide variety of device technologies on 200mm such as CMOS, Si-photonics, MEMS, specialty image sensors and packaging.

ASML notifies of synthetic buyback

NETHERLANDS headquartered lithography tool manufacturer, ASML Holding NV has confirmed that none of its creditors has opposed the capital repayment which forms part of the Customer Co-Investment Program announced on 9th July 2012.

ASML will proceed with the cash capital repayment of €9.18 per ordinary share and the consolidation of outstanding ordinary shares (the reverse stock split) in a ratio of 77 shares for every 100 shares. The firm also confirms that the ex-entitlement date will be 26th November 2012, the record date will be 28th November 2012 and the cash capital repayment will be made on 3rd December 2012. Holders of New York shares will receive the cash capital repayment in U.S. dollars at an exchange rate that will be determined on 27th November 2012. Shares issued to the three Stichtingen for participating customers under the Customer Co-investment Program will not participate in this Synthetic Buyback.

Gartner: smartphone sales increased 47 percent in Q3 2012

WORLDWIDE sales of mobile phones to end users reached almost 428 million units in the third quarter of 2012, a 3.1 percent decline from the third quarter of 2011, according to Gartner, Inc.

Smartphone sales accounted for 39.6 percent of total mobile phone sales, as smartphone sales increased 46.9 percent from the third quarter of 2011.
While the mobile phone market declined year-on-year, Gartner analysts said there were positive signs for the industry during the third quarter.

"After two consecutive quarter of decline in mobile phone sales, demand has improved in both mature and emerging markets as sales increased sequentially," said Anshul Gupta, principal research analyst at Gartner. "In China, sales of mobile phones grew driven by sales of smartphones, while demand of feature phones remained weak. In mature markets, we finally saw replacement sales pick up with the launch of new devices in the quarter."

Smartphones continued to fuel sales of mobile phones worldwide with sales rising to 169.2 million units in the third quarter of 2012. The smartphone market was dominated by Apple and Samsung. "Both vendors together controlled 46.5 percent of smartphone market leaving a handful of vendors fighting over a distant third spot," added Gupta.

Nokia slipped from No. 3 in the second quarter of 2012 to No. 7 in smartphone sales in the third quarter of 2012. RIM moved to the No. 3 spot with HTC not far behind, at No. 4. "Both HTC and RIM have seen their sales declining in past few quarters, and the challenges might prevent them from holding on to their current rankings in coming quarters," continued Gupta.

While seasonality in the fourth quarter of 2012 will help end-of-year mobile phone sales to end users, Gartner analysts said that there will be a lower-than-usual boost from the holiday season. Consumers are either cautious with their spending or finding new gadgets like tablets, as more attractive presents.

Samsung's mobile phones sales continued to accelerate, totalling almost 98 million units in the third quarter of 2012 (see Table 1 above), up 18.6 percent year-on-year. Samsung saw strong demand for Galaxy smartphones across different price points, and it further widened the gap with Apple in the smartphone market, selling 55 million smartphones in the third quarter of 2012. It commanded 32.5 percent of the global smartphone market in the third quarter of 2012.

Nokia's mobile phone sales declined 21.9 percent in the third quarter of 2012, but overall sales at 82.3 million were better than Gartner's early estimate, largely driven by increased sales of the Asha full touch range. Nokia had a particularly bad quarter with smartphone sales, and it tumbled to the No. 7 worldwide position with 7.2 million smartphones sold in the third quarter.

The arrival of the new Lumia devices on Windows 8 should help to halt the decline in share in the fourth quarter of 2012, although it won't be until 2013 to see a significant improvement in Nokia's position.

Apple's sales to end users totalled 23.6 million units in the third quarter of 2012, up 36.2 percent year-on-year. "We saw inventory built up into the channel as Apple prepared for the coming holiday season, global expansions and the launch into China in the fourth quarter of 2012," pointed out Gupta. With iPhone 5 launching in more territories in the fourth quarter of 2012, including China, and the upcoming holiday season Gartner analysts expect Apple will have its traditionally strongest quarter.

In the smartphone market, Android continued to increase its market share, up 19.9 percentage points in the third quarter of 2012. Although RIM lost market share, it climbed to the No. 3 position as Symbian is nearing the end of its lifecycle.

There was also channel destocking in preparation of new device launches for RIM, which resulted into 8.9 million sales to end users in the third quarter of 2012.

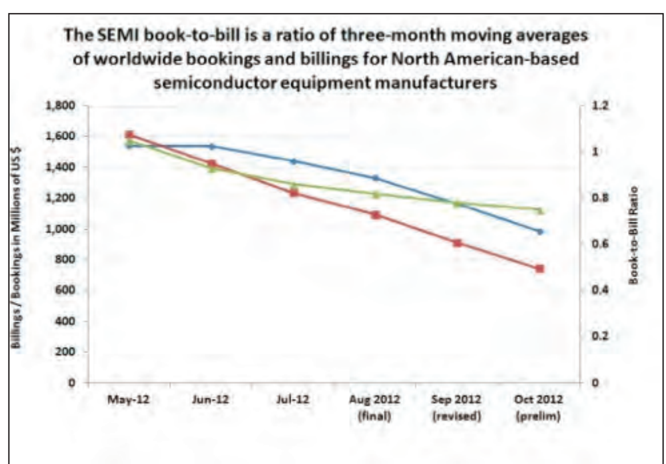
With the launch of iPhone 5, Gartner analysts expect iOS share will grow strongly in the fourth quarter of 2012 because users held on to their replacements in many markets ahead of the iPhone 5 wider roll out.

Windows Phone's share weakened quarter-on-quarter as the Windows Phone 8 launch dampened demand of Windows Phone 7 devices.

Network with leading industry professionals of the III-V chip making industry at the 3rd CS International conference in Germany 4th - 5th March 2013

North American semiconductor equipment industry waning

NORTH AMERICA-BASED manufacturers of semiconductor equipment posted $743.2 million in orders worldwide in October 2012 (three-month average basis) and a book-to-bill ratio of 0.75, according to the October Book-to-Bill Report published today by SEMI. A book-to-bill of 0.75 means that $75 worth of orders were received for every $100 of product billed for the month.



The three-month average of worldwide bookings in October 2012 was $743.2 million. The bookings figure is 18.6 percent lower than the revised September 2012 level of $912.8 million, and is 19.8 percent lower than the October 2011 order level of $926.8 million.

The three-month average of worldwide billings in October 2012 was $986.5 million. The billings figure is 15.3 percent lower than the revised September 2012 level of $1.16 billion, and is 21.6 percent less than the September 2011 billings level of $1.26 billion.

“Semiconductor industry investments remain muted as the industry enters the fourth quarter,” says Denny McGuirk, president and CEO of SEMI. ““Investments in leading-edge technologies will continue to drive spending in the near-term, while a clearer 2013 outlook will emerge over the next couple of months as capex plans are announced.”

AMAT revenues plunge 24 percent year on year

Applied Materials, Inc. a manufacturer of solutions for the semiconductor, display and solar industries, has reported results for its fourth quarter and fiscal year ended October 28th, 2012.

In the fourth quarter, Applied generated orders of $1.47 billion and net sales of $1.65 billion. The company recorded goodwill impairment and restructuring charges totalling $545 million and reported an operating loss of $499 million, with a net loss of $515 million or 42 cents per diluted share.

In FY2012, the company reported orders of $8.04 billion, net sales of $8.72 billion, operating income of $411 million, and net income of $109 million or 9 cents per diluted share. "In our fourth quarter, Applied delivered profit at the high end of our outlook despite challenging industry conditions in semiconductor, solar and display," said Mike Splinter, Chairman and CEO. "Our strong cash flow performance allowed us to increase our quarterly dividend and share buybacks, returning $1.85 billion to stockholders in the year."

"We see improving business conditions entering 2013, with orders projected to increase after bottoming in the fourth quarter," Splinter added. "Accelerated changes in device technology and the adoption of new materials in all of the industries we serve provide opportunities for Applied to build on our leadership and grow our market share."

Fourth quarter results included a $421 million goodwill impairment charge associated with the Energy and Environmental Solutions (EES) segment. The goodwill impairment reflects the deterioration in solar equipment market conditions, our customers' financial condition and reduced market valuations, causing Applied to reassess the recoverability of the segment's goodwill.

Applied also reported $124 million in charges related to previously announced restructuring plans and the integration of Varian.

TEL & imec expand STT-MRAM business collaboration

IMEC and Tokyo Electron (TEL), a supplier of semiconductor production equipment, have further extended their collaboration. This follows an announcement made regarding imec forming a new collaboration with CANON ANELVA to further develop STT-MRAM.

The new agreement comprises joint R&D on advanced STT-MRAM (spin-transfer torque magnetoresistive random access memory) within imec's research and development program on emerging memory technologies.

The collaboration between imec and TEL on STT-MRAM technology is an opportunity for TEL to accelerate the development of its next-generation etch tools for high-density emerging memory technologies.

As part of the collaboration, TEL's Tactras etch tool has been installed in imec's 300mm clean room, complementing imec's 300mm dedicated STT-MRAM tool set. The Tactras tool enables imec and TEL to jointly develop the patterning processes for high-density STT-MRAM technology. The tool is designed for in-situ cluster patterning of the Magnetic Tunnel Junction (MTJ) stack, which is key for advanced memory technology nodes.

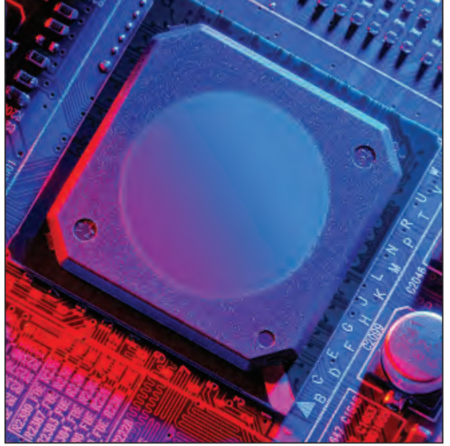
U.S. semiconductor industry boosts workforce

ACCORDING to the United States Department of Labor, Bureau of Labor Statistics, State and County Employment and Wages Database, total direct U.S. semiconductor employment is estimated at 244,800. This total comprises workers in all major occupations in the U.S. semiconductor industry.

It includes BLS's reported total for semiconductor employees in the U.S. manufacturing sector, plus an estimate for the number of semiconductor workers employed by semiconductor "fabless" firms, which BLS counts in the wholesale trade sector, not the manufacturing sector.

This is according to employment data, into the manufacturing sector of the North American Industry Classification System (NAICS) which it uses to categorise data by industries. This initiative is called the Factoryless Goods Producer (FGP) initiative and is scheduled for full implementation by the 2017 Economic Census.

Compared to all other electronic component industries in the United States, the U.S. semiconductor industry employs the greatest number of U.S. workers. According to BLS,in 2011, total employment for all U.S. electronic component manufacturing industries,



including semiconductors, was 383,513. This number is based on total employment for 2011 reported under NAICS code 3344, described as "Semiconductor and other electronic component manufacturing." United States Department of Labor, Bureau of Labor Statistics, State and County Employment and Wages Database.

Of this total, semiconductor manufacturing employment totalled 188,358, or 49 percent, by far the largest share of all U.S. electronic component manufacturing industries (see the figure above). This total does not include employees of fabless semiconductor firms, which design semiconductors but do not manufacture them. The U.S. semiconductor industry's manufacturing workforce grew by 3.7 percent in 2011, according to BLS data.

In comparison, jobs throughout the broader U.S. economy increased by 1.2 percent over the same time period.4 U.S. semiconductor industry employment in the manufacturing sector alone reached over 188,358, an increase of 6,690 jobs from the previous year (the figure below). This total does not include employees of fabless semiconductor firms. This is a significant increase, given that the unemployment rate in the broader U.S. economy has remained high.

Total U.S. Semiconductor Manufacturing Sector Employment, 2010 and 2011
In the interim, SIA has created an estimate for total fabless employment captured outside of the manufacturing NAICS codes and included it with the manufacturing NAICS employment data to arrive at the total of 244,800.

SIA estimates that approximately 56,400 fabless semiconductor jobs are counted outside of the manufacturing NAICS codes.

This number is added to the approximately 188,400 semiconductor jobs in the NAICS industry code to arrive at the total of 244,800 U.S. semiconductor jobs in 2011.

ABI Research: this could be the start of a platform war between Apple & Samsung

THE GALAXY SIII E210s was released in Korea recently and with its launch, Samsung sent a message to the chipset giant Qualcomm by dropping the Qualcomm modem in favour of its home grown solution.

Samsung has historically been known for its high-end application processors that appear in a number of its smartphones but the modem in its product has typically been supplied by companies such as Qualcomm, Intel, Broadcom, STE, or Via Telecom.

VP of Engineering, James Mielke, states that, "Mid last year it introduced a CDMA/LTE phone that was produced with a Via Telecom CDMA modem, a Samsung LTE modem, and a Samsung application processor. This combination became popular for Samsung during the remainder of the year. What makes this variant of the Galaxy SIII so interesting is the modem is a single chip HSPA/LTE integrated circuit designed and manufactured by Samsung."

Key Samsung Galaxy SIII LTE (SHV-E210s) components include Samsung's 2G/3G/4G 40nm modem- CMC221S (same main die as predecessor- CMC2200), the Samsung Quad core Exynos 4412 application processor and Samsung's ISP. Also used in the device are the Triquint quadBand EDGE PA, Avago and RFMD's 3G PAs, Broadcom's BCM4334 WiFi/BT/FM single chip and Wolfson 's audio hub WM1811AE.

Other components are the Knowles Mem microphones, STM Gyro and pressure sensor and FCI's 2G/3G/4G transceiver FC7860. As Samsung continues to capture more share of the smartphone market, its growing reliance upon captive market solutions could prove to be a major concern for suppliers such as Qualcomm and Via Telecom.

This move to manufacturing its own solutions plus Samsung's recent purchase of CSR's handset business could prove a key turning point that signifies a shift in the handset component market towards a platform battle between two major powerhouses of the mobile industry.

X-FAB becomes majority shareholder In MFI

X-FAB SILICON FOUNDRIES has increased its share in the German-based MEMS Foundry Itzehoe GmbH (MFI) from 25.5 percent to 51 percent – becoming the majority shareholder. The company has also renamed MFI to X-FAB MEMS Foundry Itzehoe.

These moves reflect X-FAB's focus on MEMS (Microelectromechanical systems) manufacturing services and technologies.

The Itzehoe site complements the MEMS capabilities and resources of the recently announced X-FAB MEMS Foundry in Erfurt, adding technologies for micro sensors, actuators, micro-optical structures and hermetic wafer-level packaging processes.

X-FAB MEMS Foundry Itzehoe will continue its long-term cooperation with the Fraunhofer ISIT MEMS Group to accelerate the exploitation and commercialisation of existing and emerging technologies, applications and intellectual property for automotive and other markets.

According to Thomas Hartung, vice president of marketing at X-FAB Group, "Our customers will benefit from both an even wider spectrum of available MEMS technologies and from direct access to X-FAB's manufacturing facilities for CMOS-compatible MEMS processes.

X-FAB MEMS Foundry Itzehoe will play an important role in the implementation of our MEMS strategy, and brings us closer to our goal of becoming one of the top three pure-play MEMS foundry providers."

"The rich combination of the versatile MEMS-specific technology portfolio at the Itzehoe-based MEMS foundry and the development expertise of Fraunhofer ISIT greatly expand the capabilities of X-FAB's technology offering," adds Peter Merz, managing director of X-FAB MEMS Foundry Itzehoe.

"We are delighted to provide the full bandwidth of MEMS technologies including vacuum and optical wafer-level packaging or Through silicon via (TSV) backed by X-FAB's existing and well-proven foundry services. This integration brings X-FAB customers bundled and accelerated product development and manufacturing cycles for micro-machined devices such as inertial sensors, micro-mirrors and piezoelectric transducers."

X-FAB is an analogue/mixed-signal foundry group manufacturing silicon wafers for analogue-digital integrated circuits (mixed-signal ICs). The firm has wafer production facilities in Erfurt, Dresden and Itzehoe (Germany), Lubbock, Texas (U.S.), and Kuching, Sarawak (Malaysia).

Wafers are manufactured based on advanced modular CMOS (Complementary metal oxide semiconductor) and BiCMOS (Bipolar junction transistor and CMOS transistor integration) processes, as well as MEMS processes. The technologies range from 1 to 0.13 μm for applications primarily in the automotive, communications, consumer and industrial sectors.

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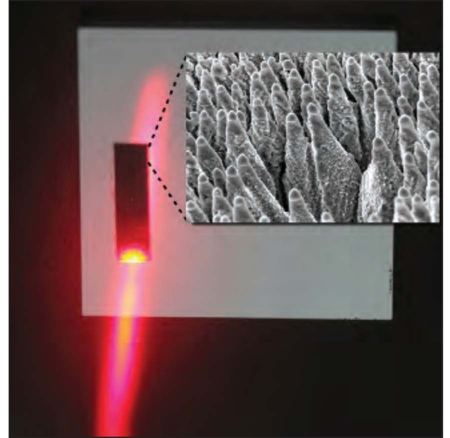
Black silicon solar cell efficiency doubled

UNLIKE standard silicon solar cells, black silicon absorbs nearly all of the sunlight that hits it, including infrared radiation, and converts it into electricity.



Solar cells convert three-quarters of the energy contained in the sun's spectrum into electricity, yet the infrared spectrum is entirely lost in standard solar cells. In contrast, black silicon solar cells are specifically designed to absorb this part of the sun's spectrum. Researchers have recently succeeded in doubling their overall efficiency.

Another company has previously explored this technology, but not in the solar market. SiOnyx, an innovator in advanced imaging systems, earlier this year, made a strategic investment and technology development agreement with In-Q-Tel (IQT). Together the collaborators aim to accelerate the integration of what is its proprietary "Black Silicon" technology into image sensors in imaging systems.

The sun blazes down from a deep blue sky, and rooftop solar cells convert this solar energy into electricity. But not all of it. Around a quarter of the sun's spectrum is made up of infrared radiation which cannot be converted by standard solar cells, so this heat radiation is lost. One way to overcome this is to use black silicon. This material absorbs nearly all of the sunlight that hits it, including infrared radiation, and converts it into electricity.

"Black silicon is produced by irradiating standard silicon with femtosecond laser pulses under a sulphur containing atmosphere," explains Stefan Kontermann, who heads the Research group "Nanomaterials for Energy Conversion." The project is part of the Fraunhofer Project Group for Fibre Optical Sensor Systems at the Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institut, HHI.

"This structures the surface and integrates sulphur atoms into the silicon lattice, making the treated material appear black." If manufacturers were to equip their solar cells with this black silicon, it would significantly boost the cells' efficiency by enabling them to utilise the full sun spectrum. The image above shows black silicon being irradiated with a laser. The smaller image is a scanning electron image of the black silicon. Researchers at HHI have now managed to double the efficiency of black silicon solar cells. In other words, they have created cells that can produce more electricity from the infrared spectrum. "We achieved that by modifying the shape of the laser pulse we use to irradiate the silicon," says Kontermann.

This enabled the scientists to solve a key problem of black silicon. In normal silicon, infrared light does not have enough energy to excite the electrons into the conduction band and convert them into electricity, but the sulphur incorporated in black silicon forms a kind of intermediate level. You could compare this to climbing a wall. The first time you fail because the wall is too high, but the second time you succeed in two steps by using an intermediate level. However, in sulphur this intermediate level not only enables electrons to climb the 'wall', it also works in reverse, enabling electrons from the conduction band to jump back via this intermediate level, which causes electricity to be lost once again. By modifying the laser pulse that drives the sulphur atoms into the atomic lattice, researchers can change the positions that these atoms adopt in the lattice and change the height of their 'levels', in other words their energy level. "We used the laser pulses to alter the embedded sulphur in order to maximize the number of electrons that can climb up while minimising the number that can go back down," Kontermann sums up.

In the first stage of the project, the scientists modified the laser pulses and investigated how this changed the properties of black silicon and the efficiency of solar cells made from this material. Now they are working on using different shapes of laser pulses and analysing how this changes the energy level of the sulphur. In the future, they hope that a system of algorithms will automatically identify how the laser pulse should be modified in order to achieve optimum efficiency. The 'Customised light pulses' project was one of this year's winners in the '365 Places in the Land of Ideas' competition; the awards ceremony is due to be held in Goslar on October 11th, 2012.

The researchers have already successfully built prototypes of black silicon solar cells and their next step will be to try and merge these cells with commercial technology. "We hope to be able to increase the efficiency of commercial solar cells - which currently stands at approximately 17 percent - by 1 percent by combining them with black silicon," Kontermann says.

Their starting point is a standard commercial solar cell. The experts simply remove the back cover and incorporate black silicon in part of the cell, thereby creating a tandem solar cell that contains both normal and black silicon.
The researchers are also planning a spin-off. This company will be used to market the laser system that manufacturers will be able to acquire to expand their existing solar cell production lines. Manufacturers would then be able to produce the black silicon themselves and include it in the cells as standard.

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Enhancing silicon-based batteries

'CRUSHED' porous silicon anodes exhibit a dramatic increase in charge-discharge cycles. Researchers at Rice University have refined silicon-based lithium-ion technology by making a high-capacity, long-lived and low-cost anode material. The discovery could have serious commercial potential for rechargeable lithium batteries.

The team led by Sibani Lisa Biswal and Madhuri Thakur, reported their work in Nature's open access journal Scientific Reports. They detailed the creation of a silicon-based anode, the negative electrode of a battery that easily achieves 600 charge-discharge cycles at 1,000 milliamp hours per gram (mAh/g). This is a significant improvement over the 350 mAh/g capacity of current graphite anodes. That puts it squarely in the realm of next-generation battery technology competing to lower the cost and extend the range of electric vehicles.

The new work by Rice through the long-running Lockheed Martin Advanced Nanotechnology Centre of Excellence at Rice (LANCER) is the next and biggest logical step since the partners began investigating batteries four years ago. "We previously reported on making porous silicon films," says Biswal, an assistant professor of chemical and biomolecular engineering. "We have been looking to move away from the film geometry to something that can be easily transferred into the current battery manufacturing process. Madhuri crushed the porous silicon film to form porous silicon particulates, a powder that can be easily adopted by battery manufacturers."

Porous silicon powder mixed with pyrolyzed polyacrylonitrile is the basis for a robust anode for lithium-ion batteries (Credit: Madhuri Thakur/Rice University)

Silicon can hold 10 times more lithium ions than the graphite commonly used in anodes today. But there's a problem: Silicon more than triples its volume when completely lithiated. When repeated, this swelling and shrinking causes silicon to quickly break down.

Many researchers have been working on strategies to make silicon more suitable for battery use. Now, scientists at Rice and elsewhere have created nanostructured silicon with a high surface-to-volume ratio, which allows the silicon to accommodate a larger volume expansion. Biswal, Thakur and Michael Wong tried the opposite approach; they etched pores into silicon wafers to give the material room to expand. Earlier this year, they had advanced to making sponge-like silicon films that showed even more promise.

But even those films presented a problem for manufacturers, Thakur says. "They're not easy to handle and would be difficult to scale up." But by crushing the sponges into porous grains, the material gains far more surface area to soak up lithium ions. Biswal held up two vials, one holding 50 milligrams of crushed silicon, the other 50 milligrams of porous silicon powder. The difference between them was obvious. "The surface area of our material is 46 square metres per gram," she says. "Crushed silicon is 0.71 square metres per gram. So our particles have more than 50 times the surface area, which gives us a larger surface area for lithiation, with plenty of void space to accommodate expansion."

The porous silicon powder is mixed with a binder, pyrolyzed polyacrylonitrile (PAN), which offers conductive and structural support. "As a powder, they can be used in large-scale roll-to-roll processing by industry," Thakur adds. "The material is very simple to synthesise, cost-effective and gives high energy capacity over a large number of cycles. This work shows just how important and useful it is to be able to control the internal pores and the external size of the silicon particles," Wong continues.

In recent experiments, Thakur designed a half-cell battery with lithium metal as the counter electrode and fixed the capacity of the anode to 1,000 mAh/g. That was only about a third of its theoretical capacity, but three times better than current batteries. The anodes lasted 600 charge-discharge cycles at a C/2 rate (two hours to charge and two hours to discharge). Another anode continues to cycle at a C/5 rate (five-hour charge and five-hour discharge) and is expected to remain at 1,000 mAh/g for more than 700 cycles.

"This successful endeavour between Rice University and Lockheed Martin Mission Systems and Sensors will provide a significant improvement in battery technology by the development of this inexpensive manufacturing technique for silicon anode material," comments Steven Sinsabaugh, a Lockheed Martin Fellow who works with LANCER and a co-author of the paper along with Lockheed Martin researcher Mark Isaacson. "We're truly excited about this breakthrough and are looking forward to transitioning this technology to the commercial marketplace."

A half-cell battery that incorporates a porous silicon which has achieved more than 600 charge-discharge cycles in the lab. (Credit: Jeff Fitlow/Rice University) "The next step will be to test this porous silicon powder as an anode in a full battery," Biswal concludes. "Our preliminary results with cobalt oxide as the cathode appear very promising, and there are new cathode materials that we'd like to investigate."

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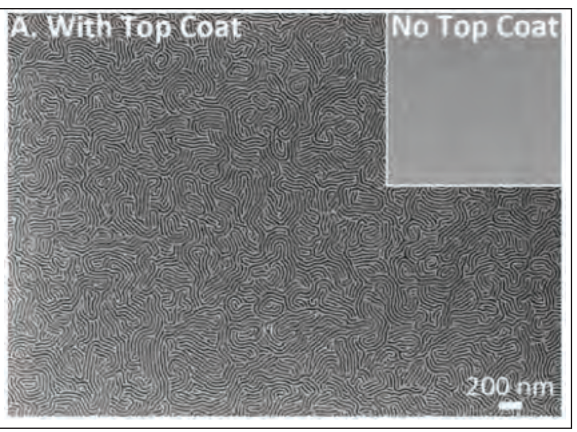
Boosting computer memory fivefold

THE STORAGE capacity of hard disk drives could increase by a factor of five thanks to processes developed by chemists and engineers at The University of Texas at Austin.
The researchers' technique, detailed in the journal Science, relies on self-organising substances known as block copolymers. It is being given a real-world test run in collaboration with HGST, an innovator in disk drives.



"In the last few decades there's been a steady, exponential increase in the amount of information that can be stored on memory devices, but things have now reached a point where we're running up against physical limits," says C. Grant Willson, professor of chemistry and biochemistry in the College of Natural Sciences and the Rashid Engineering Regents Chair in the Cockrell School of Engineering. With current production methods, zeroes and ones are written as magnetic dots on a continuous metal surface. The closer together the dots are, the more information can be stored in the same area.

But that tactic has been pretty much maxed out. The dots have now gotten so close together that any further increase in proximity would cause them to be affected by the magnetic fields of their neighbouring dots and become unstable.

"The industry is now at about a terabit of information per square inch," says Willson, who co-authored the paper with chemical engineering professor Christopher Ellison and a team of graduate and undergraduate students. "If we moved the dots much closer together with the current method, they would begin to flip spontaneously now and then, and the archival properties of hard disk drives would be lost. Then you're in a world of trouble. Can you imagine if one day your bank account info just changed spontaneously?"

There's a quirk in the physics, however. If the dots are isolated from one another, with no magnetic material between them, they can be pushed closer together without destabilisation. This is where block copolymers come in. At room temperature, coated on a disk surface, they don't look like much. But if they're designed in the right way, and given the right prod, they'll self-assemble into highly regular patterns of dots or lines. If the surface onto which they're coated already has some guideposts etched into it, the dots or lines will form into precisely the patterns needed for a hard disk drive.

This process, which is called directed self-assembly (DSA), was pioneered by engineers at the University of Wisconsin and the Massachusetts Institute of Technology.

When Willson, Ellison and their students began working with directed self-assembly, the best anyone in the field had done was to get the dots small enough to double the storage density of disk drives. The challenge has been to shrink the dots further and to find processing methods that are compatible with high-throughput production. The team has made great progress on a number of fronts. They've synthesised block copolymers that self-assemble into what they claim are the smallest dots in the world. In some cases they form into the right, tight patterns in less than a minute, which is also a record.

"I am kind of amazed that our students have been able to do what they've done," adds Willson. "When we started, for instance, I was hoping that we could get the processing time under 48 hours. We're now down to about 30 seconds. I'm not even sure how it is possible to do it that fast. It doesn't seem reasonable, but once in a while you get lucky."

Most significantly, the team has designed a special top coat that goes over the block copolymers while they are self-assembling. "I've been fortunate enough to be involved in the experimental work of the top coat project from its inception all the way to our final results," says Leon Dean, a senior chemical engineering major and one of the authors on the Science paper. "We've had to develop an innovative spin-on top coat for neutralising the surface energy at the top interface of a block copolymer film."
This top coat allows the polymers to achieve the right orientation relative to the plane of the surface simply by heating.

"The patterns of super small dots can now self-assemble in vertical or perpendicular patterns at smaller dimensions than ever before," maintains Thomas Albrecht, manager of patterned media technology at HGST. "That makes them easier to etch into the surface of a master plate for nanoimprinting, which is exactly what we need to make patterned media for higher capacity disk drives."

Willson, Ellison and their students are currently working with HGST to see whether these advances can be adapted to their products and integrated into a mainstream manufacturing process. Other industry collaborators are Nissan Chemical Company, which partially funded the research, and Molecular Imprints, an Austin-based company co-founded by Willson that is a pioneer in nanoimprint lithography. Further details of this work has been published in the paper, "Polarity-Switching Top Coats Enable Orientation of Sub-10-nm Block Copolymer Domains," in the journal Science, Vol. 338 no. 6108 pp. 775-779. DOI:10.1126/science.1226046

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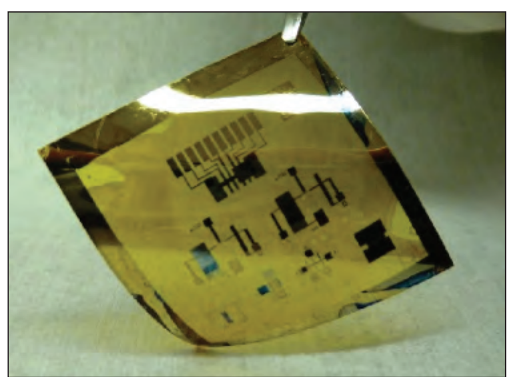
Cadmium selenide to take on amorphous silicon in electronics

ELECTRONIC circuits are typically integrated in rigid silicon wafers, but flexibility opens up a wide range of applications. In a world where electronics are becoming more pervasive, flexibility is a highly desirable trait, but finding materials with the right mix of performance and manufacturing cost remains a challenge. Now a team of researchers from the University of Pennsylvania has claimed that nanoscale particles, or nanocrystals, of the semiconductor cadmium selenide (CdSe) can be "printed" or "coated" on flexible plastics to form high-performance electronics. The research was led by David Kim, in the Department of Materials Science and Engineering in Penn's School of Engineering and Applied Science and the work was published in the journal Nature Communications.



"We have a performance benchmark in amorphous silicon, which is the material that runs the display in your laptop, among other devices," Kagan, a co-author of the publication, says. "Here, we show that these cadmium selenide nanocrystal devices can move electrons 22 times faster than in amorphous silicon."
Besides speed, another advantage cadmium selenide nanocrystals have over amorphous silicon is the temperature at which they are deposited.

While amorphous silicon uses a process that operates at several hundred degrees, CdSe nanocrystals can be deposited at room temperature and annealed at mild temperatures, opening up the possibility of using more flexible plastic foundations.
Another innovation that allowed the researchers to use flexible plastic was their choice of ligands, the chemical chains that extend from the nanocrystals' surfaces and helps facilitate conductivity as they are packed together into a film.

"There have been a lot of electron transport studies on cadmium selenide, but until recently we haven't been able to get good performance out of them," Kim says. "The new aspect of our research was that we used ligands that we can translate very easily onto the flexible plastic; other ligands are so caustic that the plastic actually melts."

Because the nanocrystals are dispersed in an ink-like liquid, multiple types of deposition techniques can be used to make circuits. In their study, the researchers used spincoating, where centrifugal force pulls a thin layer of the solution over a surface, but the nanocrystals could be applied through dipping, spraying or ink-jet printing as well. On a flexible plastic sheet a bottom layer of electrodes was patterned using a shadow mask, essentially a stencil, to mark off one level of the circuit. The researchers then used the stencil to define small regions of conducting gold to make the electrical connections to upper levels that would form the circuit. An insulating aluminium oxide layer was introduced and a 30nm layer of nanocrystals was coated from solution. Finally, electrodes on the top level were deposited through shadow masks to ultimately form the circuits.

"The more complex circuits are like buildings with multiple floors," Kagan says. "The gold acts like staircases that the electrons can use to travel between those floors."

The image above shows the flexible circuit fabricated in the Kagan lab. Using this process, the researchers built three kinds of circuits to test the nanocrystals performance for circuit applications: an inverter, an amplifier and a ring oscillator.

"An inverter is the fundamental building block for more complex circuits," Lai, another co-author of the paper, comments. "We can also show amplifiers, which amplify the signal amplitude in analogue circuits, and ring oscillators, where 'on' and 'off' signals are properly propagating over multiple stages in digital circuits."
"And all of these circuits operate with a couple of volts," Kagan says. "If you want electronics for portable devices that are going to work with batteries, they have to operate at low voltage or they won't be useful."

With the combination of flexibility, relatively simple fabrication processes and low power requirements, these cadmium selenide nanocrystal circuits could pave the way for new kinds of devices and pervasive sensors, which could have biomedical or security applications.

"This research also opens up the possibility of using other kinds of nanocrystals, as we've shown the materials aspect is not a limitation anymore," Kim points out.

More details of this work can be accessed in the paper, "Flexible and low-voltage integrated circuits constructed from high-performance nanocrystal transistors," by David K. Kim et al in Nature Communications, 3, Article number 1216,. DOI: 10.1038/ncomms2218

The research was supported by the U.S. Department of Energy and the National Science Foundation.

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Nanoelectronics could aid computer chip designers

TO BUILD the computer chips of the future, designers will need to understand how an electrical charge behaves when it is confined to metal wires only a few atom-widths in diameter.

A Team of physicists at McGill University, in collaboration with General Motors R&D, have shown that electrical current may be drastically reduced when wires from two dissimilar metals meet.

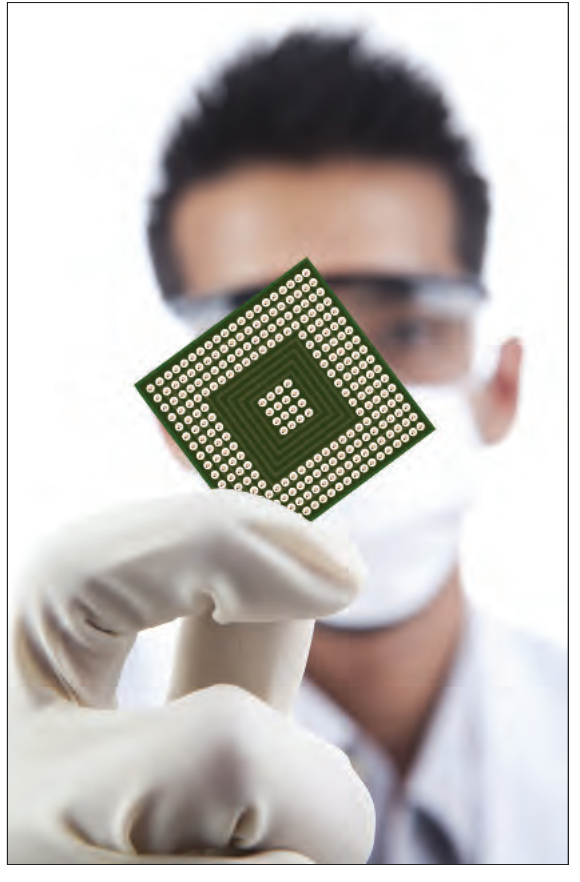
The surprisingly sharp reduction in current reveals a significant challenge that could shape material choices and device design in the emerging field of nanoelectronics.

The size of features in electronic circuits is shrinking every year, thanks to the aggressive miniaturisation prescribed by Moore's Law. The theory postulates that the density of transistors on ICs would double about every 18 months.

This steady progress makes it possible to carry around computers in our pockets, but poses serious challenges. As feature sizes dwindle to the level of atoms, the resistance to current no longer increases at a consistent rate as devices shrink; instead the resistance "jumps around," displaying the counterintuitive effects of quantum mechanics, says McGill Physics professor Peter Grütter.

"You could use the analogy of a water hose," Grütter explains. "If you keep the water pressure constant, less water comes out as you reduce the diameter of the hose. But if you were to shrink the hose to the size of a straw just two or three atoms in diameter, the outflow would no longer decline at a rate proportional to the hose cross-sectional area; it would vary in a quantised ('jumpy') way."

This "quantum weirdness" is exactly what the McGill and General Motors researchers observed, as described in a paper appearing in Proceedings of the National Academy of Sciences. The researchers investigated an ultra-small contact between gold and tungsten, two metals currently used in combination in computer chips to connect different functional components of a device.



On the experimental side of the research, Grütter's lab used advanced microscopy techniques to image a tungsten probe and gold surface with atomic precision, and to bring them together mechanically in a precisely-controlled manner.
The electrical current through the resulting contact was much lower than expected. Mechanical modelling of the atomic structure of this contact was done in collaboration with Yue Qi, a research scientist with the General Motors R&D Centre in Warren, Michigan.

State-of-the-art electrical modelling by Jesse Maassen in professor Hong Guo's McGill Physics research group confirmed this result, showing that dissimilarities in electronic structure between the two metals leads to a fourfold decrease in current flow, even for a perfect interface. The researchers also found that crystal defects generated by bringing the two materials into mechanical contact, was a further reason for the observed reduction of the current.

"The size of that drop is far greater than most experts would expect -on the order of 10 times greater," notes Grütter.

The results point to a need for future research into ways to surmount this challenge, possibly through choice of materials or other processing techniques. "The first step toward finding a solution is being aware of the problem," Grütter adds. "This is the first time that it has been demonstrated that this is a major problem" for nanoelectronic systems."

Funding for this research was provided by the Natural Sciences and Engineering Research Council of Canada, le Fonds Québécois de la Recherche sur la Nature et les Technologies, and the Canadian Institute for Advanced Research.

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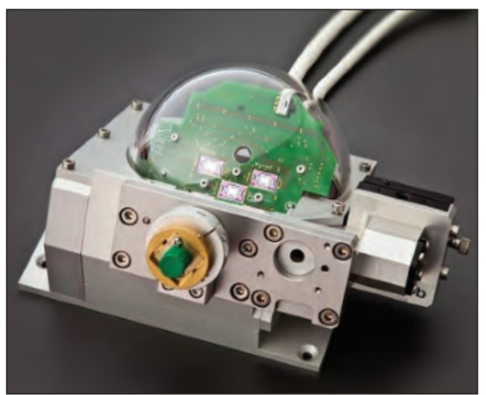
Robots could do your work thanks to MEMS & lasers



A NEWLY developed scanner technology developed by Fraunhofer IPMS opens up new possibilities for laser scanners and laser projectors.

The Fraunhofer IPMS is part of the Fraunhofer Group Microelectronics, and is engaged in various regional and international networks in microsystems and photonics. The research institute's new LinScan technology allows switching of the target positions of its laser beam quickly, and a dynamic adjustment of the scanning speed. 3D cameras or miniaturised laser projectors equipped with this technology offer a very high resolution and make innovative solutions possible.

These include robot eyes with sharp vision or compact cell phone projectors with high image quality. The Fraunhofer Institute for Photonic Microsystems (IPMS) will be presenting this technology to industry professionals at Vision 2012, taking place from November 6th to 8th. The image above shows an optical scan head of a 3D-TOF-camera with integrated MEMS scanning mirror array. IPMS suggests that service robots could replace humans in the future.

In particular, when jobs endanger health and safety, or are too awkward or complicated, or just make life easier for us humans. However, to rely on the robots to perform such complex tasks independently and reliably, they need to not only see, but also be capable of interpreting their environment. They should also be able to control their vision according to ambient conditions.This depends on the assumption that their environmental visualisation functions work similarly to the way the human eye does.

In other words, the sharpest area of vision, on the retina of the human eye, or so-called fovea is concentrated upon objects within our surroundings that we deem as interesting or important. "That is exactly what a camera with LinScan technology is capable of," says Thilo Sandner, Project Manager at Fraunhofer IPMS. He explains,

"The camera potentially imitates the human visualisation system by first scanning the surroundings and then resolving interesting objects with greater precision".

Fraunhofer IPMS says the LinScan technology poses a massive developmental leap for applications in compact laser projectors as well. It is unlike the double-resonant scanning principle used for many pico-projectors. In this technology, the mirror oscillates in a sinusoidal manner with a frequency predefined by the geometry of the component. LinScan, on the other hand, makes it possible for the laser beam to jump from line to line with a flexible scanning speed. Image resolutions of SVGA (800 x 600) and more become possible with miniaturised architectures.

The LinScan manufacturing technology developed for resonant microscanners is to tilt the drive combs of the hitherto existing resonant scanner towards each other. This makes the linear drive of the mirror plate on one axis possible. What's more, a resonant drive with a defined frequency on the fast horizontal axis can be combined with a variable quasi-static oscillation on the vertical axis.

The components are manufactured in the Fraunhofer IPMS cleanroom in a bulk micromachining manufacturing process. All of the micro-mechanical components are manufactured as two-dimensional structures in a layer of monocrystalline silicon.

The vertical comb electrodes are realised in an adhesive wafer bonding process with a second planar-structured silicon wafer. Mechanical solid state structures on the second wafer tilt or stagger the in-plane comb drive,The entire device is fixed by subsequent wafer-bonding fusing.

Given the small tolerances of micromachining processes, the structures on the two wafers are optimally aligned to each other. This component concept is extremely flexible and makes it possible to realise a broad spectrum of component characteristics.One initial prototype of an optical scanning head with five integrated, synchronically operated LinScan scanning mirrors, as well as a linear projector, will illustrate the current technical possibilities of the LinScan component concept.

The double resonant scanning principle will be demonstrated using the examples of both an endomicroscope as well as a confocal 3D fluorescent microscope. Together, the partners are working on implementing the foveal principle. In other words, the rough scanning of objects appearing within the range of sight, in a 3D camera system to detect the objects looked for, and record objects with a much higher resolution.

The researchers plan to combine the LinScan scanning technology with a three-dimensional object survey. This will be based on time of flight as well as software for ultra-fast object capture to increase comprehension of the surroundings.

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Overcoming Moore's Law with carbon nanotubes

A NOVEL processing method will help pave the way for carbon technology as a viable alternative to silicon in future computing. IBM scientists have demonstrated a new approach to carbon nanotechnology that opens up the path for commercial fabrication of dramatically smaller, faster and more powerful computer chips. For the first time, more than ten thousand working transistors made of nanosized tubes of carbon have been precisely placed and tested in a single chip using standard semiconductor processes. IBM says these carbon devices are poised to replace and outperform silicon technology. They could allow further miniaturisation of computing components and advance future microelectronics.

Rapid innovation over four decades has enabled silicon microprocessor technology to continuously shrink in size and improve performance to drive the information technology revolution. Silicon transistors, tiny switches that carry information on a chip, have been made smaller year after year, but they are approaching a point of physical limitation.

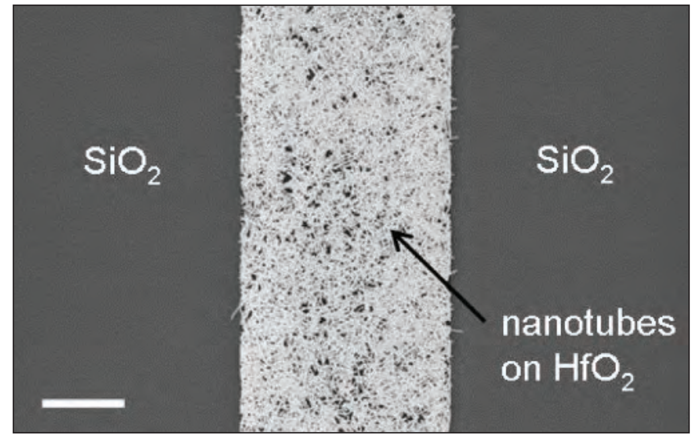
Their increasingly small dimensions, now reaching the nanoscale, will prohibit any gains in performance due to the nature of silicon and Moore's law. Within a few more generations, classical scaling and shrinkage will no longer yield the sizable benefits of lower power, lower cost and higher speed processors that the industry has become accustomed to.

Carbon nanotubes represent a new class of semiconductor materials whose electrical properties are more attractive than silicon, particularly for building nanoscale transistor devices that are a few tens of atoms across.

For a start, electrons in carbon transistors find it easier to move in these structures as opposed to in silicon-based devices. And as such, they make it easier to speed up data transport.
The nanotubes are also ideally shaped for transistors on the atomic scale, another advantage over silicon. These qualities are among the reasons to replace the traditional silicon transistor with carbon – and coupled with new chip design architectures – will allow computing innovation on a miniature scale for the future.

The approach developed at IBM labs paves the way for circuit fabrication with large numbers of carbon nanotube transistors at predetermined substrate positions. The ability to isolate semiconducting nanotubes and place a high density of carbon devices on a wafer is crucial to assess their suitability for a technology. Eventually more than one billion transistors will be needed for future integration into commercial chips.

Until now, scientists have been able to place at most a few hundred carbon nanotube devices at a time, not nearly enough to address key issues for commercial applications.



"Carbon nanotubes, borne out of chemistry, have largely been laboratory curiosities as far as microelectronic applications are concerned. We are attempting the first steps towards a technology by fabricating carbon nanotube transistors within a conventional wafer fabrication infrastructure," says Supratik Guha, Director of Physical Sciences at IBM Research.

"The motivation to work on carbon nanotube transistors is that at extremely small nanoscale dimensions, they outperform transistors made from any other material. However, there are challenges to address such as ultra high purity of the carbon nanotubes and deliberate placement at the nanoscale. We have been making significant strides in both," adds Guha.

Originally studied for the physics that arises from their atomic dimensions and shapes, carbon nanotubes are being explored by scientists worldwide in applications that span integrated circuits, energy storage and conversion, biomedical sensing and DNA sequencing.

Carbon, a readily available basic element from which crystals as hard as diamonds and as soft as the "lead" in a pencil are made, has wide-ranging IT applications.

Carbon nanotubes are single atomic sheets of carbon rolled up into a tube. The carbon nanotube forms the core of a transistor device that will work in a fashion similar to the current silicon transistor, but will be better performing. They could be used to replace the transistors in chips that power our data-crunching servers, high performing computers and ultra fast smart phones.

Earlier this year, IBM researchers demonstrated carbon nanotube transistors can operate as excellent switches at molecular dimensions of less than ten nanometres – the equivalent to 10,000 times thinner than a strand of human hair and less than half the size of the leading silicon technology.

Comprehensive modelling of the electronic circuits suggests that about a five to ten times improvement in performance compared to silicon circuits is possible.
There are practical challenges for carbon nanotubes to become a commercial technology notably, as mentioned earlier, due to the purity and placement of the devices. Carbon nanotubes naturally come as a mix of metallic and semiconducting species and need to be placed perfectly on the wafer surface to make electronic circuits.

For device operation, only the semiconducting kind of tubes is useful which requires essentially complete removal of the metallic ones to prevent errors in circuits. Also, for large scale integration to happen, it is critical to be able to control the alignment and the location of carbon nanotube devices on a substrate.

To overcome these barriers, IBM researchers developed a novel method based on ion-exchange chemistry that allows precise and controlled placement of aligned carbon nanotubes on a substrate at a high density – two orders of magnitude greater than previous experiments, enabling the controlled placement of individual nanotubes with a density of about a billion per square centimetre.

The process starts with carbon nanotubes mixed with a surfactant, a kind of soap that makes them soluble in water. A substrate is comprised of two oxides with trenches made of chemically-modified hafnium oxide (HfO_2) and the rest of silicon oxide (SiO_2). The substrate gets immersed in the carbon nanotube solution and the nanotubes attach via a chemical bond to the HfO_2 regions while the rest of the surface remains clean.
By combining chemistry, processing and engineering expertise, IBM researchers are able to fabricate more than ten thousand transistors on a single chip.

What's more, rapid testing of thousands of devices is possible using high volume characterisation tools due to compatibility to standard commercial processes.

As this new placement technique can be readily implemented, involving common chemicals and existing semiconductor fabrication, it will allow the industry to work with carbon nanotubes at a greater scale and deliver further innovation for carbon electronics.

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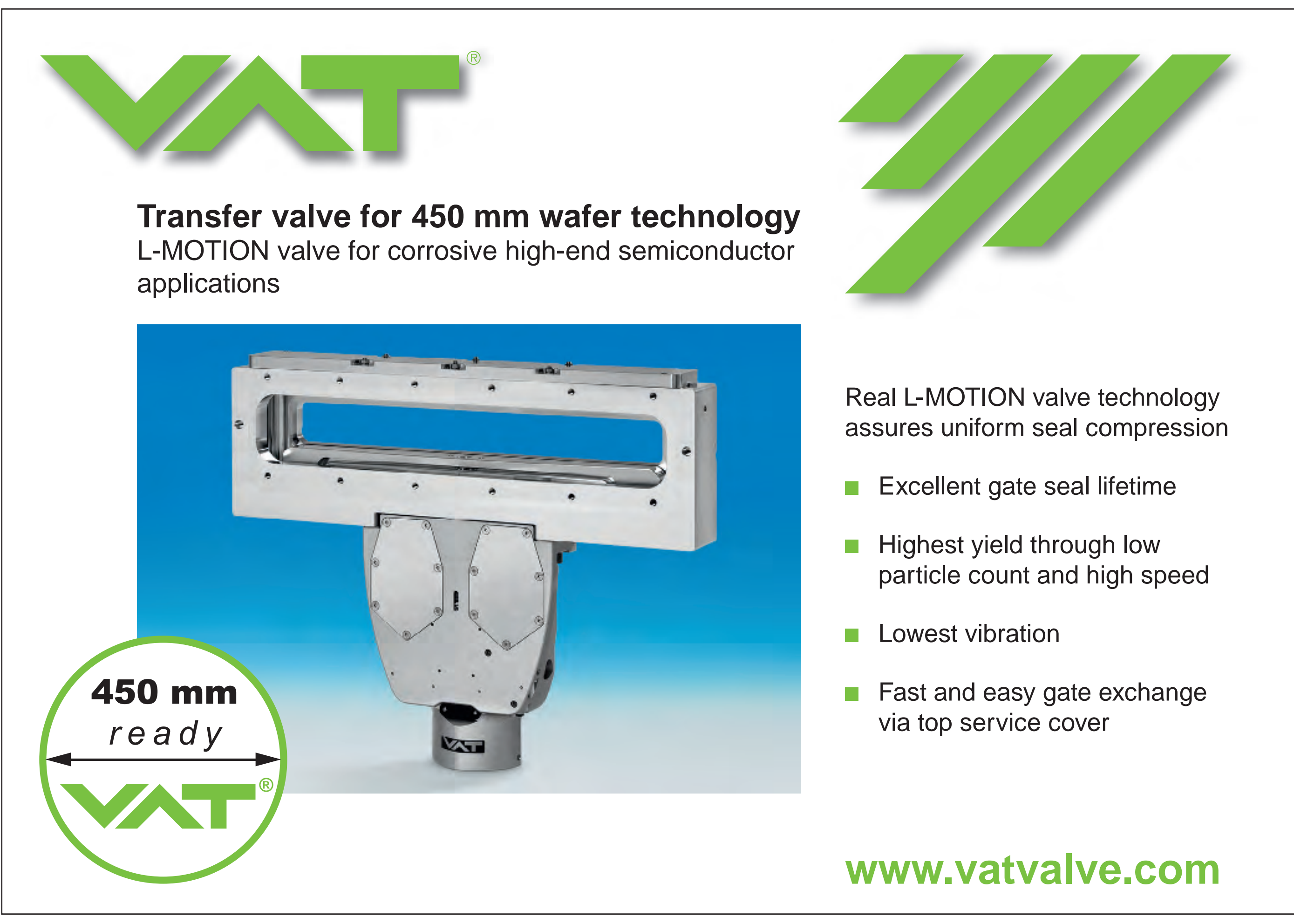

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Keynote speaker

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Program Manager of Technology Manufacturing Group, Intel III-V CMOS for High Performance and Low Power Logic Devices

Asif Anwar, Strategy Analytics
Director Strategic Technologies Practice
What's the Future of GaAs Microelectronic Manufacturing

Dr Thomas Uhrmann, EV Group
Business Development Manager
Wafer-Level Packaging of Compound Semiconductor Devices

Michelle Bourke, Oxford Instruments
Senior Product Manager
Review of The Various Deposition Techniques and Their Uses in Compound Semiconductor Devices

Gunnar Stolze, Oclaro Inc
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Malcolm Harrower, Indium
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Overview of CS Critical Elements – Indium, Gallium and Germanium

Allan Jaunzens, Evatec
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Presentation TBC

Dr Elisabeth Steimetz, LayTec AG
Director Marketing and Sales
In-Situ Monitoring - The Key to MOCVD Production Process Control and Yield Enhancement

Dr Michael Lebby, Translucent Inc
General Manager & Chief Technology Officer
Challenges & Opportunities of Using Epitaxial GaN, GeSn, & Rare Earth Oxides on Large Format Silicon Wafers for Power Electronics, Solar, & Lighting

Noriyuki Matsubara, Panasonic Europe
Dry Etching and Photolithography Engineer
Dry Etching Technology for III-V Devices

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Managing Director
Fundamental E-Beam Coating Collection Efficiency & Paths to Improvement

Pars Mukish, Yole Développement
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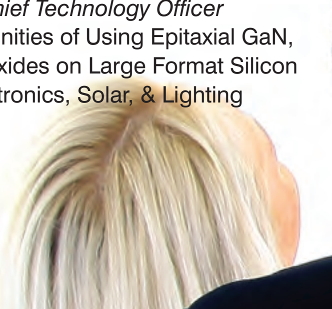

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Bryan Bothwell, TriQuint Semiconductor
Strategy and Business Development Manager
Maximizing Gallium Nitride Product Solutions and Foundry Services for Advanced RF Design Success

Dr Markus Behet, Dow Corning Corporation
Global Market Segment Manager Power Electronics
Large Diameter SiC and GaN/Si Substrates as Cost-Effective Solutions for Power Electronic Applications

AJ Nadler, RF Micro Devices (RFMD)
General Manager, R&D and Engineering Gallium Nitride for High Voltage Power Electronics

Keynote speaker

Dr YiFeng Wu, Transphorm
Vice President, Product Development
Status of High-Voltage GaN Power Electronics

Dr Vijit Sabnis, Solar Junction
Vice President, Technology
Really High Efficiency Triple-Junction Solar Cells

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Spray coating fundamentals

Coating over topography and reducing material consumption through the application of spray coating technology for MEMS and 3DICs.

Eric F. Pabo, Business Development Manager (EV Group Inc), Hirokazu Kurotaki (EV Group Japan), Process Technology Engineer, Dr. Antun Peić, Business Development Manager, and Dr. Thorsten Matthias, Business Development Director (EV Group) explain.

The photolithography process is a core process for the manufacturing of any type of integrated circuit (IC) regardless of whether the substrate for the IC is silicon, gallium arsenide, indium phosphide, or gallium nitride. One of the steps in the photolithography process is the application of the photoresist and this is normally done using spin coating.

Micro electro mechanical system (MEMS) manufacturing leverages the process technologies developed for IC manufacturing and therefore spin coating is normally used for the application of photoresist and other materials in the MEMS manufacturing processes. Spin coating is based on depositing the photoresist on the substrate and then rotating or spinning the substrate to leave a thin and uniform layer behind. Although spin coating has fundamental limitations with respect to device topography, material consumption, oversized substrates and fragile substrates these constraints are often met and then spin coating is a very useful and well understood technology.

Spin coating's fundamental limitations

Spin coating is based on applying an excess of photoresist or other material at or near the centre of the wafer and then rotating or spinning the wafer at a significant radial velocity. As the wafer is spun the resultant centrifugal force acting on the photoresist causes it to flow radially outward and most of the material is cast off of the substrate. Spin coating can be and is used for the vast majority of photoresist application with excellent results; however it has the following limitations:

- It is not suitable for applying photoresist on wafers that have significant surface topography because this topography interferes with the flow of the material caused by the centrifugal force from rotating the wafer. [1]
- It is not suitable for large substrates that cannot be spun or would be impractical to spin.
- It is not suitable for substrates that are fragile and cannot withstand the centrifugal force
- It is not suitable for non round substrates because the corners of the substrate will have non uniformities in flow of the photoresist.
- In spin coating greater than 80% of the material is normally spun off the wafer and this is an issue when using expensive materials.
- The flow of the material at the edge of the wafer immediately before being cast off normally leaves thicker area which is commonly known as an edge bead and often requires edge bead removal to prevent problems in subsequent process steps.

Spray coating fundamentals

Spray-coating can be divided in the following steps. The first step is the dilution of the photoresist material with the appropriate solvents. The second step is the delivery of the diluted material to the nozzle. The third step is atomization of the material into droplets and the transport of the droplets to the surface to be coated. The final step is the behaviour of the coated droplets on the surface being coated.

Dilution of the photoresist or material to be spray coated is important because spray coating requires lower viscosity material than typically used for spin coating and this dilution effects how the droplets interact and coalesce after landing on the substrate surface as well how the coalesced material flows on the topography of the substrate surface due to the effect of gravity.

Typically two solvents which are compatible with the material to be coated are used with one of the solvents having a high vapour pressure (low boiling point) and one of the solvents having a low vapour pressure (high boiling point). By adjusting the ratio of high vapour pressure solvent to the low vapour pressure solvent one can control the amount of solvent evaporation during coating and by adjusting the total amount of solvent to the amount of resist

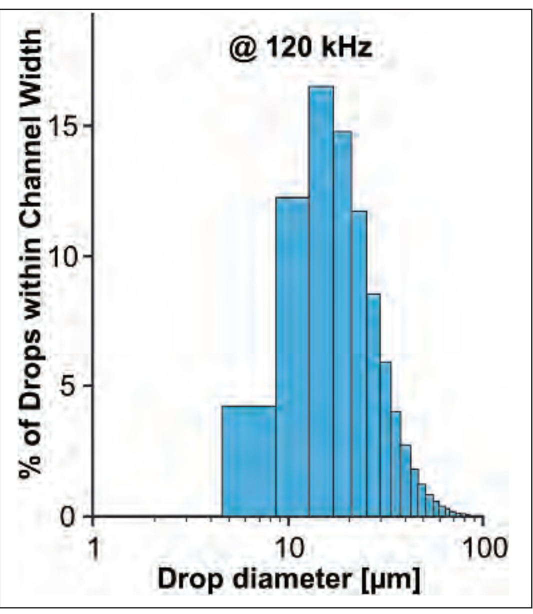

Fig 1: Ultrasonic nozzle droplet size distribution

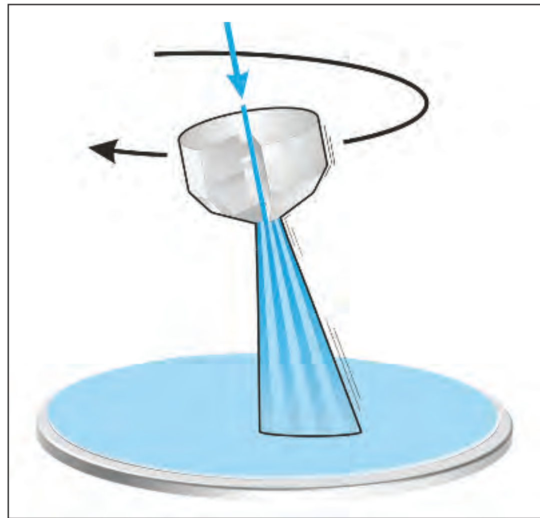
Fig 2: Radial path of spray coating nozzle

one can control the viscosity and solute content of the fluid deposited on the substrate. This optimization process is described in reference [2]

The diluted material is delivered in a controlled manner by a specialized pump system to a spray nozzle that atomizes the material and propels the droplet to the surface being coated.
This atomization can be done by the action of the carrier gas in the nozzle on the photoresist but this has the problem of coupling the droplet size with the droplet velocity. Using an ultrasonic nozzle allows the droplet size to be decoupled from the droplet velocity which is controlled by the flow rate of the carrier gas (typically N_2).

The time of flight of the droplet from the nozzle to the wafer is determined by the velocity of the droplet and the spacing from the nozzle to the surface being coating. For a given nozzle the velocity of the droplet is controlled by the flow rate of the carrier gas. The time of flight effects the evaporation of the solvents and therefore the viscosity of the particle when it hits the surface. The dispersion angle of the coating nozzle is an important factor as this determines how many of the droplets contact the vertical surfaces on the substrate and is a function of the selected nozzle. The motion of the spray nozzle relative to the

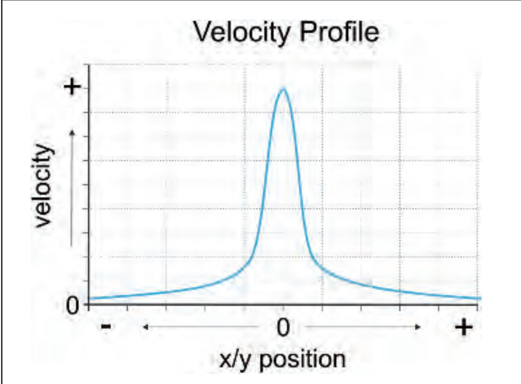

Fig 3: Angular velocity of pivoting spray nozzle

substrate being coated is important as this drives the macro level uniformity across the wafer. There are two primary approaches to this relative motion. The first is to mount the spray nozzle on a pivoting arm where the arc of the spray nozzle's path coincides with the centre of the wafer and to rotate the wafer slowly. In this case it is necessary to adjust the scan rate of this arm to avoid the result of thin coating at the wafer edge and thick coating at the centre of the wafer.

The other option is to move the spray nozzle in an X-Y scan relative to the substrate or to scan the nozzle in the X direction and move the panel in the Y direction. One of these techniques must be used if it is impractical to rotate the substrate and is commonly used on large substrates.

The other variables that need to be considered and controlled are (1) the temperature of the substrate being coated because this effects the evaporation of the solvents on the surface and therefore the final coating. A heated chuck is often used to control the substrate temperature. (2) The spray coated layer may be treated by the standard post coating processes used by spin coating such baking or chilling.

Spray coating over topography

Because spray coating does not depend on the flow of the photoresist due to centrifugal force from rotation it is possible to apply photoresist over significant topography. This issue drove the initial work on spray coating. [1, 2, 3] The images below are from a 500 um deep cavity with vertical side walls

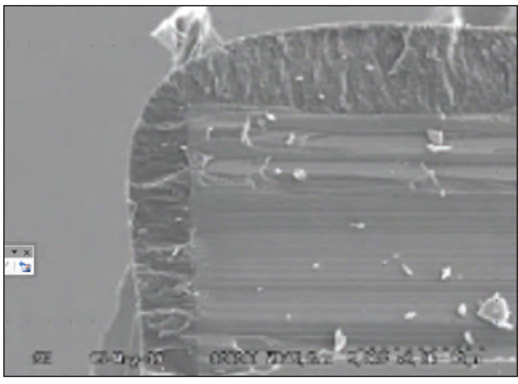
Fig 4: Image of corner between 500 um vertical sidewall and wafer surface. Resist thickness on top surface is ~7.5 um, the corner ~ 2.8 um and the sidewall ~5.3 um

Spray coating of non standard substrates

Eliminating the need for high speed rotation with spray coating allows the coating of substrates that can not be spun or are be very difficult to spin coat because of the required rotational velocity. Additionally fragile substrates can be spray coated

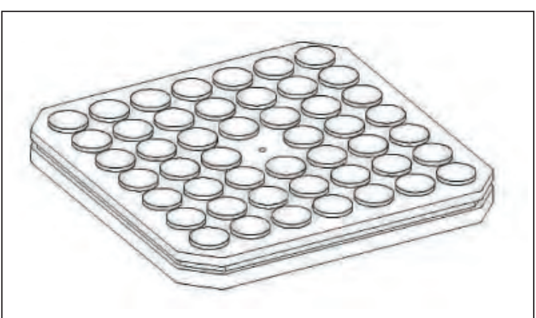

Fig: 5 Multiple small parts in a holder for spray coating

Resist Thickness versus Location for 500 μm Deep Cavity

Measurement Location	Resist Thickness in um
Top surface	7.5
Top Corner	2.8
Upper Sidewall (vertical)	5.3
Lower Sidewall (vertical)	1.5
Bottom (horizontal)	5.1

Table: 1. Resist thickness versus location for 500 μm deep cavity

without damage to the substrate from centrifugal forces of rotation. As shown in the image below it is possible to put multiple small parts in a holder and spray coat simultaneously.

Square substrates with topography may be properly coated as there is no need to rapidly rotate the substrate and photoresist flow issues associated with the topography or the corners. Eliminating the need for high speed rotation means spray coating can be and is used to coat over sized substrates. Currently 370 mm by 470 mm glass panels are being spray coated on fully automated equipment and there is no fundamental reason that this could not be done on larger panels.

Spray coating material consumption

Another primary driving force for the use of spray coating is that it normally results in dramatic reductions in material consumption as compared to spin coating. Resist volume reductions of 10-15 times have been reported [3]. The cost savings is small when inexpensive resists are being used but the cost reduction becomes very significant when using expensive photoresists or expensive materials like BCB (BenzoCycloButane). BCB is used as a bonding layer for some MEMS devices and is available in photo-sensitive formulations. When expansive materials are being the materials saving from switching to spray coating can have a payback period of less than a year.

The patterned result

The reason for applying photoresist is deposit a layer which may be exposed and developed thereby transfer a pattern. The figures 9 and 10 show examples of exposed and developed photoresist at the bottom of cavities.

Advanced spray coating for high aspect ratio vias

Special enhancements to the basic technology for spray coating now allow the coating of blind vias. This Nanospray technology allows the uniform coating of photoresist in high aspect ratio vias. This technology has been demonstrated 30-150 μm wide and 50-300 μm deep vias with aspect ratios of up to 1:4. The result of using Nanospray technology to coat 300 μm deep by 100 μm vias is shown in the cross section in Fig 11.

Spray coating challenges

Spray coating does, unfortunately, have limitation; if did not it would have displaced or be displacing spin coating. Spray coating has several challenges with respect to spin coating which are:

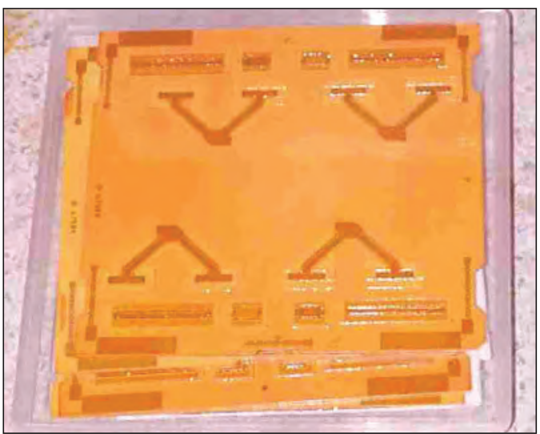

Fig: 6: Uniform and conformal coating applied by spray coating unto a pre patterned square substrate with severe topography

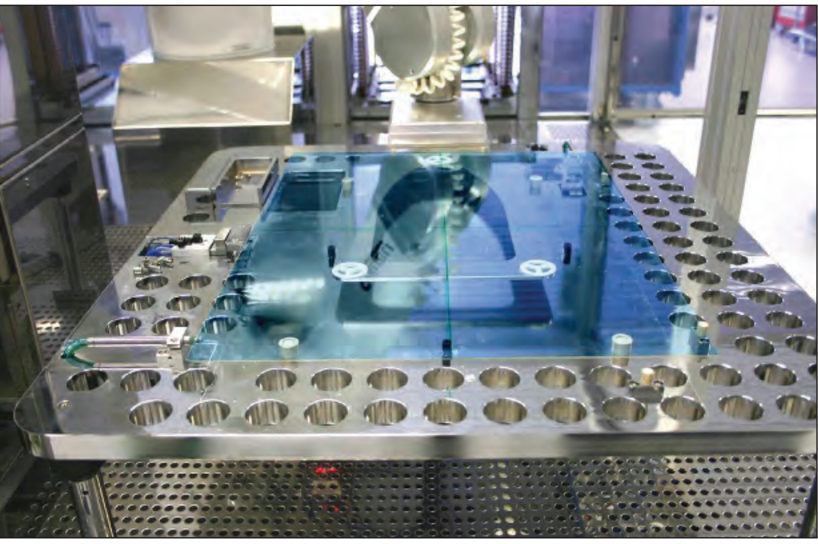

Fig 7: A 370 mm by 470 mm glass panel being prealigned prior to the application of photo resist by spray coating

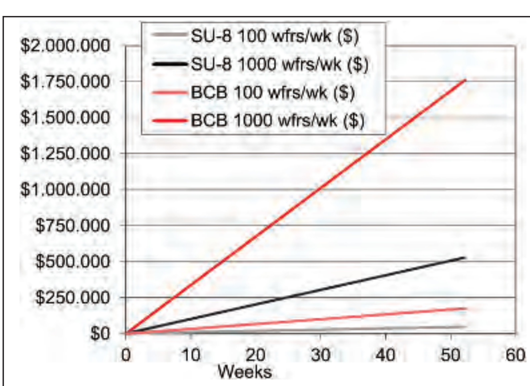

Fig 8: A plot showing the cumulative cost savings assuming an 80% material consumption reduction by use of spray coating Does not include the saving of the costly disposal of solvent-based and partly toxic photoresist

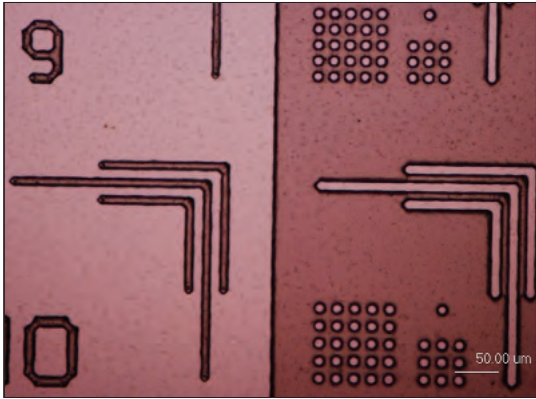

Fig 9: 10 um features at the bottom surface of a 100 um cavity

- Spray coating process parameters depend on the material being applied and the topography of the surface to which they are being applied thus they are more application specific than spin coating and are more likely to require process development.
- A small decrease in across wafer uniformity.
- Depending on the process recipe the surface of the spray-coated resist may be have a rougher surface and in some cases this causes challenges with reading small alignment marks with low contrast

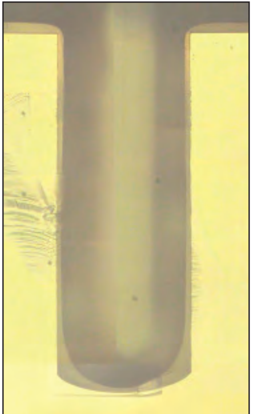

Fig 11: A 300 µm deep by 100 µm wide via coated using the NanoSpray process

Future work regarding spray coating

There are numerous standard process recipes for common photoresists and substrates and more are being developed. Unfortunately, because of the large number of photoresists and other materials available, the nearly limitless topographical patterns of the substrates and the variety of applications it is not possible have standard recipes which cover all applications of spray coating.

Therefore most spray coating equipment vendors, such as EV Group, offer access to their spray coating equipment in applications laboratories and offer process development services.

Also, there is the opportunity for the development of additional standard recipes regarding substrates size and shape, the topography of the substrate, and the material being applied.

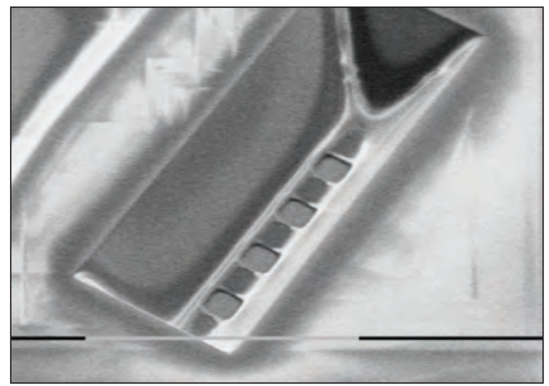

Fig 10: Features at the bottom of a trench (Courtesy of TU Delft)

Conclusions

Spray coating allows the coating of substrates with significant surface topography, in addition to material consumption reductions of up to 90%. The coating of substrates without spinning the substrates, and the coating of oversized or multiple substrates, the equipment is currently available and resources are available for optimizing spray coating for specific applications.

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Acknowledgments

Hirokazu Kurotaki from EV Group Japan.

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Unlocking the potential of diamond

Diamond is a very successful material, a source of power and an object of beauty. For semiconductor devices, thermal issues are a primary consideration, while for MEMS devices, the chemical and physical properties of diamond have enabled new devices to yield hitherto unseen performance levels, which silicon cannot deliver. Because of the scarcity of natural diamond, much of its potential has been held back; hence, there has been a long running quest for ways to synthesize diamond using technologies such as chemical vapour deposition (CVD).

CVD diamond is used in a wide variety of microelectronic, optoelectronic and specialty applications including: cutting tools, MEMS, semiconductor, electrode, etc. The properties of diamond are being increasingly utilized in high-energy research for both detection and imaging applications. As a chemical detector material, diamond's key characteristics include fast response, low noise, and corrosion stability in very aggressive media such as phosphoric or hydrochloric acid. Aerospace and defence applications have found diamond to be a useful material that can circumvent the challenges of size and weight compared to conventional materials. CVD diamond has also found its way into the design of RF power packages, amplifiers, radar devices and infrared cameras.

Silicon on Diamond

For semiconductors, thermal conductivity is the most promising diamond property that can enhance the performance of silicon and III- V based devices. Diamond large-grain polycrystalline has 50X improvement in thermal conductivity over silicon dioxide (SiO2). There are many problems associated with the poor thermal conductivity of the SiO2 layer, especially as power densities increase in a convectional SOI structure. The replacement of the SiO2 layer with a diamond film can help solve this power density problem. Silicon on diamond (SOD) wafer is a silicon device layer adjacent to a diamond heat spreader layer,

which is grown on a silicon handle wafer. This generates the SOD structure shown in Fig. 1. The high thermal conductivity of the diamond layer enables the locally generated heat to quickly spread away from the junction and into the underlying silicon with 1000X the efficiency of a traditional SOI structure. This reduces junction temperature and allows operation at much higher speeds (or power levels) at the same junction temperatures.

SOD substrates that have been developed can have a compound semiconductor device top layer or silicon device top layer. GaN on Diamond substrates have also been developed and utilized in high power III-V products typically deployed for defense applications and commercial cellular base stations. GaN on Diamond wafers address the classic heat problems that are plaguing this industry. According to researchers, a 0.5um thick layer of diamond can reduce the device operating temperature by 20% [1]. Recently, a "gate after diamond" approach has been successfully demonstrated to improve the thermal budget of the process by depositing Nano-Crystalline diamond before the thermally sensitive material.

MEMS

Diamond films prepared by hot filament chemical vapor deposition (HFCVD) have attracted increasing interest in recent years for their potential microelectronics and micro electro-mechanical system (MEMS) applications. CVD diamond film can address both thermal and mechanical management issues for MEMS applications. Diamond films exhibit a significant advantage over Si and GaAs technology platforms, thus enabling higher performance. The high thermal conductivity of diamond enables thin-film diamond coatings to be used in MEMS, photonic and microelectronic devices for improved thermal management. The high Young's modulus of diamond allows the operational frequency of MEMS RF resonators to be pushed into the GHz frequency bands. Due to diamond's hardness, thin-film diamond protects MEMS and nano-devices against surface wear, and its high lubricity contributes to low stiction.

To demonstrate the viability of diamond films for novel MEMS resonators, UC Berkeley fabricated an RF MEMS with unprecedented performance. Diamond films clearly stand out among other materials to enable high Q and acoustic velocity for MEMS applications, making it the material of choice for high frequency micromechanical resonators. Berkeley's folded-beam electro static comb driven resonator design (shown in figure 3) was used for demonstration. Q values of 146,580 at 232.4 kHz and 71,400 at 299.86 MHz were obtained for the folded beam and disk resonator design, respectively. These values are higher than previously achieved on similar devices constructed using other materials [3].

All diamond is not created equal

Microwave plasma chemical vapour deposition (MPCVD) and hot filament chemical vapour deposition (HFCVD) are the most commonly used processes to grow diamond thin films. While MPCVD offers more versatility in choice of gas and process control, the deposition area of MPCVD is limited by the frequency of the plasma generator to about 6''. HFCVD is currently capable of deposition on substrates of over twelve inches in diameter, which is far beyond the capability of the current MPCVD systems.

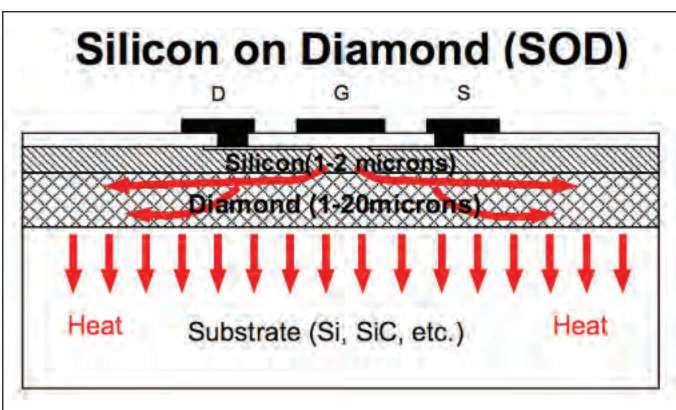

Figure 1: Silicon on diamond cross section. GaN on SOD

HFCVD is also more attractive economically and easier to operate and maintain. It is the only method that is scalable for larger wafer sizes; therefore it has become the most common technique for manufacturing diamond film.

Key factors in growing diamond for semiconductor applications

CVD techniques for producing diamond films require the activation of gas phase carbon containing precursor molecules, which involve thermal or plasma. In the MPCVD system, a plasma ball is used while in the HFCVD system, arrays of wires (usually tungsten) are heated. The HFCVD deposition process is controlled by thermal management of both filament and substrate temperatures. A methane (CH_4) and hydrogen (H_2) gas mixture flow in patterns around both the filament and substrate. The hydrogen undergoes a thermal dissociation reaction to produce monoatomic hydrogen when the filament is heated to above 1800 °C, then diamond is deposited on a substrate at a distance of about 10-15mm from the hot filaments [4]. The monoatomic hydrogen has two primary functions: (1) to etch non-diamond carbon (sp2 bonds) from the film and (2) to hydrogen terminate the surface to prevent its collapse into the reconstructed graphitic surface, essentially shutting down the diamond (sp3 bonds) growth completely.

Changes in processing parameters and time can be utilized to alter the nucleation density, growth rate, grain size and other characteristics to produce coatings with markedly different morphology. Each process can be tailored to provide an optimum coating for a given application.

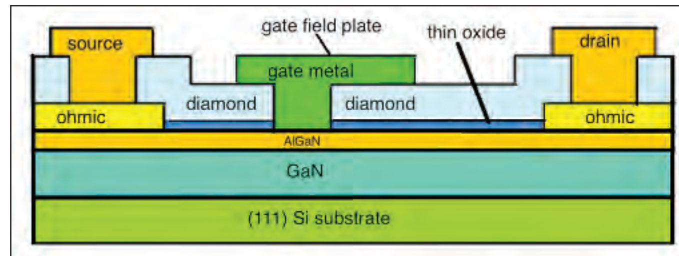

Figure 2: Reduced self-heating in AlGaN/GaN HEMTs using nanocrystalline diamond heating spreading film (2)

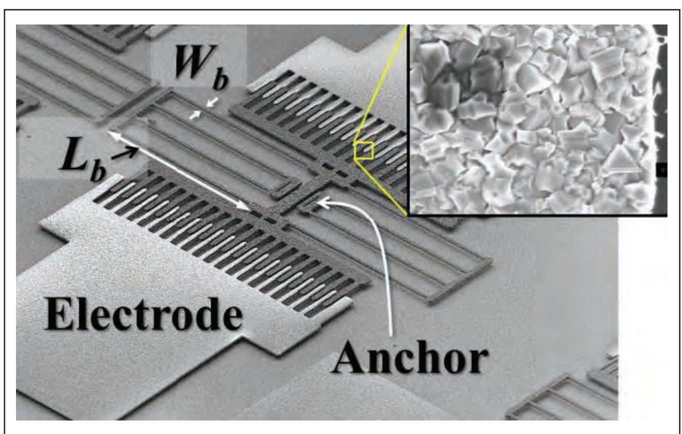

Figure 3: SEM of a fabricated com driven folded beam resonator by UC Berkeley (3)

Seeding

Diamond only grows on diamond. For continuous film growth to occur, a sufficient density of crystallites must be formed before each stage of growth, and a specific sample preparation known, as "seeding" is required. Nanodiamond growth of 4nm has recently improved seeding techniques. It helps to reduce pinhole densities, increase seeding densities, improve repeatability from part to part, and improve the life of corrosion resistant films. Nanodiamond seeding also allows for much thinner coatings [5].

Influence of temperature

For good quality diamond films, substrate temperatures during the deposition of diamond are in the range of 650-900°C. At 400°C or below, studies show a decrease in the quality of diamond film [5]. Due to the need for high temperatures, substrates have been limited to materials such as silicon, silicon carbide, silicon nitride, tungsten carbide and molybdenum. A significant decrease in the substrate temperature would allow many new diamond film applications, which is being explored.

Reactor Pressure

Another important parameter to consider in diamond synthesis is the effect of pressure. Typically pressure is in the range of 5 Torr to 50 Torr for the growth steps. Lower pressure favors smaller grain size, which is attributed to secondary nucleation processes and a faster growth rate.

Reactant Composition

The HFCVD method possesses the ability to incorporate a wide variety of carbon gas sources, such as methane. For example, in nucleation on carbide-forming substrates, it has been observed that diamond nucleation density increases as the inlet methane concentration (CH4) increases. The gas composition not only influences the nucleation density, but also the nucleation behavior and the resultant crystal morphology. Increasing the methane percentage will increase the grow rate and sp2 content of the film. HFCVD diamond film growth methods are reasonably simple in their execution. DC power is used and the control is straightforward. Control comprises gas ratios, flow rates, pressure and the amount of DC power in the filaments. HFCVD growth methods also have proven to be efficient and cost effective diamond deposition techniques for a wide set of applications. With respect to manufacturing cost, diamond deposition represents only a small portion of the total cost of most products. In cutting tools, for example, the diamond deposition cost is less than 30% of total product costs.

Conclusion

Whether it is for industrial applications or semiconductor manufacturing, diamond is clearly a preferable material that could enhance the performance of a device given its superior physical, electrical, and thermal properties. It is cost effective to grow diamond thin film on wafers synthetically using the HFCVD process, and it is a more economical method when compared to the MPCVD process. With its promising potential and continuous scientific development, diamond will soon be the next big name on the growing material list for semiconductor manufacturing.

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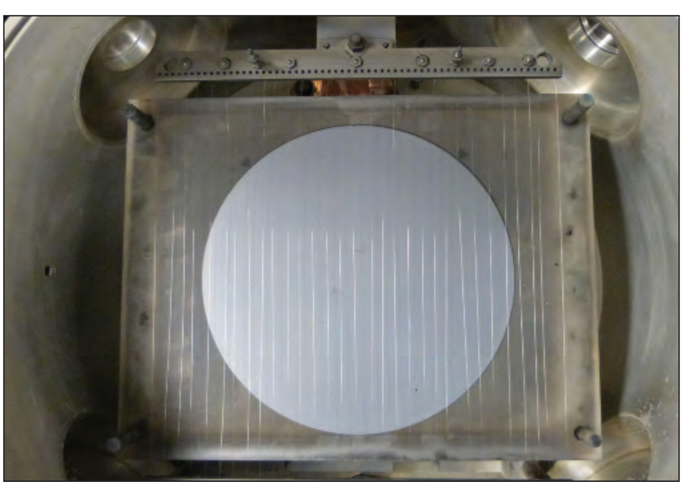

Figure 4: sp3's HFCVD Reactor: Tungsten Filament Array over 300mm Si substrate

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Rewriting the book on cleanroom insulation

Cleanrooms in pharmaceutical and semiconductor industries are adopting a new "slimmer" insulation that can reduce cleanroom size requirements and eliminate downtime costs.

In some respects, the insulation traditionally used in cleanroom manufacturing is like those1980s-era cellular phones: much too clunky and somewhat prone to performance problems. But then, of course, the conventional open-celled polyethylene foam insulation used in cleanrooms dates back to the 1980s or earlier.

The problems with those cumbersome insulation designs become very pronounced in the manufacturing cleanroom environment, where thousands of feet of fairly narrow reactor piping form a congested maze of plumbing, once the insulation has been installed. A half-inch line with three-inch insulation becomes a hefty 6-1/2 inches in diameter. When you consider the multitude of lines in the typical manufacturing cleanroom, it's no wonder the space gets crowded.

"One of the problems with the traditional melamine fiber or foam insulation design used in most cleanrooms is that it severely constricts the space needed by technicians to access the many points in the lines where instruments and controls are located," explains Mark Ginchereau, Vice President of Termar, Inc, a Ventura, CA-based maintenance contractor and insulation installer. Ginchereau adds that, until recently, the only alternative to having a cleanroom densely packed with open-celled or polyethylene insulated lines was to build a larger cleanroom and install longer

Above: Cleanrooms in pharmacutical and semiconductor industries are adopting a new "slimmer" insulation that can reduce cleanroom size requirements and eliminate downtime costs

lines so that there would be more "elbow room" for technicians - a highly expensive solution. He mentions other drawbacks to conventional insulation as well. Standard open-celled insulation sheds particulate when cut. This makes it necessary to provide additional protection from cross contamination and exposure. Yet, standard open-celled insulation can also shed particulate due to everyday contact from workers who need to gain access through tight spaces. Any uncontrolled particulate shedding can require extensive replacement and unscheduled cleanroom downtime.

Ginchereau also mentions that cleanrooms with melamine fiber-filled insulation in some chilled-water applications may be susceptible to condensates forming in fiber, due to chinks or even cracks resulting from impact damage or normal wear and tear from worker contact. Condensate formations can provide a breeding ground for biological growth, a highly undesirable intruder to any cleanroom environment. The condensate problem aside, cracks or other leaks in insulation are detrimental to maintaining exacting temperatures in cleanroom applications.

Another serious concern about the use of bulky traditional insulation is the possibility of serious worker injuries due to contact with superheated or frigid lines. Ginchereau explains that the greater the congestion of plumbing due to the use of insulation, the greater the potential for injury.

A new breed of insulation

One of the newer materials that has provided a breakthrough in cleanroom insulation is Kynar PVDF based, high-purity Zotek F foam. This specialty plastic material is a closed-cell foam that in a thickness of only ¼ inch offers chemical and heat resistance as well as other properties that are equivalent to 8 times that which conventional foam provides for clean room applications. In other words, ¼ inch of Kynar PVDF insulation is equivalent to 2 inches of open-celled insulation.

In recent years UFP Technologies (Georgetown, MA) a producer of innovative foam, plastic, and composite products, incorporated the new PVDF technology into an advanced tube and pipe

The T-Tubes system includes custom-moulded coverings for fitting and overlapping, self-adhering tape that provide a superior seal

insulation system specifically developed for process lines and equipment in cleanroom environments. "This product re-wrote the book for cleanroom insulation," says Ginchereau, who recently installed it at a large bio-pharmaceutical laboratory in California. Known by the brand name T-Tubes, this advanced insulation replaces the bulky traditional product with a wall thickness of only ¼ inch. "When you consider that instead of 6-inch-plus insulation on dozens of reactor lines, you are adding only ½ inch in diameter to a 1-inch or 2-inch pipe, you can save a lot of real estate," Ginchereau explains. "In the overall, the insulation is taking up only about 1/10th the space of traditional fiberglass."

This savings of space translates to many benefits, including reduced cleanroom size requirements. When you consider the space requirements of cleanrooms housing multiple reactors connected to thousands of feet of pipeline with "fat" insulation, the amount of space is dramatically reduced with the use of T-Tubes.

Also, with thinner pipe insulation, more space is available for technicians to access reactors and plumbing, resulting in improved worker productivity as well as less exposure to contact with super-heated or super-cooled lines. This PVDF-based product offers several other features that render important benefits to operators of manufacturing cleanrooms. The T-Tubes system includes custom-molded coverings for fittings, and an overlapping, self-adhering tape that provides a superior seal. This reduces the possibility of condensate, which can saturate ordinary foam insulation, creating leaks and enabling biological contamination.

"In a few instances during this project, we were able to collaborate with the T-Tubes engineers, to custom design components on-the fly," he says. "Within a couple of days I received a sample that we could test, and in most cases it was a good solution. It worked perfectly."

Unlike traditional open-cell insulation, this technology does not shed when cut. This means fewer impurity problems while cleanrooms are live, and no need for protective bags and hoods or downtime during installation. The PVDF-based product doesn't burn or smoke either, which is very important to pharmaceutical cleanrooms where millions of dollars worth of drugs could become tainted and lost if exposed to smoke. In fact, this is the only pipe insulation in the world that is compliant with Factory Mutual Approvals 4910 standard for cleanroom materials. It has also successfully completed FM's 4924 Pipe Chase Flammability Test and is rated for use by the semiconductor industry.

Ginchereau describes this PVDF-based insulation system as very easy to install. And ease of installation spells major savings of manpower. Traditional foam or polyurethane products coated with melamine require added installation time and efforts because there are two layers involved. The PVDF-based product is literally a single layer installation. In one case the labour savings on a 30,000-foot insulation project saved a UFPT customer over $800,000.

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Defect inspection challenges and solutions for ultra-thin SOI

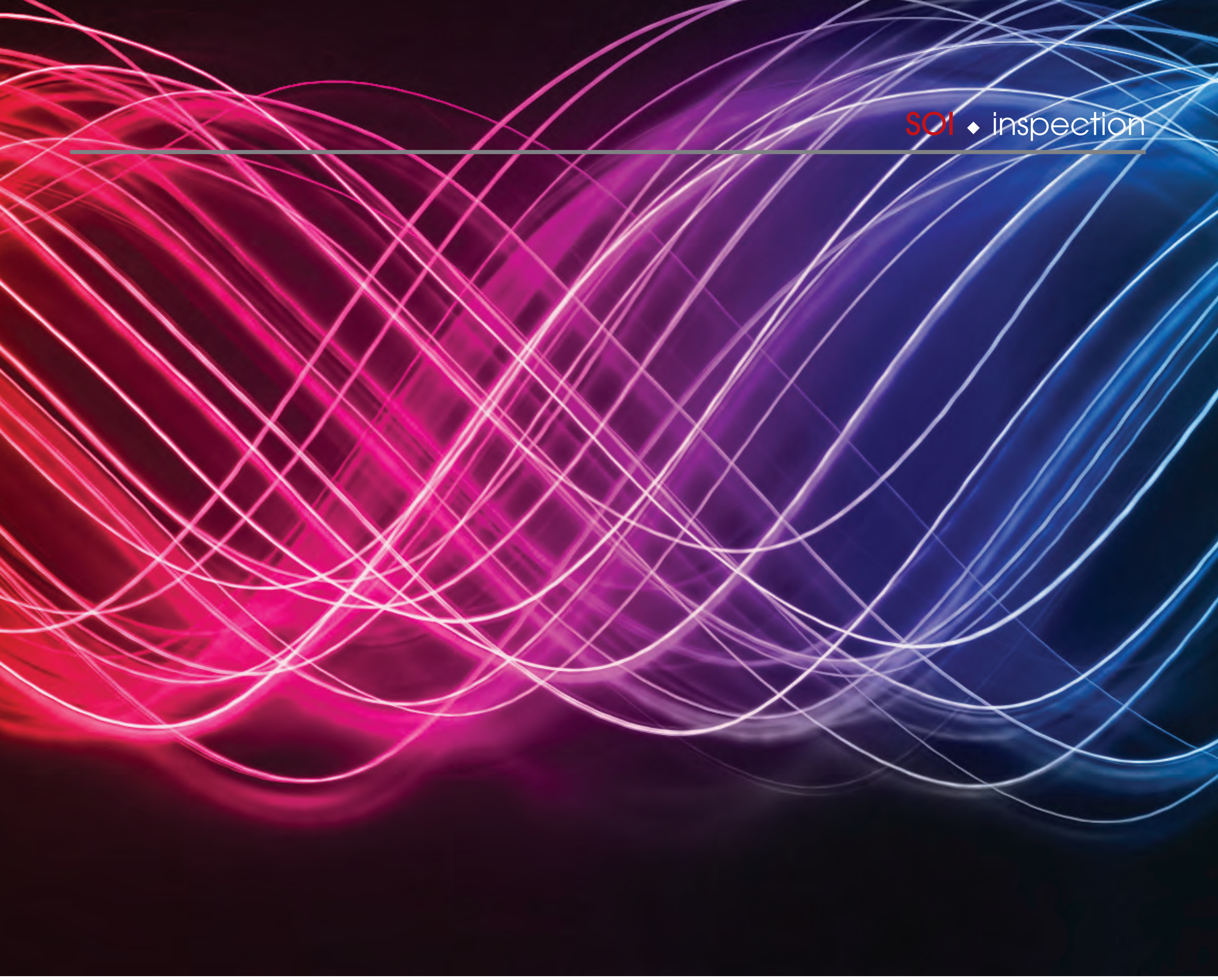
What are the challenges for ultra-thin SOI inspection using a laser light scattering system? Using an unpatterned DUV inspector, Roland Brun, Cecile Moulin, Walter Schwarzenbach SOITEC, and Gerhard Bast, Victor Aristov, Alexander Belyaev KLA-Tencor Corp consider the impact of reflectivity on haze and minimum threshold, the required sensitivity for 28nm and beyond SOI inspection.

Fully Depleted (FD) devices are an attractive option for the 28nm and beyond technology nodes. The combination of ultra-thin silicon-on-insulator (SOI) and buried oxide (BOX) films greatly improves short channel effects and threshold voltage (Vt) matching, while offering a low variation solution compared to alternatives [1]. Moreover, these devices enable the modulation of Vt using back bias [2]. The foundation of the Planar-FD technology is Ultra-Thin SOI (called UTBOX) substrates, for which the SOI can be thinned down to 10nm and BOX layers to 25nm [3]. A 12nm SOI / 25nm BOX substrate (UTBOX25, figure 1) is targeted for the 28nm technology node. Other substrate options with thinner BOX and/or a strained SOI layer are identified to support 20nm and beyond technologies and are merged in the so-called FD2D (Fully Depleted 2 Dimension) SOITEC product family [5]. The most widely used inspectors for SOI substrates utilize scattered laser light to detect wafer surface defects. For inspection using these systems, problems can occur when the top silicon thickness is thinner than the wavelength penetration depth: it results in interferences and multiple reflections, unique for each stack, making the layer difficult to analyze. We explore the challenges encountered when inspecting FD2D SOI products, and demonstrate how a new-generation inspector provided the solution.

In addition, advanced classification capabilities that combine haze information and defect type were used to classify typical SOI defects such as voids, stains and scratches, with results showing exceptional accuracy and purity. This information, collected at the inspection step, should help improve manufacturing yield without the need for additional defect review.

Current limitations

Absorption of light is driven by the n & k values from silicon, and for a given wavelength, there is a thickness below which silicon does not absorb light. When stacking a silicon layer on top of an oxide/silicon stack, interference will occur. This phenomenon will impact the light scattered by the



surface and by the defects, thereby requiring different inspection conditions for each substrate type.

At the top silicon thickness used in FD2D SOI, no laser-based inspector available on the market can prevent the interference effect. The interference artifact is evident in the haze data collected by the tool. Haze is the low frequency background scatter signal, proportional to the quantity of light scattered by the wafer surface. On thin films, optical properties of transparent films and surface characteristics like microroughness are the parameters that drive the amount of haze.

Figure 2a is a graph of the surface haze obtained with a UV laser-based inspector (KLA-Tencor's Surfscan SP2). Wafers with three different buried oxide film thicknesses were measured (represented by the three different curves on the graph). For each wafer, the top silicon layer was successively thinned from 40nm down to 7nm. The haze rises, then falls slowly as the top silicon layer thickness decreases below 35nm, and sharply increases below a top silicon layer thickness of 15nm. Below the critical thickness of 35nm, haze data will be sensitive to both top layer silicon thickness and surface roughness. UTBOX25 (12nm of silicon over 25nm of oxide) is the most unfavorable case, showing more than three times higher haze than product with 10nm of buried oxide.

UTBOX25 is the substrate selected for FDSOI introduction at the 28nm node because of device performance and integration reasons. Therefore, inspection capability needs to be adapted to provide the best performance on this specific thickness combination. In addition, the effects of the top silicon layer thickness on haze must be minimized so that the haze value can be used as a metric to evaluate the top silicon layer's surface roughness.

Models predict a higher absorption at shorter inspection wavelengths. This could result in a desired decrease in critical thickness – the top

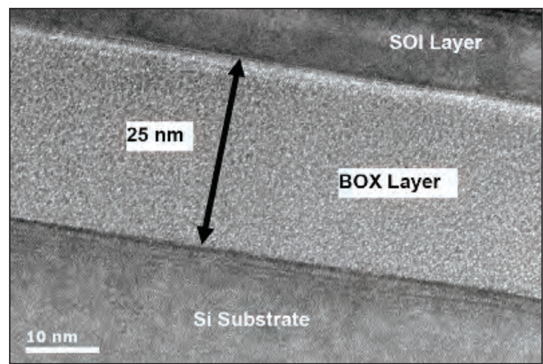


Figure 1: Transmission Electron Microscope (TEM) cross section of UTBOX25 substrate (4)

silicon layer thickness below which the haze value is sensitive to stack thickness. When we re-ran the experiment using a Surfscan SP3 system, which has a DUV wavelength, we observed that the haze variation arising from stack thickness was not an issue until the top silicon layer thickness reached 20nm. The change from UV to DUV wavelength on the inspector resulted in a decrease in critical thickness from 35nm to 20nm, enabling inspection of substrates that utilize thinner top silicon layers. When setting inspection thresholds, the ratio between the defect signal and the local noise needs to be higher than 2:1 in order to guarantee repeatable detection of defects. This local noise is proportional to the square root of the average haze; higher haze directly drives higher noise, limiting the minimum threshold and thereby, the sensitivity of the inspection.

In Figure 2b, the threshold achieved (defined using signal-to-noise ratio rule of 2:1) using a common inspection tool is plotted for different substrates showing different haze values (each point represents a different wafer). All these substrates show the same surface roughness (as measured by

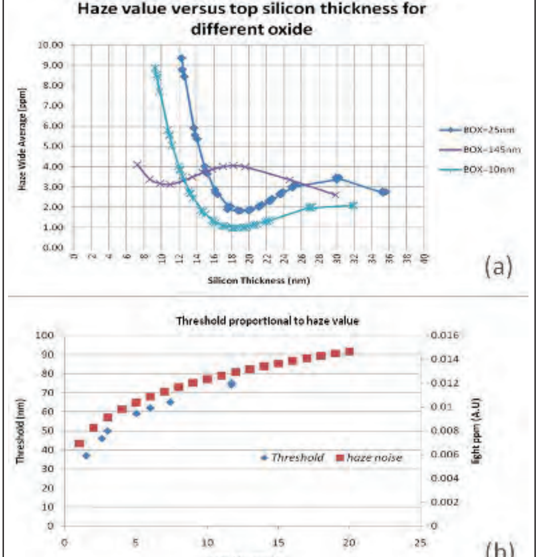


Figure 2: (a) Haze versus thickness of top silicon layer of FD UTSOI substrate, as measured by haze channel of Surfscan SP2; (b) Minimum inspection threshold versus haze value

Atomic Force Microscope (AFM)), so the average haze variation is directly related to the change in the top-level silicon thickness. We can see that the threshold curve and the haze noise curve follow a similar trend.

This experimental data demonstrates that we can set the minimum inspection threshold from the haze value for a given layer of substrate product. We are facing strong limitations due to the effect of the multiple reflections when top silicon layer thickness is below 20nm.

In order to meet defect sensitivity requirements, inspector characteristics play an important role. The scattering intensity of a defect (Pscattering) is strongly affected by the intensity (Iincident) and the wavelength (Ï) of the incident beam (equation 1). Other parameters are defect dependent: defect size (d) and refractive index for the defect's material composition (n).

$$P_{scattering} \; \alpha \; \frac{d^6 (n^2 - 1)^2}{\lambda^4} \; I_{incident}$$

Using the Surfscan SP3 system with its shorter wavelength, a strong improvement in minimum threshold (best defect sensitivity) achievable across various substrate products was demonstrated when compared to the longer wavelength Surfscan SP2. Figure 3 shows the sensitivity difference between the two tool generations while keeping throughput constant.

Moving to the latest generation inspection system helped SOITEC inspect its products at the best sensitivity possible. The level reached, however, is still not sufficient to comply with the 22nm node and beyond for FDSOI.

FD UTSOI inspection solution

In order to achieve the required inspection sensitivity for thin UTSOI substrates, we carried out studies to determine whether or not a special aperture could help. With laser-based inspectors, the direction of scattered light depends on the surface spatial frequencies. The reflections from defects and surface topography are composed of different spatial frequencies, and thus, will not scatter light in the same direction.

Apertures can be introduced to block scattering from surface components. The difficulty of this approach is ensuring that defects of interest do not scatter in directions blocked with the apertures. During the development of the new UTBOX25

optics, it was verified that defect signal was not lost by systematically comparing the defects detected using the aperture and without the aperture, using SEM review to identify the lost defect types. One specific defect type with morphology close to the surface scattering drove the need to try multiple apertures. In the end the best compromise between minimum haze and maximum capture rate for all defects of interest was found.

After systematic investigation, two apertures were selected: XFS_J, created for UTSOI products having top silicon layer thickness of 12nm and oxide thickness of 25nm; and XFS_G, created for products having thick top silicon layers. These apertures allowed a decrease in the minimum detection threshold from 74nm to 50nm for the 12nm-over-25nm product. This improvement was achieved on the stack having the most challenging reflectivity, and allows UTBOX25 to be inspected at the level required for the 22nm technology node. As part of future studies, we will explore how the aperture can be adapted to different stacks, for example, when oxide thickness is reduced from 25nm to 20nm. Initial work seems to confirm that as long as spatial frequencies do not change dramatically, apertures developed are still valid.

Advanced defect classification

Unpatterned wafer defect inspectors traditionally provide a limited amount of information about defect type. Defect classification algorithms are mainly based on spatial distribution of defects on the wafer on which signature recognition is performed (slipline, cluster or scratch). Specific defect type information is obtained by reviewing the wafer on a SEM defect review system.
With advanced substrate manufacturing, quick feedback is required to limit impact on manufacturing yield and improve learning. Timely feedback can be obtained using inspectors with integrated, automatic defect classification methods.

Voids defects appear at specific locations where the top silicon layer is not transferred. Differentiating voids from other big defects like particles that can be removed during a chemical clean is of strong interest for improving SOI quality. Analysis of inspection results shows that some defects,

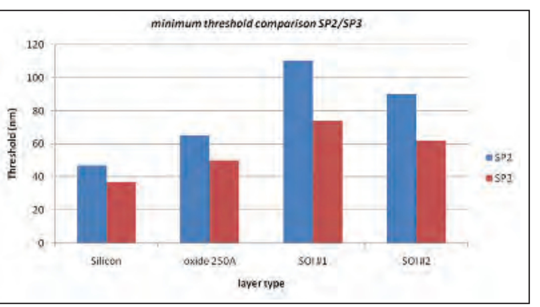


Figure 3: Minimum achievable threshold (best defect sensitivity) of Surfscan SP2 versus Surfscan SP3 on various substrate products

including voids, are detected in two different channels: as a cluster in the darkfield (DF) channel and as a bright spot in the haze channel. Since particles are only seen in DF, channel information can be used to separate voids from particles.
With previous-generation inspectors, individual defects can be detected in DF or haze channels, but no capability is available to merge the information from these two channels to identify a defect with a unique classification code. The Surfscan SP3 inspector offers integration of SURFmonitor, a subsystem capable of quantitative analysis of high resolution haze images and dual-channel processing. In addition, SURFmonitor introduces a flexible method of classification called "Rule Based Binning" (RBB).

The classification scheme shown in Figure 4 was used to separate voids from other defects. We were able to achieve excellent accuracy and purity results with this classification process: more than 90% of the voids can be classified correctly, with classification purity higher than 95%. The limiting

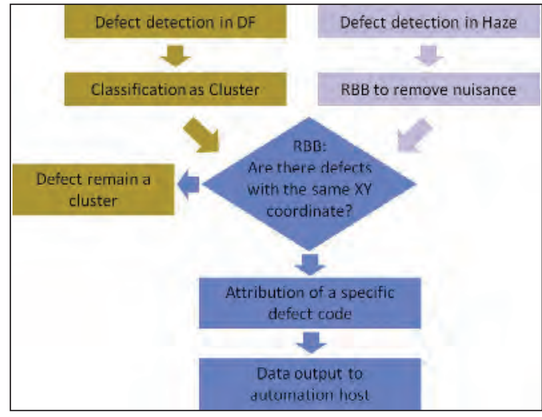


Figure 4: Schematic of the defect classification process, combining Rules Based Binning (RBB) and traditional classification methods

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factor is the size of the voids, which can prevent their detection in the haze channel.

Classification of residue was also tested. These defects have a unique signature – absorbing more light than the background, so that the defect appears dark. Standard algorithms are designed to detect "positive" variations, pixel to pixel. An algorithm available in SURFmonitor divides the wafer map into small grid squares, and haze pixel statistics (max, min, mean, standard deviation) are computed inside each square.

For squares with dark defects, we apply RBB to check the ratio of the minimum value to the median value, flagging bad squares and reporting them on the map. These results are available for automated process control.

These two examples, detection and classification of voids and residue, support our finding that the new inspector and its new capabilities have helped our process teams to better identify wafer defectivity. The new inspector has also helped us improve overall wafer quality by enabling sorting and grading based on additional parameters.

Conclusion

New products like UTBOX25 introduce new challenges for inspection of unpatterned substrates. We have been able to solve these challenges and achieve 50nm and below inspection capability. The use of a DUV unpatterned wafer inspector demonstrated that wavelength reduction and higher laser power are the key parameters required to reach lower defect detection thresholds. The development of a unique aperture was a key element to address challenges related to high reflectivity due to the low SOI thickness used on UTBOX25.

New information available from the different channels on this inspector, and the ability to merge this information with the integration of the SURFmonitor data, helped in the development of new and accurate classification schemes. A more detailed version of this manuscript originally appeared in 2012 23rd Annual Advanced Semiconductor Manufacturing Conference (ASMC) Proceedings.

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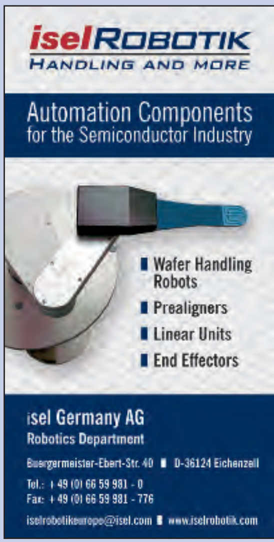

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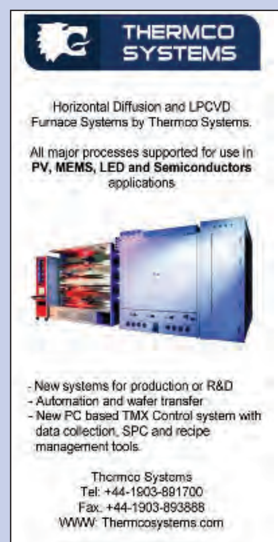

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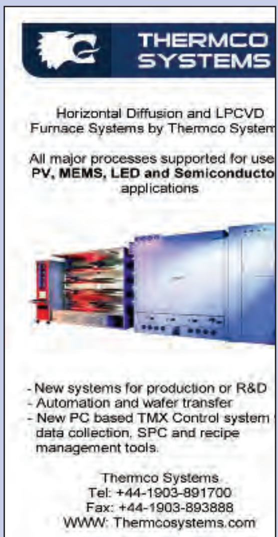

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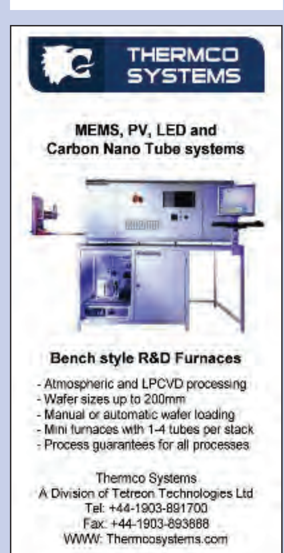

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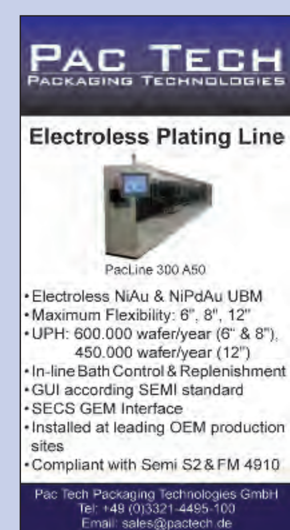

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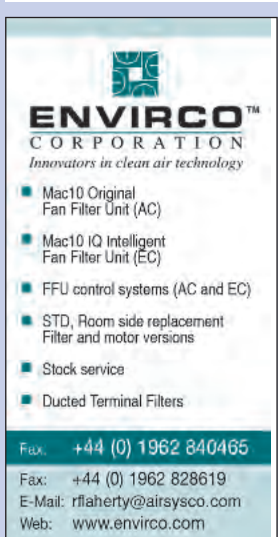

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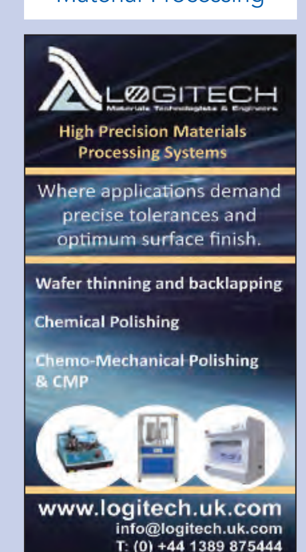

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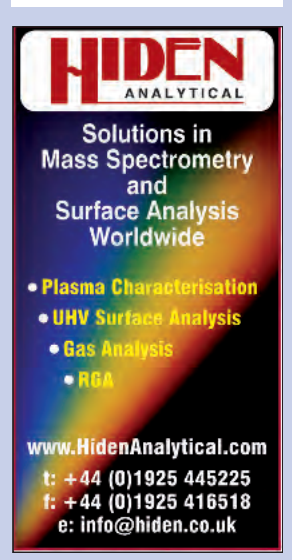

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