SILICON SEMICONDUCTOR

Connecting the Silicon Semiconductor Community

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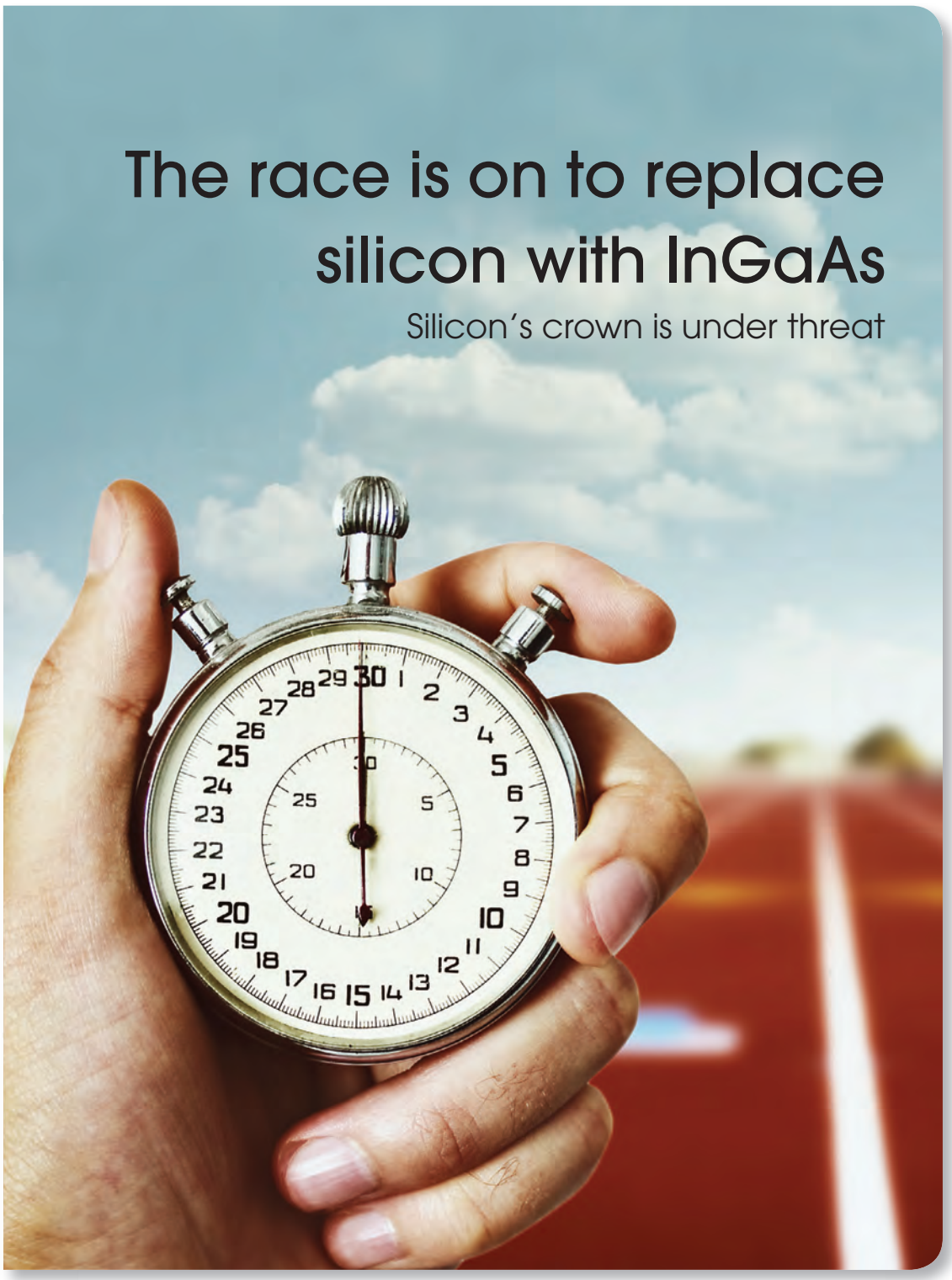
The race is on to replace silicon with InGaAs

Silicon's crown is under threat



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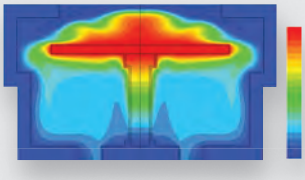

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executiveview

By Jay Shah, Worldwide Marketing Operations, Keithley Instruments, Inc.

Capable power semiconductor testing solutions required

Power semiconductors will become more important in 2013 given the burgeoning demand for efficient energy production and management. With fossil fuel prices remaining volatile, there is renewed focus on green energy sources like solar power and wind farms. The demand for efficiency management in motor drivers, lighting, and power supplies is rising, which in turn drives demand for power semiconductor devices. The developers of test and measurement instrumentation have a responsibility to help their customers meet the challenges that come with researching (universities/labs) and building (fabs) the next generation of power devices.

As power semiconductor manufacturers have continued to explore wide-bandgap alternatives to traditional silicon-based devices, testing these devices has become increasingly challenging. Higher voltage ratings, higher peak current ratings, and lower leakage specifications, made possible by the use of silicon carbide (SiC) and gallium nitride (GaN), are complicating design, characterization, and testing.

From a characterization and test perspective, SiC and GaN require far more powerful instrumentation than silicon-based technologies ever did. Devices based on these materials typically have much higher power density, smaller size, better high temperature performance, higher frequency response, lower leakage, and lower ON resistance than their silicon equivalents, all of which add up to greater operating efficiency. They also have far lower leakage than silicon, so at the same time as there is a need for sourcing higher voltages in testing; there is also a need for greater current measurement sensitivity.

For all their technical advantages, there are a variety of barriers to the mass adoption of SiC and GaN devices, the most significant of which is price. Making these devices more affordable will depend on manufacturers' ability to improve material quality and processing efficiency, both of which require intensive characterization and testing.

Solutions such as custom systems that attempt to integrate power sources with current measurement instruments simply can't provide the low current accuracy required to characterize next-generation devices and materials. As single-quadrant devices, power supplies cannot sink power; therefore, they require several seconds for the capacitance charge to bleed off after testing, which slows the test process, which is particularly problematic in production applications. In addition, in many cases, they lack the necessary power to support today's operating or characterization levels. Such custom-designed systems also typically require large test engineering teams to develop and maintain them.

Although commercial ATE systems have always been used for power semi production test, their cost, size, and lack of characterization and low current measurement capabilities make them impractical for R&D and QA/FA applications. Curve tracers were once the solution of choice for device characterization, but they are now largely unavailable. Fortunately, a number of T&M innovators, including Keithley Instruments, have begun applying the integrated sourcing and measurement capabilities of high-power SMU (source measure unit) instruments to this challenge.

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Volume 35 Issue 1 2013

Features

Magazine & Front Cover: Designed by Mitch Gaynor

THE GAME CHANGER
for Semiconductor Manufacturing

Introducing GF135, the revolutionary new PTI mass flow controller that tests accuracy in real time.

The new GF135 delivers revolutionary technology that will set new standards in semiconductor manufacturing. The GF135 provides smarter functionality with real-time, integrated rate-of-decay flow measurement. Patent-pending flow error detection technology and advanced diagnostics verify accuracy, check valve leak-by and monitor sensor drift – all without stopping your production.

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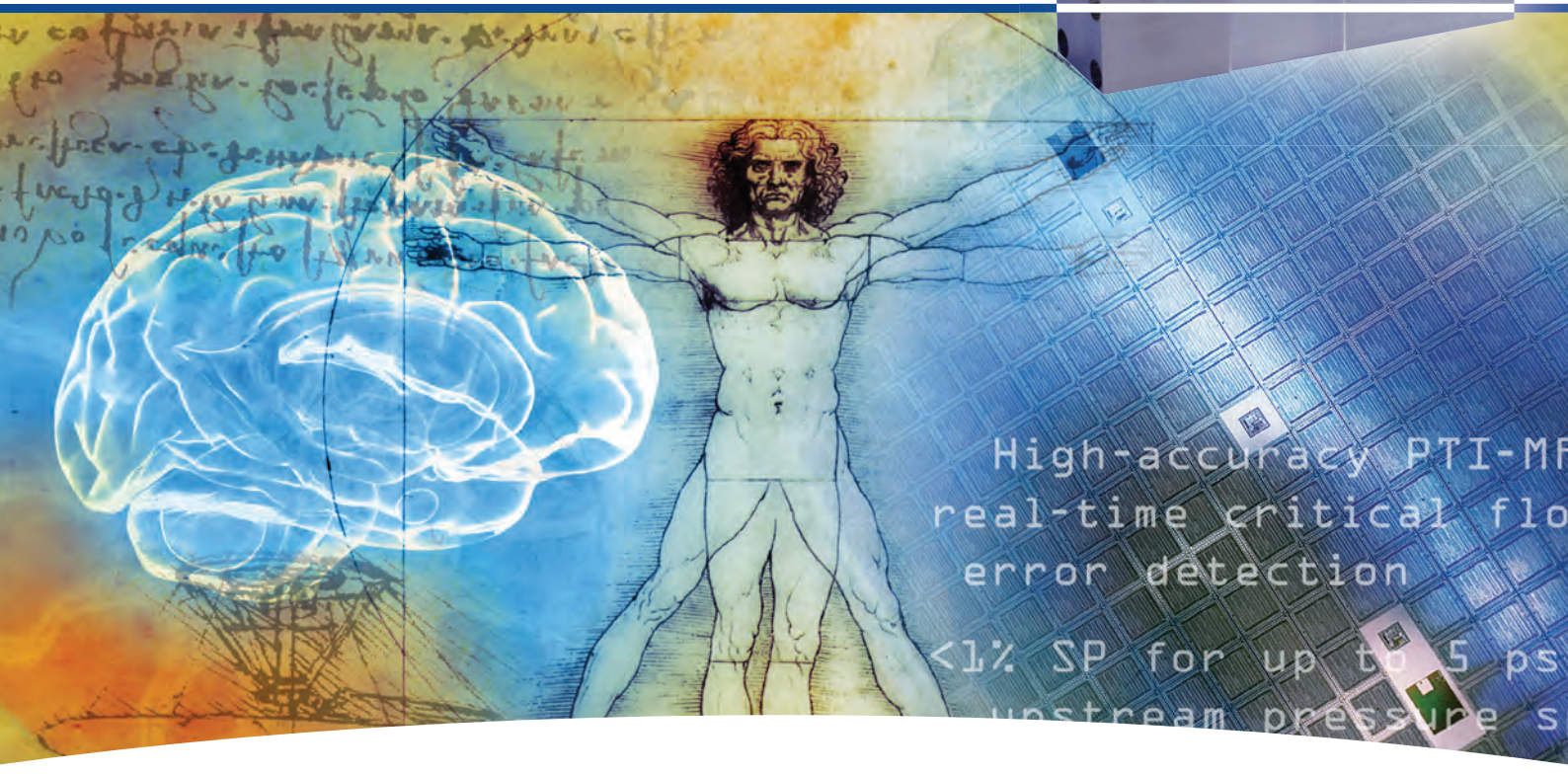

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EV Group ships 300mm wafer bonding system to China

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment, has announced that it has installed a fully automated 300-mm system from EVG's Gemini product family of integrated wafer bonding clusters to a leading Chinese semiconductor foundry. This customer will use the system for 3D IC integration and advanced packaging-two high-volume applications.

"This order from one of the largest Chinese foundries further cements EV Group's position as the market and technology leader in wafer bonding for leading-edge applications," stated Hermann Waltl, executive sales and customer support director at EV Group.

"China is an important market for us, and this order is further testament to our continued success in penetrating leading high-volume microelectronics manufacturers in China-from advanced substrate suppliers to light emitting diode (LED) and semiconductor device makers."

EVG won this order following a competitive bid with other leading process equipment suppliers.

Reasons cited by the customer for choosing EVG included high alignment accuracy, comprehensive process development and support, successful demo results in EVG cleanrooms, unmatched expertise in wafer bonding and other high-volume process solutions, and a technology roadmap that is strongly aligned with that of the customer.

Brewer Science upgrades production

LITHOGRAPHY INNOVATOR Brewer Science has installed a scale-up reactor to increase production of its CNTRENE C100 family of electronics-grade carbon nanotube (CNT) materials by tenfold. Such materials are used in chemical and biological sensors and nanotube-based non-volatile random access memory (RAM) device applications, which require extremely low levels of metal ion contaminants with concentration limits in parts per billion.

CNT technology is developing at a rapid rate and is quickly becoming a worthy rival to silicon in memory applications. "Small-scale reaction equipment can only take manufacturing so far with respect to quality and delivery time. This new scale-up reactor will provide the capability to complete weeks of reactions in three days while producing materials that meet stringent microelectronics specifications," says Stephen Gibbons, Director of Technology of Brewer Science's Carbon Electronics Centre.

Jim Lamb, Director of Business Development for the Carbon Electronics Centre adds, ''With increasing customer usage and the move toward commercial adoption in devices, we needed to implement our third round of scale-up to support market demand. Growth of our CNTRENE C100 family of products is driven by their use in nanotube-based non-volatile random access memory devices, a universal CNT memory structure developed by Nantero, Inc., sold under the name NRAM, which could replace embedded memory, DRAM, SRAM, and flash memory devices."

"This structure allows flexible placement of memory in the device stack and can be stacked for vertically placed memory cells. NRAM devices provide other key benefits including robustness, 3-nanosecond write speeds, low operating power, radiation-hardened memory cells, and the ability to perform at high operating temperatures," continues Lamb.

imec announce launch of integrated silicon photonics platform

NANOELECTRONICS research centre imec has announced the launch of its fully integrated silicon photonics platform through a cost-sharing Multi-Project Wafer (MPW) service via ePIXfab. The platform enables cost-effective R&D of silicon photonic ICs for high-performance optical transceivers (25Gb/s and beyond) and optical sensing and life science applications. The offered integrated components include low-loss waveguides, efficient grating couplers, high-speed silicon electro-optic modulators and high-speed germanium waveguide photo-detectors.

Since 2007, imec and its associated laboratory at Ghent University have been offering a platform for passive silicon photonic components via ePIXfab, for R&D under shared cost conditions. Now, imec extends its silicon photonics offering, using a standard130nm CMOS toolset, with active components such as high-speed optical modulators and integrated germanium photo-detectors.

"imec's Silicon Photonics platform provides robust performance and solutions to integrated photonics products in medical diagnostics, telecom and datacom industries. Companies can benefit from our silicon photonics capability through established standard cells, or explore the functionality of their own designs in MPW," stated Philippe Absil, program director at imec. "This Silicon Photonics MPW offer provides a cost-efficient solution, with state-of-the-art performance, design flexibility and superior CD and thickness control". The first run opens for registration with tape-in on 9th of Oct 2013 and first devices will be out in May 2014. Support, registration and design kit access will be organized by Europractice IC service, in collaboration with world-wide MPW partners.

AGC and nMode collaborate

TOKYO-BASED Asahi Glass Co., Ltd. (AGC) and nMode Solutions Inc. of Tucson, Arizona, have invested $2.1 million to co found a subsidiary business, Triton Micro Technologies. The new company will develop innovative via-fill technology for interposers, enabling next-generation semiconductor packaging solutions using ultra-thin glass.

Headquartered in Tucson with a manufacturing facility planned in California, the subsidiary will combine nMode's interposer technology for electrically connecting semiconductor devices with AGC's materials technology and micro-hole drilling techniques to produce 2.5-dimensional (2.5D) and three-dimensional (3D) through-glass-via (TGV) interposers needed for advanced semiconductor devices. To achieve the next generation in high-density semiconductor packaging, interposer technologies are needed to form the high number of electrical connections between a silicon chip and a printed circuit board. Interposers allow high packaging integration in the smallest available form factors.

Triton will manufacture ultra-thin glass interposers using a high-efficiency continuous process that lowers costs and helps to commercialize the widespread use of interposers. The company will draw upon nMode's intellectual property and AGC's carrier-glass technology and via-hole drilling methodologies to fabricate its interposers. Triton will then apply its proprietary technology to fill the high-aspect-ratio via holes with a copper paste that has the same coefficient of thermal expansion as glass. This reduces the potentially damaging effects of thermal stress during manufacturing and long-term use. Triton's process creates high-quality electrodes within the interposer to provide the electrical interface capable of accommodating advanced, high-density ICs. Triton's interposers are compatible with wafers having diameters from 100mm to 300mm and thicknesses of 0.7mm and below. The company can also design and manufacture customised solutions for unique applications.

"The global semiconductor industry recognises that silicon is approaching its performance limits as an interposer material, but the need remains to create smaller, more efficient packages for today's and tomorrow's high-performance ICs," comments Tim Mobley, CEO at Triton. "Our technology allows us to achieve known-good-die testing at the highest levels of packaging integration, faster cycle times and the lowest cost per unit in the market."

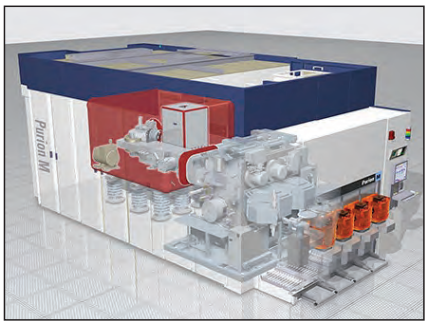
Axcelis wins order from major memory & flash device maker

AXCELIS TECHNOLOGIES has announced that its Purion M medium current implanter has been selected by one of the world's leading chipmakers. The system will be used to develop and manufacture next generation memory and FLASH devices.

Bill Bintz, executive vice president of product development, engineering and marketing comments, "We're very excited about this, new win and the growth opportunities the system provides Axcelis."

He continues, "The Purion M was selected after an extensive evaluation focused on implant accuracy, purity and repeatability; key requirements to achieve the customer's most challenging demands for emerging new device architectures. The system's innovative angle control system provides significant advantages over the competition in this critical area."

"In addition, the Purion M effectively demonstrated its ability to maintain the industry's highest levels of productivity,



beyond the traditional operating range for medium current implanters, resulting in unmatched levels of manufacturing flexibility and capital efficiency, significantly reducing their implant bay operating costs," Blintz adds.

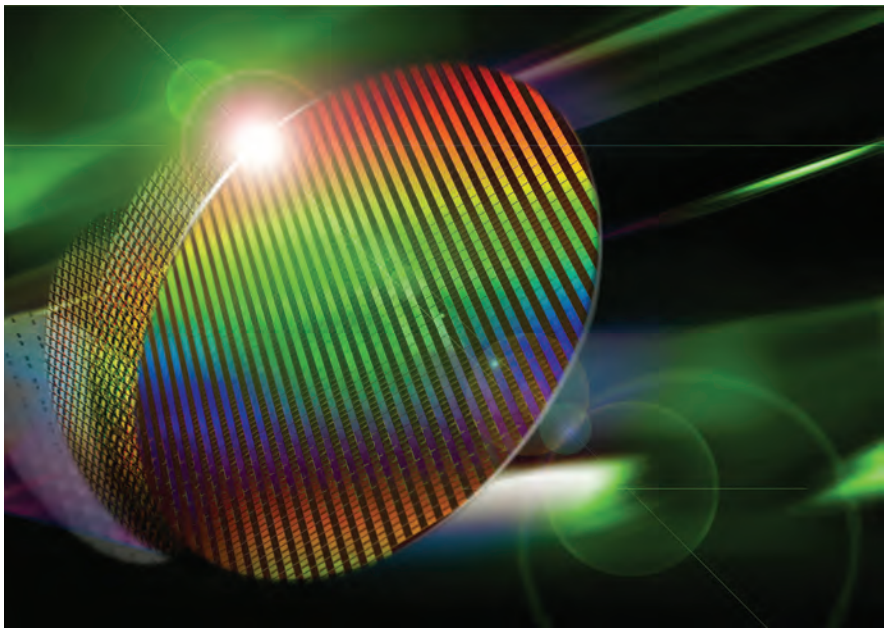
Infineon's 300mm CoolMOS silicon chips now shipping globally

INFINEON TECHNOLOGIES AG says it has achieved a major breakthrough in the manufacturing of power semiconductors on 300 millimetre thin wafers.

In February, the company received the first customer go-aheads for products of the CoolMOS family produced by the 300 millimetre (mm) line at the Villach (Austria) site. The production process based on the new technology has completed qualification from start to finish and customers have given the go-ahead.

Infineon believes its revolutionary silicon CoolMOS power family sets new standards in the field of energy efficiency. Using high voltage MOSFETs, CoolMOS offers a significant reduction of conduction and switching losses and enables high power density and efficiency for superior power conversion systems.

CoolMOS products are application specific and optimised for consumer products, renewable energy, telecom power supply, adapters and many others. "Infineon put its faith in this manufacturing technology very early on and continued to invest even in economically difficult times. We think and act with foresight and are now reaping the benefits: The qualification of our entire 300mm line represents a veritable leap ahead of the competition," says Reinhard Ploss, CEO of Infineon Technologies AG. "300mm thin-wafer manufacturing for power semiconductors will enable us, with the corresponding demand, to seize the opportunities that the market offers."



Infineon says it is the first and only company worldwide to produce power semiconductors on 300mm thin wafers. Thanks to their larger diameter compared to standard 200mm wafers, two-and-a-half times as many chips can be made from each one.

The next step is for the present manufacturing concept for CoolMOS products, qualified from start to finish, with the front-end site Villach and assembly of the thin chips at the back-end site Malacca (Malaysia), to be expanded to the front-end site Dresden. Here the focus is on high-volume production in a fully automated 300mm line.

The basis for the processes required and the manufacturing technology is currently being developed in research projects in Dresden. The technology transfer to Dresden is running on schedule and qualification of the first CoolMOS products will be completed in March.

Shortly, in Villach more power semiconductor technologies will be transferred to the 300mm line and produced. The development of the next power technology generation will focus on 300 instead of 200mm technology.

With these solutions customers can reduce development times and put new, more powerful products on the market more quickly. 300mm thin-wafer technology guarantees that in the future Infineon will continue to be able to produce sufficient quantities at competitive costs.

Martin L. Edelman jumps on board at AMD

AMD has appointed Martin Edelman to the company's board of directors as a representative of West Coast Hitech L.P., an affiliate of Mubadala Development Company and AMD's largest stockholder. Edelman's appointment follows the resignation of Waleed al Muhairi after four years of service on the AMD Board.

Edelman currently serves as Of Counsel, Real Estate Department for the law firm Paul, Hastings, Janofsky & Walker LLP, a New York City law firm where he is responsible for real estate transactions as well as corporate mergers and acquisitions. He serves as a member of the board of directors at several private and public companies, including Avis Budget Group, Ashford Hospitality Trust and Capital Trust.

Edelman is also a senior advisor to Mubadala Development Company, a strategic investment and development company headquartered in Abu Dhabi. He brings an extensive legal background to the board of directors, with more than 40 years of experience in the legal profession.

Oxford Instruments awarded patent for plasma film deposition

OXFORD INSTRUMENTS says plasma enhanced deposition processes typically decrease the deposition temperature, compared to chemical vapour deposition processes driven by heat alone. Using a high density plasma source offers a significant decrease in processing temperature for the same quality material, and can deposit silicon dioxide layers below 1000C. This development opens up this style of plasma processing to a new range of substrate materials including polymers.

The European patent EP1889946B1 cites Thomas, Griffiths and Cooke as inventors, and discloses a method of optimising uniformity over larger areas using a plasma transmission plate.

This technique has been used in more than 25 tools shipped by Oxford Instruments since the patent application was filed. Oxford Instruments Plasma Technology's CTO Mike Cooke says, "The grant of this patent covering high density plasma assisted thin film deposition is part of a broad platform of intellectual property rights which continue to be developed by our company. Oxford Instruments now has multiple patents, and we believe that this intellectual property reinforces our influential position in the plasma technology field."

Oxford Instruments Plasma Technology are leaders in the manufacture of flexible, configurable process tools and leading-edge processes for the precise, controllable and repeatable engineering of micro- and nano-structures.

The company's systems provide process solutions for the etching of nanometre sized features, nanolayer deposition and the controlled growth of nanostructures.

Silicon threatens to muscle in on III-V devices

DEVICE REVENUES for gallium arsenide (GaAs), a compound semiconductor, grew slightly from 2011 to 2012. The primary drivers for the increase were in handset growth, particularly smartphones. Strategy Analytics maintains that although Skyworks and WIN Semiconductors remain at the top of this market, the silicon threat is looming.

According to the market research firm's "GaAs Device Industry Closes up in 2012" report, the silicon device market has seen recent developments which could compete with GaAs device revenues in the immediate future.

In the short-term, revenue in the GaAs device market is expected to exceed the historical average. But in the longer term, it is expected that recent developments in CMOS multi-mode, multi-band handset PAs from Qualcomm and others will pose a significant threat to the GaAs device market.

"Smartphones continue to grow faster than the overall handset market. This growth, coupled with more bands and increased GaAs device content remains the single biggest driver for revenue growth in the GaAs device market," notes Eric Higham, Director of the Strategy Analytics GaAs and Compound Semiconductor Technologies Service (GaAs). "In the short-term, we anticipate this combination of factors will drive GaAs device revenue growth above historical averages."

Asif Anwar, Director, Strategy Analytics Strategic Technologies Practice, adds, "Strong growth in the last quarter of 2012 provides a good starting point for the GaAs industry in 2013.

However, recent announcements about CMOS multi-mode, multi-band PAs and envelope tracking will threaten the GaAs device market and these developments will be monitored closely."

Watlow acquires Semiconductor Tooling Services

WATLOW, a designer and manufacturer of complete thermal systems, has acquired San Jose, California-based Semiconductor Tooling Services, Inc. (STS) as a wholly-owned subsidiary. The terms of the agreement will not be disclosed.

STS' primary offering is the development and application of precision bonds between critical components in a process tool assembly. These bonds are responsible for adhesion, as well as to provide specific heat conducting properties.

The acquisition will allow Watlow and STS to provide its shared customers a greater product offering. and increased capabilities.

"We are pleased that STS is now a part of Watlow because it helps us provide even more value to our semiconductor customers. One of Watlow's goals is to improve our domain knowledge and elevate our technical expertise in our strategic markets," says Tom LaMantia, Watlow's president.

"We fully support this acquisition," adds John Lilleland, owner of STS. "We have worked with Watlow for many years and have developed a mutual respect. Our complementary capabilities and mutual strengths will allow us to provide industry-leading solutions for our customers." Watlow designs and man ufactures industrial heaters, temperature sensors, controllers and supporting software as well as assemblies - all of the components of a thermal system.

The company partners with its customers to optimize thermal performance, decrease design time and improve efficiency of their products and applications. Watlow brings its experience to numerous industries, including semiconductor processing, and environmental chambers.

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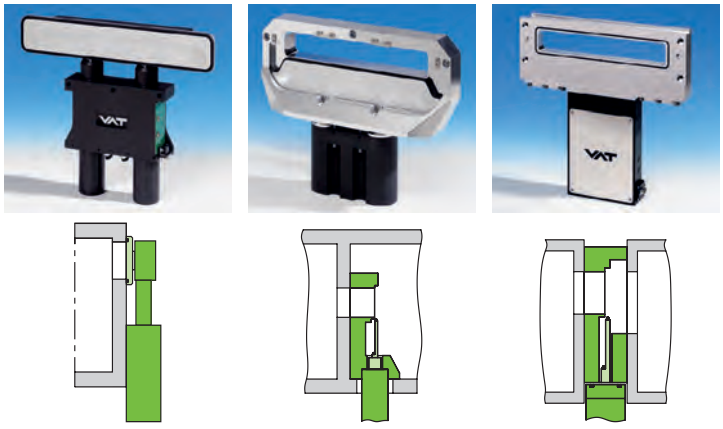

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The race is on to replace silicon with InGaAs

Silicon's crown is under threat. The semiconductor's days as the king of microchips for computers and smart devices could be numbered, thanks to the development of the smallest transistor ever to be built from III-V semiconductor indium gallium arsenide (InGaAs).

RESEARCHERS AT PURDUE UNIVERSITY have announced a new type of transistor shaped like a Christmas tree, where each transistor contains three tiny nanowires made of InGaAs.

So III-Vs replacing silicon seems to be a hot research topic, with InGaAs being one of the main contenders. Now scientists at MIT's Microsystems Technology Laboratories have also created a compound transistor, which performs well despite being just 22nm length. This also makes it a promising candidate to eventually replace silicon in computing devices, says co-developer Jesús del Alamo, the Donner Professor of Science in MIT's Department of Electrical Engineering and Computer Science (EECS), who built the transistor with EECS graduate student Jianqian Lin and Dimitri Antoniadis, the Ray and Maria Stata Professor of Electrical Engineering.

To keep pace with our demand for ever-faster and smarter computing devices, the size of transistors is continually shrinking, allowing increasing numbers of them to be squeezed onto microchips. "The more transistors you can pack on a chip, the more powerful the chip is going to be, and the more functions the chip is going to perform," del Alamo says.

But as silicon transistors are reduced to the nanometre scale, the amount of current that can be produced by the devices is also shrinking, limiting their speed of operation. This has led to fears that Moore's Law - the prediction by Intel founder Gordon Moore that the number of transistors on microchips will double every two years - could be about to come to an end, del Alamo says.

To keep Moore's Law alive, researchers have for some time been investigating alternatives to silicon, which could potentially produce a larger current even when operating at these smaller scales. One such material is the compound InGaAs, which is already used in fibre-optic communication and radar technologies, and is known to have extremely good electrical properties, del Alamo says.

But despite recent advances in treating the material to allow it to be formed into a transistor in a similar way to silicon, nobody has yet been able to produce devices small enough to be

packed in ever-greater numbers into tomorrow's microchips. Now del Alamo, Antoniadis and Lin have shown it is possible to build a nanometre-sized metal-oxide semiconductor field-effect transistor (MOSFET) - the type most commonly used in logic applications such as microprocessors - using the material. "We have shown that you can make extremely small indium gallium arsenide MOSFETs with excellent logic characteristics, which promises to take Moore's Law beyond the reach of silicon," del Alamo says.

Transistors consist of three electrodes: the gate, the source and the drain, with the gate controlling the flow of electrons between the other two. Since space in these tiny transistors is so tight, the three electrodes must be placed in extremely close proximity to each other, a level of precision that would be impossible for even sophisticated tools to achieve. Instead, the team allows the gate to "self-align" itself between the other two electrodes.

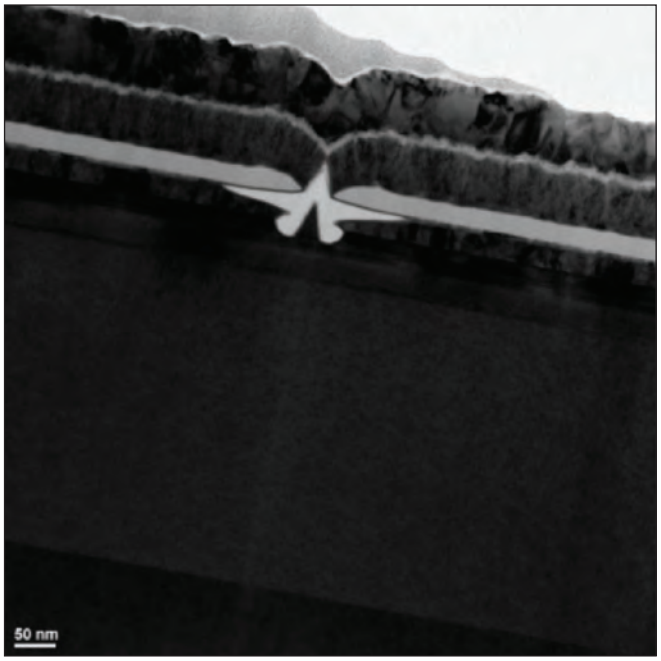
The researchers first grow a thin layer of the material using molecular beam epitaxy (MBE), a process widely used in the semiconductor industry in which evaporated atoms of indium, gallium and arsenic react with each other within a vacuum to form a single-crystal compound. The team then deposits a layer of molybdenum as the source and drain contact metal. They then "draw" an extremely fine pattern onto this substrate using a focused beam of electrons - another well-established fabrication technique known as electron beam lithography.

Unwanted areas of material are then etched away and the gate oxide is deposited onto the tiny gap. Finally, evaporated molybdenum is fired at the surface, where it forms the gate, tightly squeezed between the two other electrodes, del Alamo says. "Through a combination of etching and deposition we can get the gate nestled [between the electrodes] with tiny gaps around it," he says.

The image above, courtesy of the researchers, shows a cross-section transmission electron micrograph of the fabricated transistor. The central inverted V is the gate. The two molybdenum contacts on either side are the source and drain of the transistor. The channel is the InGaAs light colour layer under the source, drain, and gate.

Although many of the techniques applied by the MIT teamare already used in silicon fabrication, they have only rarely been used to make compound semiconductor transistors. This is partly because in applications such as fibre-optic communication, space is less of an issue.

"But when you are talking about integrating billions of tiny transistors onto a chip, then we need to completely reformulate the fabrication technology of compound semiconductor transistors to look much more like that of silicon transistors," del Alamo says.



> "Although many of the techniques applied by the MIT team are already used in silicon fabrication, they have only rarely been used to make compound semiconductor transistors. This is partly because in applications such as fibre-optic communication, space is less of an issue"

The team presented its work at the International Electron Devices Meeting in San Francisco. Their next step will be to work on further improving the electrical performance, and hence the speed of the transistor by eliminating unwanted resistance within the device.

Once they have achieved this, they will attempt to further shrink the device, with the ultimate aim of reducing the size of their transistor to below 10 nm in gate length.

Matthias Passlack, of Taiwanese semiconductor manufacturer TSMC, says del Alamo's work has been a milestone in semiconductor research. "He and his team have experimentally proven that indium arsenide channels outperform silicon at small-device dimensions," he says. "This pioneering work has stimulated and facilitated the development of CMOS-compatible, III-V-based-technology research and development worldwide."

The research was funded by DARPA and the Semiconductor Research Corporation.

Chips steer light in the right direction

"Record-setting" 'optical phased arrays' could lead to better laser rangefinders, smaller medical-imaging devices and even holographic TVs.

IF YOU WANT TO CREATE A MOVING LIGHT SOURCE, you have several possibilities. One is to mount a light emitter in some kind of mechanical housing - the approach used in, say, theatrical spotlights, which stagehands swivel and tilt to track performers. Another possibility is to create an array of light emitters and vary their "phase" - the alignment of the light waves they produce. The out-of-phase light waves interfere with one another, reinforcing each other in some directions but annihilating each other in others. The result is a light source that doesn't move, but can project a beam in any direction.

Such "phased arrays" have been around for more than a century, used most commonly in radar transmitters, which can be as much as 100 feet tall.

Now researchers from MIT's Research Laboratory of Electronics (RLE) have demonstrated a 4,096-emitter array that fits on a single silicon chip. Chips that can steer beams of light could enable a wide range of applications, including cheaper, more efficient, and smaller laser rangefinders; medical-imaging devices that can be threaded through tiny blood vessels; and even holographic televisions that emit different information when seen from different viewing angles. In a paper published this week in the journal Nature, the MIT team, led by Michael Watts, an associate professor of electrical engineering, report on two new chips. Both chips take in laser light and re-emit it via tiny antennas etched into the chip surface.

Calculated incoherence

A wave of light can be thought of as a sequence of crests and troughs, just like those of an ocean wave. Laser light is coherent, meaning that the waves composing it are in phase. In other words, their troughs and crests are perfectly aligned. The antennas in the RLE researchers' chips knock that coherent light slightly out of phase, producing interference patterns. In the 4,096-antenna chip, a 64-by-64 grid of antennas, the phase shifts are pre-calculated to produce rows of images of the MIT logo, as shown in the figure at the top of this story.

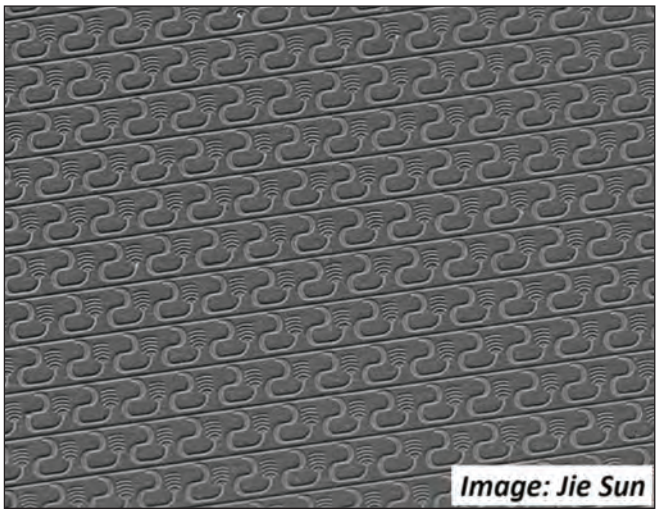
The antennas are not simply turned off and on in a pattern that traces the logo, as the pixels in a black-and-white monitor would be. All of the antennas emit light, and if you were close enough to them (and had infrared vision), you would see a regular array of pinpricks of light. Seen from more than a few millimetres away, however, the interference of the antennas' phase-shifted beams produces a more intricate image.

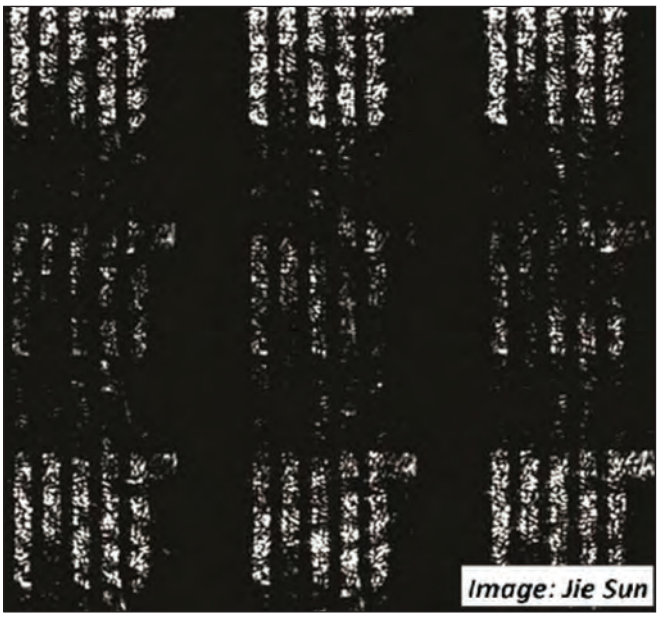
In the other chip, which has an eight-by-eight grid of antennas, the phase shift produced by the antennas is tuneable, so the chip can steer light in arbitrary directions. In both chips, the design of the antenna is the same; in principle, the researchers could have built tuning elements into the antennas of the larger chip. But "there would be too many wires coming off the chip," Watts says. "Four thousand wires is more than Jie (the lead author of the paper), wanted to solder up."

Indeed, Watts explains, wiring limitations meant that even the smaller chip is tuneable only a row or column at a time. But that's enough to produce some interesting interference patterns that demonstrate that the tuning elements are working. The large chip, too, largely constitutes a proof of principle, Watts says. "It's kind of amazing that this actually worked," he says. "It's really nanometre precision of the phase, and you're talking about a fairly large chip."

Precision engineering

In both chips, laser light is conducted across the chip by silicon ridges known as "waveguides." Drawing light from the optical signal attenuates it, so antennas close to the laser have to draw less light than those farther away. If the calculation of either the attenuation of the signal or the variation in the antennas' design is incorrect, the light emitted by the antennas could vary too much to be useful.





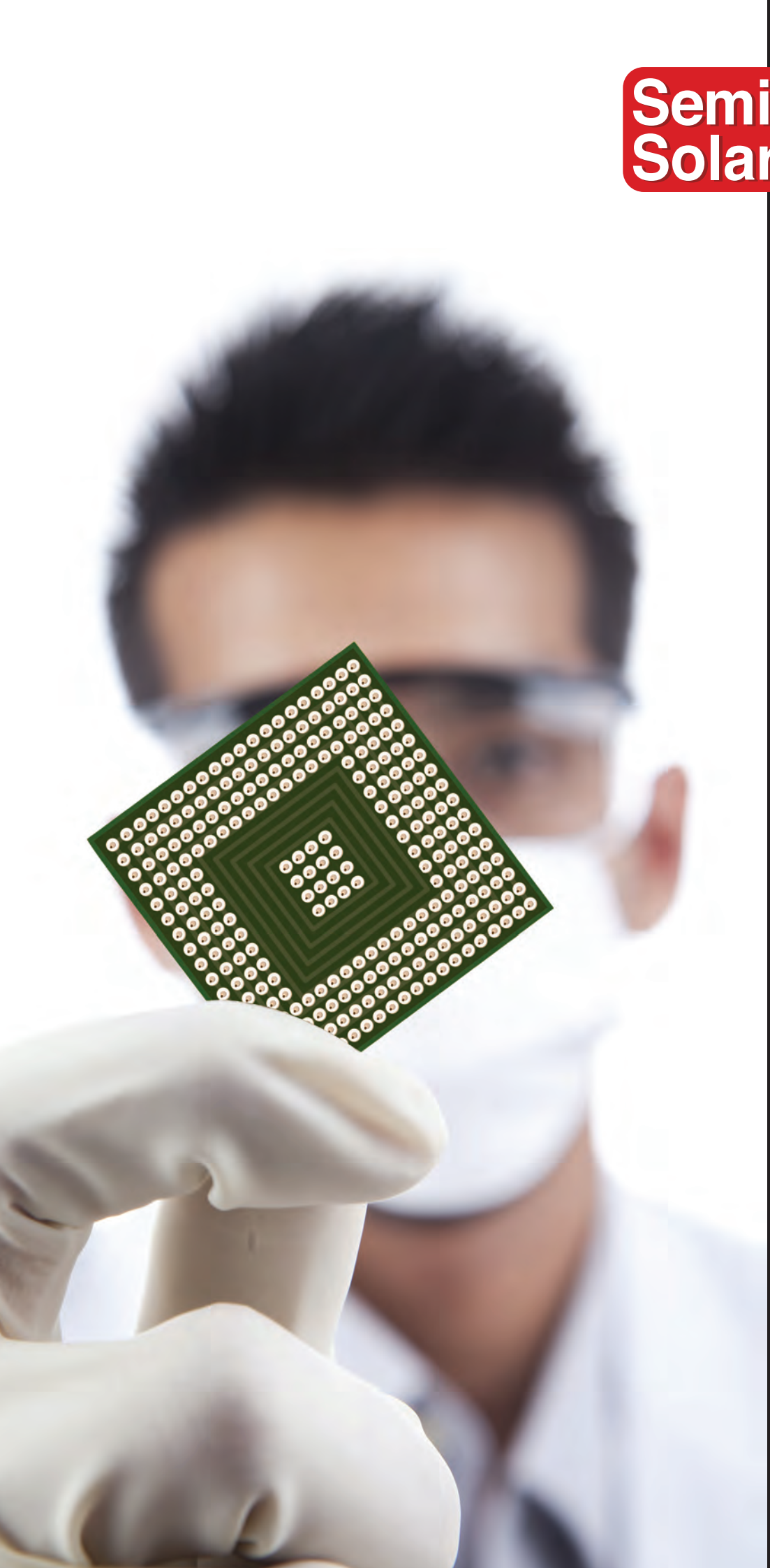
Because of the interference of the phase-shifted light beams emitted by the antennas, images of the MIT logo appear to hover above the surface of the chip

Both chips represent the state of the art in their respective classes. No two-dimensional tuneable phased array has previously been built on a chip, and the largest previous non-tuneable (or "passive") array had only 16 antennas. Nonetheless, "I think we can go to much, much larger arrays," Watts says. "It's now very believable that we could make a 3-D holographic display."

"I think it's one of the first clearly competitive applications where photonics wins," says Michal Lipson, an associate professor of electrical and computer engineering at Cornell University and head of the Cornell Nanophotonics Group.

"Within the photonics community, Lipson says, most work is geared toward "the promise that if photonics is embedded in electronic systems, it's going to really improve things. Here, (the MIT team) has developed a complete system. It's not a small component: This system is ready to go. So it's very convincing."

Lipson adds that the tuning limitation of the MIT researchers' prototype chips is no reason to doubt the practicality of the design. "It's just physically hard to come up with a very high number of contacts that are external," she says. "Now, if you were to integrate everything so that it's all on silicon, there shouldn't be any problem to integrate those contacts."
More details of this work are published in the paper, " Large-scale nanophotonic phased array," by Jie Sun et al in Nature, 493, 195–199, (10 January 2013). DOI: 10.1038/nature11727.



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Germanium p-type transistor boasts highest ever 'carrier mobility'

Almost all computer chips use two types of transistors: p-type (positive), and n-type (negative). Improving the performance of the chip as a whole requires parallel improvements in both types.

AT THE IEEE's International Electron Devices Meeting (IEDM) in December 2012, researchers from MIT's Microsystems Technology Laboratories (MTL) presented a p-type transistor which they claim has the highest "carrier mobility" yet measured. By that standard, the device is twice as fast as previous experimental p-type transistors and almost four times as fast as the best commercial p-type transistors.
Like other experimental high-performance transistors, the new device derives its speed from its use of a material other than silicon.

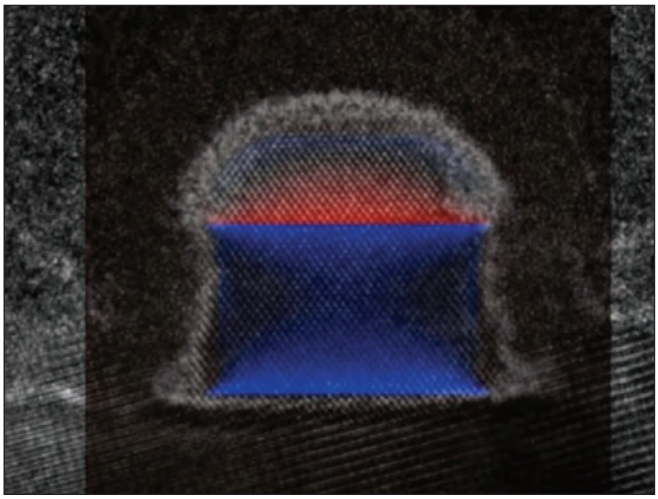
The researchers in this case, used germanium. Alloys of germanium are already found in commercial chips, so germanium transistors could be easier to integrate into existing chip-manufacturing processes than transistors made from more exotic materials. The new transistor also features what's called a trigate design, which could solve some of the problems that plague computer circuits at extremely small sizes (and which Intel has already introduced in its most advanced chip lines). For all these reasons, the new device offers a tantalising path forward for the microchip industry - one that could help sustain the rapid increases in computing power, known as Moore's Law, that consumers have come to expect.

Pluses and minuses

A transistor is a switch that in one position allows charged particles to flow through it ; in the other position, it doesn't. In an n-type transistor, the electrons, which are the charge carriers, produce an ordinary electrical current. In a p-type transistor, the charge carriers are positively charged "holes." A p-type semiconductor doesn't have enough electrons to balance out the positive charges of its atoms; as electrons hop back and forth between atoms, trying futilely to keep them electrically balanced, holes flow through the semiconductor, in much the way waves propagate across water molecules that locally move back and forth by very small distances.

"Carrier mobility" measures how quickly charge carriers - whether positive or negative - move in the presence of an electric field. Increased mobility can translate into either faster transistor switching speeds, at a fixed voltage, or lower voltage for the same switching speed.

For decades, each logic element in a computer chip has consisted of complementary n-type and p-type transistors whose clever arrangement drastically reduces the chip's power consumption. According to the MIT scientists, in general, it's easier to improve carrier mobility in n-type transistors; the MTL researchers' new device demonstrates that p-type transistors should be able to keep up.



Handling the strain

The researchers from MIT and the University of British Columbia achieved their "record-setting" hole mobility by "straining" the germanium in their transistor. This forced its atoms closer together than they'd ordinarily find comfortable. To do that, they grew the germanium on top of several different layers of silicon and a silicon-germanium composite. The germanium atoms naturally try to line up with the atoms of the layers beneath them, which compresses them together. The micrograph at the top of this story, shows an experimental transistor. Blue highlighting indicates areas of "strain," where germanium atoms have been forced closer together than they find comfortable. One of the reasons for the transistor's record-setting performance is that the strain has been relaxed in the lateral direction.

"It's kind of a unique set of material structures that we had to do, and that was actually fabricated here, in the MTL," professor of electrical engineering and computer science at MIT, Hoyt says. "That's what enables us to explore these materials at the limits. You can't buy them at this point."

"These high-strain layers want to break," Teherani, lead author of a paper describing the work, adds. "We're particularly successful at growing these high-strain layers and keeping them strained without defects."

Indeed, Hoyt is one of the pioneers of strained-silicon transistors, a technology found today in almost all commercial computer chips. At last year's IEDM, she and Eugene Fitzgerald, the Flemings-SMA Professor of Materials Science and Engineering at MIT, received the IEEE's Andrew S. Grove

> As transistors have grown smaller, their gates have shrunk, too. But at smaller sizes, that type of lockstep miniaturisation won't work: Gates will become too small to reliably switch transistors off

Award for outstanding contributions to solid-state devices and technology. The award announcement cited Hoyt's "groundbreaking contributions involving strained-silicon semiconductor materials."

Gatekeeping

Another crucial aspect of the new transistor is its trigate design. If a transistor is a switch, throwing the switch means applying a charge to the transistor's "gate." In a conventional transistor, the gate sits on top of the "channel," through which the charge carriers flow. As transistors have grown smaller, their gates have shrunk, too. But at smaller sizes, that type of lockstep miniaturisation won't work: Gates will become too small to reliably switch transistors off. In the trigate design, the channels rise above the surface of the chip, like boxcars sitting in a train yard. To increase its surface area, the gate is wrapped around the channel's three exposed sides - hence the term "trigate."

By demonstrating that they can achieve high hole mobility in trigate transistors, Hoyt and her team have also shown that their approach will remain useful in the chips of the future."The germanium part helps in increasing the drive current, and the trigate part helps in reducing the leakage in the off state," says Krishna Saraswat, the Rickey/Nielsen Professor in Engineering at Stanford University, who was not involved in this research. "So a combination of those two just gives you an ideal transistor for the next generation."

Saraswat believes that the semiconductor industry is already planning a move toward germanium circuits. "The choice is to scale the silicon transistor without any performance gains - just get to higher packing density - or get higher packing density as well as better performance," he says. "And it's fairly clear that the industry will go for high-strain germanium."

The MIT researchers' work was supported by the U.S. Defence Advanced Research Projects Agency and the Semiconductor Research Corporation.

RESEARCHERS FROM THE UNIVERSITY OF WÜRZBURG have modified SiC crystals to exhibit new and surprising properties. This makes them interesting with regard to the design of high-performance computers or data transmission. SiC crystals consist of a regular lattice formed by silicon and carbon atoms. At present, these semiconductors are extensively used in micro and optoelectronics. They are particularly suited for use in high temperature applications in power semiconductors. Now physicists from Saint Petersburg and the University of Würzburg have succeeded in manipulating SiC in a way so it can be used in novel, super-fast quantum computers.

Improving on diamond in supercomputers

By creating a silicon vacancy defect in silicon carbide, scientists have generated additional energy levels in the so band gap for use in supercomputers.

A defect in the crystal

"We have removed a silicon atom from the crystal lattice, thus creating a silicon vacancy defect," Georgy Astakhov says, explaining the method applied by the physicists. Astakhov is a research fellow at the Department for Experimental Physics VI of the University of Würzburg.

To the researchers' surprise, this crystallographic defect gives the material interesting new properties. In order for the semiconductor to emit light, its electrons must be raised to a higher energy level by means of energy-rich light, for instance. The silicon vacancy defect leads to the generation of additional energy levels in the so-called band gap.

Stepladder for electrons

Vladimir Dyakonov, chair of the Department for Experimental Physics VI, explains the process with a simple analogy; "In a regular, perfectly structured silicon carbide crystal, the electron must overcome a big hurdle with only one step. This requires a lot of energy. Due to the defect, the electron is provided with a ladder. It can clear the hurdle with two steps, requiring less energy."

When the electrons "fall back" from the higher energy level to the lower one, this type of silicon carbide emits infrared rather than ultraviolet light. According to Astakhov, such light is better suited to transfer information in an optical fibre. "This requires wavelengths in the infrared range," the physicist says.

Application in a quantum computer

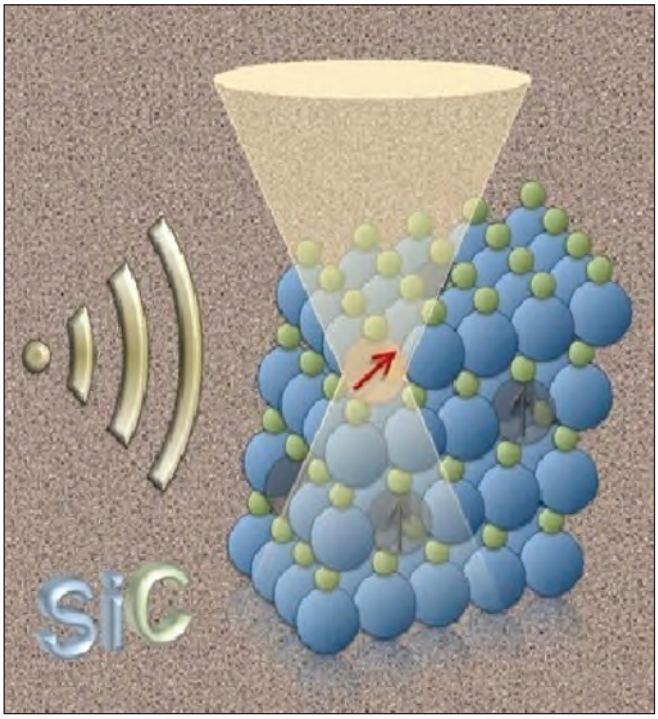
The modified SiC is particularly promising for another application – as a semiconductor and storage medium in novel quantum computers. "Since their invention, transistors have shrunk from several tens of micrometers to approximately 10nm, i.e. about one thousandth of their original size," Astakhov notes. If the miniaturisation continues at this speed, transistors would have to consist of one individual atom in ten years' time. At this scale, however, special physical laws apply, namely the laws of quantum mechanics. The computers of today process information with the binary system (0/1): Electricity flows or it does not. A quantum computer processes information in the form of so-called qubits.

These can be based on the spin of electrons. In simplified terms, the spin represents their angular momentum. It can point in several directions, for which reason it can represent much more information than a classical bit.

The information lies in the defect

"In this field of research, a lot of attention has been paid to the colour centres in diamond, which exhibit defects that are similar to those of our silicon carbide," says Astakhov.

Their qubits can be easily addressed, changed or read even at room temperature. However, the diamond production technology is not nearly as advanced as that of silicon semiconductors. "For this reason, there is a worldwide hunt for quantum systems that combine the advantages of diamond and silicon within one material," Astakhov explains.



The Würzburg physicists believe SiC with a vacancy defect to be a suitable candidate for this purpose. “The missing atom also has as a consequence that the crystal lattice lacks an electron, which in turn is equivalent to the spin that can be used as information carrier in a quantum computer,” Dyakonov explains. What’s more, the SiC technology is fairly well developed. LEDs, transistors, micro-electro-mechanical components or sensors made from this material are already on the market.

Exposing the material to light and radio waves

The Würzburg physicists conducted their experiments in collaboration with researchers from Saint Petersburg. By “hitting” the silicon crystals simultaneously with light and radio waves, they were able to manipulate the spins in a targeted way, enabling them to store and retrieve information at will.

What the physicists are particularly enthusiastic about is the fact that the silicon vacancy qubits in a densely packed crystal behave almost like atoms with well-defined, very sharp optical resonances. “This is very unusual,” Astakhov adds.

“This is a new research field where experimental data of other study groups are still scarce at the moment. However, the reviewers looked favourably on our experiments and immediately recommended our manuscript for publication. We are very curious to know how the scientific community will react to our study,” Astakhov reveals. The first reaction has already materialised; Astakhov has been invited to present his results at the Quantum Science Symposium in Cambridge.

Spin quantum computers not only require the ability to process information, but also to store the information for as long as possible. This is still a problem at this point, since the stray field of adjacent nuclei can gradually erase the information stored in the defects.

Therefore, the researchers from Würzburg and Saint Petersburg plan as a next step to produce SiC crystals that are formed from a silicon isotope without a magnetic moment. “We know that spin-free isotopes of silicon and carbon atoms exist,” concludes Astakhov. A SiC crystal exclusively consisting of such isotopes should therefore be capable of storing the information over a long period of time.

Further details of this work have been published in the paper, “Resonant addressing and manipulation of silicon vacancy qubits in silicon carbide”, by D. Riedel, et al in Physical Review Letters, 109, 226402 (2012). DOI:10.1103/PhysRevLett.109.226402

Si-InP sandwich chips combine the best of both worlds

The integration of a silicon chip with an indium phosphide chip could hold the key to faster and more powerful terahertz chips for high resolution and mobile applications.

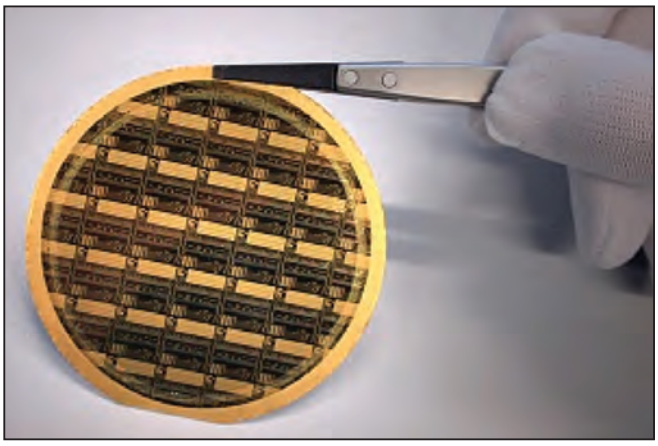
TWO LEIBNIZ INSTITUTES have broken new technological ground; they have successfully combined their - up to now separate technologies. Due to their high performance, the novel chips developed within the HiTeK project promise to open the door to new applications.

Wolfgang Heinrich and Bernd Tillack are convinced of holding the key to faster and more powerful terahertz chips. The two scientists and their teams come from the Berlin-based Ferdinand-Braun-Institut (FBH) and from the IHP-Leibniz-Institut für innovative Mikroelektronik in Frankfurt/Oder. FBH is one of the leading institutes in developing III-V semiconductors, while IHP is specialised in silicon-based systems and circuits. Both Leibniz institutes joined forces within the HiTeK project to combine the advantages of silicon-based CMOS (Complementary Metal Oxide Semiconductor) circuits from the IHP with those of indium phosphide (InP) circuits from the FBH.

The partners have taken an important step within the project by successfully integrating both circuits onto a semiconductor wafer, with experimental results demonstrating their high performance. With the integration on one chip, new ambitious applications in the THz range are within reach. These include high-resolution imaging systems for medical and security technology as well as ultra-broadband mobile communication applications.

For such applications, high output powers along with faster computer processors are needed, offering enhanced computer operation per second. In order to achieve this, circuits on the chips need to become smaller - the key reason which boosts miniaturisation in the semiconductor industry. If the frequency range around 100 gigahertz (GHz) and beyond is to be covered, however, the breakdown voltage in the CMOS switching circuits decreases significantly. As a consequence, the available output power of the chips declines. This implies that the capability of generating sufficiently strong signals to establish a radio link and to detect material defects becomes insufficient.
To find a solution to this problem, IHP conducted research on bipolar CMOS based on SiGe, enhancing the breakdown voltages at high speed compared to pure CMOS. By combining a standard CMOS circuit with a second InP circuit promised further improvement.

Both circuits are realised in a “sandwich-like” structure and lie one on top of another. Where the traditional silicon-based CMOS technology reaches its limits, this novel material



combination delivers the desired properties; high output powers at high frequencies. The sandwich chips enable a high level of production and integration of CMOS circuits - particularly regarding the fact that 95 percent of all digital and analogue-digital circuits are based on this technology.

“It was particularly challenging to make both technologies compatible at the interfaces”, underlines Wolfgang Heinrich from the FBH. To achieve this, the whole development environment of both processes as, for example, the software for the circuit layout had to be merged in a first step. Subsequently, both layers had to be dimensioned so that they reach the essential good transmission properties for frequencies around 200 GHz. Precision work was also highly demanded to adjust the circuits precisely to each other with an accuracy of less than 10μm.

Heinrich is especially proud of the friction-less cooperation, “We managed to align both technology worlds so smoothly that the circuits deliver fully the specified high-frequency performance. This also demonstrates what added value can be created by bundling the competencies of two institutes like IHP and FBH”. The next steps are to further stabilise the process and to optimise the circuits. A follow-up project has already been granted. In this way, the potential of the hybrid chips will be exploited fully to reach the borders of what is feasible . This will set the stage for the novel sandwich circuits to be integrated in sophisticated applications in the near future.

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SEMI: Flat Fab equipment in 2013 to rocket 24% in 2014

Fab equipment spending for Front End facilities is expected to hover around flat in 2013 and with an increase of 24 percent in 2014 as shown in Table 1 below. The SEMI World Fab Forecast, published at the end of February, reveals little has changed from the projections published at the end of November when the report was last issued. The report tracks equipment spending at over 180 facilities in 2013.

At the time of the November 2012 publication, semiconductor companies had not announced their capex plans for 2013, so fab spending predictions were based on extensive modelling. More than 262 updates have been made since the last publication and are based on announced spending plans, including major changes for TSMC, Samsung, Intel, SK Hynix, Globalfoundries, UMC, and for some Japanese facilities and LED facilities.

Despite these adjustments, the overall forecast for equipment spending for 2013 has remained about the same. Depending on macro-economic risk factors, possible scenarios project a range of -3 percent to +3 percent change rate for fab equipment spending in 2013; in other words, hovering around flat. Global chip sales have started on a bright note in 2013, as the SIA reports that three-month average for global chip sales for January increased 3.8 percent above January 2012. It also appears that the average sentiment for revenue growth is in the upper single digits in 2013, about 7 percent Y-o-Y, compared to about -3 percent in 2012.

Though the overall outlook has improved some, fewer players in the market can afford the rising costs for R&D and upgrading facilities as the amount of money needed to upgrade facilities at the leading edge technologies is immense.

The World Fab Forecast report shows increases for fab equipment spending, varying by technology node. Fab equipment spending for 17nm and below is expected to kick off in 2013 and increase by a factor of 2.4 to about $25 billion from 2013 to 2014. Fab construction spending is now expected to increase more than previously predicted.

Back in November 2012, a change of 3.7 percent Y-o-Y was forecasted; now, 6.7 percent growth is forecasted with construction spending to reach almost US$6 billion. In 2014, however, construction project spending is expected to contract by about 18 percent. Construction spending is led, far and away, by TSMC, with seven different projects for the year; followed by Intel with projects including D1X module 2, Fab 42 and some other sites. Fab construction spending in China will increase by a factor of four because of Samsung's Mega fab in Xian. Since the 2008/2009 economic downturn, the industry has been adding capacity more slowly than ever, as reflected in SEMI's World Fab Forecast data. Capacity is now forecasted to expand by just 2.8 percent for this year, and to improve to 5.4 percent growth in 2014.

Excluding 2009, the years 2012 and 2013 show the lowest growth rate for new capacity over that past ten years. The World Fab Forecast gives detailed capacity information by industry segment and by individual company and fab. Dedicated foundries are expected to add 10 to 11 percent more capacity in 2013 and 2014. Flash will add 4 percent new capacity in 2013 and about 10 percent in 2014. New capacity expansions for the System LSI segment should drop from the double digits of previous years to single digits in 2013 and 2014.

SEMI believes that there will be a pent-up demand for some product types because capacity additions have been cut to a minimum level while chip demand keeps increasing. Capacity additions and equipment spending are expected to pick up in the second half of 2013. In 2014, at least 5 percent in new capacity will be added and fab equipment spending will increase by 24 percent.

Fab Equipment Spending: Front End

	2010	2011	2012	2013	2014
Equipment spending in US$ Million	33,530	38,710	31,802	31,668	39,266
Change %	-	15.4%	-17.18%	-0.4%	24%

including used and in-house

Source: SEMI World Fab Forcast reports (February 2013)

IC suppliers to monopolise 300mm wafer space

SEMICONDUCTOR INDUSTRY capital spending is becoming more concentrated with a greater percentage of spending coming from a shrinking number of companies. As a result, IC industry capacity is also becoming more concentrated and this trend is especially prevalent in 300mm wafer technology. The table lists the 300mm installed capacity leaders for 2012 and IC Insights' forecast for 2013.

The list was compiled and included in IC Insights' updated report titled, "Global Wafer Capacity 2013 - Detailed Analysis and Forecast of the IC Industry's Wafer Fab Capacity".

Samsung was by far the leader in 2012 having about 61 percent more 300mm capacity than second-place SK Hynix. Intel was the only other company that held a double-digit share of 300mm capacity at the end of 2012.

Assuming Micron is successful in acquiring Elpida in the first half of 2013, the combined 300mm wafer capacity of the two companies will make the merged company the second-largest holder of 300mm capacity in the world behind Samsung.

Of the top 10 companies on the list, half are primarily memory suppliers, two are pure-play foundries, and one company, Intel, is focused on MPUs. Samsung is expected to maintain its lead in installed capacity through 2017, with aggressive capital spending plans seen over the past few years continuing over the next five years.

However, in terms of growth rate, IC Insights expects the largest increase in 300mm capacity to come from the pure-play foundries - TSMC, GlobalFoundries, UMC, and SMIC. In total, IC Insights expects these four companies to more than double their collective 300mm wafer starts per month by 2017.

IC Insights believes that the companies listed in the table above will represent essentially all the advanced 300mm IC production and capacity in the future. The market research firm also anticipates that the top seven or eight companies - Samsung, "Micron-Elpida," TSMC, SK Hynix, Intel, Toshiba/SanDisk, and GlobalFoundries - can be considered an "elite" group that is just about guaranteed to be a driving force in 300mm capacity additions.

The remaining companies are likely to participate in future 300mm capacity expansion, but all have varying degrees of risk associated with fully realising their long-term 300mm IC production capacity goals.

Meanwhile, there is still much uncertainty as to when the industry will make the next wafer-size transition - from 300mm to 450mm - and how much it will cost to do so, but momentum continues to build and the transition can now be considered certain to happen.

IC manufacturers have yet to fully optimise the high-volume manufacturing cost structure for the 300mm wafer size. However, the potential per-die cost savings that the larger wafer can provide is enough of a motivating factor to make the transition happen.

300mm Wafer Capacity Leaders Forecast (Installed Monthly Capacity in 300 mm Wafers x 1000)

2013F Rank	Company	2012 Installed Capacity (K w/m)	2012 % of WW Total	2013F installed Capacity (K w/m)	2013 F% of WW Total
1	Samsung	675	18.8%	717	18.4%
2	Micron-Elpida*	512	14.4%	536	13.8%
3	SK Hynix	420	11.7%	450	11.6%
4	Intel	388	10.8%	441	11.3%
5	TSMC	356	9.9%	414	10.7%
6	Toshiba/SanDisk	320	8.9%	320	8.2%
7	Global Foundries	125	3.5%	150	3.9%
8	Nanya	125	3.5	127	3.3%
9	UMC	97	2.7%	115	3.0%
10	Powerchip**	125	3.5%	90	2.3%
11	TI	51	1.4%	57	1.5%
12	SMIC	51	1.4%	57	1.5%
-	Top 12	3245	90.4%	3477	89.5%
-	Others	346	9.6%	410	10.5%
-	Total	3591	100%	3887	100%

*Assumes Micron completes acquisition of Elpida in 1H13
** Assumes Powerchip either sells or tears down B3 Fab as it plans to do
Source: Companies, IC Insights

Cu pillar and micro-bumping flip-chip platforms invigorates the market

OVER THE NEXT FIVE YEARS, wafer growth is expected to triple for the Flip-Chip platform, which will reach over 40 million of 12''eq wspy by 2018.

This is according to Yole Développement's "Flip Chip Market and Technology Trends" report, which updates the business status of the Flip-Chip market including data for TIM, underfills, substrates and Flip-Chip bonders.

Despite its high 19 percent CAGR, Flip-chip is not new - in fact, it was first introduced by IBM over 30 years ago. As such, it would be easy to consider it an old, uninteresting, mature technology but this is far from true. Instead, Flip-Chip is keeping up with the times and developing new bumping solutions to serve the most advanced technologies, like 3DIC and 2.5D.

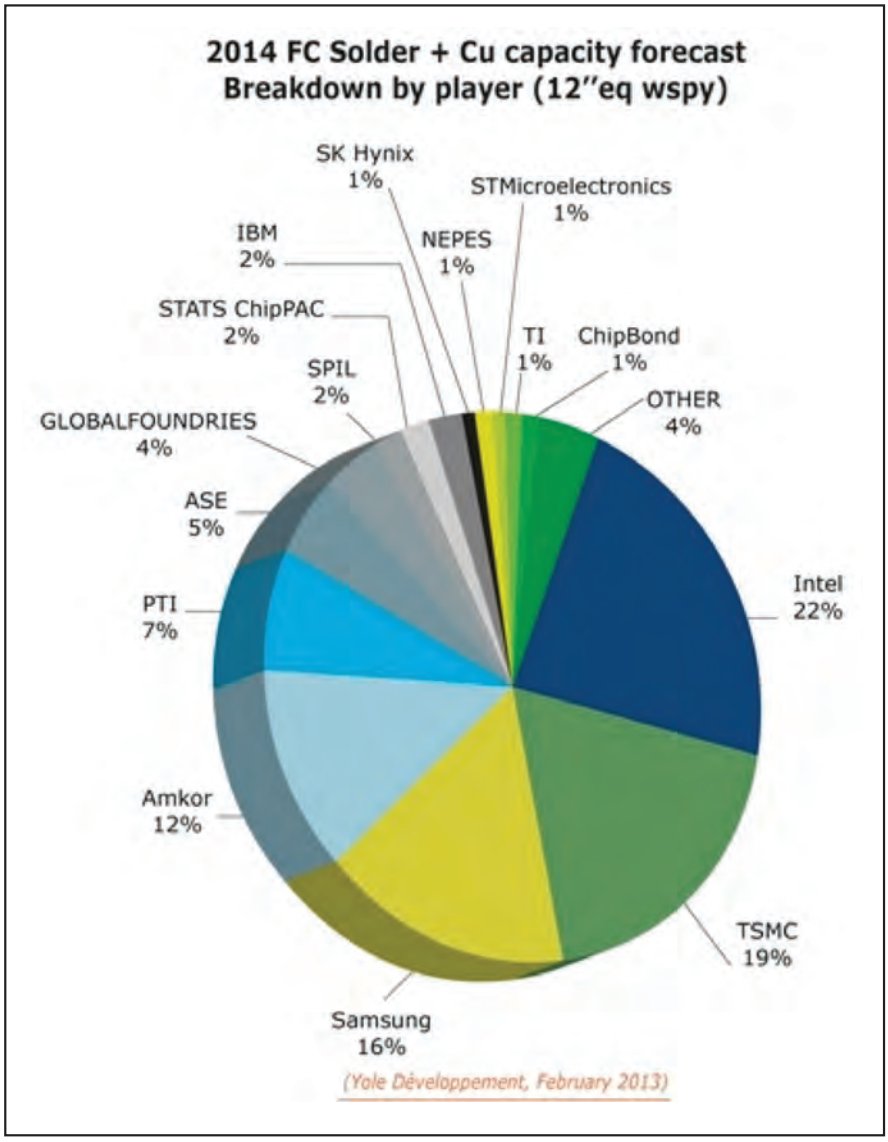
Indeed, no matter what packaging technology you're using, a bumping step is always required at the end. In 2012, bumping technologies accounted for a massive 81 percent of the total installed capacity in the middle end area. This represents over 14 million 12''eq wafers. What's more, fab loading rates are high, especially for the Cu pillar platform (88 percent).

Flip-Chip is also big on value: in 2012 it was a $20 billion market (making it the biggest market in the middle-end area), and Yole expects it to continue growing at 9 percent, ultimately reaching $35 billion by 2018.

Flip-Chip capacity is expected to grow over the next five years to meet large demand from three main areas. These are CMOS 28nm IC, including new applications like APE and BB, next generation DDR memory and 3DIC/2.5D interposer using micro-bumping.

Driven by these applications, Cu pillar is on its way to becoming the interconnect of choice for Flip-Chip.

In addition to traditional applications which have used Flip-Chip for a while now (laptop, desktop and their CPUs,



GPUs & Chipsets - which are growing slowly but still represent significant production volumes for Flip-Chip), Yole's analyst expects to see strong demand from mobile & wireless (smartphones), consumer applications (tablets, smart TV, set top box), computing and high performance/ industrial applications such as network, servers, data centres and HPC.

The new "Flip-Chip packaged ICs" are expected to radically alter the market landscape with new specific motivations that will drive demand for wafer bumping. "In the context of 3D integration and the "More than Moore" approach, Flip-Chip is one of the key technology bricks and will help enable more sophisticated system on chip integration than ever before," says Lionel Cadix, Market & Technology Analyst, Advanced Packaging, at Yole Développement.

Flip-Chip is being reshaped by a new kind of demand that is hungry for Cu pillars and micro-bumps, which are on their way to becoming the new mainstream bumping metallurgy for die interconnection.

Meanwhile, Cu pillar is fast becoming interconnect of choice for advanced CMOS (less than 28nm), memory, and micro-bumping for 2.5D interposer and 3DIC.

Yole believes Cu pillar bumping, which is becoming increasingly popular for a wide variety of applications. The massive adoption of Cu pillars is motivated by a combination of several drivers, including very fine pitch, no UBM needed, high Z standoff, etc.

Cu pillar Flip-Chip is expected to grow at a 35 percent CAGR between 2010-2018 (in terms of wafer count). Production is already high at Intel, the #1 Flip-Chip producer - and by 2014, more than 50 percent of bumped wafers for Flip-Chip will be equipped with Cu pillars.

As early as 2013, micro-bumping for 2.5D & 3DIC, in conjunction with new applications like APE, DDR memory, etc., will boost Flip-Chip demand and create new challenges and new technological developments. Today, Flip- Chip is available in a wide range of pitches to answer the specific needs of every application.

The ultimate evolution in bumping technologies will consist of directly bonding IC with copper pads.

3D integration of ICs using this bump-less Cu-Cu bonding is expected to provide an IC-to-IC connection density higher than 4 x 105 cm-2, making it suitable for future wafer-level 3D integration of IC in order to augment Moore's Law scaling. Taiwan is the #1 location for Flip-Chip bumping according to Yole.

The major OSATs are preparing to produce fcBGA based Cu pillar packages and won't limit the reach of cu pillar bumping to fcCSP. This will allow every company involved in CPU, GPU Chipset, APE, BB, ASIC, FPGA and Memory to access Cu pillar Flip-Chip technology.

Cu pillar capacity is expected to grow rapidly over the 2010 - 2014 timeframe (31 percent CAGR), hitting ~ 9 million wspy by 2014 and supporting the growing demand for micro-bumping and advanced CMOS IC bumping.

In the mutating middle-end area, CMOS foundries now propose wafer bumping services (TSMC, GLOBALFOUNDRIES, etc.), as opposed to bumping houses, which are dedicated to bumping operations (FCI, Nepes, etc.), and OSATs, which keep investing in advanced bumping technologies.

In 2012, OSATs owned 31 percent of installed capacity in ECD solder bumping and 22 percent of installed capacity in Cu pillar bumping. A full overview of 2012 installed capacities for all bumping platforms is provided in this report.

Regionally, Taiwan has the biggest overall bumping capacity (regardless of the metallurgy), with important capacity coming from foundries and OSAT factories.

Taiwan currently leads the outsourcing "solder & copper" Flip-Chip wafer bumping market. Flip-Chip market growth, spurred on by the emergence of the "middle-end" environment, has challenged traditional "IDM vs. fabless" supply chain possibilities more than ever before.

"Airbus for chips"

could take European chip industry to the future

The semiconductor industry is fighting an uphill battle against the forces of the globalization: could the concept of an "Airbus for chips" generate new thrust?

OVER THE PAST DECADE, the semiconductor industry was fighting an uphill battle against the forces of the globalization - and of Moore's Law. Smaller geometries and increasingly complex manufacturing processes caused the investment for leading-edge manufacturing lines to skyrocket; the fragmented European chip industry saw its significance in the global markets dwindle. But now the concept of an "Airbus for chips" as formulated by Nellie Kroess, EU Commissioner of the Digital Agenda, could generate new thrust.

Semiconductors are at the core of just about any technical product. Microprocessors run the software that brings computers and smartphones to life; without chips, today no car would be able to drive safely - perhaps it would not even drive at all. Integrated circuits are not merely ubiquitous; they are the basis for many functions in consumer products and manufacturing equipment. What's more: they are enablers for innovation per se, from the digitization of lighting to the smart power grid. The connected car of the future will help to keep personal mobility affordable - without the environmental problems mobility is associated with today. All these technologies and emerging business are widely based on the availability of semiconductors.

Equally important, the semiconductor industry is a job machine: In Europe alone, more than 200.000 high value jobs are directly associated to the semiconductor value chain, from materials to chip production - not to mention the hosts of engineers and factory workers that that use these chips to design and build industrial controls, radar equipment, ECG units and all these products indispensible for modern living.

Over the past years however, government subsidies and more favourable general conditions in some Asian countries, led to the concentration of semiconductor manufacturing activities in these geographies. Increasingly, this phenomenon creates the risk that engineering and innovation - main pillars of the European economy - follow the way of manufacturing.

At the recent International Semiconductor Strategy Europe forum (ISS Europe), hosted by industry association SEMI Europe, high-ranking representatives of the European chip

industry, research institutions and the European Commission discussed the situation and possible strategies to re-strengthen Europe's competiveness in the semiconductor value chain.

In his presentation, Barnett Silver, Senior Vice President and Principal of advisory firm ATREG, provided a sound analysis of the current situation and its consequences. During the evolution of the semiconductor technology over the past decade, chip geometries shrunk from 130nm in 2001 to 22nm in 2012. In the same period, the costs to build a leading-edge fab climbed from $1.3 billion to $7 billion, an increase of 440 percent.

This cost explosion deprived many chipmakers of the ability to maintain production in-house. In this period, the number of players able to run leading-edge manufacturing lines fell dramatically - from 19 firms to just four in 2012.

The next fab generation is associated to the transition to 450mm silicon wafers and to EUV lithography, and again, both technologies are considered as extremely capital-intensive. The investment for the construction of fabs able to handle these technologies is estimated at $10 billion. "It is obvious that amounts of eight to ten billion dollars can hardly be raised anymore by any single company or even by single nations", comments SEMI Europe President Heinz Kundert.

This dilemma also led to the development of two incompatible strategies within the European chip industry: On one side, there is the "More Moore" group, advocating a strategy that adheres to Moore's Law. The other camp bets on the design of cost-optimized and value-added semiconductor solutions, a strategy for which the expression "More than Moore" has been coined. The "More Moore" strategy includes, among others, the transition to more powerful and complex production lines, which can process 450mm semiconductor.

This move will boost productivity, but only the top league of manufacturers will be able to finance these factories - and this strategy inherently bears substantial risks. The "More than Moore" strategy, in contrast, basically capitalizes on existing technologies and abilities and avoids these risks. The incompatibility of these two strategies is increasingly seen as a risk in itself since it intensifies the fragmentation across the European industry.

In this situation, voices are being raised calling for joint efforts from the industry and for more support from the side of politics at European level. The European Commission started to show increased understanding for the difficult situation of the European semiconductor industry several months ago when European Commissioner, Neelie Kroess, suggested a European effort to boost Key Enabling Technologies (KETs) in order to strengthen the competiveness of Europe's industry. As one of these KETs, she identified semiconductor manufacturing.

Inspired by the success of Airbus Industries in the seventies she sub-sequentially aired a concept of an "Airbus for chips". Much like Airbus Industries led to a revival of the European aerospace industry in the seventies, the Airbus for chips could reinforce the position of the European semiconductor industry in the

global competition. In this context, the EC announced to foster the KETs with a total of about 6.7 billions, of which the lion's share would be spend to micro and nano electronics, nano technologies, material research and manufacturing.

At the ISS Europe, this concept sparked great interest though it was clear that it still needs to be discussed how precisely the idea of an "Airbus for chips" could be transferred to the semiconductor industry. Such a manufacturing concept offers a broad range of business and operational options. In any case, it would open the perspective to the European chip industry to get access to the technology associated with next-gen 450mm wafer processing and the users could benefit from its productivity gains.

The European semiconductor industry has plenty of assets, tangible as well as intellectual, to build upon, participants of a high-ranking panel discussion agreed. Among these strengths are Europe's world-class research and development institutions - like Belgium's IMEC, France's CEA-LETI and Germany's Fraunhofer Gesellschaft. In many segments of the semiconductor technology, European companies take leading positions.

Examples are low-power digital technologies and security. Bosch and Infineon are globally recognized market leaders in power semiconductors. In addition, European chip companies possess a very dense and broad IP portfolio. Again, an example: 95 percent of the world's smartphones are based on microprocessor IP from British vendor ARM. In materials science and process technologies, Europe also holds a strong position. Dutch equipment manufacturer ASML dominates the lithography section, a very critical segment of the semiconductor production chain. In addition to these industry giants, thousands of small and medium-sized enterprises across Europe contribute to Europe's strength. All told, Europe's equipment industry has a global market share of 25 percent, significantly more than its current market share in semiconductor production.

The prospect of supporting large scale pilot production lines in addition to R&D institutions brings into reach the possibility to stay in the game when the industry globally moves towards the next generation of manufacturing sites.

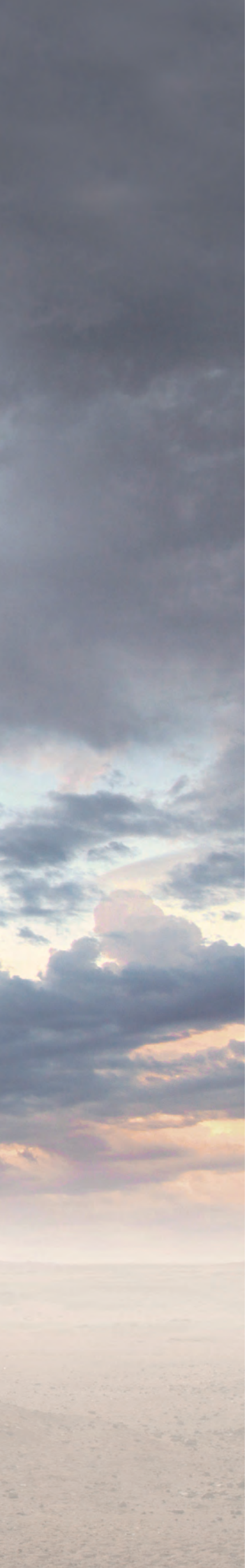
"An Airbus for chips could be a very powerful tool", commented IMEC CEO Luc Van der hove who has a reputation as one of the most distinguished masterminds of a joint approach. "It does not need to be a single company, it also can be a framework of companies", added Laurent Malier, CEO of French research centre CEA-LETI."

In order to get there, it however is necessary to really close ranks and bundle forces. "We have to think in European terms", demanded Van den hove. "Talking in a common voice allows the European Commission to act and support this industry". This statement precisely met the sentiment of the ISS participants. Van den hove's fellow campaigner Rob Hartman, Director Strategic Program for ASML, summarized: "We have all the knowledge, the materials and the equipment. Let's do it in the EU".

Design challenges

of high voltage instrument development

Designing an instrument capable of measuring very low currents and having an output stage capable of producing 3000V is extremely challenging. **Kevin Cawley Principal Engineer, Keithley Instruments, Inc.** recounts the hurdles and how the team overcomes them.



DURING THE DEVELOPMENT of Keithley's Model 2657A High Power SourceMeter Source Measurement Unit (SMU), the design team encountered a range of challenges related to the high voltage levels involved. The last high voltage SMU Keithley had developed was an 1100V/20W unit introduced in the 1990s. The Model 2657A, which is equipped with a ±3000V, 200W power source, is the highest voltage instrument we've ever designed. In order to characterize and test the next generation of high power semiconductors, however, this instrument also requires the precision to measure down to hundreds of femtoamps.

This combination of requirements forced us to re-evaluate all safety practices, from the design labs to the manufacturing, calibration and repair facilities. It also demanded exceptional discipline and ingenuity in terms of design.

We encountered challenges related to issues designers can usually take for granted, such as the components and equipment used, debugging techniques, and especially the project schedule: Just about everything was more difficult, more costly, and more time-consuming than with a lower voltage project. In addition, from a broader, system-level perspective, we had to factor in how customers would use the product and how sales and applications personnel would demonstrate it. Ensuring the system was simple to use and demonstrate was a major consideration. Special test fixtures were also necessary to ensure the safety of the user and prevent damage to other equipment integrated into the system.

Safety First

Our first step was preparing people and the work environment for the new safety requirements. That involved in-house personal safety training for working with high voltages and CPR training for our design and manufacturing teams. Later, we developed safety training for the product's end users. We also created new high voltage lab areas for engineering, manufacturing, calibration, and repair in both our U.S. and international locations, equipping them with emergency power shutdown and interlock safety switches.

With our focus on designing a safe product for our customers, we involved our safety team at the early stages of our design effort, working with them to develop a system insulation block diagram (IBD) that defined the voltage circuit groups and determined the required spacing, creepage, and clearance distances between each group. These voltage spacing rules are defined by international standards. These requirements posed many mechanical and electrical layout challenges, with some circuit groups requiring more than two inches of spacing between them. The ability to enter these voltage spacing rules into PCB design CAD software helped us enforce the IBD spacing rules during the PCB layout; we also used 3D mechanical CAD software to view board-to-board or board-to-chassis spacing before the boards were built.

We came up with a variety of innovative solutions to minimize the impact of these spacing requirements. In one case, the chassis-based screws used to mount the main analog PCB would have forced us to keep analog components or traces a minimum of 17 millimeters away from each screw head. The board's large size required 12 mounting locations, which would have forced us to leave a lot of space on the PCB unoccupied. To minimize this loss of PCB real estate, we developed a mechanical mounting device that isolated the screw into the PCB from the chassis, providing the necessary creepage distance from the screw to the chassis. By "floating" the screw head, we freed up that PCB real estate for component placement. In other cases, the only way to achieve the required spacing was to separate the circuit groups physically onto multiple smaller PCBs.

Another challenge was high speed digital communications from the chassis-based microprocessor board to the floating analog circuitry. We can usually use low cost off-the-shelf multi-channel digital isolators to meet our voltage spacing requirements. In this case, because there are no single-component solutions available, we ended up using optical fiber with discrete transmitters and receivers to meet the high voltage spacing. This is an expensive solution with large components, so to minimize the impact on space and cost, we redesigned our communications scheme, which originally involved eight signal paths, to be just a three-signal solution.

One advantage of using fiber with separate transmitters and receivers was that it allowed us to move the chassis-based communication signals off the main floating analog board, freeing up space on the PCB that was reserved for the creepage from the analog circuits to the chassis-based communication signals.
Even with all the information provided by the advanced CAD tools we used, we were still occasionally surprised by the zap of an electrical arc while powering up new revisions, a not-so-subtle way of telling us we hadn't allowed sufficient spacing somewhere. As the design project progressed, we began holding regular safety reviews to address new problems as they emerged. As we refined the product, we had to

adjust and refine the IBD continually. A complete rethink of design techniques

Designing an instrument capable of measuring very low currents and having an output stage capable of producing 3000V is extremely challenging. Previous SMUs in this particular product family were only capable of sourcing voltages up to 200V. For this design, the level of energy in capacitances in the circuit was multiplied by more than 100 (E=0.5*C*V^2) for the roughly 10X increase in voltage. In addition, components that connected 3000V to the low current section, including the PCB, demanded impedances greater than 3000V/100fA or 3E18 ohm. All this required rethinking layout techniques, guarding and protection techniques, and the selection of isolation components that spanned the output voltage to a low current sensitive node.

In this particular design, the current measurement section incorporated many MOSFET components for bypass and switching of ranges. In addition, we used several compensation capacitors to connect the output voltages to the current measure section. Although these parts worked well in similar low voltage products, the higher voltage of this design meant that the capacitors stored much more energy (E=CV^2) than in the low voltage designs. As a result, when a DUT would short suddenly, this energy would be dumped into the current measure section, damaging these sensitive MOSFET devices, leading to either a complete failure of the MOSFET or increased leakage. That meant we needed to develop some innovative ways of reducing the voltage or rerouting this dumped energy around the circuits to protect these sensitive devices.

These bypass circuits needed either to have high impedance inherently or to be guarded to achieve this high level of impedance. The problem components included the compensation capacitors that connected the high voltage to the current sense circuit. These components could not be guarded, yet needed to achieve high impedance. After a long search, we finally identified a compensation capacitor that could handle the high voltage while ensuring low leakage, as well as meet other critical parameters, such as for part size and dielectric absorption.

Finding suitable high voltage capacitors was far from the only difficulty we encountered in component sourcing. Connecting the source and sense leads to the DUT required low noise triax cables capable of withstanding 3000V from center to guard and guard to shield. They also had to have low leakage from center to guard to allow sub-picoamp measurements. Before we started this project, such a cable simply didn't exist, so we began working with cable manufacturers to develop one to our specifications. Once we had the cable defined and verified, we moved on to develop triax connectors that could meet our high voltage and low leakage specs and our safety requirements. This connector design had to be adaptable to a variety of applications, including board mount, panel mount, and panel pass through designs. We contacted half a dozen connector manufacturers, but only one had the capabilities of designing a custom high voltage triax connector.

3D printing to the rescue

Ultimately, the most complicated component design task was creating an output relay that could switch the high voltage, withstand twice the maximum voltage, and have low leakage. We wanted to be able to use this relay as an output ON/OFF relay for the product as well as use it in a switch system. This complicated the relay definition because each relay application had a different set of safety spacing requirements. These differing requirements had to be combined into a single relay definition based on the worst-case safety spacing. We started working with engineers at two different vendors to develop possible solutions, approve prototypes, and then test their capabilities. After holding multiple meetings and testing several prototypes, we determined that a split guard reed relay offered the best solution.

Our prototype tests let us determine the best material to provide the high isolation and low current leakage that we required. By this time, we were down to a single relay vendor with the capabilities to provide us with a solution. To further complicate the design, some of the required creepage distances could not be met by using off-the-shelf bobbins. This resulted in some creative bobbin designs by the relay vendors to meet our requirements and still have a manufacturable relay. The vendor used 3D printing, which allowed developing bobbin prototypes quickly for faster reviews and tests. In the end, we have a robust relay that meets our stringent requirements.

The design and debugging processes took significantly longer than in earlier SMU development projects because of the complexities inherent in high voltage design prototyping and

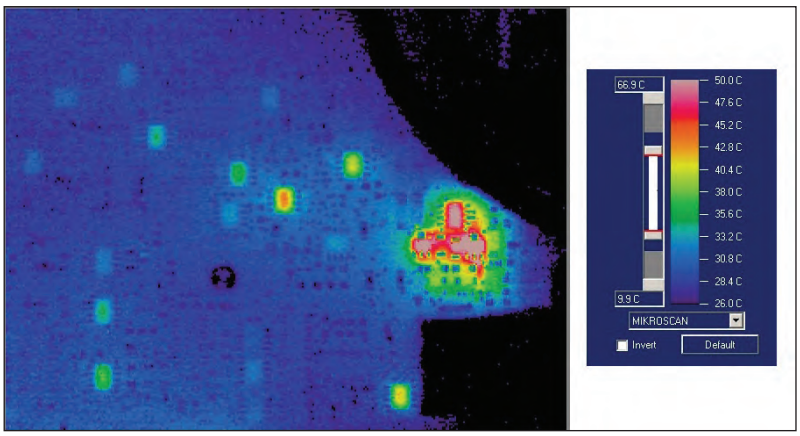


Figure 1. Thermal video imaging was used to identify hot or damaged components on PCBs during the evolution of the Model 2657A's design

high voltage measurements. For example, to prepare for the first prototype boards, we needed to acquire high voltage, high power supplies to power the circuits for debugging. We also needed to find (or in some cases, develop our own) DC and AC probes to make the high voltage measurements. Floating circuits are common in SMUs and some can float to the full voltage of 3kV. Significant analysis was required to determine where to place probes and which equipment to use to make specific measurements.

All equipment had to be properly grounded to ensure safe operation. The increased energy from the high voltage meant that any measurement mistake had the potential to damage the test equipment or the SMU circuits under test, leading to costly downtime for repairs. In many cases, a high voltage arc on the board meant several days of debugging and repair due to the number of components damaged. Until we could determine the source of a problem, we had to repeat the process of powering a unit, running a test until the arc occurred and hoping to detect its source, repairing the unit, and rerunning the test. In some cases, we had to work in a dark room to spot the source of the arc.

Simply making measurements was difficult given the high voltages involved. The usual procedure was to start with the power off, determine which test was needed, set the probes, power up the unit, and make a measurement. Moving a probe required powering off the unit, relocating the probe, and then repowering the unit to make the next measurement. Although this was an extremely time-consuming routine, it was the only way to work with floating high voltages safely. High voltages also made it impossible to handle a DUT under power; DUTs were located in an interlocked fixture that had to be opened (turning off the power to the fixture) before changing the DUT and rerunning a test.

When designing low voltage instruments, engineers can typically identify hot or damaged components by touch, but that wasn't possible with the Model 2657A. A thermal video camera was invaluable for finding these components safely. When an arc occurred, this camera also helped us identify damaged areas of the circuit board quickly (Figure 1). Designing the Model 2657A SMU itself was only part of the process of high power/high voltage system development. Users needed an interlocked high voltage test fixture to connect to their DUTs and the sales team needed it to demonstrate the instrument's capabilities safely. Special interface boxes were essential to connect multiple high and low voltage instruments' LO terminals together safely, as well as special protection interface modules that could connect the HI terminals of multiple low and high voltage instruments and protect the low voltage instruments from damage in case of a device failure. Finally, we had to engineer a way to cable and ground the multiple instruments and interface boxes together in a system with multiple configurations (Figure 2).

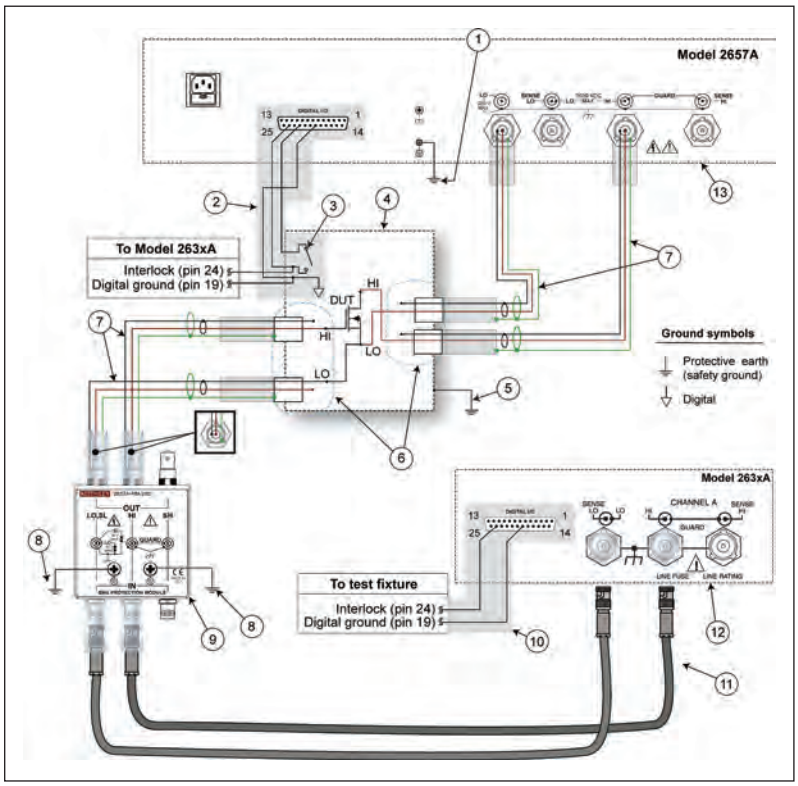


Figure 2. A test system configuration illustrating cabling and connections for measuring MOSFET characteristics with the Model 2657A and another Keithley SMU

High voltage instrument design brings with it a whole new level of prototyping and testing challenges. Things that can usually be taken for granted, like the availability of suitable lab instruments, lab locations, and cabling, grounding, and safety interlock requirements all demand special consideration. Instead of a single PCB, we needed multiple smaller PCBs to meet voltage group spacing requirements for creepage and clearance. System debug was much more complex due to the difficulty of making measurements because of the high voltages involved. Even something seemingly as simple as connecting two instruments to the same DUT was more complicated.

These complications also made it difficult to avoid schedule slippage. Despite all of the challenges that complicated the process, we created a high voltage system design that combines high safety for users and test equipment with the characterization capabilities that the next generation of power semiconductors demand. At the same time, we expanded our own product development capabilities substantially, developing new skills and practices that we can apply to the next high voltage design project we undertake.

Digital power market forecast to quadruple in five years

The digital power market is currently one of the fastest growing segments of the power management industry for power supply and power IC manufacturers. IMS Research – now part of IHS (NYSE:IHS) – has been analyzing the power management and conversion market for 20 years and offers an analysis of the digital power market.

ALTHOUGH A MARKET FOR DIGITAL POWER has existed for many years in some form, growth is now accelerating as adoption increases across many different applications and sectors. The market is forecast to quadruple to $15 billion in the five years from 2012 to 2017. The market for digital power supplies is projected to be worth almost $12.5 billion of this in 2017 with the digital power IC market accounting for the other $2.5 billion. The digital power IC market is projected to grow at a faster rate due to their use in the end-equipment at board level and also in digital power supplies.

Competition, especially on the power IC side, has grown rapidly over the last five years and many suppliers have increased their capabilities via acquisitions. Examples of this include Infineon's acquisition of Primarion in 2008, Intersil's acquisition of Zilker Labs, again in 2008 and International Rectifiers acquisition of CHiL Semiconductor in 2011. Power Supply companies have continued to develop in-house expertise and several have entered into licensing agreements with other suppliers.

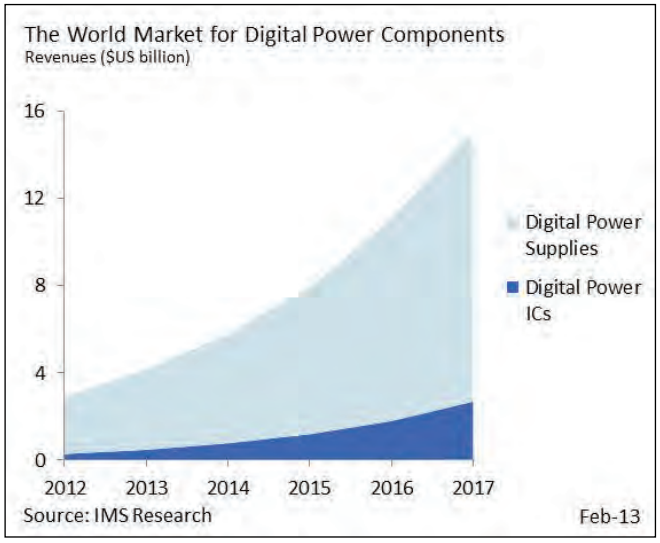
Adoption of digital power was first seen in telecommunications applications dating back to the early 1980s. Since then,

manufacturers of digital power supplies have produced many products aimed at this market. Growth in this market is driven largely by demands for greater efficiency which digital power solutions can help achieve by offering system monitoring, power sequencing and optimisation of power usage in applications. It can also help to simplify the power management function which for many applications is growing in complexity, particularly for those with higher power ratings. Demand for higher reliability under constant usage is another key growth driver.

The use of digital power in designs can offer greater power density and a reduction in the number of components which can result in higher system reliability. With rising demands for scalability and minimal system downtime of applications in this sector, the ability to monitor, control and sequence power at numerous levels of the telecom/datacom system is becoming ever more important and is predicted to drive even greater adoption of digital power components.

The server market has been another major early adopter of digital power solutions. Adoption has again been driven by greater energy efficiency demands. Standards bodies such as Energy Star continue to demand higher efficiencies and low idle power draws. The majority of enterprise servers now use digital power solutions for the Vcore (which supplies power to the processing core) and memory. Outside of the applications already mentioned, adoption of digital power solutions is predicted to occur rapidly and drive aggressive growth as manufacturers become more aware of the benefits they can offer compared with some analog products. These include reducing the overall bill of materials cost by reducing the number of discrete components, reducing the overall footprint, increasing power density, providing the ability to monitor and optimise power levels and system requirements whilst in operation and speeding up product time to market. Over two-thirds of the manufacturers and designers surveyed by IHS predicted that more than 10 percent of their products will have digital control or digital management in 2015.

Applications, besides telecom/datacom and servers that are projected to have strong growth in the next five years include notebooks, some industrial applications, high-end consumer



“The server market has been another major early adopter of digital power solutions. Adoption has again been driven by greater energy efficiency demands. Standards bodies such as Energy Star continue to demand higher efficiencies and low idle power draws. The majority of enterprise servers now use digital power solutions for the Vcore (which supplies power to the processing core) and memory”

devices, solar inverters and towards the end of the period, lighting. However, there are still barriers to adoption. Of the manufacturers and designers surveyed by IHS, 27 percent stated that cost was still the largest barrier. This highlights lack of knowledge from some potential implementers regarding the overall cost savings that digital solutions can provide and shows that there is still some way to go in educating designers at OEMs/ODMs. Another issue, raised mainly by the digital power supply and digital power IC manufacturers was that there are many designers that are wary of digital solutions and prefer to continue using the analog approach that they know and are comfortable with.

To combat this, many manufacturers who were manufacturing just digital control products (where the feedback loop and PWM output is entirely within the digital domain) have started producing digital management products that are a hybrid to bridge the gap between analog and digital solutions. These products have an on-board microcontroller or microprocessor that works in conjunction with an analog PWM. Whilst these products provide feedback and allow monitoring, they might not have a communication protocol in which the parameters of the product can be modified. Despite this, it is expected that in the long term, solutions with full digital control will dominate the market due to the increased functionality. The full report on this market is available from IMS Research.

Jonathon Eykyn, Analyst, Power Management & Conversion for IHS.

Driving innovation

"If I'd asked my customers what they wanted, they would have said a faster horse." – Henry Ford. This quote from the automotive pioneer is bound to stir debate about how companies should approach the innovation process. Should they take calculated risks in anticipation of market needs, as Ford did?

Greg Shaw, Director, Technology Development, Swagelok discusses.

IN TECHNOLOGY DEVELOPMENT CIRCLES, there is no obvious answer. Often, companies realize innovations through a combination of market research, internal idea generation, customer requests, and a variety of other factors. They also frequently discover innovative solutions by chance. While no formula exists for approaching the innovation process, companies can benefit by following a few best practices when responding to customer requests:

- Ask "Why?" often to gain a full understanding of the request, including market needs, application parameters, and customer challenges.
- Bring the right parties to the table as part of an integrated team that is open to collaboration.
- Track and understand technology developments to anticipate new solutions and market applications.
- Look to existing solutions that can be adapted to meet the current challenge. Look outside the comfort zone.
- Prototype early and often, whether developing products or processes.
- Be willing to accept – and recognize – that not every project will result in a desired outcome.

Following a disciplined process that includes these steps can help companies respond effectively to customer inquiries for new solutions. In addition, the process can strengthen customer-developer relationships and lead to future collaboration and mutual successes.

Gather all the facts

Creating a solution for a customer challenge begins with a clear understanding of the customer's needs – the real needs, not just the stated needs. Developers should not simply respond to the request. They need to first ask a series of in-depth questions to clarify the context, which may include: Why do you need the requested product or technology? How does it fit into a complete system? What processes affect its performance? What alternatives have worked and/or failed? Gaining comprehensive insight may reveal that a more complete solution exists rather than one that simply fulfils the customer's initial request.

For example, a customer asked Swagelok for a specific instrumentation ball valve made of Hastelloy® for use in sour gas applications. Because sour gas is both toxic and corrosive, the valve components must be made of highly corrosion-resistant materials to ensure that the gas is fully contained. Through an in-depth review of the application requirements with the customer, Swagelok identified that an alternative trunnion-style ball valve made of alloy 625 could be a better choice.

The 625 nickel-chromium alloy provided comparable corrosion resistance to Hastelloy at a lower cost and shorter lead time. In addition, the alternative valve had a higher pressure rating, which provided an extra margin of safety for the application. By switching to the alternative valve, the customer reduced costs, improved delivery time and enhanced application safety.

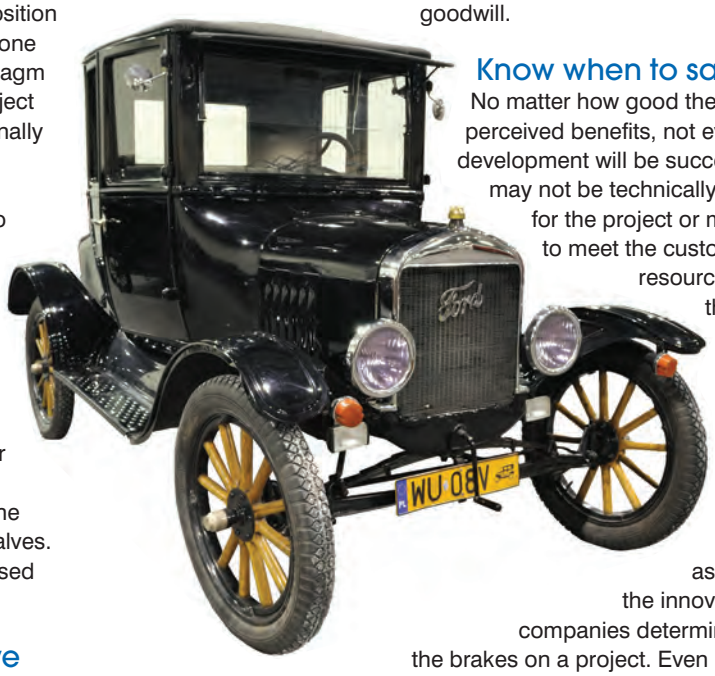
Get the right parties together

Open, unfiltered communication is vital to arriving at the best possible solution for customer-centric development challenges.

Often, customers share their initial requests with marketing and sales contacts. It is important for these parties to facilitate collaboration between technical groups on both sides to ensure the proper handoff of information and encourage engineer-to-engineer communication. Engineers from both organizations need to share detailed application information and explore technical challenges together as early in the design cycle as possible. Bringing people together who speak the same technical language encourages information sharing, brainstorming, and efficiency, while enabling the parties to gain as in-depth an understanding of the project as possible.

For example, when a customer asked Swagelok to develop an application-specific high-temperature diaphragm valve with a service rating above 400°C (752°F), engineers from both companies collaborated to find the best solution. Together, they determined that the footprint for the customer's new system tool did not have to match that of the old system. By expanding the footprint, they were able to use physical space to their advantage and position system components apart from one another. By doing so, the diaphragm valve actuator would not be subject to temperatures as high as originally expected.

Therefore, Swagelok was able to use different materials of construction than originally planned, resulting in better performance and a lower cost for the new-technology valve. Had engineers come to this conclusion after finalizing the system design, the customer would have either needed to redesign the system or accept the investment in more expensive valves. Either alternative would have raised development costs.



Stay ahead of the curve

Technology developers have a greater chance of successfully meeting future customer requests when they proactively explore potential market opportunities and applications. Staying ahead of the curve involves keeping up with technology developments in areas like corrosion resistance, system designs, material compatibilities and production processes. Engaging in internal development efforts with emerging technologies, in advance of customer demands, ensures that developers can properly apply those technologies when needed to meet application requirements. In doing so, developers will be able to respond more quickly and effectively to customer needs.

Allow innovation to breed innovation

Often, an innovative solution spurs the development of another innovative solution. In the fluid system component arena, for example, technologists may discover that a specialty valve for the oil and gas market works for a power market application. The developer may be able to place the original valve directly into the new application, make minor modifications to fit the new application, or at least use design principles from the first valve to develop the new one. By adapting existing solutions to new applications, developer companies expand opportunities to capitalize on their innovations; they improve their return on investment for technology development.

Prototype early and often

Developing early prototypes – even for individual components – enables developers to test and refine parts before moving too far down the product development path. Developers should test concepts and engage in continuous feasibility studies throughout a project to determine the potential for success or failure. Then, as development proceeds, opportunities exist to make adjustments without requiring major overhauls.

Testing those parts that present the highest risk or biggest challenges first is a wise practice. In doing so, companies have greater potential to determine if any barriers are insurmountable prior to substantive investments in time, energy, dollars, or goodwill.

Know when to say "when"

No matter how good the idea or how attractive the perceived benefits, not every attempt at collaborative development will be successful. The potential solution may not be technically, or economically, feasible for the project or market. There may be no way to meet the customer's request with existing resources. It's best to recognize that a project is not going to yield the desired outcome as soon as conceivably possible to minimize the expenditure of time and resources.

As noted earlier, engaging in continuous feasibility assessments throughout the innovation process will help companies determine if and when to put the brakes on a project. Even if a project does not meet its initial goals, it can still be considered a success. The collaboration process strengthens customer-developer relationships and gives each party a better idea of the other's needs and capabilities, which can help facilitate the next project.

Drive innovation to drive success

Developing new solutions is far from an exact science. Companies approach the process in a number of ways, but a disciplined process goes a long way in favouring success. A disciplined process includes gathering all pertinent information, collaborating with key parties, testing solutions early and often, and using existing solutions to spur the development of new solutions. Whether they address specific customer challenges or enable new capabilities, innovations allow companies to differentiate themselves in the marketplace. This has held true for Ford in the early 20th century, and it's still the reality today.

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