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Connecting the Silicon Semiconductor Community

Volume 35 Issue 2 2013

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Self-healing circuits are a reality

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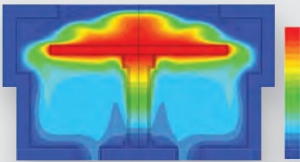
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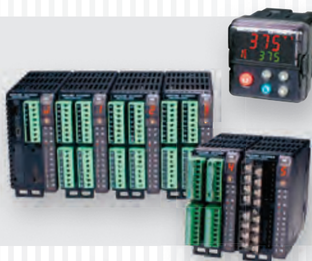
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executiveview

by Larry Vandendriessche, Director, Semiconductor Marketing, Swagelok Company

How to prepare for the next upturn

IT CERTAINLY IS A CHALLENGE to be a highly valued supplier today. Fluctuating demand has resulted in a production environment that is fast-paced, high pressured, and unpredictable. This pressurises suppliers, and exposes any company fault lines. It's not just production and delivery that lead to outstanding performance. It's supplier's systems, culture, and approach. How do you determine which potential or current supplier will serve you best ?

At Swagelok Company, we believe that at the heart of a high quality supplier is a culture of continuous improvement. This cultural trait is about perpetual vigilance, in contrast to cycles of hard work, rest, celebration, and pauses. No company is flawless, especially during an extended period of peak production in the semiconductor industry. So we believe that it's how a company responds and reacts to past performance, and how it prepares for future performance, that matter most. Preparation should be ongoing. We've identified areas key to a culture of continuous improvement, and we evaluate ourselves and our own suppliers in each.

Risk Management. What is the company's track record in mitigating risk, and what improvements have been introduced?

Capable Systems and Processes. What is the level of sophistication, documentation, and methodology in company processes, from manufacturing through fulfillment? Does the company employ Lean, Six Sigma, or other industry protocols?

Quality and Reliability. How does the company ensure there will be no compromises in quality, even while demand increases ?

Workforce Development. How does the company continue to develop a highly trained and skilled workforce through upturns and downturns? Does the company practice cross-training?

Industry Commitment. What is the company's level of involvement in SEMI and other trade associations? What conversations is it having with industry leaders? What is the company's commitment to science and research?

New Product Capabilities. What is the company's capacity to design and produce new products in response to customer needs? Can it can collaborate with the customer during the planning, feasibility, and development stages?

Service and Communication. What is the company's capacity to respond to customer needs at any time? Where are its service locations? What is the degree of company-wide support?

Capacity Response. How flexible is the supplier's capacity? What is the company's track record during previous upturns, and what improvements have been implemented?

Taking each area into account – with an eye toward cost management and future investment – separates a highly valued supplier from the pack.

These areas help to structure a conversation with a supplier or assist in evaluating your organization's readiness to manage the next upturn. In either case, it's a process. How we manage them provides important insight into our company culture.

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Silicon Semiconductor is published four times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/e158 pa (UK & Europe), £138.00 pa (air mail), $198 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2013. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing.
US mailing information: Silicon Semiconductor (ISSN 1096-598X) is published four times a year for a subscription of $198 by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. Periodicals postage paid at Rahway, NJ. POSTMASTER: send address changes to: Silicon Semiconductor, c/o Mercury International Ltd, 365 Blair Road, Avenel, NJ 07001.
Printed by: Pensord Press.
© Copyright 2013. ISSN 2050-7798 (Print) ISSN 2050-7801 (Online).

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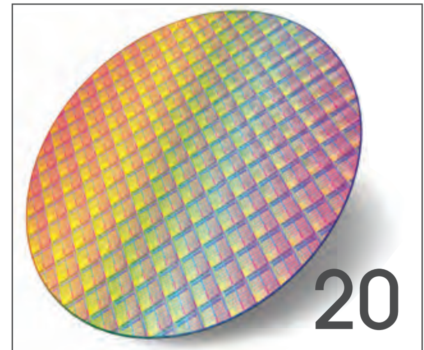
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Magazine and Front Cover: Designed by Mitch Gaynor

Imec and Renesas Electronics in new strategic research collaboration

TOGETHER, the companies will collaborate to enhance ultra-low power (ULP) wireless technologies for short range communication, targeting sensor networks for automotive and industrial purposes.

As the newest member of imec's ULP wireless systems program, Renesas will work to jointly develop multi-standard radio solutions for small battery-operated or harvested wireless handheld devices.

By combining innovative architectures, advanced ULP design IP and efficient low power circuits, imec's ULP radios achieve best-in-class performance and reduce power consumption by a factor of 3 to 10 lower than today's radios.
What's more, imec's ULP high-performance radios are compliant with wireless standards, such as Bluetooth Low Energy (2.4GHz band) and ZigBee (2.4GHz band).
"Building on a proven track record of designs, our research program on ULP wireless systems offers great value to our industrial partners.

Combining application, circuits and technology know-how, we provide a complete solution, shortening the time-to-market for our industrial partners," says Harmke de Groot, program director ULP wireless technologies at imec/Holst Centre.
"After five years of successful collaboration in our Green Radio program, we are pleased that a prominent semiconductor company as Renesas now joins our ULP wireless systems R&D. We look forward to developing enhanced ULP solutions contributing to the realization of the internet of things in mass market applications," continues de Groot.
"Various applications of sensor networks for a smart society need

EV Group rolls out next-generation automated resist processing system

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nano and semiconductor markets, has introduced the latest version of its EVG 120 automated resist processing system. The EVG120 boasts new features and improved productivity in an ultra-small footprint design: the system supports coating and developing applications for a variety of markets, including MEMS, advanced packaging and compound semiconductors. The flexible tool can be configured with combined spin and spray coating modules—a unique feature that maximizes productivity and optimizes cost of ownership (CoO).

Dr. Thomas Glinsner, head of product management for EV Group, noted, "Our new EVG120 system reflects EVG's 15 years of experience in resist coating and developing, and our unique process skills. In independent surveys, our customers consistently attribute the highest scores to EVG's lithography equipment, and we've listened to their feedback to create a more optimized system. Based on a proven platform, the next-generation EVG120 coater/developer offers increased functionality and reliability in a highly customizable and economical package."

The EVG120 automated resist processing system features a new robot with dual arms for fast wafer swapping and additional processing chambers, which result in enhanced throughput and overall productivity. To optimize throughput and overall productivity, the new EVG120 runs the same EVG CIM Framework software as EVG's high-end XT Frame systems and offers full software integration with SECS/GEM standards. Two customizable wet processing bowls are complemented by 10 stacked modules for vapour prime, soft and hard bake, and chill processes. Like its predecessor, the EVG120 system can accommodate wafers up to 200 mm in diameter.

Other new features of the EVG120 system include EVG's innovative CoverSpin rotating bowl cover that allows improved coating uniformity across the substrate regardless of substrate shape. A new, temperature-controlled chuck further enhances EVG's proprietary OmniSpray coating technology, which specifically allows conformal coating of high-topography surfaces via its proprietary ultrasonic nozzle. OmniSpray coating is ideally suited for ultra-thin, fragile or perforated wafers and can the company says result in an 80-percent or greater reduction in material consumption compared to traditional spin coating.

Intel invests in $1.5m research

Intel Corporation has announced details of the second phase of its research investment at Ireland's ICT research Institute, the Tyndall National Institute at University College Cork.

The investment of $1.5 million over the next 3 years secures the continued collaboration between Tyndall and the heart of Intel's process technology research group in the U.S. and is a testament to the success of the first phase of the program which ran from 2009 to 2012.

The agreement will again provide Intel with a commercial exploitation license to technology created through the collaboration with Tyndall.

Intel and Tyndall have been working closely for a number of years on a range of different technologies leading to the first phase of research investment by Intel in the Institute in 2009.

This latest funding agreement, which is the only one of its kind for Intel in Ireland, enables the continuing relationship directly between Tyndall and Intel's internal research group in Portland. An event to inaugurate the event was held at Intel's campus in Leixlip.

$5m nano research initiative announced

SEMICONDUCTOR RESEARCH CORPORATION (SRC) and the National Institute of Standards and Technology (NIST) have announced the second phase of the Nanoelectronics Research Initiative (NRI). For this phase, SRC and NIST will provide a combined $5 million in annual funding for three multi-university research centres tasked with demonstrating non-conventional, low-energy technologies that outperform current technologies on critical applications in 10 years and beyond.

The second phase of NRI also features joint projects with the National Science Foundation (NSF) and the multi-university research network involves 34 universities in 17 states. The three research centres are:

The Institute for Nanoelectronics Discovery and Exploration (INDEX) at SUNY's College of Nanoscale Science and Engineering (CNSE);
The Center for Nanoferroic Devices (CNFD) at the University of Nebraska-Lincoln; and The South West Academy of Nanoelectronics (SWAN) 2.0 at the University of Texas at Austin.

"In 2012, the first phase of NRI culminated with a comprehensive assessment of the various NRI device concepts through performance bench marking," said Tom Theis, the new SRC program executive director. "NRI 2.0 will focus on key research opportunities identified in the bench marking study and will explore the ultimate scalability of emerging digital device concepts and their functionality beyond digital logic. For example, researchers will explore magnetoelectric devices that promise improved energy efficiency and the ability to combine memory and logic."

NIST will provide $2.6 million to the effort each year for up to five years, matched by $2.4 million each year from NRI. NRI is made up of participants from the semiconductor industry including GLOBALFOUNDRIES, IBM, Intel, Micron Technology and Texas Instruments.

Additional universities involved in the NRI network include:
INDEX at SUNY's College of Nanoscale Science and Engineering (CNSE): Purdue, Virginia, Cornell, Georgia Institute of Technology and Columbia. CNFD at University of Nebraska-Lincoln: Wisconsin-Madison, Oakland, SUNY Buffalo, UC Irvine, Delaware.

SWAN 2.0 at University of Texas at Austin: UT Dallas, North Carolina State, Texas A&M, UC San Diego, Stanford and Harvard. In collaboration with the National Science Foundation, NRI also supports Nanoscale Interdisciplinary Research Teams (NIRTs) as part of the National Nanotechnology Initiative's Signature Initiative "Nanoelectronics for Beyond 2020." Funding for these projects flows to many other leading U.S. universities.

NRI 2.0 is the successor to an earlier multi-year collaboration between NRI and NIST that focused on the long-term goal of "developing the next logic switch," or the basic logic elements that serve as the building blocks of electronic devices. The NRI initiative was originally launched by the Semiconductor Industry Association (SIA) in 2005.

The NRI and the collaboration with NIST are managed by the Nanoelectronics Research Corporation (NERC), a special purpose subsidiary of SRC, the world's leading university-research consortium for semiconductors and related technologies.

UMC Singapore fab to advance CMOS, Memory & TSV

UNITED MICROELECCTRONICS CORP (UMC) has established FAB 21 in Singapore as its "centre of Excellence" to spearhead the company's R&D and manufacturing for advanced speciality process technologies.

The centre was set up with an initial investment of US $110million and will work with local research institues such as Singapre Institue of Microelectronics. Technologies being developed include CMOS image sensor backside illumination, embedded memory, high voltage applications and TSV (through silicon via) connections. Such specialty processes will enable new products with stronger capabilities in growing markets such as automotive, mobile, smartphone and tablet to help customers offer products which benefit from the increasing connectivity of everyday devices. In 2013, UMC plans to increase the headcount of Fab 12i by over 80 engineers to focus on specialty process development. Terence Gan, Director of Electronics, Singapore Economic Development Board, says, "We are delighted that UMC, one of the world's top wafer foundries, has chosen Singapore to carry out R&D activities for its specialty manufacturing processes." He concludes, "This centre strengthens R&D capabilities in complex manufacturing processes and adds to the base of higher value-added products that the Singapore electronics industry produces. UMC's continued investment in Singapore reflects confidence in Singapore's network of R&D institutes and availability of skilled talent, to support the company in developing proprietary manufacturing processes for tomorrow's advanced electronics products."

UMC's Fab 12i is UMC's only 300mm fab outside of Taiwan.

SSDs on course to claim one-third of the PC storage solution market by 2017

GLOBAL SHIPMENTS of solid state drives (SSD) in PCs are set to rise by a factor of seven by 2017, claiming more than one-third of the market for PC storage solutions by that time, according to an IHS iSuppli Storage Market Tracker Report from information and analytics provider IHS.

SSD shipments in PCs will rise to 227 million units in 2017, up 600 percent from 31 million in 2012. Shipments of PC hard disk drives (HDD) will decline to 410 million in 2017, down 14 percent from 475 million in 2012.

The divergent outlook for the two products will allow SSDs to climb and claim 36 percent of the PC storage market in 2017, up from just 6 percent in 2012. HDDs will see their long-term dominance in PCs erode, with their share falling to 64 percent in 2017, down from 94 percent in 2012.

The SSD space includes the cache SSD segment where NAND flash is used alongside a hard disk drive, as well as a separate segment in which NAND flash is embedded on top of an HDD in an integrated, hybrid form factor.

"For SSDs, the major factors driving growth this year will be Ultrabooks and other ultrathin notebook PCs, especially as Intel's upcoming Haswell processors bring about a robust combination of performance and efficiency for the superthin computers," said Fang Zhang, analyst for storage systems at IHS.

"In the coming years, Ultrabooks and ultrathins—combined with appealing touch-screen displays and convertible form factors—are likely to become more compelling as the machines attempt to lure consumers away from smartphones and tablets, boosting demand for SSDs used in these systems. Meanwhile, SSDs will become more attractive to PC makers and buyers alike as costs decline for the NAND flash memory at the heart of the storage devices."

PC HDD shipments in 2013 are forecast to decline to 436.9 million units, down 8 percent from 475.4 million last year. SSD shipments in PCs will jump to 68.9 million units, up 122 percent from 31.1 million. From 2012 to 2017, the compound annual growth rate for PC HDD shipments will be in negative territory at -2.9 percent, while PC SSDs comes out to an enviable 48.0 percent.

"The HDD industry is suffering the multi layered effects of a depressed market, resulting from a weak global economy, upgrades not being made for desktop and notebook PCs alike as replacement cycles get extended, and cannibalization by flashier devices like mobile handsets and tablets," Zhang observed.

PC HDD revenue is expected to decline to $26.4 billion in 2013, down from last year's record of $30.6 billion that resulted mainly from higher average selling prices after the floods in Thailand.

The SSD space has been extremely competitive, closing out last year on record-high revenue and with the vigorous enterprise SSD segment enjoying expansion. The fourth quarter last year was strong period for computer-related SSDs with shipments of 12 million units, boosting year-end revenue to $6.8 billion. By 2017, PC SSD industry revenue of $22.6 billion will come close to PC HDD revenue of $23.5 billion.

Despite the rapid adoption of SSDs, hard disk drives will continue to lead the overall storage market because of their cost advantage on higher densities and dollars-per-gigabyte pricing.

HDD shipments also will gradually pick up in the second half this year as Windows 8 and Ultrabooks gain traction among consumers, after failing to perform as expected upon launch last year.

In the enterprise HDD segment, competition is set to heat up as arch rivals Western Digital and Seagate Technology contend for leadership, and Western Digital is expected to launch a 5-terabyte HDD sporting the new helium technology for higher disk capacity and lower power consumption. Other new HDD technologies are on the horizon as well, including nearline and hybrid hard disk drives.

HDDs also will continue to play a major role in cloud storage, remaining the final destination for the majority of digital content.

While HDDs retain dominance despite declining shipments and SSDs maintain impressive growth momentum, a third segment of the storage industry is mired in poor results and deteriorating prospects. Optical disk drives (ODD), used for playing CDs and DVDs in PCs, continue to worsen on both shipment and revenue terms.

ODD shipments this year will amount to 262.6 million units, down from 287.4 million in 2012; while revenue will slip to $7.4 billion from $8.6 billion. By 2017, ODD shipments will shrink a further 100,000 units compared to 2012 levels, and revenue will reduce by half.

Consumer and lighting could make digital power go higher

THE GLOBAL MARKETS for digital power supplies and digital power integrated circuits (ICs) are projected to boom from 2013 to 2017. Global market revenue for digital power supplies will rise to $12.4 billion in 2017, more than three times the $3.7 billion predicted for 2013.

This is according to a new report entitled, "The World Market for Digital Power," from IMS Research, now part of IHS. Revenue this year will soar 37 percent from $2.7 billion in 2012, as presented in the figure above. Explosive growth in digital power ICs is also forecast with revenues increasing more than fivefold from 2013 to reach $2.6 billion in 2017. "The digital power market is currently one of the fastest-growing segments of the power management industry," says Jonathon Eykyn, power supply and energy storage analyst at IHS. "Early adopters of digital power components include information technology and communications infrastructure applications such as servers and telecommunications/data-communications equipment. But now digital power is also entering the consumer realm, as other sectors adopt digital power solutions."

Digital power trip

Manufacturers at present mainly employ analog power-management systems. However, they are migrating to digital technology because of its flexibility and programmability, which leads to increased performance and reliability.

This will reduce hardware complexity, cutting the amount of time and effort to design systems and ultimately lowering the cost of electronic systems.

"Digital power can reduce the overall bill-of-materials cost by reducing the number of discrete components, reducing the overall footprint, increasing power density and providing the capability to monitor as well as optimize power levels and system requirements while in operation," Eykyn said. "All this can help accelerate time to market for a range of products."

Power to the people

Severs now is the largest single market for digital power, accounting for an expected 33 percent of market revenue in 2013. This segment will rise at a compound annual growth rate (CAGR) of 44.8 percent from 2012 to 2017.

The fastest-growing application for digital power will be lighting, with the segment anticipated to expand at a CAGR of 146 percent from 2012 to 2017. The increase will be driven by the rising usage of light-emitting diode (LED) lighting solutions, which lend themselves to digital power control and monitoring. Meanwhile, digital power in notebooks and tablet PCs will rise at 99 and 82 percent CAGR, respectively, during the same period. Major home appliances will surge by 76 percent and cellphones will increase by 52 percent.

Power chips for power players

The rise of digital power supplies will fuel the rapid growth in the market of associated semiconductors. The digital power IC market is projected to grow at a faster rate than the digital power supply market because the chips are used in end equipment at the board level and also in digital power supplies.

Money and power

One obstacle to even faster adoption of digital power supplies is their perceived expense. A total of 27 percent of manufacturers and designers surveyed by IHS indicated that cost is still the largest barrier in the market.

This highlights the lack of knowledge from some potential implementers regarding the overall cost savings that digital solutions can provide, and shows that there is still some way to go in educating designers at electronics manufacturers.

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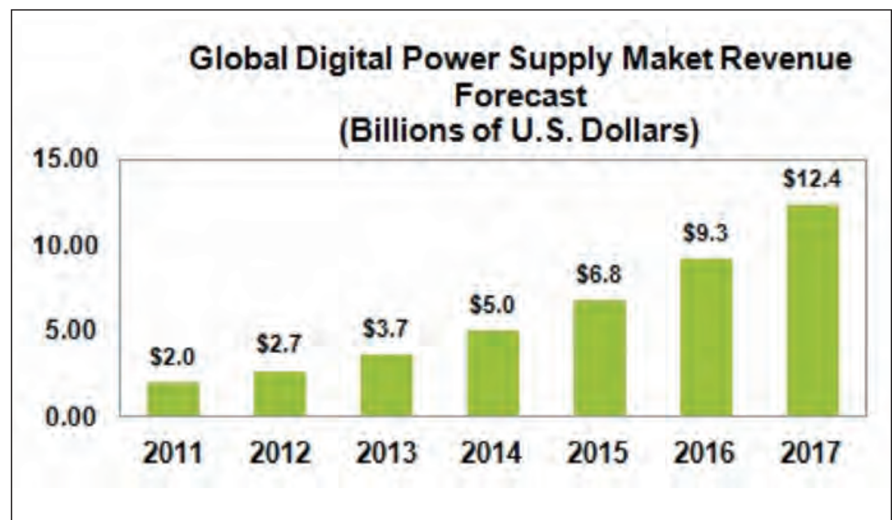

IBM drives Flash forward

IBM HAS UNVEILED a strategic initiative to drive Flash technology further into the enterprise to help organisations better tackle the mounting challenges of big data.

Flash, a highly efficient re-writable memory, can speed the response times of information gathering in servers and storage systems from milliseconds to microseconds - orders of magnitude faster. Because it contains no moving parts, the technology is also more reliable, durable and more energy efficient than spinning hard drives.

Such benefits have led Flash to pervade the consumer electronics industry and be built into everything from cell phones to tablets. Today, as organisations are challenged by swelling data volumes, increasing demand for faster analytic insights, and rising data centre energy costs, Flash is quickly becoming a key requirement to enable the Smarter Enterprise.

"The economics and performance of Flash are at a point where the technology can have a revolutionary impact on enterprises, especially for transaction-intensive applications," says Ambuj Goyal, General Manager, Systems Storage, IBM Systems & Technology Group. "The confluence of Big Data, social, mobile and cloud technologies is creating an environment in the enterprise that demands faster, more efficient, access to business insights, and Flash can provide that access quickly."
To help lead this transformation, IBM is investing $1 billion in research and development to design, create and integrate new Flash solutions into its expanding portfolio of servers, storage systems and middleware.

As part of that commitment, the company plans to open 12 Centres of Competency around the globe. These sites will enable clients to run proof-of-concept scenarios with real-world data to measure the projected performance gains that can be achieved with IBM Flash solutions. Clients will see first-hand how IBM Flash solutions can provide real-time decision support for operational information, and help improve the performance of mission-critical workloads, such as credit card processing, stock exchange transactions, manufacturing and order processing systems. IBM is currently targeting Centres of Competency in China, France, Germany, India, Japan, Singapore, South America, U.K., and the U.S to all be operational by the end of the year.

IBM also announced the availability of the IBM FlashSystem line of all-Flash storage appliances, which are based on technology acquired from Texas Memory Systems. The IBM FlashSystem provides organisations instant access to the benefits of Flash.

The IBM FlashSystem 820, for example, is the size of a pizza box, is 20 times faster than spinning hard drives, and can store up to 24 terabytes of data – more than twice the amount of printed information stored in the U.S. Library of Congress. Flash systems can provide up to 90 percent reductions in transaction times for applications like banking, trading, and telecommunications; up to 85 percent reductions in batch processing times in applications like enterprise resource planning and business analytics; and up to 80 percent reductions of energy consumption in data centre consolidations and cloud deployments. Sprint Nextel Corp., an early adopter of Flash, recently completed a deal with IBM to install nine flash storage systems in its data centre, for a total of 150TB of additional Flash storage. The company was looking for a way to improve the performance and efficiency of its phone activation application.

When performance rose and energy consumption dropped, the company began to expand the technology to other parts of the data centre. According to Sprint officials, this latest installation is part of the company's new strategy to move its most active data to all-Flash storage systems. The new IBM FlashSystem joins the company's growing stable of all-Flash and hybrid (disk/Flash) solutions which include IBM Storwize V7000, IBM System Storage DS8870, and the IBM XIV Storage System.

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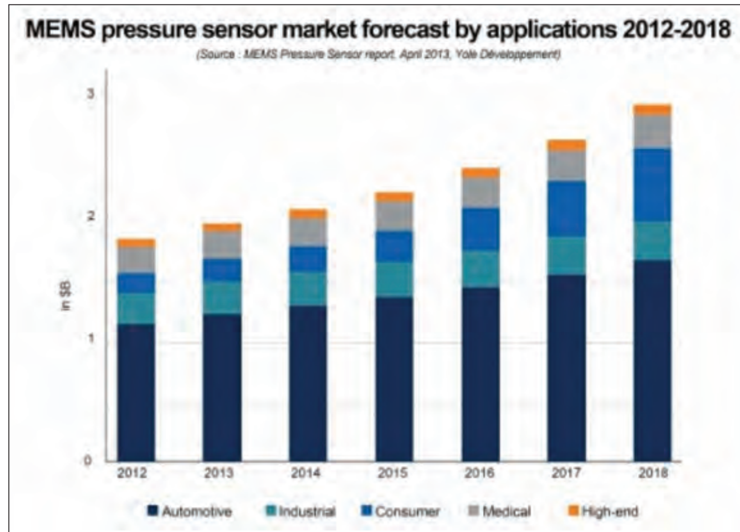
MEMS pressure sensors boosted by consumer applications

AFTER YEARS OF LIMITED GROWTH, the MEMS pressure sensor market is growing due to consumer electronic applications and is expected to show a 22 percent CAGR. Pressure sensors are currently playing an important role in modern industries. MEMS pressure sensors are already widely adopted in different applications for their high-performance, low cost and small size.



In its new report, "MEMS Pressure Sensor," Yole Développement gives a detailed overview of the MEMS market. The firm says emerging consumer applications are boosting the growth of the MEMS pressure sensor market and reshuffling the main players, MEMS pressure sensors are one of the very first MEMS components appearing in the microsystem world.

The technologies are quite mature and the market is big and expected to grow from $1.9 billion in 2012 to $3 billion in 2018. MEMS pressure sensors for consumer applications, especially for smartphones and tablets, is following the model of accelerometers and gyroscopes. This adoption should help the MEMS pressure sensor market to boom again.

This huge opportunity is expected to result in the global volume of the MEMS pressure sensor market to hit 2.8 billion units by 2018 says Wenbin Ding, Technology & Market Analyst, MEMS Devices & Technologies at Yole Développement.

"Consumer pressure sensor will represent 1.7 billion units and will overtake automotive as the market leader in volume,"she adds.

Even though consumer applications have a much lower ASP than other applications, this promising segment will bring more than 8 percent CAGR to the global MEMS pressure sensor market .

Yole's report presents a global overview of the current MEMS pressure sensor technologies, market and competitive landscape.

The covered industries in the MEMS pressure sensor 2013 report are automotive, industrial, medical applications, consumer electronics and high-end (aeronautic, military, defence) applications.

Automotive applications are still dominating this market. TPMS, MAP and BAP will be the biggest sub applications in this field. Automotive, medical, industrial and high-end markets are growing by 4 to 7 percent.

However the consumer market is growing 25 percent in value, equating to 38 percent in volume, because of new opportunities in smartphones and tablets.

MEMS pressure sensors find new applications in each domain,
For example, in cylinder pressure sensing for automotive, CPAP (Continuous Positive Airway Pressure) machine for medical use, smartphone (Samsung Galaxy SIII for indoor navigation) and tablets for consumer electronics industry, among other things.

All these emerging applications are still in their infancy, but they appear promising and Yole analysts believe MEMS pressure sensor will find new ways to satisfy end users in each domain.

MEMS technologies are still gaining market share compared to other classic technologies. Pressure sensors in particular are showing advantages compared to other current technologies, such as ceramic thick-film, ceramic capacitive and thin-film technologies.

Thin-film technologies are still needed for use in harsh environments, particularly with high temperatures and corrosive medias. MEMS pressure sensor manufacturers are also working on components which could be used in these environments. Since the MEMS pressure sensor market is huge, it's not surprising that more than 50 players are involved. Yole says the top 5 players are Bosch, Denso, Sensata, GE Sensing and Freescale.

Together they represent about 50 percent of the total market. Automotive, medical, industrial, and high-end markets already have their mature leaders and smaller companies following. The consumer electronics market is still emerging with some conventional MEMS sensor companies interested.

Lots of companies are targeting this industry but Bosch has always dominated this sector. The supply chain of the automotive industry is complicated with different types of players: Car Manufacturers, Tier1 Automotive Part & Systems Suppliers (related to Pressure Sensors), Full Package Sensors Specialists and MEMS & Semiconductor Specialists.With new opportunities appearing in consumer electronics, new comers from the USA and China are targeting this segment.

According to Yole, local Chinese companies are making an effort to try and fulfil the huge domestic demand in automotive and consumer applications.

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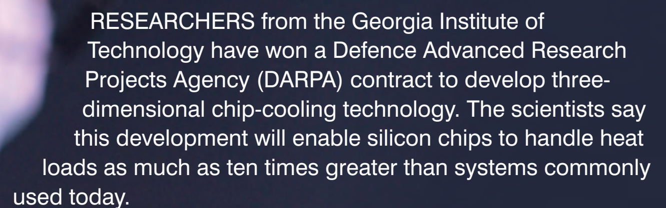
DARPA invests $2.9 million in cooling silicon chips



RESEARCHERS from the Georgia Institute of Technology have won a Defence Advanced Research Projects Agency (DARPA) contract to develop three-dimensional chip-cooling technology. The scientists say this development will enable silicon chips to handle heat loads as much as ten times greater than systems commonly used today.

In addition to higher overall chip heat dissipation demands, the new approach will also have to handle on-chip hot-spots that dissipate considerably more power per unit area than the remainder of the device. Such cooling demands may be needed for future generations of high-performance integrated circuits embedded in a wide range of military equipment. “There is really no good way to address this heat dissipation need with existing technology, and the problem is getting worse because computing power is increasing and the capabilities being put on chips are expanding,” says Yogendra Joshi, a professor in Georgia Tech’s Woodruff School of Mechanical Engineering and the project’s principal investigator.

“There is a real need for developing schemes that can address high power on the whole chip coupled

with very high power dissipation areas that are only a few millimetres square," he adds.
DARPA's Microsystems Technology Office, which provided the three-year $2.9 million contract, is seeking techniques to dissipate heat of as much as one kilowatt per square centimetre in the overall integrated circuit, and five kilowatts per square centimetre on smaller areas. The research is part of DARPA's Intrachip/Interchip Enhanced Cooling (ICECool) program.
"The approaches that we are talking about are relatively high-risk," notes Joshi, who specialises in electronic cooling from the chip-level on up to full-sized data centres. "They have not been tried before, so there are real questions of reliability – whether they can hold up under repeated cycles of being powered up and powered down."

In addition to Joshi, the research team includes:

- Muhannad Bakir, an associate professor in the Georgia Tech School of Electrical and Computer Engineering, who specialises in three-dimensional interconnected systems;
- Andrei Fedorov, a professor in the Georgia Tech School of Mechanical Engineering, who specializes in understanding and utilising unique physical properties at the nanoscale, and Suresh Sitaraman, also a professor in the Georgia Tech School of Mechanical Engineering, who specializes in evaluating electronic device reliability through innovative characterization techniques and physics-based modelling.
- Georgia Tech researchers Muhannad Bakir, Andrei Fedorov, Yogendra Joshi and Suresh Sitaraman are developing three-dimensional chip cooling technology that will be able to handle heat loads as much as ten times greater than systems commonly used today.

While applications for the high-powered chips aren't specified, their installation in systems intended for field use will add to the level of challenge.

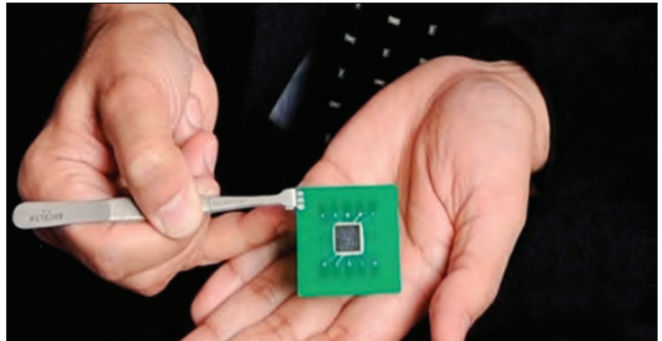
"For speed and performance issues, this computing power may be embedded where it is needed in the field," Joshi adds. "The challenges of cooling these high performance integrated circuits will be even more challenging because they will operate in environments that may be adverse compared to an office or computer room situation."

There are a number of significant challenges ahead.
The first is in implementing non-uniform cooling using liquid evaporation in three dimensional integrated circuits. The program calls for two dies to be cooled together, but the approaches developed for that could be used in multiple stacked dies. Being able to cool smaller areas with higher heat dissipation needs will provide an additional challenge. Also, meeting reliability standards whilst ensuring that the coolant and vaporisation within tiny microfluidic passages does not induce liquid dry-out, passage cracking, fluid leakage or undesirable electronic performance is needed. Finally, fabricating micron-scale cooling structures smaller than the thickness of a hair in the integrated circuit stack and understanding the flow and heat transfer physics taking place at that scale is another of the aims.

"It is well known that cooling constraints play a critical role in designing electronic systems," says Bakir. He adds, "Often a favourable electronic system configuration may not be realizable due to lack of adequate cooling. The novel microscale thermal technologies that will result from this project will address the most demanding thermal needs of future heterogeneous 3-D nanoelectronic systems and will enable new levels of performance and energy efficiency."

Beyond the technology challenges, the researchers will also need to develop a detailed and fundamental understanding of how liquids boil at the micron size scale. "The physics of how liquids boil has been well studied for large systems such as power plant boilers," Joshi notes. "What we are talking about here is boiling that will take place in passages that are produced by microfabrication techniques that may be only 50 micrometres by 50 micrometres. The physics of what will be going on there is very different than what happens at the large scale, and how these liquids boil in the passages of interest will result in new scientific insights."

Selecting an appropriate coolant able to provide the necessary phase change performance, while not damaging the silicon chips, will be part of the project. In an earlier research program supported by the Office of Naval Research, Georgia Tech developed new coolant candidates that will be considered along with traditional dielectric fluids. The research will be done in collaboration with industry partner Rockwell-Collins, a major manufacturer of electronic systems for the military. That collaboration will help ensure that solutions developed will be compatible with defence system requirements.



"The challenges for material characterization and physics-based modelling are to consider the larger features of the electronic system without overlooking the micrometer and sub-micrometre scale features that are the main locations for fracture and failure," says Sitaraman. "Mechanical characterisation and physics-based modelling will be important to understanding the reliability of microelectronic systems operating with fluid passages."

Beyond meeting the project requirements, the research will produce technology advances that should be broadly useful for future microsystems.

"The technologies we have proposed aim to explore uncharted territory in multiple science and technology domains to bring about an order-of-magnitude improvement in the current state-of-the-art," says Fedorov. "The project represents a significant challenge on the most fundamental level of materials and fluid behaviour down to the sub-micron scale. We're confident that this project will produce some really new technologies to address the needs of future 3-D microsystems."

- This research is supported by DARPA under contract HR0011-13-2-0008.

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INDUSTRY RESEARCH

Self-healing circuits are a reality?

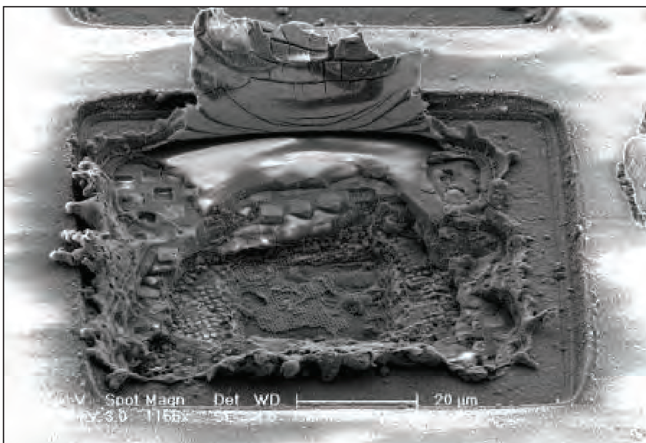
Researchers have found that electronic chips can repair themselves.

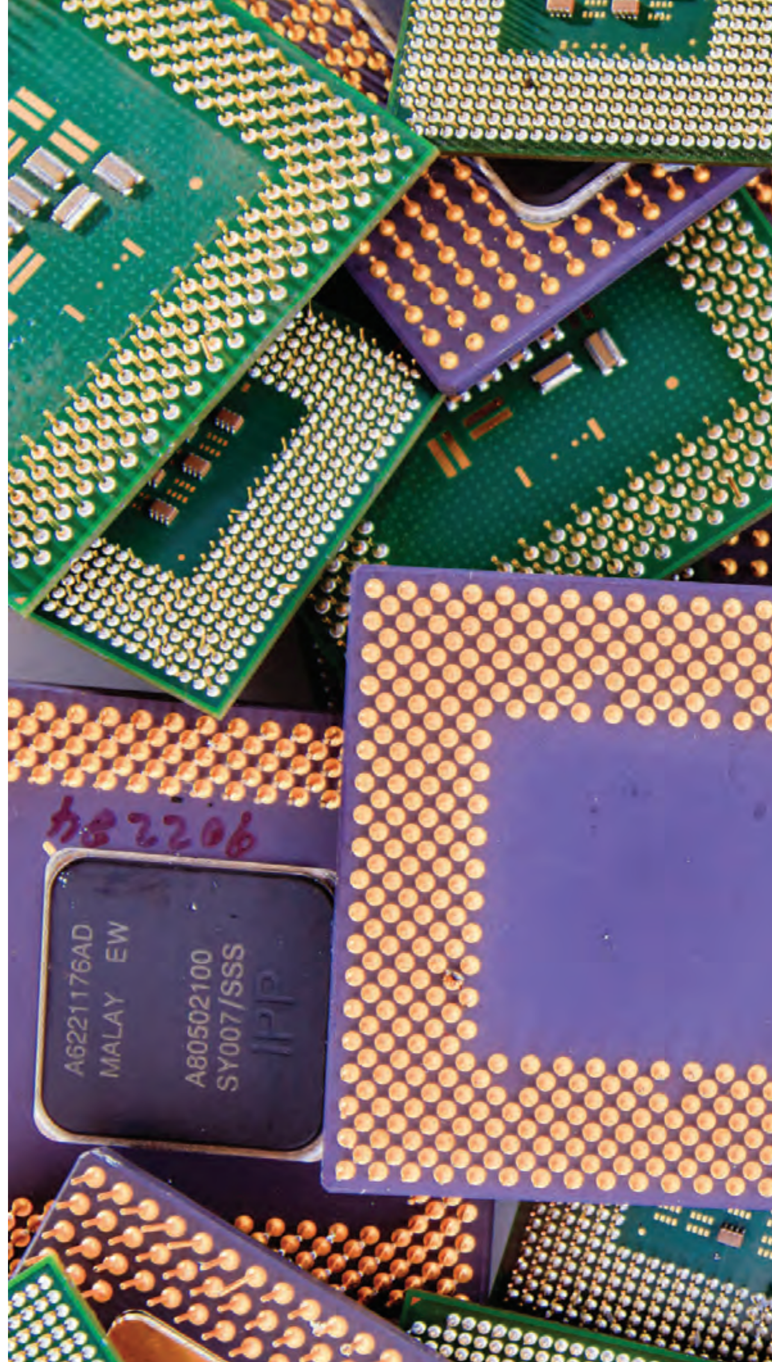
IMAGINE THAT THE CHIPS in your smart phone or computer could repair and defend themselves on the fly, recovering in microseconds from problems ranging from less-than-ideal battery power to total transistor failure. It might sound like the stuff of dreams, but a team of engineers at t he California Institute of Technology (Caltech); say they have, for the first time ever, developed just such self-healing integrated chips.

The team, made up of members of the High-Speed Integrated Circuits laboratory in Caltech's Division of Engineering and Applied Science, has demonstrated this self-healing capability in tiny power amplifiers. The amplifiers are so small, in fact, that 76 of the chips - including everything they need to self-heal - could fit on a single penny.

In perhaps the most dramatic of their experiments, the team destroyed various parts of their chips by zapping them multiple times with a high-power laser, and then observed as the chips automatically developed a work-around in less than a second.

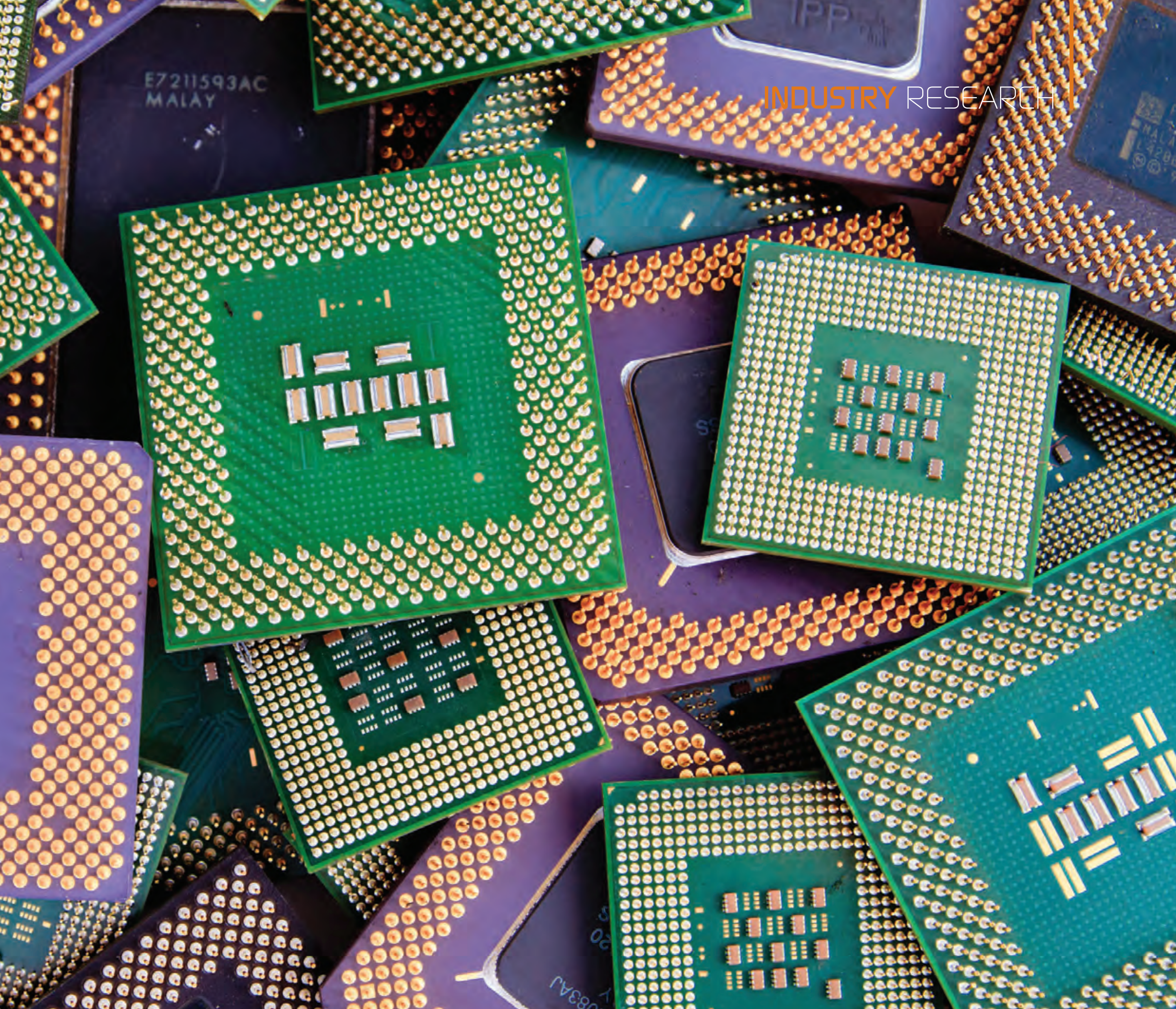
"It was incredible the first time the system kicked in and healed itself. It felt like we were witnessing the next step in the evolution of integrated circuits," says Ali Hajimiri, the Thomas G. Myers Professor of Electrical Engineering at Caltech. "We had literally just blasted half the amplifier and vaporised many of its components, such as transistors, and it was able to recover to nearly its ideal performance."





Until now, even a single fault has often rendered an integrated-circuit chip completely useless. The Caltech engineers wanted to give integrated-circuit chips a healing ability akin to that of our own immune system - something capable of detecting and quickly responding to any number of possible assaults in order to keep the larger system working optimally. The power amplifier they devised employs a multitude of robust, on-chip sensors that monitor temperature, current, voltage, and power. The information from those sensors feeds into a custom-made application-specific integrated-circuit (ASIC) unit on the same chip, a central processor that acts as the "brain" of the system. The brain analyses the amplifier's overall performance and determines if it needs to adjust any of the system's actuators - the changeable parts of the chip.

Amazingly, the chip's brain does not operate based on algorithms that know how to respond to every possible scenario. Instead, it draws conclusions based on the aggregate response of the sensors. "You tell the chip the results you want and let it figure out how to produce those results," says Steven Bowers, a graduate student in Hajimiri's lab and lead author of a recent paper describing the study. "The challenge is that there are more than 100,000 transistors on each chip. We don't know all of the different things that might go wrong, and we don't



need to. We have designed the system in a general enough way that it finds the optimum state for all of the actuators in any situation without external intervention," he adds. Looking at 20 different chips, the team found that the amplifiers with the self-healing capability consumed about half as much power as those without, and their overall performance was much more predictable and reproducible.

"We have shown that self-healing addresses four very different classes of problems," says Kaushik Dasgupta, another graduate student also working on the project.

The classes of problems include static variation that is a product of variation across components; long-term aging problems that arise gradually as repeated use changes the internal properties of the system; and short-term variations that are induced by environmental conditions such as changes in load, temperature, and differences in the supply voltage; and, finally, accidental or deliberate catastrophic destruction of parts of the circuits.

The Caltech team chose to demonstrate this self-healing capability first in a power amplifier for millimetre-wave frequencies. Such high-frequency integrated chips are at the cutting edge of research and are useful for next-generation communications, imaging, sensing, and radar applications. By showing that the self-healing capability works well in such an advanced system, the researchers hope to show that the self-healing approach can be extended to virtually any other electronic system.

"Bringing this type of electronic immune system to integrated-circuit chips opens up a world of possibilities," says Hajimiri. "It is truly a shift in the way we view circuits and their ability to operate independently. They can now both diagnose and fix their own problems without any human intervention, moving one step closer to indestructible circuits."

The work was funded by the Defence Advanced Research Projects Agency and the Air Force Research Laboratory.

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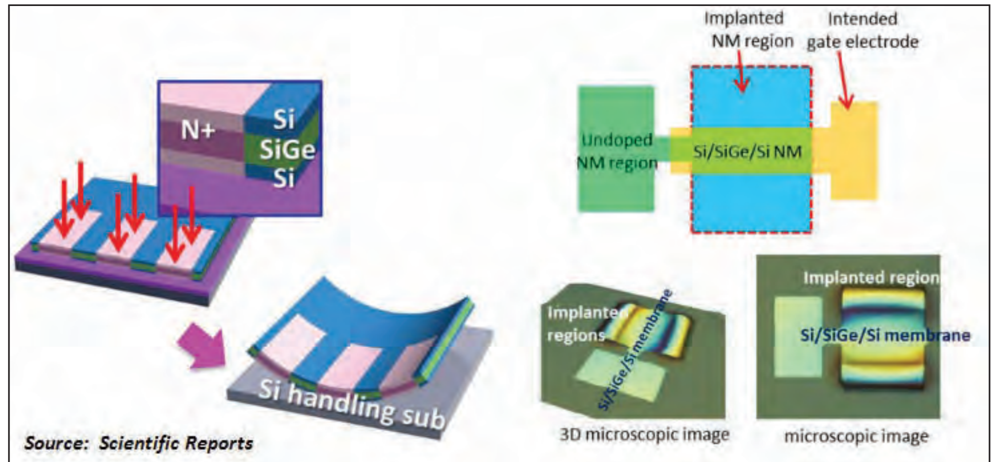
Further details of this research has been published in the paper, "Integrated Self-Healing for mm-Wave Power Amplifiers." by Foreman et al, in Microwave Theory and Techniques, IEEE Transactions, 61, 3, p1301 - 1315, 2013. DOI: 10.1109/TMTT.2013.2243750.

Doubling the speed & efficiency of flexible electronics

Stretching out the atomic structure of the silicon in the critical components of a device can be a good way to increase a processor's performance.

HISTORICALLY, the semiconductor industry has used strained silicon to squeeze a bit more efficiency and performance out of the conventional microprocessors that power the desktop and laptop computers we use today.

However, manufacturers' inability to introduce strained silicon into flexible electronics has limited their theoretical speed and power to, at most, approximately 15 gigahertz.



Source: Scientific Reports

Now, thanks to a new production process being pioneered by University of Wisconsin-Madison engineers, that cap could be lifted.

"This new design is still pretty conservative," says Zhenqiang (Jack) Ma, a professor of electrical and computer engineering. "If we were more aggressive, it could get up to 30 or 40 gigahertz, easily."

Ma and his collaborators reported their new process in Nature Scientific Reports on February 18th, 2013. Ma tried to address a paradox for straining and doping silicon electronics built on a flexible substrate. The straining process is similar to stretching out a T-shirt: the researchers pull a layer of silicon over a layer of an atomically larger silicon germanium alloy, which stretches out the silicon and forces spaces between atoms to widen.

This allows electrons to flow between atoms more freely, moving through the material with ease-just as a T-shirt stretched over a dummy will have more space between threads, allowing it to breathe.

The problem comes during the doping process. This critical step in semiconductor manufacturing introduces impurities that provide electrons that ultimately flow through the circuit. Doping a stand-alone sheet of strained silicon is like ironing a decal onto a stretched T-shirt. Just as an ironed-on design cracks when the T-shirt is stretched and unstretched, the act of doping distorts the flexible free-standing silicon sheet, limiting its stability and usefulness as a material for integrated circuits.

Ma believes that using the material to design next-generation flexible circuits will yield flexible electronics that offer much higher clock speeds at a fraction of the energy cost. "We needed to dope this material in a way that the lattice structure within would not be distorted, allowing for silicon that is both strained and doped," says Ma. The solution is akin to dying a pattern into the fabric of a shirt, rather than ironing it on. Ma and his UW-Madison collaborators - Max Lagally, the Erwin W. Mueller Professor and Bascom Professor of Surface Science and Materials Science and Engineering; and Paul Voyles, an associate professor of materials science and engineering - have developed a process through which they dope a layer of silicon, then grow a layer of silicon germanium on top of the silicon, then grow a final layer of silicon over that. Now, the doping pattern stretches along with the silicon. The structure is shown in the schematic at the top of this story.

"The structure is maintained, and the doping is still there," says Ma. The researchers call the new structure a "constrained sharing structure." Ma believes that using the material to design next-generation flexible circuits will yield flexible electronics that offer much higher clock speeds at a fraction of the energy cost. The next step will be to realise processors, radio frequency amplifiers, and other components that would benefit from being built on flexible materials, but previously have required more advanced processors to be feasible. "We can continue to increase the speed and refine the use of the chips in a wide array of components," says Ma. "At this point, the only limit is the lithography equipment used to make the high-speed devices."

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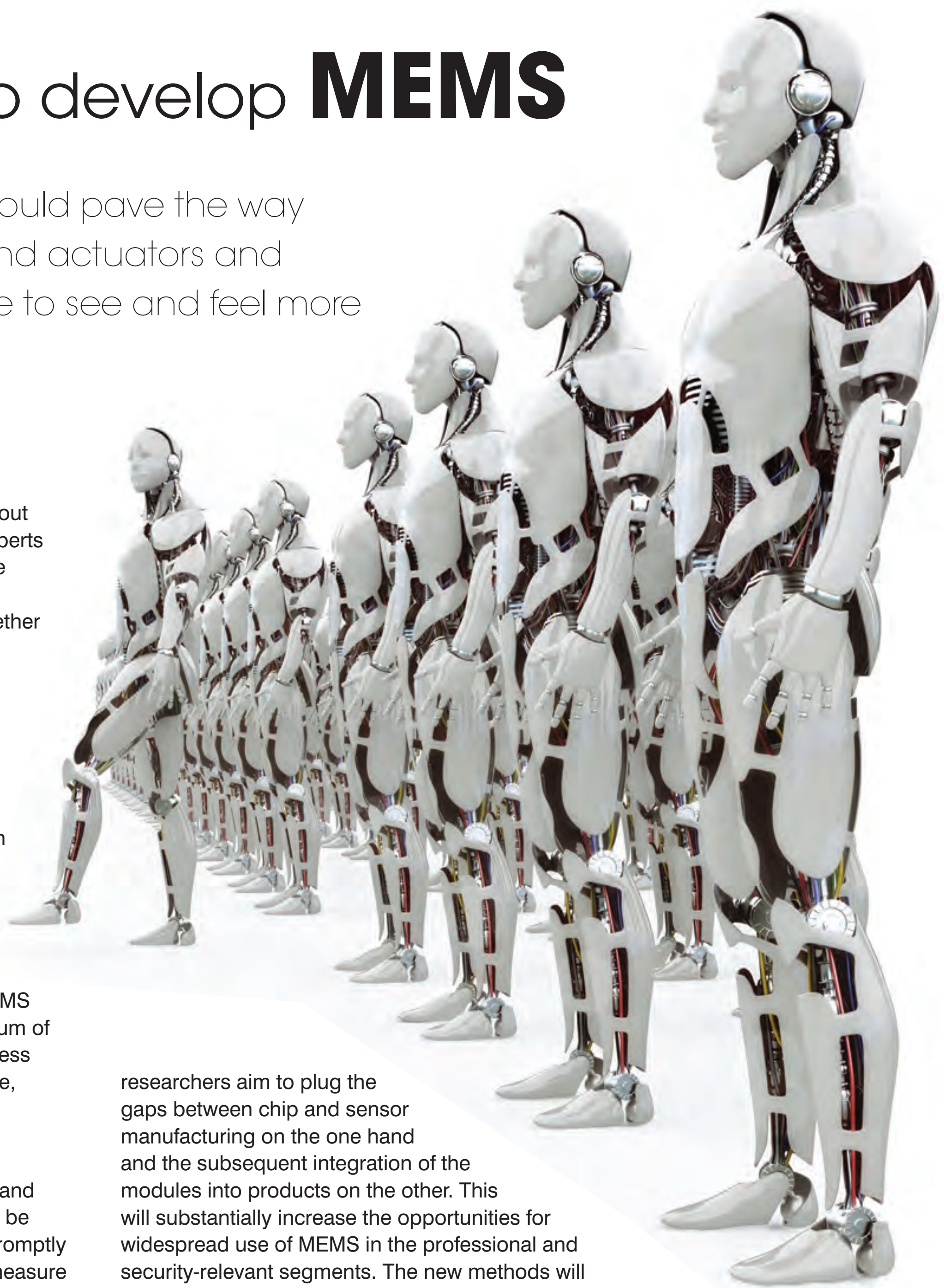
This work is further described in the paper, "Fast flexible electronics with strained silicon nanomembranes," by Han Zhou et al in Scientific Reports, 3, Article number: 1291. DOI : 10.1038/srep01291

A new way to develop **MEMS**

A novel methodology could pave the way for innovative sensors and actuators and robots which will be able to see and feel more effectively in the future.



EDACENTRUM says the design of micro-electromechanical systems (MEMS) is about to undergo a technological revolution. Experts from research institutions and industry are investigating entirely new methods for developing MEMS. They are working together in the research project known as "Circuit Diagram-Based Design of MEMS for Applications in Optics and Robotics" – or MEMS2015 for short.

This project is funded by the Federal Ministry of Education and Research (BMBF) and coordinated by Robert Bosch GmbH. The aim is to develop the first ever universal design methodology for MEMS to plug the gaps between electronics and mechanics design, manufacturing, and subsequent integration into products. MEMS are tiny components that require a minimum of space to measure and electronically process parameters such as acceleration, pressure, distance, temperature, light, or chemical concentrations.

With their sophisticated, compact sensor and actuator systems, MEMS can for instance be used to ensure that airbags are inflated promptly before a car is involved in a collision, to measure blood pressure or oxygen content in intensive care applications, or to enable digital cameras to eliminate camera shake.

Potential 50 percent increase in the market for MEMS

The new development methods for MEMS will allow innovative sensor and actuator systems to be developed – providing robots, for instance, with more effective sight and touch in the future. What is more, the potential market for MEMS stands to increase by up to 50 percent as a result.
Using a type of modular system, the MEMS2015 researchers aim to plug the gaps between chip and sensor manufacturing on the one hand and the subsequent integration of the modules into products on the other. This will substantially increase the opportunities for widespread use of MEMS in the professional and security-relevant segments. The new methods will also allow small and medium-sized enterprises to design MEMS and integrate them into their products much more often, as well as in a wider range of configurations than at present.

Projecting images directly onto the retina

These new development methods for MEMS will pave the way for entirely new solutions in the leading-edge applications of optics and robotics. This opens up the prospect of the wide-ranging use of micromirror arrays, similar to the devices already being used in projectors. This technology

> These new development methods for MEMS will pave the way for entirely new solutions in the leading-edge applications of optics and robotics. This opens up the prospect of the wide-ranging use of micromirror arrays, similar to the devices already being used in projectors.

allows images to be projected directly onto the retina using special glasses. In robotics, force sensors and profilometers can be developed that analyse surfaces even more accurately than before, or that simulate an extremely precise sense of touch. The project findings are being verified as part of the project on the basis of real MEMS prototypes which, in turn, serve as demonstrators.

"The project opens up innovations in mechanical engineering and process plant engineering by using powerful sensor and actuator systems based on groundbreaking MEMS and chip technologies," says Mirco Meiners, the project coordinator for MEMS2015 who works in the Bosch Automotive Electronics division.

"The clear focus of funding from Germany's Federal Ministry of Education and Research (BMBF) helps companies maintain their lead in innovation for key technology topics and develop new innovative, complex products."

"The MEMS2015 project raises the bar when it comes to the quality and especially the productivity of MEMS design," says Ralf Sommer, the scientific director of the Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH, one of the eight partners in the project.

Photo by Andreas Karguth

The image shows a test of a "BioRob" arm with a smart phone: which would not exist without MEMS

"Basic concepts such as circuit diagram-based design, which are already successfully used in microelectronics design, are now being transferred to MEMS design. This offers users enormous advantages: for one thing, MEMS2015 facilitates new highly complex products, such as micromirror arrays, and speeds up the process of bringing them to market. For another, the project will allow us in the long run to produce a Lego-brick-style design. This will above all benefit small and medium-sized enterprises, allowing them to put together their own individual, tailor-made solutions in a flexible modular MEMS and electronics system."

Eight partners from research and industry

The MEMS2015 research project, which has a three-year term and around 3.5 million euros in funding from Germany's Federal Ministry of Education and Research (BMBF) as part of the German government's High-Tech Strategy and the ICT 2020 development program, brings together the potential of eight partners from research and industry. These are Cadence Design Systems GmbH, Carl Zeiss SMT GmbH, Institut für Mikroelektronik- und Mechatronik-Systeme GmbH, Robert Bosch GmbH, the Technical University of Munich, TETRA Gesellschaft für Sensorik, Robotik und Automation mbH, the University of Bremen, and X-FAB Semiconductor Foundries AG. The edacentrum in Hannover is responsible for project management for MEMS2015.

Edacentrum is an institution dedicated to promote electronic design automation (EDA) research and development funded by the BMBF (Federal Ministry of Education and Research). It initiates, evaluates and supervises industry-driven R&D projects and offers a comprehensive spectrum of services on all matters concerning EDA, particularly project management of R&D projects.

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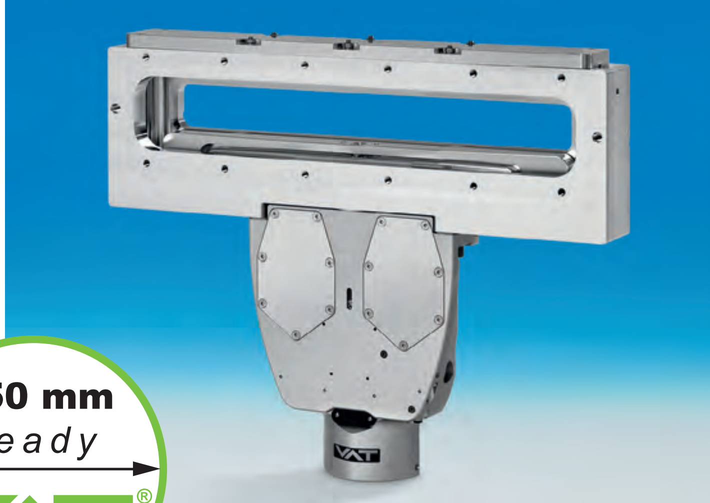
Transfer valve for 450 mm wafer technology
L-MOTION valve for corrosive high-end semiconductor applications



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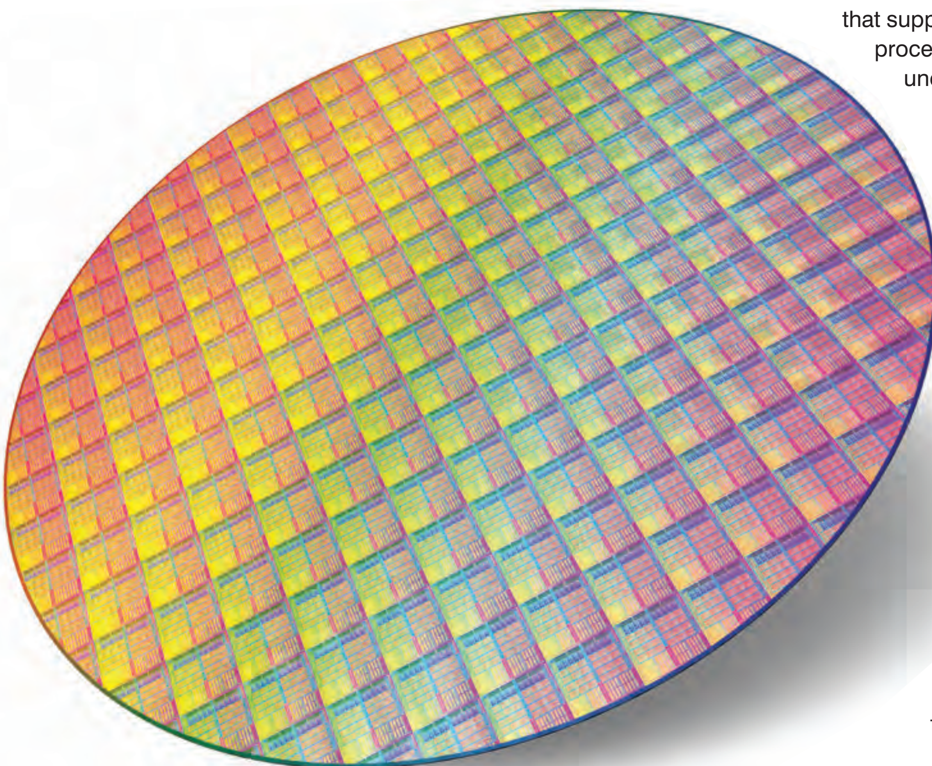
The Business of Science®

Brewer Science aims to revolutionise wafer bonding

Brewer Science, inventor of anti-reflective coatings that have contributed to the progress of advanced lithography, continues to push the boundaries of diverse technology solutions for device fabrication. CTO Tony Flaim tells Dr Su Westwater, @ Silicon Semiconductor why ZoneBOND technology has significant advantages over conventional TSV.

FROM front end to back end, there are a number of intricate steps which a wafer must go through to become a finished product or chip. After processing, bonding and debonding is one of these. This is illustrated in fig 1 which gives an idea of the processes a wafer must go through.

Now, Brewer Science has made a new development in wafer bonding. The company has a TSV or "through silicon via" patented ZoneBOND temporary wafer bonding process through its latest developments. The firm develops and supplies materials, processes, and equipment for carrier-assisted ultrathin wafer handling, which is generally, recognised as a critical need within most backside TSV processing flows. (Fig 2)



But what are the advantages of ZoneBOND over other competitor's solutions? Su Westwater asks the expert, Tony Flaim, about this technology.

Q What are the main advantages of this process over other TSV etching?

A The firm's expertise centres on the use of thermoplastic polymeric bonding materials for temporarily attaching device wafers or other electronic substrates to a rigid carrier that supports the substrate while it is being thinned and processed on the backside at high temperatures and under vacuum.

Brewer Science's bonding materials and specialised carrier treatments enable the carrier, which is typically a silicon or glass wafer, to be removed from the bonded structure at room temperature and using very low force after backside processing has been completed.

This mode of debonding is a key step in the Brewer Science ZoneBOND temporary wafer bonding process, which has been widely embraced by the industry and is the process of record at several international microelectronic research consortium sites.

In the ZoneBOND process, the thin device wafer is usually attached to a film frame or another carrier prior to removing the primary carrier so that the thin device wafer

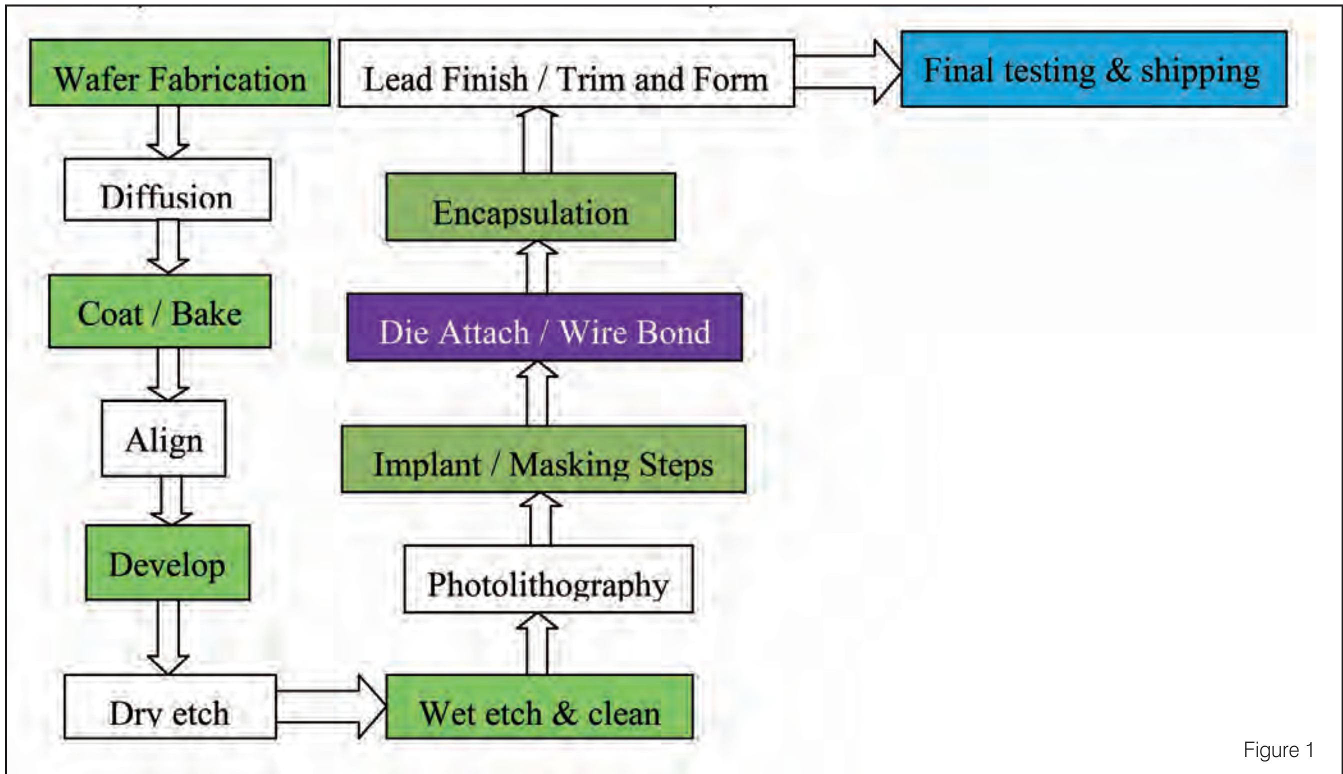


Figure 1

can be further handled without damage. Unlike the photo- or thermally cured adhesives used in most other temporary wafer bonding processes, which must be removed by peeling, our WaferBOND and ZoneBOND thermoplastic bonding materials can be readily removed by solvent cleaning to leave a residue-free wafer surface. The industry is investigating other low-stress debonding methods such as laser debonding in which the carrier is released from the adhesive layer by a laser scanning process that decomposes a special release layer on the carrier surface. This approach has two main drawbacks.

Firstly, it requires a specialised, optically transparent carrier, meaning an ordinary silicon carrier cannot be used as in the ZoneBOND process.

Secondly, the laser scanning procedure is slow, which translates to low wafer throughput.

Q Can this process be used for GaN on silicon or any other up and coming structures?

A Yes, according to Flaim. He says, “We have shown that our temporary bonding materials and processes can be adapted to transfer ultrathin epitaxial layers such as GaN and InP from a growth substrate to a final device substrate. Our original demonstration involved transferring ~ 5μm thick GaN layers grown on sapphire after removing the bulk of the sapphire by backgrinding.”

So it seems that this technology could be adopted throughout the whole semiconductor value chain.

Q But what are the challenges to its adoption?

A There are two main challenges to adoption, but this applies to all temporary wafer bonding processes.

The first is that semiconductor manufacturers and advanced packaging suppliers are largely unfamiliar with wafer bonding processes (permanent or temporary) and the many associated steps involved with spin-applying, baking, and cleaning polymeric bonding materials that can be 50-100μm thick.

Hence such manufacturers are walking on much unknown territory. What’s more, there is a lack of highly integrated materials, processes, and high-volume manufacturing (HVM) equipment for temporary wafer bonding. And in some cases, HVM equipment for certain processing steps is not available.

Q So who are the main competitors and processes in the market who compete with this and other technologies?

A One of the main competing temporary wafer bonding processes was mentioned above and utilises laser debonding to remove the carrier.

There is a variant of laser debonding in which the adhesive is a photo-cured material. It must be removed by peeling and tends to leave insoluble residues on the device wafer surface. Another competing process utilises a specialised peel-type release layer that must be deposited on the device wafer surface by

chemical vapour deposition (CVD). The requirement for CVD increases cost of ownership and reduces wafer throughput. Older temporary bonding processes that utilise thermal slide debonding or solvent dissolution of the adhesive to separate the device wafer are still in some use but are considered too slow and/or too low yielding for reliable HVM, especially with 300mm wafer sizes.

Q How do these competitors compare in terms of performance and cost to your process?

A From the perspective of the industry, all temporary bonding processes now being evaluated are not sufficiently reliable and are too expensive. We believe our challenges in that regard are very manageable and can be or will be addressed in the course of making normal progress and gaining experience. Our main objectives for improving the reliability and reducing the cost of our process are as follows:

- Increase the mechanical stability of our bonding materials at temperatures above 250°C to eliminate the possibility of thin wafer edge lifting and blistering and reduce stress-induced wafer bowing.
- Formulate our bonding materials to provide at least a 50μm thickness with improved surface planarity when applied by spin coating. Achieve post-bonding total thickness variation (TTV) of ≤ 3μm at a bond line thickness of 50μm.
- Reduce cleaning chemical consumption to one-tenth of current usage for removing bonding materials from fully processed thin device wafers. • Reduce carrier removal time to < 3 min/wafer.

Q So what does the future hold for Brewer Science and what part will they play as the industry looks to 450mm manufacturing?

A The application of temporary bonding processes to 450mm wafer sizes is definitely a long way in the future. The bulk of the applications will likely be at 300mm until the end of the decade," notes Flaim.

However, he does mention that Brewer Science plans to be very active in the 450mm space through its lithographic materials

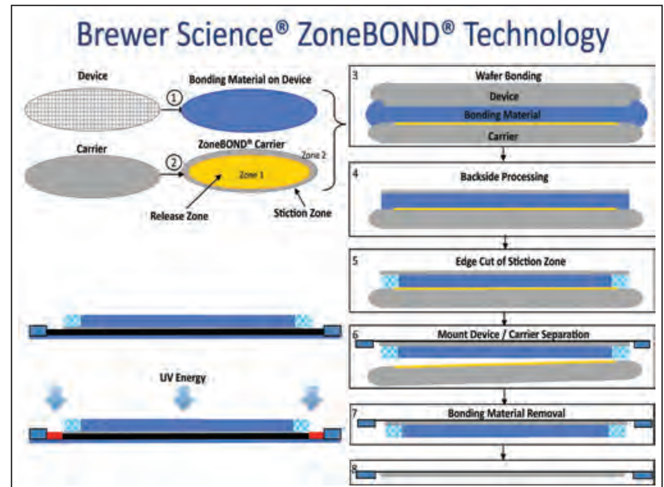


Figure 2

business, which has been the mainstay of its operation for over 30 years.

Q How do you see this going forward - what are your targets for the future?

A The use of temporary bonding and the ability to process ultrathin substrates on a carrier are concepts for which the industry is only beginning to scratch the surface as far as applications are concerned. Ultimately, Flaim believes that in the future, carrier-assisted handling will be viewed as a means for transferring layers as thin as graphene from one substrate to another.

It is conceivable that subtractive processing in which multiple device levels are created by sequential deposition and etching steps may be replaced by "stacking" techniques in which a level or series of levels are forged on one substrate and then transferred and bonded to a final, permanent substrate. Brewer Science says it wants to help device makers see the many possibilities of ultrathin layer stacking as a new approach to integrated device construction.

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> "We have shown that our temporary bonding materials and processes can be adapted to transfer ultrathin epitaxial layers such as GaN and InP from a growth substrate to a final device substrate. Our original demonstration involved transferring ~ 5µm thick GaN layers grown on sapphire after removing the bulk of the sapphire by backgrinding."

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- Superior load and controllability for increased material removal rates, while maintaining low surface damage
- Enhanced plate flatness monitoring and higher accuracy jig control for superior flatness and TTV
- Development of user friendly, industry standard software platforms.

In response to client and market demand Logitech has developed a High Speed Lapping and Polishing System, primarily for hard materials. This benchtop solution is ideally suited to research laboratories and small scale production, due to its flexibility, reliability and low cost of ownership. The system is perfect for the processing and pilot production analysis of Silicon and Silicon based substrates.

An array of advanced in-situ sensors constantly provide the operator with real-time process information. Monitored parameters include Coefficient of Fricton, slurry and pad/plate interface temperatures.
All of which are paramount for optimal performance. The High Speed Lapping and Polishing system can process substrates, wafers and part wafers up to 100mm/4" diameter quickly and easily due to the 300rpm variable plate speed and higher sample load capability. The user friendly interchangeable plate/pad design ensures that the High Speed system maintains maximum efficiency across the complete process. This is further highlighted with the high level of automated system operations and programmability, allowing full processes or sub processes to be run with minimal intervention.

Key applications for Logitech Lapping and Polishing Systems include:

- Wafer polishing to sub-nm levels
- Removal of epi-layers with nanometer level precision
- Capability to delayer up to 100mm (4") diameter wafers
- Polishing accuracy to nanometer levels for fault isolation
- Preparation of substrates for use in electronic device manufacture

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A CLEAR EDGE: Innovation in vacuum and abatement technology drives savings for fabs?

Over the last 15 years vacuum and abatement technologies have made steady gains in performance and efficiency. Incrementally, the advances may escape notice, but when considered together, the benefits are significant. Mike Percy, Business Manager, Semicon Vacuum, Edwards and Michael Boger, Global Market Sector Manager, Semicon, Edwards consider the technological advancements and identify the opportunities to realize cost savings.

Semiconductor manufacturing provides a convincing example of what can be achieved when an industry is built on the premise that 'good enough never is'. For decades naysayers have warned that fundamental limits will soon prevent further advances in integrated circuit performance, and for decades scientists and engineers have found clever ways to take just one more step. The generations of process vacuum and the abatement of noxious process chemicals and by-products, though perhaps not the most glamorous aspects of the industry, are nonetheless absolutely essential capabilities, and the technologies used to provide them have had to evolve along with the process.

Recent years, in particular, have brought an increasing emphasis on saving energy to reduce manufacturing costs and to minimise the adverse effects of the industry on the environment. The result has been a continuous stream of incremental improvements, and while each has been significant in its own right, it is only in their cumulative effect that their full benefit becomes

apparent. We recently had an opportunity to perform an interesting experiment and the results illustrate powerfully the cumulative value of constant innovation.

Greenfield fab development: an ideal case study

A major semiconductor manufacturer undertook the green field development of a new foundry and commissioned Edwards Group to be the exclusive provider of vacuum and abatement systems. This provided Edwards with the opportunity to develop, first hand, a complete list of equipment required for such an undertaking - a list that is not easy to compile otherwise given the complexity of a modern semiconductor fab. The facility was designed to process 40,000 wafers per month. Ultimately, it required nearly 1,500 vacuum pumps and over 260 abatement units -- all connected to nearly 400 process tools. The equipment list allowed us to look back at the various technologies we had introduced over four generations of development, starting 15 years ago (when DRAMs had a 250μm half pitch), and calculate the cost savings accruing to the current generation from each generation past.

Cost savings

In the end, we determined that advancements in abatement technology now deliver more than $17.8M per year in utility cost savings, $15M of which is achieved through over a 90% reduction in water consumption and the remainder from reductions in fuel consumption. Advancements in vacuum pump technology now provide more than $3.3M per year in utility cost savings, the majority through improvements in pump mechanisms and the remainder through green mode operation that cuts energy consumption during idle periods. When new products currently in development come into production, we expect to be able to deliver an additional $1M per year in savings.

Key metrics

As the semiconductor industry continues to evolve, production models have become increasingly sophisticated, allowing manufacturers to measure and predict costs more precisely and promoting cost-of-ownership as a key metric in equipment usage and acquisition decisions. Power consumption is a significant contributor to cost of ownership, particularly in localities where environmental concerns or other factors restrict increases in power generation and distribution. SEMI specification S23 establishes standards for measuring and reporting energy consumption as well as targets for reducing energy usage. Any cost of ownership evaluation of an abatement system must include not only power consumption, but also any treatment and disposal costs for by products and effluents of the system under consideration (for instance, water supply and treatment costs).

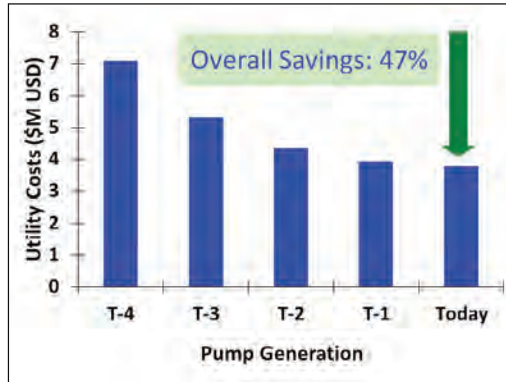

Figure 1 Overall utility cost for each generation of vacuum pump technology

In the 15-year period covered by this analysis (1997 to 2012), device sizes have shrunk by an order of magnitude (DRAM half pitch has gone from 250 nm to 2X nm) and new processes and materials have greatly increased the complexity of semiconductor manufacturing. In that same period, process vacuum and abatement systems have evolved through roughly four generations, incorporating major innovations to increase efficiency and reduce operating costs. (In order to generalize this discussion and avoid overly frequent references to Edwards-specific model numbers, the generations are numbered negatively from TØ, the current generation, back through T-1, T-2, T-3 and T-4).

Innovation in vacuum pumps

Several trends are apparent over the four generations of vacuum pumps. Inverters have been added to permit energy efficient operation at varying speeds and enable low energy green mode when the pump is idle. Smaller mechanisms operating at higher speeds have increased efficiency in both power and material consumption. Pump designs have diversified with specific models customized to match the requirements of specific processes. Pumps have incorporated sophisticated thermal management to improve reliability and reduce energy consumption.

Dry pumps

Dry vacuum pumps were introduced for semiconductor manufacturing in the 1980's. Although available in a range of sizes they were all similar in design. With high reliability, oil-free

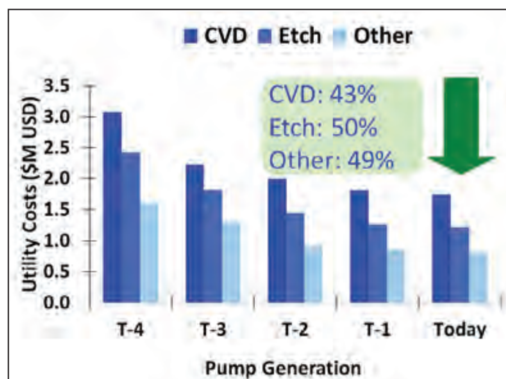

Figure 2 Process specific utility costs for each generation of vacuum pump technology

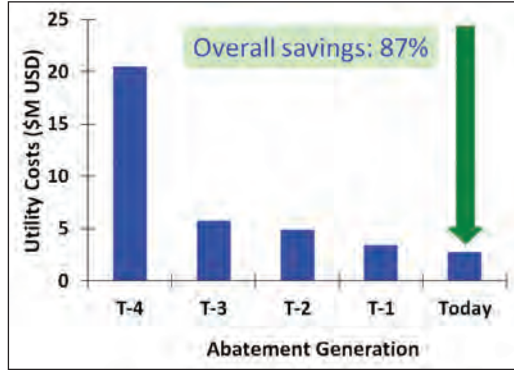

Figure 3 Overall utility costs for each generation of abatement technology

cleanliness and low maintenance requirements, their use proliferated in the industry. In the 1990's (T-4) pumps began to be designed for specific families of processes: one design for clean, light duty, and another design for dirty, harsh duty applications. By T-2, a medium duty pump application was introduced to address intermediate process conditions, such as those for processes such as dielectric material reactive ion etching.

In general, lighter duty pumps are designed with lower power motors with low torque capability for relatively clean applications such as wafer handling and load lock evacuation. Harsh duty pumps have the power and torque required for dirtier deposition processes and may incorporate special measures to prevent pumped gases from forming solids on internal components, or to handle powder and process by-products in the gas flow.

Introduction of inverter-driven motors for heavy-duty pumps

Looking at the evolution of harsh-duty pumps, generation T-3 saw the introduction of inverter-driven motors that not only enabled more efficient operation, but also allowed for the rotational speed of the pump to be increased significantly. By increasing the rotational speed, the physical size of the vacuum pump can be reduced. This reduction relates directly to the amount of material and energy required to manufacture the product. A convenient figure of merit for quantifying this savings is the ratio of peak pumping speed to mass of the pump. For harsh-duty pumps, this figure of merit represented up to 49% savings. Inverters also remove the dependence of pumping performance on the frequency of the electrical supply, a significant feature that can reduce the required time to stabilize a process for customers that operate globally.

Generations T-2 and T-1 also saw the introduction of additional process specific modifications, such as thermal management, which ensures precise control of internal temperatures to allow tighter mechanical tolerances and prevent gas condensation on critical pump components. Green mode, a selectable operating mode that reduces input power to the pump when in an idle state, saw introduction at T-2.

Table 1 Utility costs

Utility Costs Used in Modeling (USD)					
Electricity ($/kWh)	0.07	Natural gas ($/m^3)	0.10	Oxygen ($/m^3)	0.15
Compressed air ($/m^3)	0.05	Nitrogen ($/m^3)	0.06	Hydrogen ($/m^3)	0.5179
Industrial water and drain ($/m^3)	4.00	Process cooling water ($/m^3)	0.214	Cabinet extraction ($/m^3)	0.0005
Exhaust extraction ($/m^3)	0.0006	Process time	70%	Idle / maintenance time	30%

Load lock pumps - reducing scale & co-location

Light duty pumps are widely used to evacuate load locks, where they pump only air or nitrogen. In this application, the most important performance criterion is chamber evacuation time, the time it takes to reduce the pressure in the chamber from atmospheric to process levels. Load lock pumps have developed along two parallel axes. The first axis began with the introduction in T-3 of small, low vibration pumps that could be mounted directly beneath process tools on the same floor.

Eliminating the long pipe run from the tool to the sub-fab, where T-4 pumps were installed, permitted much smaller pumps to achieve the same evacuation performance. This, plus further improvements in small pumps that could be installed on or close to the tool (T-2 to TØ), reduced power consumption, physical volume, and mass by roughly 86%, while at the same time achieving a reduction in pump down time of 47%.

Introduction of inverters & increasing rotational speed

The second axis of development for load lock pumps followed a path similar to that of harsh-duty pumps: adding motor inverters, specialization in pumping mechanism design, and increasing rotational speeds. These changes resulted in equally dramatic improvements (T-3 to TØ), reducing power consumption, volume and mass by 79% and shortening evacuation time by 14%.

Gas a batement systems

The majority of abatement systems deployed in semiconductor manufacturing use heat generated through combustion to destroy noxious compounds in the exhaust gas stream. In the 15 years considered in this discussion, these systems also went through four generations of improvements, beginning at T-4 with the basic thermal processing unit which burned natural gas and used a continuous flow of water to scrub solid and gaseous combustion products from the exhaust stream. T-3 saw the addition of water recirculation, which reduced water consumption by 91% and generated significant savings in both

water supply and water treatment costs.

At T-2 a new combustor design increased the destruction and removal efficiency (DRE) of the system while reducing fuel costs by 39%. More inlets for process gases allowed the system to support up to six process tools simultaneously. (Since the gases are not mixed until they reach the combustor there is no requirement for compatibility or sequencing of the exhaust flows.) T-1 and TØ introduced green mode to reduce fuel consumption during idle periods, and automated monitoring and control of numerous system functions to increase system reliability and lengthen maintenance intervals.

Foundry cost modeling

To estimate the aggregate annual savings accruing from the effects of each generation of changes, engineers modeled the vacuum and abatement requirements of a state of the art fab based on the equipment list generated for the green field development of a major new foundry. The facility was designed to start 40,000 wafers per month. The final equipment list included approximately 1,500 vacuum pumps and 260 abatement units, supporting 400 process tools. Table 1 shows the assumptions used for utility and other costs. Figures 1 and 2 show the overall utility costs and process specific utility costs (respectively) for each generation of vacuum pumps. Figures 3 and 4 show the same information for each generation of gas abatement system.

Improving the efficiency of the installed base

Improvements in efficiency are not limited to equipment installed in new facilities. Upgrades to existing vacuum and abatement systems can provide significant utility savings. Figure 5 shows increases in energy efficiency for two different sizes of harsh duty pump, 80 m3/h and 600 m3/h pumping speeds, achieved by upgrading the motors to optimize performance around a tighter input voltage range and targeted operating vacuum level. The upgrades improved efficiency by 10 and 24 percentage points (respectively), and together reduce energy consumption by 570 watts.

Even larger improvements in efficiency, from 30% to 50%, can be achieved by upgrading gas abatement systems to current burner technology. The new burner can be used in most deposition and etch applications, except those using CF4 as a process of cleaning gas. The upgrade can be performed quickly and easily in the field.

If installed during required annual maintenance, when the burner is regularly replaced, the upgrade adds only about an hour of additional time. Depending on local fuel costs, the upgrade can pay for itself in as little as one year.

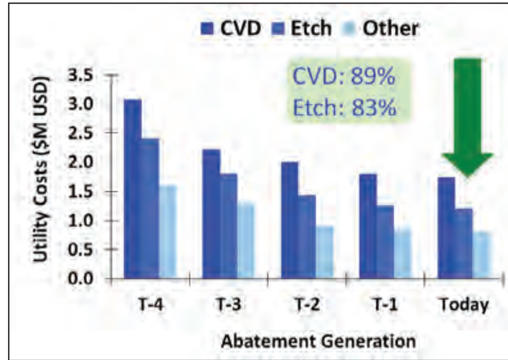

Figure 4 Process specific utility costs for each generation of abatement technology

Conclusion

The semiconductor industry never stands still. Neither can its equipment suppliers. This study demonstrates the value delivered by constant attention to improving efficiency, with annual savings totaling nearly $21M at a fab with a 40k wafer start capacity. For larger-scale fabs, or across a major manufacturer, these efficiency savings can multiply into a very significant sum, and is thus increasingly a topic of conversation at many customers, especially at the time of planning increased capacity, or upgrading lines.

Sitting across the table as a supplier, ongoing success requires continuous innovation to reduce product operating costs and environmental impact through improvements in energy efficiency and reductions in material consumption. It is equally important to support existing customers by addressing the same issues for installed systems with practical and economical upgrade paths. The R&D capability and expertise required to deliver such improvements is considerable, and only really available to the largest of vacuum players in the industry.

At Edwards, the experience gained in large-scale projects such as the Greenfield fab has been invaluable, providing numerous insights into the challenges, and rewards available at our biggest customers and placing some actual dollar values on the outcome. When combined with current industry developments such as EUV and 450mm, the pace of change is relentless, along with the pursuit of ever increasing efficiencies to support our customers and their businesses.

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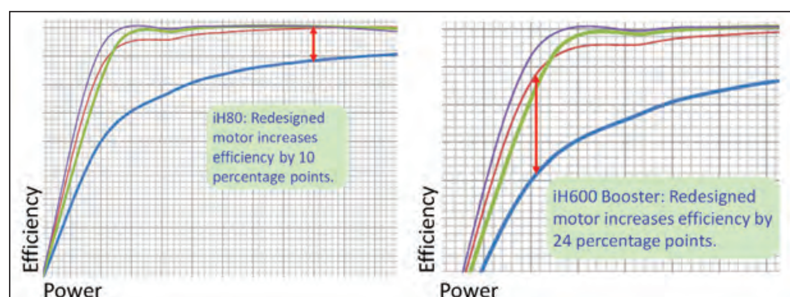
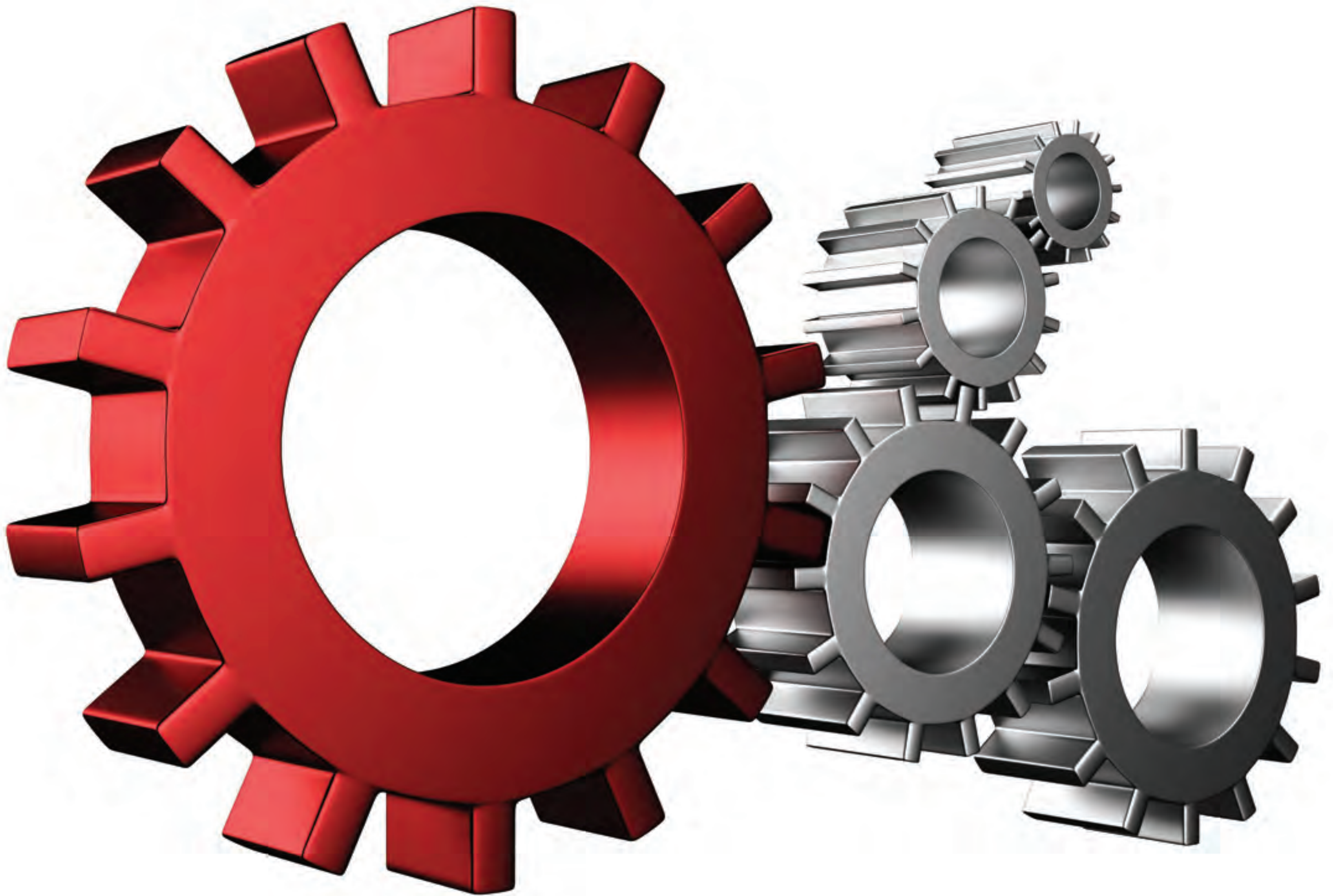
Figure 5 Increases in energy efficiency resulting from motor upgrades on installed vacuum pumps





Current trends with DRIE/DSE processing for MEMS devices and structures

The MEMS industry is outperforming the semiconductor market and is expected to continue annual double digit growth through 2015. This growth has fuelled the need for more sophisticated and higher performance processing equipment, in particular, plasma etching systems. **Thierry Lazerand, Technical Marketing Manager, Plasma-Therm, Inc.** looks at recent developments.

LED BY THE EMERGING CONSUMER MARKET, the MEMS industry has experienced a tremendous windfall after recovering from the global economic recession. In 2010, the MEMS market grew by twenty percent with an expected continued annual double-digit growth through 2015. Higher demands in consumer, industrial, medical, automotive, biomedical and other applications, the MEMS market is outperforming the overall semiconductor market by at least a factor of two. This growth is fuelling the need for more sophisticated, more efficient and higher performance processing equipment, and in particular, plasma etching systems used for out-of-plane structures, such as through-silicon vias (TSVs) and other features for MEMS devices. Deep Reactive Ion Etching (DRIE) or Deep Silicon Etching (DSE) is an industry-leading technology for creating high aspect ratio features in silicon for MEMS and nanotechnology applications. DSE is a type of anisotropic

etching technique that etches silicon indiscriminately with regards to the crystal planes, creating deep straight, trenches, and high aspect ratio side walls with excellent depth uniformity.

The most common DSE method, also known as the Bosch DRIE process, is a time-multiplexed anisotropic etching technique with alternating processing steps of passivation deposition and isotropic etching. A polymer-based passivation layer is deposited to selectively protect the surface of the substrate during the etching, preventing lateral etching of side structures. During the etch step, plasma enhanced etching is used to remove material i.e. silicon to define 3D micro-structures. The sequence is repeated, with each cycle removing a small portion at the bottom of the etched trenches or cavities until the desired depth is reached. Due to the repetitive nature of the process, the sidewalls of the vertical profiles typically become scalloped. This and other common limitations of the DSE process have been greatly improved by Plasma-Therm's Versaline DSE system.

Incorporated in 1975, Plasma-Therm has a long history, emerging as a leading supplier of plasma process equipment. Through experience and innovation, Plasma-Therm has developed and incorporated a range of key features in their Versaline platform, including a host of patented processing technologies. The Versaline DSE boasts high mask selectivity, low SOI notching and very fast process switching between the passivation and etching steps used to control scalloping effects. Other world-class processing equipment available as part of the Plasma-Therm Versaline platform include the Versaline ICP, the Versaline RIE, the Versaline PECVD and the Versaline HDPCVD.

DSE process overview

Plasma Etching or Dry Etching is a plasma based process that facilitates the removal of material from the surface of a substrate. Plasma-Therm has a unique three step process allowing optimization of passivation removal and the isotropic etch step. Competing products commonly uses two process steps; one for passivation and one for the combination passivation and isotropic etch. Since the passivation removal and isotropic etch are coupled together it is challenging to optimize both independently. This lack of decoupling is penalized with poorer etch selectivity. In comparison, a three step process can potentially have higher etch rate, allowing less polymer to be produced and increase the mean-time between cleaning (MTBC). Typically, plasma processing of semiconductor materials is performed in a vacuum environment. The key to dry etching is the creation of reactive species within the plasma that can react with the material on the substrate with the formation of volatile reaction byproducts. Dry etching processes are often broken into four mechanisms which must be understood for effective etch system design.

- Formation of active gas species.
  Gas species are activated within the plasma discharge area. These species include ions, electrons and radicals.
- Transport of the active species to the surface.
  The neutral species are transported to the substrate surface, mainly by diffusion, while the charged species are accelerated to the surface due to the negative bias on the substrate cathode.
- Reaction at the surface.
  This step can be further split into three sub-steps: the adsorption of the precursors, the surface reaction and desorption of the products. A wide variety of mechanisms occur during each sub step. For example, processes that depend mainly on the energy of the impinging ions are said to have a large physical component. During a chemical etch; activated neutrals react with the substrate independent of their kinetic energy. In practice most processes have both physical and chemical aspects.
- Pump down of the reaction products.
  After desorption, the volatile reaction products diffuse back to the bulk plasma. Here they are exhausted by a vacuum pump. The diffusion directions of etchants and reaction products are a result of concentration gradients of both species, in the bulk plasma and at the substrate surface.

DSE process requirements

Successful DSE processing depends on a range of process requirements. Some requirements can be customer specific, such as vertical sidewall smoothness and tapering of a TSV. Others are more universal and attribute to the process stability, efficiency, effectiveness and cost of system ownership.

DSE process requirements: profile control, sidewall morphology and etch rates

The etching uniformity across a wafer, from centre to edge, is a critical factor that will directly impact the consistency of the 3D structures being etched. Ideally, the structures in the outer side regions should be identical to the ones in the middle. This will ensure high processing yield and low die-to-die variation. The processing uniformity will depend on several factors, such as how the processing equipment is configured and optimized for a given wafer size. Whereas some systems are tailored to one specific wafer size, the Versaline DSE can be configured and tuned for 3" to 8" wafers.

A common phenomenon of DSE processing is the scalloping of deep trench sidewalls. This is an artefact of the alternating deposition of passivation and etching. Following a passivation step, ions are directed vertically down at the structure. The ions collide and remove the passivated bottom of the trench thereby exposing the substrate to the chemical etchant. Repeating the etch and deposit steps results in many small, incremental etches. A 500 micron thick wafer would need about 100 to 1000 cycles. Longer cycles results in higher etch rate, but more enhanced scalloping. Faster cycle time and particularly faster switching between passivation and etching can improve the smoothness of the sidewalls.

DSE is a single wafer process where the substrates are processed sequentially, one by one. The time for completing one lot is the processing time of a single wafer times the

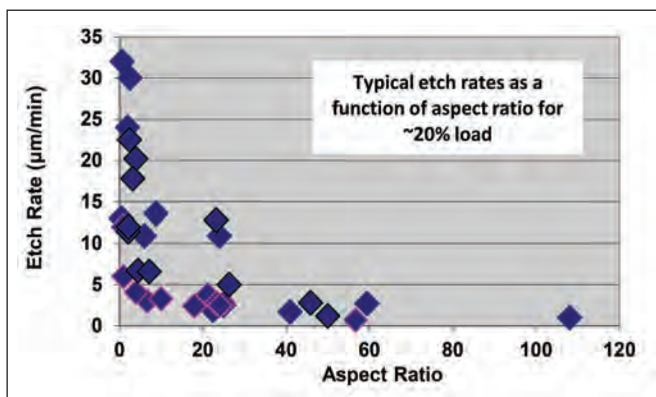


Figure 1: Etch rates for various aspect ratios at ~20% load

number of wafers in the lot. With deeper trenches of 100s of microns used for TSVs and higher density of features increasing the etch load, the DSE can become a time-consuming and costly fab process. Etch rates are highly dependent on the etch load, but also on the aspect ratio of the features being processed. A comparison chart has been included in Figure 1. Any given device company has an incentive to add as many structures per wafer as possible to leverage economies of scale and the DSE process equipment owner desires faster processing to minimize processing costs and increase the revenue per time unit. The race is on for higher etch rates to increase the efficiency and processing throughput.

DSE process requirements: SOI applications and endpoint detection

DSE is commonly used for etching Silicon-on-insulator (SOI) substrates to create 3D MEMS structures such as TSVs or other features for accelerometers, gyroscopes, pressure sensors, oscillators and much more. SOI processing uses the top oxide layer to protect areas not to be processed, and a layer of oxide is used as an etch stop layer. SOIs are offered along a wide range of parameters including substrate diameter, thickness, doping levels and oxide thicknesses.

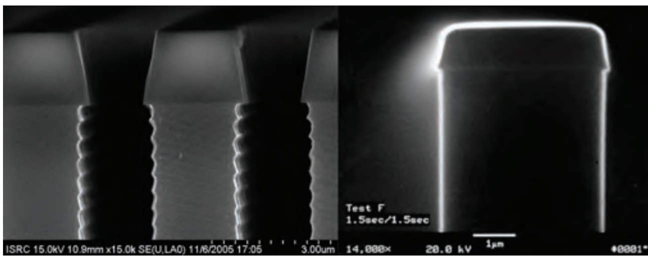


Figure 2: High aspect ratio trenches, with and without DSE morphing

Ideally, an SOI structure should be able to have aspect ratio independent vertical structures of varying sizes, shapes and density, with no undercut at the etch entry and notch free. Since DSE processing is CMOS processing compatible; the combination of SOI and DSE is very powerful.

It allows making everything from discrete MEMS sensor elements to fully-integrated, monolithic sensor(s) and signal conditioner in one silicon die. In the consumer electronics world, this is especially desirable as market forces and tough competition is aggressively driving higher volumes, better performance and lower unit price in smaller footprint packages.

	Conventional Gas Exchange	Plasma-Therm Fast Gas Switching
Process Cycle Times	Several seconds	Sub-second
Smooth Gas Exchange?	No (*pressure burst*)	Yes
Minimizing scallop without losing etch rate?	No (Scallop & etch rate tradeoff)	Yes
Process Limits	MFC response time + gas residence time	Gas residence time

Figure 3: Conventional versus Plasma-Therm's fast gas switching

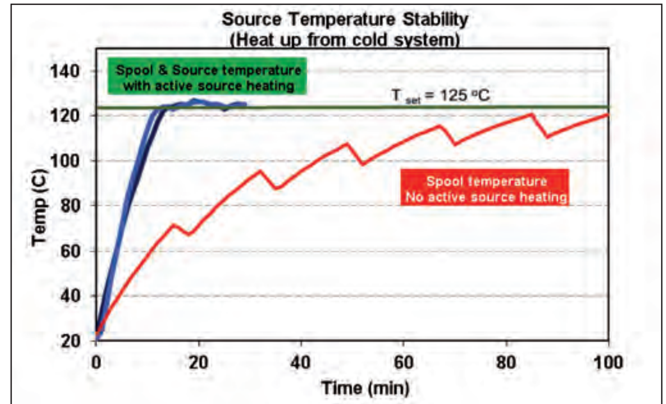


Figure 4: Active heating vs. non-active heat source

DSE process requirements: stable process, reliable platforms and easy maintenance

The importance of reliable and stable DSE processing equipment is paramount to successful manufacturing. Above all is the assurance that production recipes produce the same result each and every time it is used for processing a specific substrate type. This relies on monitoring process parameters, but the design and the inherent repeatability of the processing equipment itself is equally important. The more robust and stable a system is the tighter the process control and the associated process control window. This can be an important factor in ensuring that wafers being processed have very little die-to-die, wafer-to-wafer, lot-to-lot, day-to-day and month-to-month variability.

DSE process trade-offs and control

Plasma-Therm's experience driven DSE systems have a range of features that overcome common drawbacks and limitations of DRIE processing such as scalloping, notching and under etching.

DSE process trade-offs and control: profile control, sidewall morphology and etch rates

A key feature of the Versaline DSE is the ability to minimize scalloping of vertical trenches through the use of fast gas switching. Sidewall smoothness is now starting to impact device performance as, for example, the gap in resonators is submicron. Atmospheric devices are impacted as resonance can be affected by flow of air during vibrations. Smoothness can also affect coverage and capacitance (surface area) and field breakdown. The switching time is optimized through a set of dedicated hardware and software to speed up the process to eliminate scalloping effect and other process artifacts commonly associated with other, competitive systems. See Figure 2.

Based on controlling process basic parameters such as the power, temperature and pressure, additional metrics including etch rate, sidewall smoothness, mask undercut, SOI notching, Aspect Ratio Dependent Etching (ARDE) and etch selectivity can be controlled. For example, near vertical structures with minimal undercut can be obtained with process morphing. Process morphing allows process parameters to be automatically adjusted during the etch process to achieve improved profile control. Morph process parameters can be

selected and controlled independently. Smooth and automatic changes during processing in combination with process time can be manipulated to achieve customer selected morphing curves with deterministic slopes. For example, the relation between electrode bias, gas and pressure and respective process times can achieve linear or asymptotic, rising and falling, morphing curves.

Plasma-Therm is meeting requirements for increased performance and etch rates by providing higher gas flow and pressure, better gas utilization (See Figure 3) and higher RF power. Increased etch rates will evidently produce more heat at the substrate. This is known as a heat dissipation issue, as the temperature needs to be tightly controlled to ensure uniform and repeatable processing.

Excess heat can cause a loss of deposition efficiency potentially leading to non-uniform etching across the wafer as the heat will typically be higher at the middle of the wafer chuck. Plasma-Therm uses a closed-loop controlled cooling chuck (He) to dissipate heat from the wafer during processing.

Another exclusive feature of the Plasma-Therm DSE system is the use of an active heated source. See Figure 4. The active heating source greatly decreases the time from a cold start to production ready, minimizing equipment down time. It also minimizes variation in the source temperature, so wafers receive the same plasma conditions run-after-run and without the typical "first wafer" phenomenon seen with non-actively heated sources. Finally, the mean time between cleaning (MTBC) and maintenance is extended as hardware conditions are optimized with minimized polymer formation in the reactor.

DSE process trade-offs and control: SOI applications and endpoint detection

Typical processing of SOI structures result in flaring at the etch stop (oxide) causing notching of the structures and some level of undercut at the etching of the entry. Plasma-Therm has a patented technology to control this type of undercutting and notching. The result is almost picture perfect vertical structures as displayed in Figure 5.

Higher aspect-ratio structures require lower etching rates to achieve the same processing quality compared to other elements. This effect is known as the aspect ratio dependent etching (ARDE). Bulk micro machined MEMS devices typically include structures with a wide range of feature shapes and sizes. These structures may require different etch rates and, for example, narrow, high aspect ratio trenches may require over-etching to complete the features. Over-etching is particularly

Figure 5 | Plasma-Therm's DSE process for SOI structures

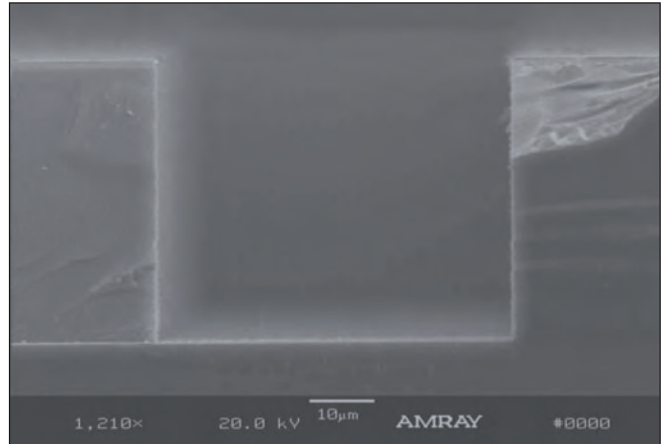


Figure 6 | Notch free SOI

undesirable as it is difficult to control and can result in less than optimal 3D structures. Plasma-Therm has developed techniques and process controls to almost eliminate ARDE effects, resulting in more efficient processing, and producing uniform feature depths for ease of design rules.

Etching of SOI wafers often use a silicon oxide layer as an etch stop and a fixed etch time for process control. If the etch proceeds beyond this time, the etchant will start removing the oxide layer and degrade the profile (i.e. notching). Optical emission spectrometry (OES) can be used to detect plasma process termination time by analyzing the light emitted from a plasma source to deduct information about the chemical and physical states.

The Versaline DSE is equipped with an integrated endpoint detection system called OES. This OES consists of a wide range spectrometer employing a CCD array, with real time monitoring and adjustable thresholds. It is highly sensitive making it capable for low load (~0.5%) applications and is proven to increase productivity and quality controlling over etching.

DSE process trade-offs and control: stable process, reliable platforms and easy maintenance

Conventional DRIE systems exhibit a "pressure burst" when changing between the passivation deposition and the etching step. Plasma-Therm has developed a smooth pressure transition; the "hold and release" pressure control. This feature eliminates pressure bursts and ensures very stable and reproducible run-to-run production results. The hold and release pressure control is a closed loop control algorithm with superior stability and reproducibility compared to more common open loop position pressure control systems.

Example 1: etching SOI

The example in Figure 6 displays a cross-section of a notch-free, vertical SOI feature. The feature is smooth along the side walls all the way down to the bottom of the cavity where the Silicon is opening to oxide. This is highly desirable, especially for MEMS devices where SOI is commonly used in 3D structures.

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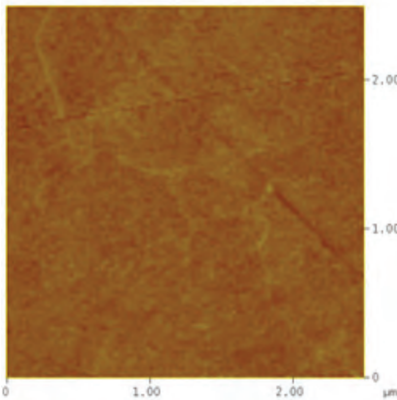

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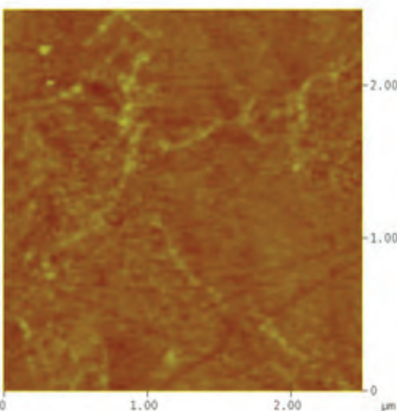

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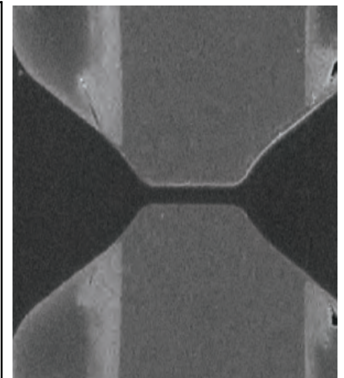

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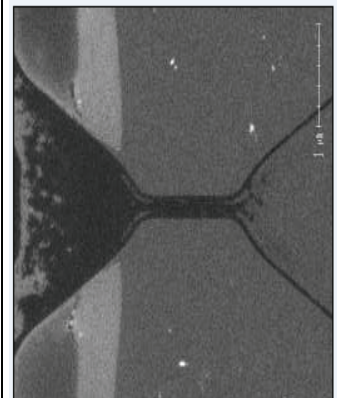

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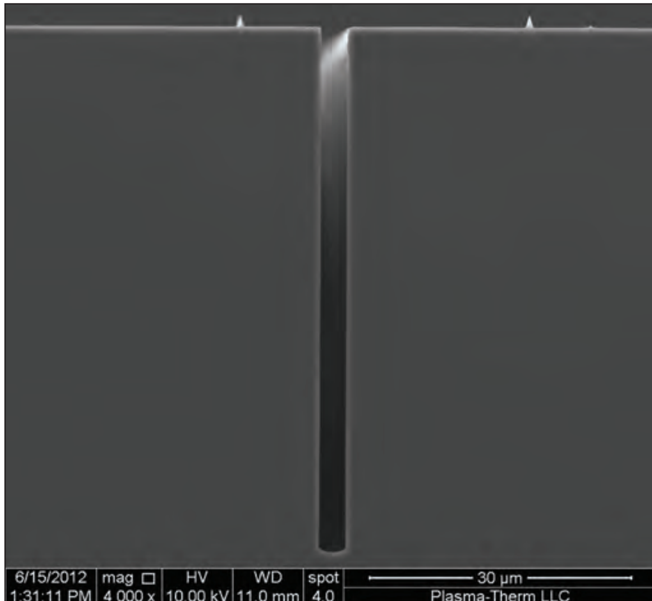

Figure 7 | High aspect ratio

Example 2: sidewall smoothness of high aspect ratio trenches

The second example, in Figure 7, is of a high aspect ratio 30:1 trench with very smooth sidewalls and outstanding profile control. Side wall scalloping for this particular feature is less than 20nm. This is a very good example of the excellent capabilities of the Plasma-Therm DSE.

Example 3: "Nano" etch and other structures

The final example displayed in Figure 8 depicts very small dimensioned nano etch trenches with smooth, vertical sidewalls. The trenches are 500nm wide with 350nm openings, 17µm height and average scalloping of 10nm.

Summary and conclusions

Plasma-Therm is an industry leader in processing equipment that specializes in modular systems with state-of-the-art technology and configuration flexibility. This paper has presented the versatile and high-performance DSE platform from Plasma-Therm. The system has a range of unique capabilities that makes it an excellent choice for processing SOI wafers for MEMS applications. Key features include patented technology for pressure control, notch-less SOI, fast gas switching and endpoint detection algorithms. Real world examples have been provided to prove the excellent process capabilities for high aspect ratio structures, notch-free SOI and unique nano scale features.

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Figure 8 | DSE nano trenches

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EU Policy Developments Impact SEMI Members

Heinz Kundert, president, SEMI Europe says that decisions made in a national Ministry or an EU institution can have a direct impact on the semiconductor industry.

BEING ABLE TO QUICKLY IDENTIFY and seize the potential offered by new technologies and new markets is critical in the semiconductor industry. Keeping track of public policy developments is equally important.

Decisions made in a national Ministry or an EU institution can have a direct impact on our industry.

A new EU patent procedure, to be introduced by mid-2014, will significantly reduce the cost and time for a company to obtain a patent valid across 25 European states. The outcomes of the current review of substances under European EHS rules, for example, may have an impact on industry's research priorities or its access to the EU market.

New EU patent procedure offers aautomatic protection in 25 countries and brings down costs

The new 'EU Unitary Patent', to be made available by April 2014, is expected to reduce the administrative and financial burden of patent protection across the EU. Companies will be able to fill out a single application to the European Patent Office — once

granted the patent is automatically valid across 25 countries (all EU member states except for Italy and Spain). A single court will be created (Unified Patent Court) with jurisdiction over infringement proceedings in any of these countries.

Companies will no longer need to apply before each national body for their patent to have effect in that territory, nor satisfy local language and administrative requirements or pay local fees. Nor will they need to defend their patents in different jurisdictions and receive different, sometimes conflicting, rulings.

This new system is also expected to significantly bring down the costs of obtaining a patent. The European Commission estimates that today, a 'classic' European patent (that needs to be validated individually in 27 Member States) costs 36 000 EUR. The new unitary patent system will bring the costs down dramatically to around 5 000 EUR, or one-seventh of today's cost.

GaAs and InP under review for a possible restriction under REACH

A recent EU study collected information on the production, import and use of 44 substances, including GaAs and InP, in articles, as a first step towards assessing the need for a possible restriction on their use in the EU. Such a restriction (under Art. 68 REACH) could have an impact not only on European manufacturing but also on imports.

In a joint response with other industry associations, SEMI listed the applications where these compounds are used and the lack of risk to consumers when they are completely encapsulated. SEMI further highlighted the strategic importance of these compounds for micro- and nano-electronics. Their restriction would have a negative impact not only on industry, but on Europe as a whole. It would curb the global competitiveness of the European semiconductor manufacturing supply chain and it would deprive the EU of the industry base and products Europe needs to achieve its strategic goals for the global digital market. GaAs and InP are the first III-V compounds being examined under the REACH microscope and SEMI is actively monitoring developments. In our upcoming advocacy activities, we will collect information on risk management measures the industry has in place to avoid exposure to workers and the environment.

EU RoHS update: Exemptions are expiring; more substances to be banned under RoHS

The EU RoHS directive currently bans six substances from being used in electric and electronic equipment. Certain products of SEMI members are not covered by the Directive, such as PV panels going into fixed installations, large-scale stationary industrial tools (LSIT) and large-scale fixed installations. SEMI members also benefit from exemptions to the Directive, which allow for specific uses of the banned substances in specified quantities and for a limited period of time.

- A number of exemptions for specific applications will expire in July 2016. These exemptions can be renewed but applications for renewal need to be submitted by end of 2014. Now is therefore the time for industry to review the list of exempted applications, determine which ones are still needed and start pooling resources to draft the renewal application.
- Additional substances will be banned under RoHS by 22 July 2014. An EU-funded study is currently underway to develop a methodology for evaluating the risk posed by hazardous substances and to determine whether they should be banned. By the end of 2013, this study will also propose additional substances that should be restricted. The European Commission will then decide on banning these substances under RoHS, the transition periods allowed for the manufacturing supply chain to adjust and start considering necessary exemptions.

The SEMI RoHS working is actively contributing to the drafting of the review methodology.

EU conflict minerals debate is launched – potential impact on industry's sourcing of raw materials from conflict zones

The EU is now also considering whether it needs to adopt EU measures to support responsible sourcing from conflict-affected or high-risk areas. It is yet not clear what minerals or what countries a possible EU initiative would focus on, nor whether its nature would be voluntary or binding. The question is also raised whether EU measures should address specific end-products or downstream industry sectors.

A number of initiatives on conflict minerals already exist, including the OECD guidelines on due diligence and the EU is looking to build on these and reinforce transparency through the supply chain. In the U.S., the Dodd-Frank act requires companies to report annually whether they or their suppliers are using conflict minerals (tin, tungsten, tantalum and gold originating from the Democratic Republic of Congo or an adjoining country) and the EU is seeking feedback on how these provisions are working in practice.

The adoption of an EU legislative measure would have significant implications for SEMI members, creating a traceability requirement across the entire manufacturing supply chain.

For further information on SEMI advocacy activities in Europe and on the SEMI Europe Advocacy Partners program, please contact Rania Georgoutsakou (gourania@semi.org; +32 2 609 5334) or Heinz Kundert (hkundert@semi.org).3
7th SEMI Brussels Forum on 24 May 2013

The SEMI Brussels Forum is Europe's leading policy event for semiconductor equipment and materials, providing a platform for top-level executives and EU representatives to exchange views and debate how to reinforce Europe's competitiveness in the global market. The 7th SEMI Brussels Forum will discuss how Europe's industry and policy-makers can increase their impact — both individually and jointly to reinforce Europe's position. www.semi.org/eu/brusselsforum.

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EUV masks/resists go dark!

Sub-20nm transistor update

In advance of the 2013 SEMICON West TechXPOTs on lithography and nonplanar transistors beyond 20nm, Debra Vogler from SEMI asked some of the speakers to comment on the challenges they wanted to highlight.

THIS YEAR'S SEMICON WEST (July 9-11) front-end processing TechXPOTs on lithography and transistors below 20nm will provide updates on how technologists are meeting the critical issues associated with each of these areas.

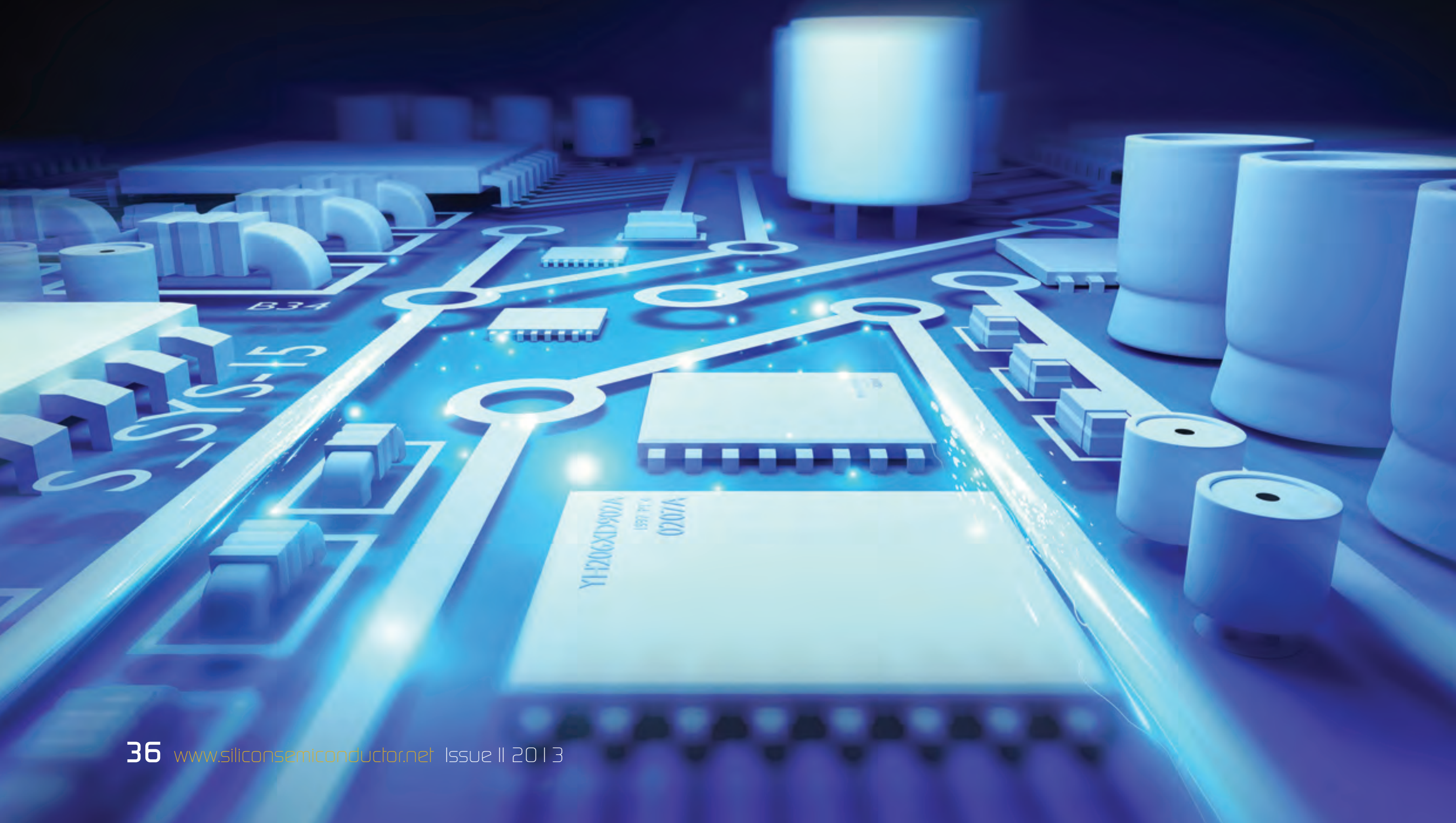
What are this years challenges?

EUV Lithography: Entering Competitive Advantage Phase

The outlook for EUV Lithography source readiness was a bit murky late last year as a review of the presentations at the 2012 International Workshop on EUV and Soft X-Ray Sources (Dublin, Ireland; 10/8-10/11, 2012) suggested. As reported by ASML at that conference, both LPP and LDP (aka DPP) source technologies were still trying to achieve 50W of power at a high duty cycle. There was even mention of a nonconventional way to achieve scaling using a free electron laser (FEL).

Given that ASML is working to acquire Cymer (which is developing the LPP source), it probably speaks volumes about which source technology has garnered the most interest on the part of ASML. Springtime came early to the industry, however, when ASML reported at the SPIE Advanced Lithography Conference (San Jose, CA) that 55W had been demonstrated at a 100 percent duty cycle (Figures 1, 2).

Additionally, results were shown for 9nm hp imaging — the first time a single-digit result from a single exposure had been achieved (Figure 3).



Stefan Wurm, director of Lithography at SEMATECH, told SEMI he was very encouraged by the results reported at SPIE. "They've demonstrated significant improvement and if they can demonstrate significant improvement at the next milestone (i.e., June-July timeframe), then tools will ship with the source productivity (i.e., 50-60wph) that IC manufacturers expect for a pilot line," noted Wurm.

Once the next source milestone is achieved, Wurm believes the industry will shift its focus to the mask side, where there is still work to be done on defects. "Nobody has really ever used an EUV mask under high-volume manufacturing (HVM) conditions, so you have to think about things like mask lifetime, use cycles, cleaning frequencies – backside and frontside - and so on," said Wurm. But don't expect to see a lot of reporting on these activities. Wurm explained that the learning the IC manufacturers are doing with respect to masks – and resists – is now seen as giving them a competitive advantage. An outsider attending an EUV conference won't see much visibility with respect to progress. "People might show a few nice pictures, but exactly how they do it, what they do, and what it takes to get there – they're not going to share that anymore."

So as the industry begins the ramp up to SEMICON West, it finds itself poised to enter the realm of EUV pilot line production which is good news indeed. But the industry is also at the point where EUV infrastructure learning is maturing and becoming a competitive advantage.

In the meantime, lithographers are working to extend optical lithography with multiple patterning and chip design approaches, an engineering effort that Wurm says the industry is perfectly capable of doing.

Searching for New Channel Materials

Whether an IC manufacturer chooses to make the giant leap to 3D transistors (e.g., the Tri-gate), or takes an evolutionary approach (e.g., using SOI-based technology as a bridge), all roads lead to the implementation of 3D transistor architectures. No matter the path, however, new channel materials will have to be developed.

Paul Kirsch, director of the Front-end Process Division at SEMATECH, anticipates that there will be a progressive range of Ge being added to Si – from perhaps 25 percent Germanium (Ge) up to 100 percent Ge – to form channels in pMOS FETs first, followed by nMOS FETs for logic applications. "Industry has a great deal of experience with SiGe already," noted Kirsch. "It's understood how to handle that material in the fab and it's had good performance benefits in the pMOS FET." What does need more attention, however, is making SiGe work for the nMOS FET – particularly for contacts and gates. Kirsch anticipates seeing SiGe entering the roadmap between the 14nm, 10nm, and 7 nm nodes, with the possibility that some IC manufacturers may be able to start even sooner than 14nm.

14nm FD-SOI

STMicroelectronics is in the evolutionary camp with respect to transistor scaling. "We have opted for the planar solution (for 14nm) built on a thin silicon film above a thin buried oxide layer, which is simpler to manufacture while still offering the same fully-depleted benefits," explained Giorgio Cesana, marketing director, Technology R&D, Digital Sector, at STMicroelectronics. With the

MOPA PrePulse Technology Validated with Power, Dose Stability and Collector Protection

Power	Dose Control	Availability	Comment
40W	99.99% of dies <0.2% dose repro, 100% duty cycle within die exposure and at full closed loop control	Proven Collector Protection settings	six 1-hour runs during 8.5 hours of operation
55W	97.5% of dies <0.5% dose repro, 100% duty cycle within die exposure and at full closed loop control	Proven Collector Protection settings	1 hour of operation
up to 60W	Open Loop	Proven Collector Protection Over 4Bpls, 40hours continuous exposures	Dedicated test to demonstrate collector protection

Figure 1. Mask-oscillator power amplifier (MOPA) PrePulse technology validated with power, dose stability, and collector protection. SOURCES: ASML/Cymer (David Brandt)

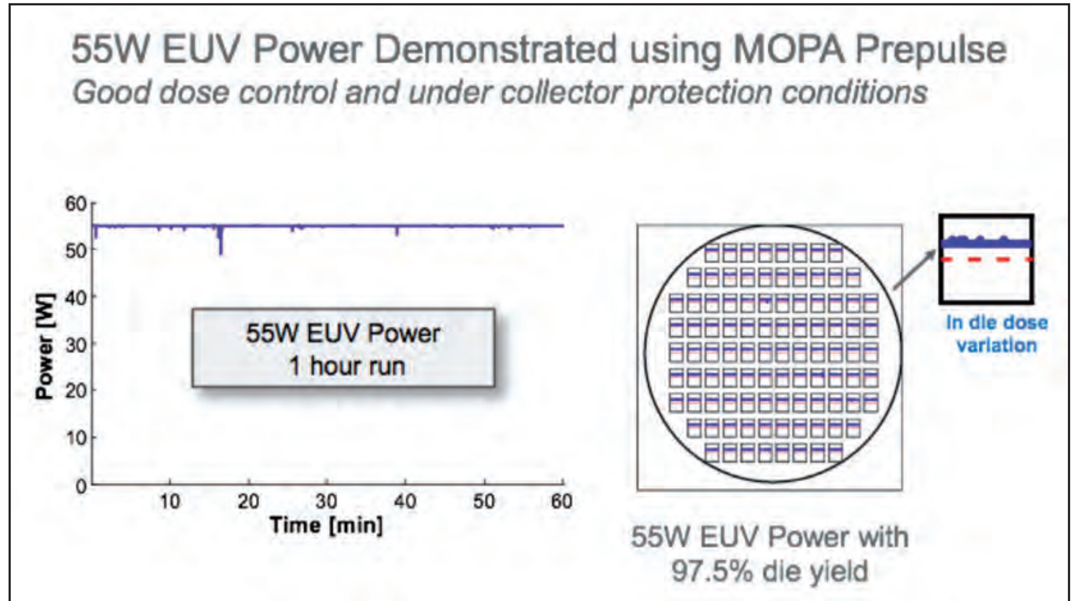


Figure 2. 55W EUV power demonstrated using mask-oscillator power amplifier (MOPA) PrePulse showing good dose control and under collector protection conditions. SOURCES: ASML/Cymer (David Brandt)

company's 28nm FD-SOI node in production, it is now focusing on the development of the next node. "At 14nm, this will implement a set of new features for further increasing performances while optimizing power consumption and operating at reduced voltage levels."

The 14nm FD-SOI node will also benefit from gate-first integration according to Cesana. "Traditionally, gate-first pFET performance is weaker than competing gate-last approaches that are better able to lower pMOS threshold voltage," he observed. "To overcome this limitation, the gate stack is built using a "flow C" integration scheme that creates fewer constraints vs. the gate-etch patterning used in the 28nm FD-SOI "flow B." Cesana further explained that another important feature of 14nm FD-SOI will be the introduction of in situ doped SiGe:B on the pFET, combined with a 110-oriented-substrate, as a key performance booster. "On an nFET, an in situ doped SiC:P is introduced to avoid a performance penalty. Still, the 14nm node will support a dual source-drain integration scheme." A SiGe channel obtained by Ge condensation is mandatory on the pFET side for lowering the device threshold voltage and STMicroelectronics will be adjusting the Ge concentration to match the suitable Vt value.

Learn more about lithography and nonplanar transistors beyond 20nm at SEMICON West 2013 (www.semiconwest.org).

Register for SEMICON West at www.semiconwest.org/register.

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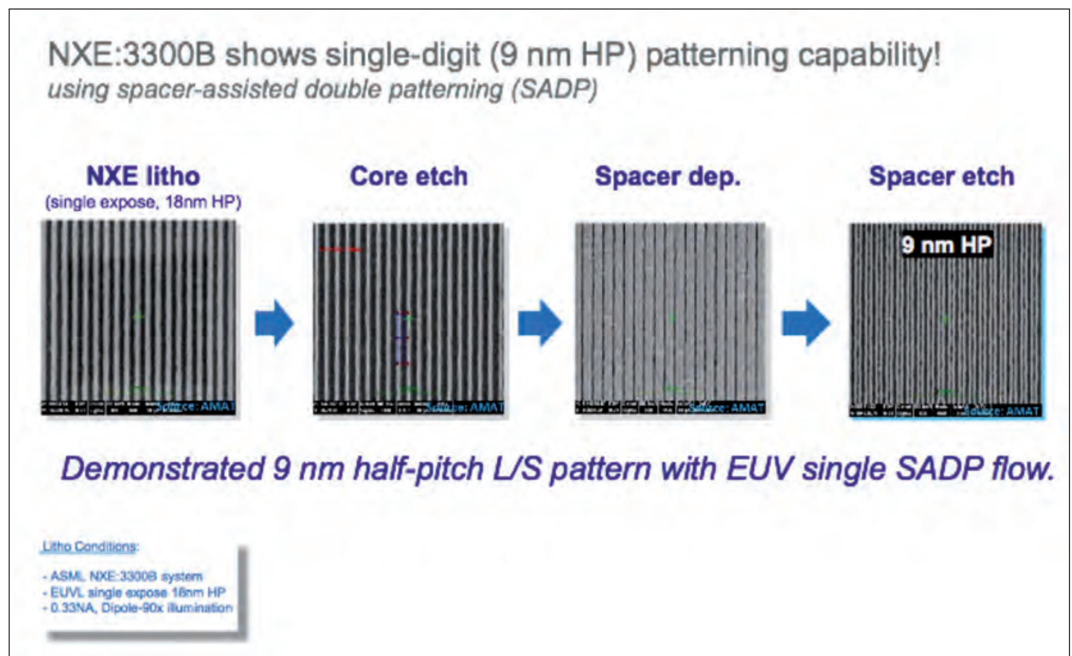

Figure 3. Demonstrated 9nm hp L/S pattern with EUV single SADP flow. SOURCES: ASML, imec, Applied Materials (2/13)

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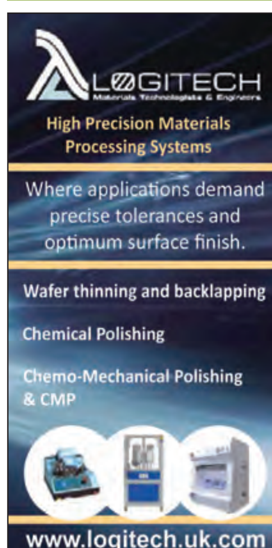

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