# SILICON SEMICONDUCTOR

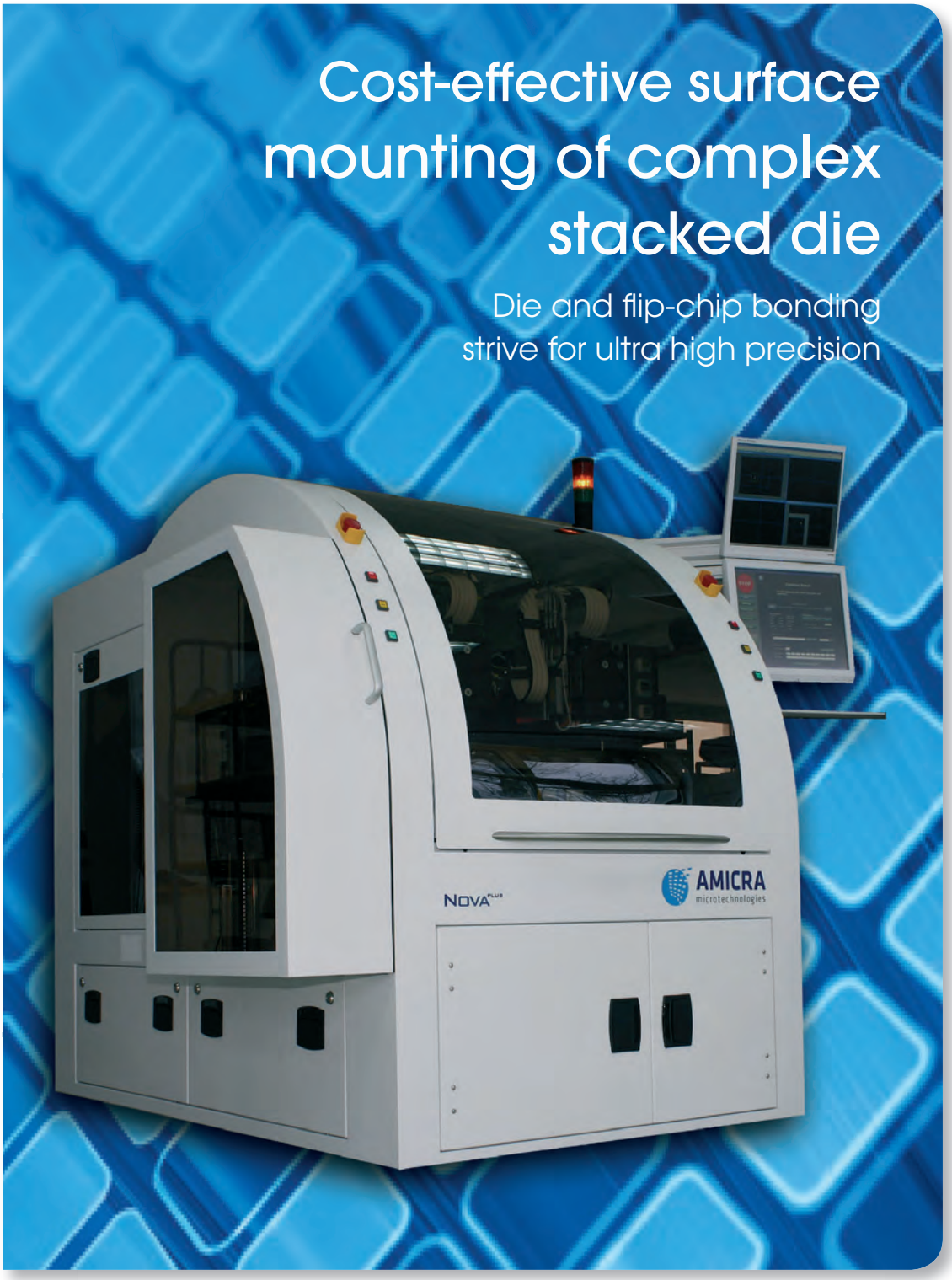
Connecting the Silicon Semiconductor Community

Volume 35 Issue 4 2013 @siliconsemi www.siliconsemiconductor.net

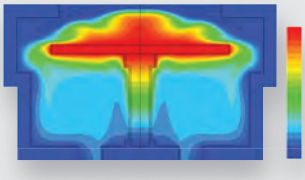



## Cost-effective surface mounting of complex stacked die

Die and flip-chip bonding strive for ultra high precision



# Optimize the Thermal Performance of your Process Equipment.



Extensive computational tools enable product designs to be highly refined for ultimate performance.

Multi-zone circuit layouts in a polyimide construction are highly customized to deliver exacting performance up to 250°C.

EZ-ZONE® RM Multi-loop controllers are fully scalable with up to 152 PID Loops and 256 monitor points per system.

Watlow provides innovative solutions to help process tool manufacturers meet the needs of the semiconductor technology roadmap. Our approach is to work collaboratively to help solve complex thermal challenges associated with state-of-the-art manufacturing processes; helping to improve yield, throughput and cost of ownership. This includes innovative heaters, controllers and sensors for use in front-end and back-end applications such as CVD, PECVD, Etch, Diffusion, Bonding, IC test and more.

ASSURANT™ gas and pump line heaters feature high temperature capabilities with low outgassing.

Contact Watlow® today for the latest thermal solutions for semiconductor applications.


European Technical Sales Offices

**Germany** +49 (0) 7253-9400-0
info@watlow.de

**France** +33 1 41 32 79 70
info@watlow.fr

**Italy** +39 02 4588841
italyinfo@watlow.com

**Spain** +34 91 675 1292
info@watlow.es

**UK** +44 (0) 115-964-0777
info@watlow.co.uk


WATLOW®

# executiveview

by Robert Cappel, Senior Director of Corporate Marketing, KLA-Tencor

## Optical & E-Beam inspection address smaller designs

SEMICONDUCTOR MANUFACTURERS are implementing new patterning techniques and structures to produce smaller, faster devices for consumer electronics. At sub-20nm design nodes, innovative process control is required to optimize fab processes and ensure optimal yields.

Metrology and inspection tools serve as the key "check and balances" branch of IC manufacturing, enabling faster learning cycles and improved ramp-to-revenue schedules. By finding design, patterning or process issues early, fabs can maximize yield and device performance, while reducing costs and risks.

The real industry work horse for defect inspection has always been optical inspectors. As design nodes shrink and critical defects become smaller, it's worth exploring whether e-Beam inspection should move to a more prominent role in a fab's inspection strategy.

Let's consider today's manufacturers who must find small defects very quickly over large areas. Suppose we scale a 10nm defect to the size of a coin and disperse hundreds of coins across an area the size of California—representative of a 300mm wafer. Currently, broadband plasma optical inspection is the only technology capable of finding all the coins across a range of surfaces over this entire area in an hour. It would take the e-Beam tool over a year to inspect the entire area; or, it could inspect a very small area in an hour, missing critical information such as the overall distribution of coins or critical areas where they are located. Lacking this information, a fab could miss a major yield excursion, resulting in hundreds of millions of dollars in lost profit.

Innovations in optical technologies such as a laser-pumped broadband light source, optics as complex as those used in steppers, selectable apertures and high-speed sensors produce the sensitivity required to find small defects on advanced devices. The combination of these technologies provide inspection flexibility and capability that cannot be found in other optical or e-Beam inspectors, enabling critical defect detection on the widest range of process layers.

Additional innovations have made optical inspection smarter: NanoPoint provides ultra-focused inspection of critical patterns that serve as early indicators of design or process issues.

Since optical inspection couples critical defect sensitivity with the speed required for monitoring wafer and lot variations, it will continue as the dominant defect inspection approach. E-Beam will continue to play a complementary role, supporting optical inspection set up and detecting defect issues related to electrical problems, such as opens, shorts and reliability issues. With this strategy, IC manufacturers can quickly identify yield and reliability issues, ensuring successful and fast product ramp.


**News Editor** Dr. Su Westwater suwestwater@angelbc.com
**Director of SEMI Publishing** Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
**Senior Sales Executive** Robin Halder robin.halder@angelbc.com +44 (0)2476 718109
**Sales Manager** Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
**USA Representatives** Tom Brun Brun Media E: tbrun@brunmedia.com Tel: 724 539-2404
Janice Jenkins E: jjenkins@brunmedia.com Tel: 724-929-3550
**Director of Logistics** Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
**Design & Production Manager** Mitchell Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214
**Circulation Director** Jan Smoothy jan.smoothy@angelbc.com +44 (0)1923 690200
**Circulation & Subscriptions Assistant** Annette Weatherilt annette.weatherilt@angelbc.com +44 (0)1923 690220
**Chief Operating Officer** Stephen Whitehurst stephen.whitehurst@angelbc.com +44 (0)2476 718970

*Directors* Bill Dunlop Uprichard – CEO, Stephen Whitehurst – COO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal

**Published by** Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK.
T: +44 (0)1923 690200 F: +44 (0)1923 690201 E: ask@angelbc.com

Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970 F: +44 (0)2476 718 971 E: info@angelbc.com

Angel BUSINESS COMMUNICATIONS PPA recycle When you have finished with this magazine please recycle it.

Silicon Semiconductor is published four times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/e158 pa (UK & Europe), £138.00 pa (air mail), $198 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2013. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing.
US mailing information: Silicon Semiconductor (ISSN 1096-598X) is published four times a year for a subscription of $198 by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. Periodicals postage paid at Rahway, NJ. POSTMASTER: send address changes to: Silicon Semiconductor, c/o Mercury International Ltd, 365 Blair Road, Avenel, NJ 07001.
Printed by: Pensord Press.

 ISSN 2050-7798 (Print) ISSN 2050-7801 (Online).

# Stepper redefined

## MEETING LITHOGRAPHY CHALLENGES HEAD-ON

- Large field of view (52mm x 66mm)
- 30 reticle library with four-reticle wheel
- On-the-fly auto focus for each exposure
- Warped wafer handling
- Superior depth of focus for thick resists
- Substrate and size flexibility
  (450mm, reconstituted wafers, square interposers, etc.)


JetStep™ Advanced Packaging Lithography System

## Advancing Tomorrow's Technology

RUDOLPH TECHNOLOGIES

www.rudolphtech.com

Volume 35 Issue 04 2013

# contents

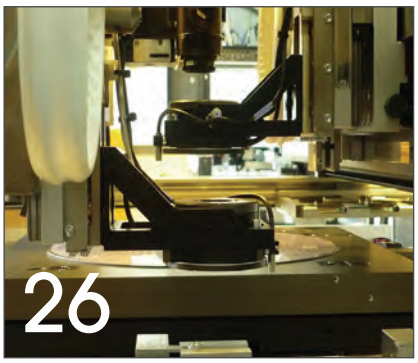
CONNECTING THE SILICON SEMICONDUCTOR COMMUNITY

## features

### COVER STORY










Magazine and Front Cover designed by Mitch Gaynor

### industry research



# Modutek partners with WRS on 450mm silicon reclaiming

MODUTEK CORPORATION is working with WRS Materials which provides silicon wafer polishing services, on a 450mm wafer cleaning development project. Richard Mee, President of WRS Materials, says, "Modutek Corporation's expertise on tank design and wet clean technology was crucial to our 450mm upgrade".

The new cleaning line will feature Modutek custom designed chemical baths that will incorporate Kiajo megasonics and custom wafer furniture capable of handling five 450mm wafers per fixture. Doug Wagner, President/CEO of Modutek Corporation, comments, "We were able to offer WRS new processing methods that will help them provide critical cost effective solutions to their customers. It will work to reduce the overall cost of the initial 450mm investments."

He goes on to say, "Our collaboration with WRS provided us the opportunity to utilise our custom designed semiconductor wet processing equipment and ensures they meet all SEMI standard requirements."

This new reclaim line is among the first in operation globally and will reclaim 450mm wafers for most of the blue chip OEM's. With a growing demand and the high cost of 450mm silicon wafers, reclaiming wafers will be a vital resource to the industry for many years to come. Worldwide, the 2011 reclaim wafer market was estimated at $374 million and is expected to reach as high as $413 million in 2013. "Technology advancements are driving higher quality standards, these new specifications demand constant investment in better tool sets, strong engineering support and improved training for our production staff. Fortunately we have found a willing partner in Modutek to help in all three areas", comments Richard Mee.

Wagner adds, "Modutek's Megasonic Cleaning Equipment offers a precision cleaning system that was developed for the unique requirements of the Semiconductor, FPD, Hard Disk, Solar and Crystal industries. Our engineers work closely with our customers to provide a solution for each specific application."

## Rudolph expands macro defect inspection series

RUDOLPH TECHNOLOGIES has launched its new NSX 220 automated macro defect inspection system. The company says its system, pictured above, provides fast, easy defect inspection for traditional back-end processes in the semiconductor, MEMS and LED market at a reduced price.

The NSX 220 tool joins the NSX 320 system in the NSX family of automated macro defect inspection and metrology systems for final manufacturing facilities. The first NSX 220 system was installed in July at a major outsourced assembly and test (OSAT) facility in Asia.

Mike Jost, vice president and general manager of Rudolph's Inspection Business Unit says, "The NSX 220 system is a streamlined version of our NSX 320 system.

The NSX 220 system is designed for traditional macro defect inspection of wafers up to 300mm at conventional semiconductor, MEMS and LED final manufacturing facilities, while the NSX 320 System serves next-generation advanced packaging processes with defect inspection and three-dimensional metrology for wafers up to 450mm." He continues, "The NSX 220 system benefits from many of the hardware and software innovations that made the NSX 320 system the market leader in advanced packaging, but is targeted for back-end facilities that do not need the full suite of capabilities offered by the NSX 320 System. Adding the NSX 220 system to the NSX family gives our customers a choice of best-in-class capabilities."

The NSX 220 is an automated macro defect inspection system that uses grey-scale image analysis (with colour image capture) to provide fast, accurate inspection and metrology in final manufacturing applications for wafers up to 300mm. It can detect traditional advanced macro defects such as scratches, mechanical damage, foreign materials, voids and probe damage, while also performing two-dimensional measurements on bumps, probe marks and edge trim processes.

The tool operates over a range of resolutions (10$\mu$m - 0.5$\mu$m) with both brightfield and optional darkfield illumination. The software platform, leveraged from the NSX 320 system's success, uses host-based image processing and delivers significant improvements in usability and productivity over older-generation NSX series equipment. Using centrally-managed recipe creation and editing, multiple NSX 220 tools can share a single recipe and be matched across the fab.

An optional suite of yield management software optimises the productivity of both the NSX 220 and 320 systems and minimises the need for operator assistance. Discover Software is designed for use with Rudolph inspection systems to allow real-time analysis for faster solutions and intelligent defect sampling for reduced offline review.

# New applications spur demand for thin layer deposition tools

THE GLOBAL MARKET for thin layer deposition equipment is projected to reach US$ 18.5 billion by 2018.

This will be driven by emerging applications in medical imaging devices, specialty packaging and industrial coatings according to Global Industry Analysts' " Thin Layer Deposition Equipment: A Global Strategic Business," report. Defined as the building block of miniaturisation and MEMS processing, thin layer deposition is a critical part of the fabrication process and is key to the production of all electronic devices.

With surface treatment applications ranging from electronic components, electronic displays, optical coatings, and optical data storage devices to antistatic coatings, thin layer deposition is expected to witness strong growth in the coming years.

A significant portion of the growth is expected to stem from the robustly growing electronics industry. Developments in equipment design and performance, innovations in thin film materials and processes will also help spur growth.

Typically, demand for Thin Film Deposition (TFD) equipment is largely tied to the demand for semiconductors, electronics, and medical devices, among others. Periods of economic slowdown tend to curtail consumer spending thus impacting business opportunities in this market.

The capital intensiveness of the industry also makes investments a cyclical pattern with growth occurring largely during periods of intermittent revolutionary technology developments.

Atomic Layer Deposition (ALD) Equipment is set to witness considerable demand in the short to medium term period, with ALD process finding large-scale adoption in several end-use application areas.

For a long time, the ALD process has been utilised to generate thin films with different compositions such as nitrides, oxides, pure metals, and carbides among others.

The hallmark of this technology is its ability to produce monolayers on a molecular or atomic scale thus making it highly suitable for deposition of nano-films with thickness less than 100 nm on various surfaces, including polymers, metals and ceramics.

ALD equipment is expected to witness increased adoption as a manipulation and fabrication tool in nanotechnology. What's more, the ALD equipment market is projected to witness increasing demand from non-IC and IC applications.

A marked trend towards miniaturisation of components is also driving the market, given the technology's proven efficiency in fabrication of smaller size components. Also, with semiconductor fabricators expected to invest in new manufacturing equipment, the market is forecast to witness tremendous opportunity in the coming years. ALD equipment will also find increased adoption in production of other advanced devices such as OLEDs.

The report says Asia-Pacific represents the largest and the fastest growing market with a projected CAGR of 4.9 percent over the analysis period. PVD equipment represents the largest product market.

## PVD system for 300mm power devices

SPTS is to launch its Sigma fxP physical vapour deposition (PVD) system (shown below) for 300mm power device manufacturing. Available system options include modules for frontside thick aluminium processing and backside metal deposition on ultra-thin wafers. The new system is designed to address the technical challenges customers face as they scale power PVD processes up to 300mm wafer size.

In a discrete MOSFET power device, current passes through the silicon substrate so electrical contacts are required on both sides of the wafer. Due to the high currents involved, thick aluminium alloy layers are deposited on the front side of the wafer (typically over 4 $\mu$m rather than less than 1 $\mu$m for mainstream silicon interconnects).

However, depositing thick films puts unusually large heat loads on process chamber hardware, potentially resulting in film contamination from outgassing in the chamber furniture.

This contamination can lead to the formation of aluminium whiskers/ extrusions in the growing film that can ultimately result in device killer defects. In traditional front end fab deposition equipment, a common technique to mitigate this issue is to reduce film deposition rates with a corresponding reduction on system productivity. However, SPTS says the Sigma fxP design overcomes that challenge without compromising throughput. Sigma fxP users routinely deposit thick aluminium layers at above 1.4 $\mu$m/min without any yield destroying whiskers or extrusions.

With frontside processing complete, wafers are thinned down to 50 $\mu$m or less to reduce 'on-state' resistance and solder metal layers are deposited on the backside. No supporting carrier substrates are used and the ultra-thin, large area wafer will deform under the influence of uncontrolled film stresses, with miss-handling a potential consequence.

The Sigma fxP carries thin wafer handling hardware and uses film deposition stress control techniques to deliver high throughput processes with low wafer bow. SPTS says that currently, seven out of the top ten power device manufacturers, and major foundries use the Sigma fxP as the process tool for power PVD processing.

With power device manufacturing moving to 300mm format wafers, SPTS has successfully transferred its process knowledge and capability to the new platform.

# JUSUNG to supply MRAM etching equipment to Crocus

JUSUNG ENGINEERING is to supply an integrated etch and deposition system for advanced MRAM technology to Crocus Nano Electronics (CNE).

Russian Based CNE is a joint venture founded by Crocus Technology, an MRAM semiconductor developer, and RUSNANO, a Russian state-owned international investment company. The supply agreement has a significant meaning to JUSUNG's global expansion strategy as the process technology was validated by Crocus Technology in the USA.

The Genaon Plus MRAM etching equipment to be supplied by JUSUNG is a core process tool that can etch non-volatile materials such as platinum, manganese and cobalt.

Conventional process tools cannot process such new materials that are used in advanced memory devices, making JUSUNG's Genaon Plus a unique enabling technology.

According to JUSUNG, the plasma etching equipment specialized for magnetic metal layers patterning, one of the most critical in MRAM processes, can completely eliminate polymer residue left behind on the side walls during the etching process, thereby enabling chip designers to utilise a variety of new materials.

As a low-power, high-density memory chip that combines storage capacity of flash memory and high speed of DRAM, MRAM is emerging as a next-generation memory. The MRAM market is engaging rapidly and is expected to grow to 925 billion Korean Won in 2018 globally.

JUSUNG is excited to participate at the early stage of such a high growth market. CJ Hwang, CEO of JUSUNG, comments, "We identified Crocus Technology as an ideal partner to launch our next-generation equipment. Crocus is an industry leader in the emerging market. While this is a new partnership for JUSUNG, our goal is unchanged to develop innovative technologies to delight our customers."

Boris Omarov, CEO of CROCUS NANO ELECTRONICS, adds, "We made the critical decision for CNE because Jusung is the leader in Magnetic Etch Technology. Jusung is the perfect partner for CNE and Russia, since they all share the same spirit of pacesetting and dedication to perfection."

# ARM acquires Cadence display tech

ARM, A SEMICONDUCTOR IP supplier, and Cadence Design Systems, Inc. an innovator in global electronic design, have signed a definitive agreement for the sale and transfer of Cadence PANTA display controller cores to ARM. The agreement enhances the companies' long-standing ecosystem collaboration and strengthens their technical alignment. Cadence's PANTA family of high-resolution display processor and scaling coprocessor IP cores was co-developed in conjunction with ARM and is targeted at advanced multimedia applications for high-end mobile devices with ultra-low power consumption. "Display technology is critical to the mobile consumer's user experience," says Pete Hutton, executive vice president and general manager, Media Processing Division, ARM. "The addition of the PANTA family of display cores to the ARM product portfolio will help our ecosystem of partners get to market quickly with high-end displays that are fully integrated with ARM's leading Mali graphics and video solutions and protected with ARM TrustZone security."

Martin Lund, senior vice president of Cadence's IP Group, adds, "ARM and Cadence work together closely on many levels, including IP integration, verification IP (VIP) for all ARM AMBA protocols, and high-performance design solutions optimised for ARM cores.

As a result, both companies offer more tightly integrated solutions to our mutual customers."

# Cabot achieves multiple orders for logic devices

CABOT MICROELECTRONICS has announced that its "Novus A7100 Aluminum" CMP slurry products have been adopted by several customers to help enable 28/20 nanometre High-K Metal Gate integration schemes used for advanced logic devices. The Novus A7100 Aluminum slurry product platform is the result of Cabot Microelectronics' CMP technology and extensive research and development in close collaboration with strategic customers.

Novus A7100 contains a combination of unique engineered abrasive particles and proprietary chemistry to remove aluminium and the complex stack of work-function metals within the transistor gates of advanced semiconductor logic devices. This CMP solution was designed to polish aluminium and then stop on the underlying dielectric material and therefore minimise dielectric material erosion and aluminium recess. Novus A7100 is formulated to optimise removal rate, limit erosion and recess, and meet low defect requirements.

Charles Chen, Cabot Microelectronics' Global Business Director, states, "The Novus A7100 Aluminum CMP slurry provides our customers with a solution for a critical process step in enabling High-K Metal Gate device integration at advanced technology nodes. We believe the extremely low recess levels that can be achieved across a wide range of feature sizes and densities, results in better device reliability and transistor performance."

Cabot Microelectronics Corporation, is a supplier of CMP polishing slurries and a growing CMP pad supplier to the semiconductor industry. The company's products play a critical role in the production of advanced semiconductor devices, enabling the manufacture of smaller, faster and more complex devices by its customers.

AMICRA microtechnologies

# Die and Flip Chip Bonding for Ultra High Precision

IWLPC, November 5-7, 2013, San Jose, CA
Productronica, November, 12-15, 2013, Munich

## AFC PLUS

- Die Attach & Flip Chip System
- Fully automatic System
- ± 0,5 µm Placement accuracy
- Cycle time < 15 seconds
- Working area up to 300 x 300 mm


## NOVA PLUS

- Die Attach & Flip Chip System
- Fully automatic System
- ± 2,5 µm Placement accuracy
- Cycle time < 3 seconds
- Working area up to 600 x 600 mm


AMICRA MICROTECHNOLOGIES GMBH
WERNERWERKSTR. 4
D-93049 REGENSBURG, GERMANY

TEL: +49- 941-208209 0
E-MAIL: SALES@AMICRA.COM
WWW.AMICRA.COM

MORE THAN PRECISION

# Chip carrier packaging grows thanks to QFN

ADVANCED PACKAGING of semiconductor chips has emerged as a key enabler in many of today's electronic system products. Put another way, package selection is increasingly important to the success of the end product.

While much attention with regard to IC packaging is on 3D stacking and integration technologies, there is another area of packaging that has quietly been flourishing during the past decade and a half.

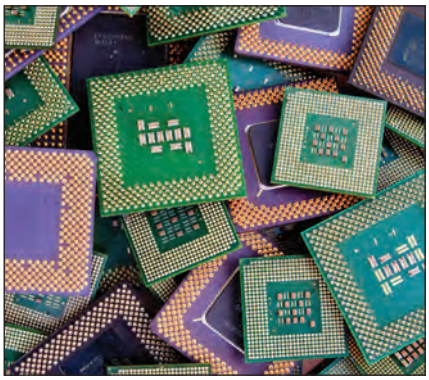
Introduced in 1998, the quad flat no-lead (QFN) package design (including the related dual-sided DFN) has enjoyed phenomenal growth from the very beginning. With its low cost, small size, and excellent thermal and electrical performance characteristics, the QFN quickly became the mainstream package of choice for many low-to-medium I/O count ICs.

In the past decade, new dual-row and even triple-row technologies have enabled QFNs to support many more I/Os and, thus, enter a wider range of IC product segments. Today, the QFN is one of the most widely used IC package types.

IC Insights forecasts that the continuous high growth in demand for QFN-type packages will help push the flatpack/chip carrier (FP/CC) category of packages past the "old" small outline (SO) group of packages for the first time ever in 2013, as shown in the figure below.

The QFN is a type of chip carrier. The SO packages emerged in the early 1980s and then grew to become the industry's most widely used package type by 1995. The FP/CC packages emerged around the same time and they offered higher I/O capabilities than the SO packages because they had leads on all four sides.

The QFN package category in the JEDEC standards includes a variety of manufacturer-specific designs such as the MicroLeadFrame (MLF) package from Amkor, Fujitsu's Bumped Chip Carrier (BCC) and small outline no-lead (SON)



packages, Carsem's Micro Leadframe Package (MLP), and ASE's microchip carrier (MCC).

There are similar JEDEC standards for DFN packages that have external bond pads or "lands" on two sides instead of four like the QFN. Besides being categorised in the FP/CC group of packages, QFNs and DFNs are also considered part of a larger group of packages called leadframe CSPs, or chip-scale packages.

QFN and DFN packages are inexpensive to manufacture. They typically don't have solder balls, are targeted at low-I/O applications (typically less than 85), and make use of pre-plated leadframes. Either wirebonds or flip-chip bumps are used to attach the IC to the leadframe.

Versions like the MLF and BCC have an exposed die-attach paddle on the bottom of the package, which serves as an excellent thermal path away from the chip as well as a good ground-plane if the pad is grounded on the circuit board.

That, in conjunction with the high electrical performance offered by short I/O connections, has made these leadframe CSPs attractive for use in packaging RF circuits for cellphones and other wireless and portable product applications.

Many companies have migrated from SO-type packages to QFNs and DFNs and their popularity continues to spread as new advancements make QFNs/DFNs capable of handling a greater amount of circuitry and functionality.

## TSMC & Imagination to drive GPUs

IMAGINATION TECHNOLOGIES is working with TSMC to drive next-generation performance to new levels on Imagination's PowerVR GPUs.

Initial efforts have already achieved 25 percent overall performance improvements for the PowerVR Series6 GPU core, with key blocks demonstrating as much as 30 percent improvement compared to existing design flows.
Imagination R&D teams working with TSMC are developing IP libraries and fully characterised reference system designs for Imagination's IP cores on TSMC's advanced processes including 28HPM and 16nm FinFET technologies.
This collaboration will enable mutual customers to achieve significant performance gains for next-generation applications.

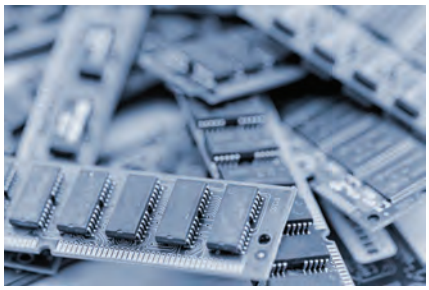
Imagination is tapping out an optimised next-generation multi-core, multi-cluster PowerVR Series6 GPU design to characterise these performance improvements and plans to demonstrate a test chip later this year.

The resulting reference flow and optimised libraries will enable SoC designers to significantly accelerate time-to-market and increase performance for similar implementations of PowerVR Series6 GPUs.

Tony King-Smith, Imagination EVP marketing says, "The growing reliance on graphics processors to power the best user experiences means the GPU has become the new silicon process driver for the coming decade. It occupies as much as 50 percent or more of leading edge SoCs, and demands the highest performance memory bandwidth while always delivering high performance at low power. These characteristics are critical to defining the key device parameters of future generation processes.

# Samsung mass producing 20nm-class DDR4 memory chips

SAMSUNG ELECTRONICS is mass producing, what it claims, is the most advanced DDR4 memory chips, for enterprise servers in next-generation data centres. With the introduction of these high-density DDR4 modules, Samsung can better support the need for advanced DDR4 in rapidly expanding, large-scale data centres and other enterprise server applications.



Early market availability of the 4-gigabit (Gb) DDR4 devices, which use 20 nanometre (nm)-class process technology, will facilitate demand for 16-gigabyte (GB) and 32GB memory modules. This compares to conventional DRAM of which 8GB modules using a 30nm-class process technology are still commonplace.

"The adoption of ultra-high-speed DDR4 in next-generation server systems this year will initiate a push toward advanced premium memory across the enterprise," says Young-Hyun Jun, executive vice president, memory sales & marketing, Samsung Electronics. "After providing cutting-edge performance with our timely supply of 16GB DDR3 earlier this year, we are continuing to extend the premium server market in 2013 and will now focus on higher density and added performance with 32GB DDR4, and contribute to even greater growth of the green IT market in 2014," he adds.

In next-generation enterprise servers, the use of higher speed DRAM raises system level performance and lowers overall power consumption significantly. By adopting DDR4 memory technology early, OEMs can minimise operational costs and maximise performance to provide more favourable returns on investments. Production of Samsung's 20nm-class 4Gb DDR4 follows the introduction of 50nm-class 2Gb DDR3 in 2008, culminating in a fully fledged transition to DDR4 for large-scale data centres and other enterprise applications in just five years.

Samsung says the 4Gb-based DDR4 has the fastest DRAM data transmission rate of 2,667 megabits per second - a 1.25-fold increase over 20nm-class DDR3, while lowering power consumption by more than 30 percent. Based on Samsung's 20nm-class DRAM compact 4Gb DRAM chip, the company has now developed a new series of products tailored to applications from servers to mobile devices. This will provide global customers with the widest range of highly advanced low-power, high-performance green memory solutions.

# Process to improve 3D-IC / TSV packaging reliability revealed to industry

EV Group (EVG)has developed a new polymer via-filling process for 3D-IC/ through-silicon-via (TSV) semiconductor packaging applications.

Available on the EVG100 series of resist processing systems, the new NanoFill process provides void-free via filling of very deep trenches and high-aspect ratio structures, and is suitable for all common polymeric dielectrics-offering a highly flexible, low-cost and production-ready via-fill platform for interposer development for 3D-integrated image sensors and other device types.

TSV interconnects are critical to the development of 3D-ICs since they enable through-chip communication between the vertically stacked device layers. Currently, most TSVs employ a solid copper via structure.

However, the mismatch in coefficient thermal expansion (CTE) between the copper via and the surrounding silicon can create a high amount of stress on the via structure, which results in long-term reliability issues.Replacing copper as the conducting material is not practical due to the general ease of use of the process. Also, the tooling infrastructure for copper is already well established.

However, replacing the solid copper via with a partial copper-plated via that is filled with a polymeric dielectric has been demonstrated to reduce CTE mismatch and stress, thus minimising reliability issues.

EVG's proprietary process and system enable simultaneous void-free via filling and dielectric redistribution layer (RDL) formation utilising a field-proven process technology that is compatible with all standard polymeric materials.

"3D packaging represents a fundamental change in the semiconductor industry that paves the way for continued advances in device performance and cost reduction through 'More than Moore' approaches," states Markus Wimplinger, corporate technology development and IP director at EV Group.

"EV Group has made significant investments in our portfolio of wafer-level manufacturing solutions to add new products and capabilities, such as our NanoFill solution, to help our customers accelerate the commercialization of 3D-integrated devices."

# ABI: Global semiconductor market to reach $298 billion

THE WORLDWIDE semiconductor market is expected to grow 3 percent from 2012 to 2013. This is according to ABI Research's new "Worldwide Semiconductor Market -2Q13" Market Data report which tracks the market and market shares for the top 20 suppliers.

There has been sequential market growth from 1Q13 to 2Q13 and the vast majority of the top 20 vendors are expecting 3Q13 to experience revenue growth again.

"It has been a tough few years for the semiconductor industry. While we haven't seen a dramatic decline in overall revenues since the 2008/2009 period the market has been pretty stagnant since 2010," comments Peter Cooney, practice director.

He adds, "We will see some growth in 2013 as the wider economic environment improves but major market growth is not expected until later in 2014/early 2015."

Consolidation continues to be rife in the industry: a number of major mergers and acquisitions are expected to take place in the second half of 2013; these include the merger of Fujitsu and Panasonic semiconductor divisions and the acquisition of Elpida by Micron. There have also been many smaller M&A transactions such as Intel's acquisition of ST-Ericsson GPS business and Broadcom's acquisition of Renesas Mobile's LTE assets as major vendors exit the mobile device semiconductor market.

"As the semiconductor market has been squeezed we have seen an increase in consolidation amongst the major players," adds Cooney. "Margins are falling and the competitive environment is tough - especially in the mobile device market - this is driving vendors to re-evaluate their overall strategy and pull out of some of their once major markets."

He concludes, "We have seen a number of major vendors exit the mobile device market - Freescale, TI, STMicroelectronics, and Renesas and we expect there are more to come."

## Entegris & SEMATECH collaborate

Entegris and SEMATECH have partnered to move forward the development of advanced nanoscale particle removal processes and cleaning technologies for next-generation wafers and devices.

This collaboration will address some of the profound changes taking place in the semiconductor industry that are impacting fundamental aspects of process and equipment design - as integration of new materials and process technology for sub-20nm node manufacturing, next-generation lithography requirements and the progression to 450mm wafers.

One key issue relates to the preparation of critical surfaces through the entire semiconductor manufacturing process. Entegris will work with experts from SEMATECH's Nanodefect Centre to develop new technologies and solutions to reduce nano-scale particle contamination during wafer processing.

"We are pleased to partner with SEMATECH to provide early solutions for wafer surface cleaning," says Bertrand Loy, president and CEO of Entegris. "Our goal is to leverage our contamination control expertise to develop filtration and particle detection methods for the most advanced cleaning processes."

"SEMATECH's Nanodefect Centre aims to build industry participation in detecting, modelling, characterising, and providing solutions for defect issues as geometries shrink below the 10nm node," comments Michael Lercel, senior director of Nanodefectivity and Metrology.

"Our partnership with Entegris brings additional expertise to SEMATECH, and in turn will raise the level of our research efforts and further strengthen SEMATECH's commitment in identifying the challenges of future technology nodes."

## Finetech unveils high force bonder

FINETECH has developed a new high force configuration of its FINEPLACER pico ma platform targeting anisotropic conductive film (ACF) applications.

The tool achieves applied bonding forces of up to 700 N, which is critical to ensuring coherent and durable bonds between the chip and ACF to achieve higher signal densities and smaller overall packages.

Polymer-based ACF is used to create an electro-mechanical connection between two components. During ACF bonding, a combination of low temperature and high force is applied to the device, which activates the conductive spheres in the film.

ACF technology has traditionally been used in LCD or chip-on-glass (COG); additional target applications include flex-on-glass (FOG), flex-on-board (FOB), flex-on-flex (FOF), chip-on-flex (COF) and chip-on-board (COB). "This new configuration showcases the continued flexibility of Finetech's FINEPLACER platform," says Neil O'Brien, Director, Finetech USA. "ACF bonding faces unique challenges, such as high density interconnects in an enlarged bond area combined with multi chip settings.

Addressing these requirements necessitates a system with a reinforced mechanical structure capable of applying high bonding forces. The new pico ma configuration increases the FINEPLACER's range of capabilities, further extending this modular bonding platform." The high force bonder integrates a novel 700 N bonding force module as well as a new multi-chip transfer station and precision z-hub positioning table for high forces. The transfer station allows up to 4 components to be placed simultaneously and bonded with defined distances.

# Taking nanoscale lithography into the third dimension

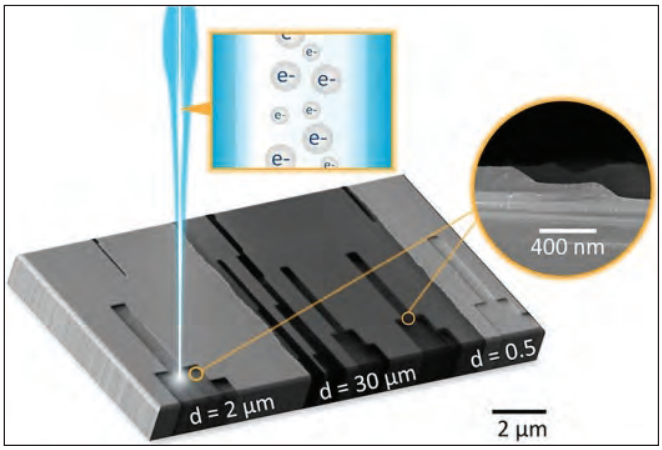
Using a combination of different techniques, researchers can etch trenches and other high aspect ratio structures with nanometre scale features without using masks.

ENGINEERS AT THE NIST CENTRE for Nanoscale Science and Technology (CNST) have developed a new technique for fabricating high aspect ratio three-dimensional (3D) nanostructures over large device areas. They used a combination of electron beam (e-beam) lithography, photolithography, and resist spray coating.

While it has long been possible to make complicated 3D structures with many mask layers or expensive grayscale masks, the new technique enables researchers to etch trenches and other high aspect ratio structures with nanometre scale features without using masks and in only two process stages. The fabrication of 3D semiconductor and dielectric structures that are patterned by exposing resist with varying intensity grayscale gradients has been essential to a broad range of applications such as digital lenses, micro-electromechanical systems, and fluidic medical devices.

Unlike devices that rely on conventional masks, which have areas that simply transmit or block light to form a pattern, the fabrication of these devices has typically relied on 3D grayscale masks which have varying levels of transparency and depend on the use of proprietary materials.

Because the chemistry is proprietary and because the masks are prepared using complicated processes best suited to small surface areas, they are often prohibitively expensive. The next generation of these devices requires lower costs, larger surface areas, and ever-smaller feature sizes. The researchers' new approach capitalises on the high throughput capability of photolithography to generate large area grayscale structures with large processing flexibility and the ability of e-beam lithography to add grayscale features smaller than 200 nm.

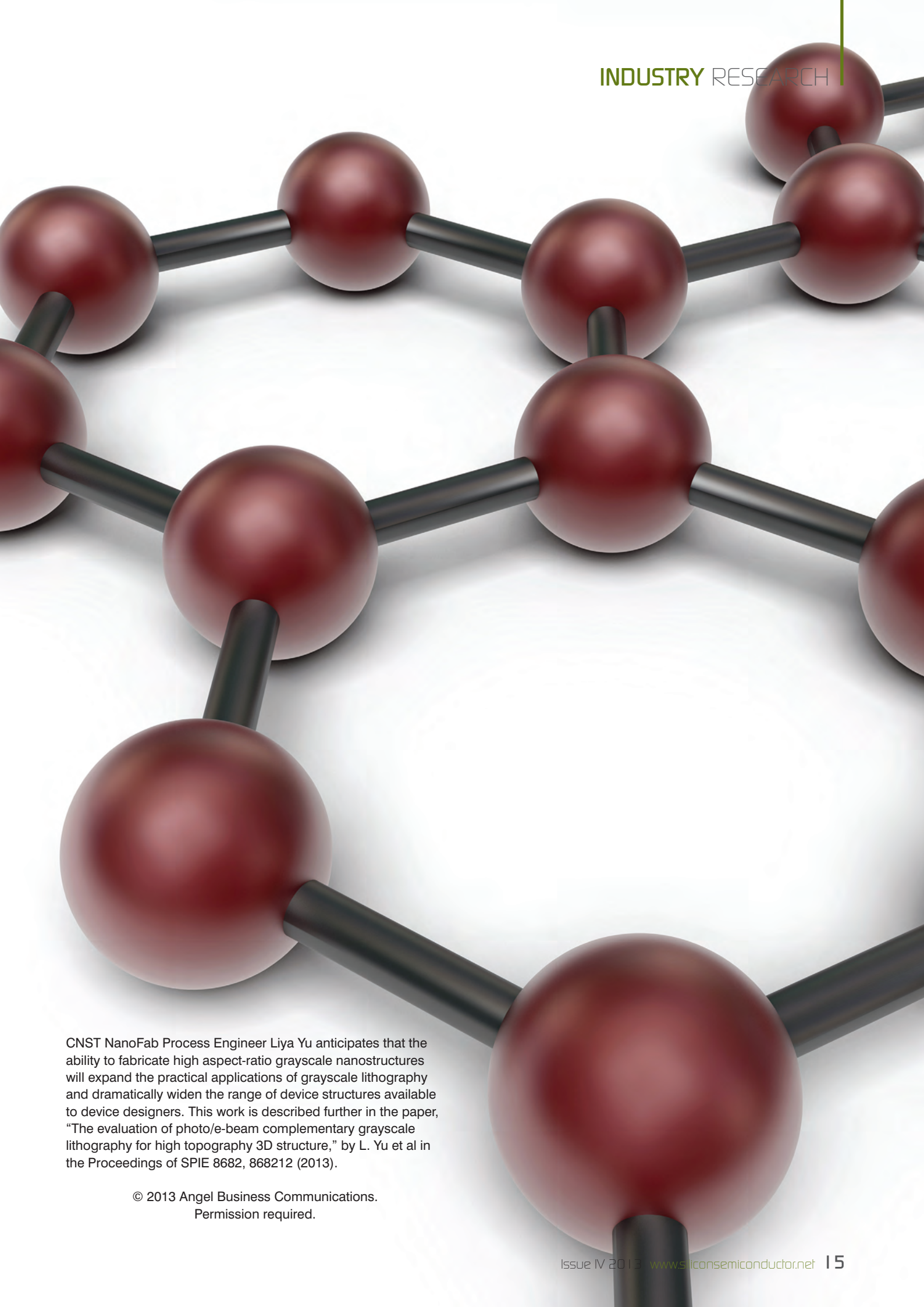



The first phase of this mix-and-match approach is to pattern a layer of photoresist by exposing it with a focused laser beam. By locally modulating the intensity of the light to form a grayscale gradient, varying levels of photoreaction in the photoresist are generated.

After the sample is immersed in the developer solution, material is dissolved in areas corresponding to the degree of induced photoreaction, leaving the photoresist layer with varying thicknesses matching the initial exposure pattern.
The sample is exposed to a deep reactive ion etch (DRIE) which removes substrate material at varying depths that depend on the thickness of the photoresist, transferring the 3D photoresist pattern vertically into the substrate to form deep grayscale micro-structures. The second phase applies similar processing steps but with feature sizes ten times smaller.

First, a high pressure e-beam resist spray coating is applied to obtain conformal coverage of the high-aspect ratio topography produced in the first phase. Then, by manipulating a high-energy e-beam with nanometre-scale resolution, patterned grayscale step heights are directly written in the e-beam resist in different locations. Finally, the resist is developed and the sample is exposed to DRIE as it was in the first step.
The two stage process results in a vertical feature sizes of 45 ± 6 nm within a substrate structure that varies from 2 $\mu$m to 30 $\mu$m deep and with horizontal feature sizes of 100 nm to 200 nm and an overall pattern size potentially as large as a whole wafer.

The scanning electron micrograph (SEM) at the top of this article shows a top-view along with an SEM (inset) showing a cross-sectional view of grayscale structures fabricated using a combination of e-beam lithography, photolithography, and resist spray coating. The superimposed schematic illustrates e-beam direct writing of nanoscale vertical staircases (SEM inset) on a substrate with microscale grayscale topography. The initial grayscale patterns were generated on a laserwriter. After reactive ion beam etching, the patterns were simultaneously written into 2 $\mu$m, 0.5 $\mu$m, and 30 $\mu$m deep features.



CNST NanoFab Process Engineer Liya Yu anticipates that the ability to fabricate high aspect-ratio grayscale nanostructures will expand the practical applications of grayscale lithography and dramatically widen the range of device structures available to device designers. This work is described further in the paper, “The evaluation of photo/e-beam complementary grayscale lithography for high topography 3D structure,” by L. Yu et al in the Proceedings of SPIE 8682, 868212 (2013).

# Revolutionising consumer electronics with nanotechnology

Nanopatterning, or self-assembling molecular materials, form an organised lithographic pattern on semiconductor crystals, for use as integrated circuits. Now newly developed materials, when integrated into electronics, will enable the development of ultra-lightweight, compact and efficient devices.

UNIVERSITY OF AKRON (UA) researchers have developed new materials that function on the nanoscale, which could lead to the creation of lighter laptops, slimmer televisions and crisper smartphone visual displays.

Known as “giant surfactants” - or surface films and liquid solutions - the researchers, led by Stephen Z.D. Cheng, dean of UA’s College of Polymer Science and Polymer Engineering used a technique known as nanopatterning to combine functioning molecular nanoparticles with polymers to build these novel materials. Surfactants are compounds that lower the surface tension (or interfacial tension) between two liquids or between a liquid and a solid. Surfactants may act in a number of ways - as detergents, wetting agents, emulsifiers, foaming agents, or dispersants, to name a few.

The giant surfactants developed at UA are large, similar to macromolecules, yet they function like molecular surfactants on a nanoscale, Cheng says.

The outcome? Nanostructures that guide the size of electronic products.

Nanopatterning, or self-assembling molecular materials, is the genius behind the small, light and fast world of modern-day gadgetry, and now it has advanced one giant step thanks to the UA researchers who say these new materials, when integrated into electronics, will enable the development of ultra-lightweight, compact and efficient devices because of their unique structures.

During their self-assembly, molecules form an organised lithographic pattern on semiconductor crystals, for use as integrated circuits. Cheng explains that these self-assembling materials differ from common block copolymers (a portion of a macromolecule, comprising many units, that has at least one feature which is not present in the adjacent portions) because they organise themselves in a controllable manner at the molecular level.

“The IT industry wants microchips that are as small as possible so that they can manufacture smaller and faster devices,” says Cheng, who also serves as the R.C. Musson and Trustees Professor of Polymer Science at UA. He points out that the current technique can produce the spacing of 22 nm only, and

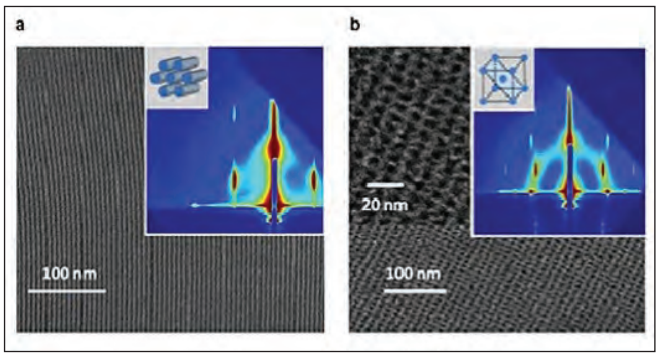
cannot go down to the 10 nm or less necessary to create tiny, yet mighty, devices. The giant surfactants, however, can dictate smaller-scale electronic components.

“This is exactly what we are pursuing - self-assembling materials that organize at smaller sizes, say, less than 20 or even 10 nanometres,” says Cheng, equating 20 nm to 1 /4,000th the diameter of a human hair.

An international team of experts from UA, Peking University in China, National Tsinghua University in Taiwan and McMaster University in Canada have shown how well-ordered nanostructures in various states, such as in thin films and in solution, offer extensive applications in nanotechnology. “These results are not only of pure scientific interest to the narrow group of scientists, but also important to a broad range of industry people,” says Cheng, noting that his team is testing real-world applications in nanopatterning technologies and hope to see commercialisation in the future.

The team’s study is highlighted in a pending patent application through the University of Akron Research Foundation and the article, “Giant surfactants provide a versatile platform for sub-10-nm nanostructure engineering” by Xinfei Yu et al, published in Proceedings of the National Academy of Sciences of the United States of America, 110, 10078-10083, 2013.






Patterns of two giant surfactant samples in thin-film state

# Simplifying MEMS pressure sensor technology

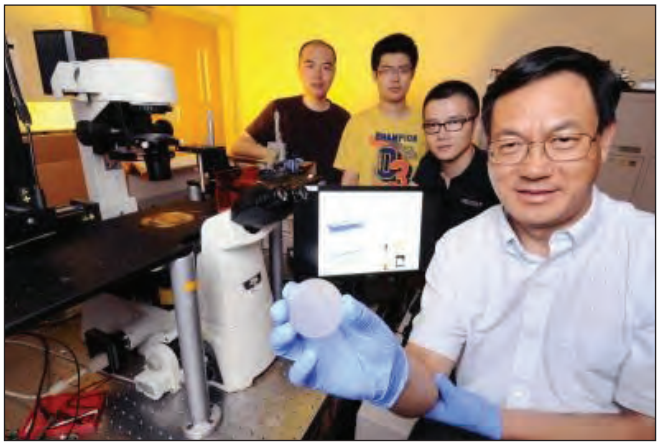
A new sensor incorporating gallium nitride and zinc oxide nanowires could provide an artificial sense of touch and be used in MEMS systems.

USING THOUSANDS OF nanometre-scale wires, researchers at the Georgia Institute of Technology have developed a sensor device that converts mechanical pressure - from a signature or a fingerprint - directly into light signals that can be captured and processed optically.

The sensor device could provide an artificial sense of touch, offering sensitivity comparable to that of the human skin. Beyond collecting signatures and fingerprints, the technique could also be used in micro-electromechanical (MEMS) systems and biological imaging. And ultimately, it could provide a new approach for human-machine interfaces.

“You can write with your pen and the sensor will optically detect what you write at high resolution and with a very fast response rate,” says Zhong Lin Wang, Regents’ professor and Hightower Chair in the School of Materials Science and Engineering at Georgia Tech. “This is a new principle for imaging force that uses parallel detection and avoids many of the complications of existing pressure sensors.”

Individual zinc oxide (ZnO) nanowires that are part of the device operate as tiny LEDS when placed under strain from the mechanical pressure. They allow the device to provide detailed information about the amount of pressure being applied. Known as piezo-phototronics, the technology - first described by Wang in 2009 - provides a new way to capture information about pressure applied at very high resolution: up to 6,300 dots per inch.



Zhong Lin Wang holding the sensor device along with his research team in the background

Piezoelectric materials generate a charge polarisation when they are placed under strain. The piezo-phototronic devices rely on that physical principle to tune and control the charge transport and recombination by the polarisation charges present at the ends of individual nanowires.

Grown on top of a gallium nitride (GaN) film, the nanowires create pixelled light emitters whose output varies with the pressure, creating an electroluminescent signal that can be integrated with on-chip photonics for data transmission, processing and recording.

“When you have a zinc oxide nanowire under strain, you create a piezoelectric charge at both ends which forms a piezoelectric potential,” Wang explains. “The presence of the potential distorts the band structure in the wire, causing electrons to remain in the p-n junction longer and enhancing the efficiency of the LED.» The efficiency increase in the LED is proportional to the strain created.

Differences in the amount of strain applied translate to differences in light emitted from the root where the nanowires contact the GaN film. To fabricate the devices, a low-temperature chemical growth technique is used to create a patterned array of ZnO nanowires on a GaN thin film substrate with the c-axis pointing upward.

The interfaces between the nanowires and the GaN film form the bottom surfaces of the nanowires. After infiltrating the space between nanowires with a PMMA thermoplastic, oxygen plasma is used to etch away the PMMA enough to expose the tops of the ZnO nanowires. A nickel-gold electrode is then used to

form ohmic contact with the bottom gallium-nitride film, and a transparent indium-tin oxide (ITO) film is deposited on the top of the array to serve as a common electrode.

When pressure is applied to the device through handwriting, nanowires are compressed along their axial directions, creating a negative piezo-potential, while uncompressed nanowires have no potential.

A schematic showing a device for imaging pressure distribution by the piezo-phototronic effect is shown at the top of this article. It shows a nanowire-LED based pressure sensor array before (a) and after (b) applying a compressive strain. A convex character pattern, such as "ABC," molded on a sapphire substrate, is used to apply the pressure pattern on the top of the indium-tin oxide (ITO) electrode.

The researchers have pressed letters into the top of the device, which produces a corresponding light output from the bottom of the device. This output - which can all be read at the same time - can be processed and transmitted.The ability to see all of the emitters simultaneously allows the device to provide a quick response. "The response time is fast, and you can read a million pixels in a microsecond," says Wang.

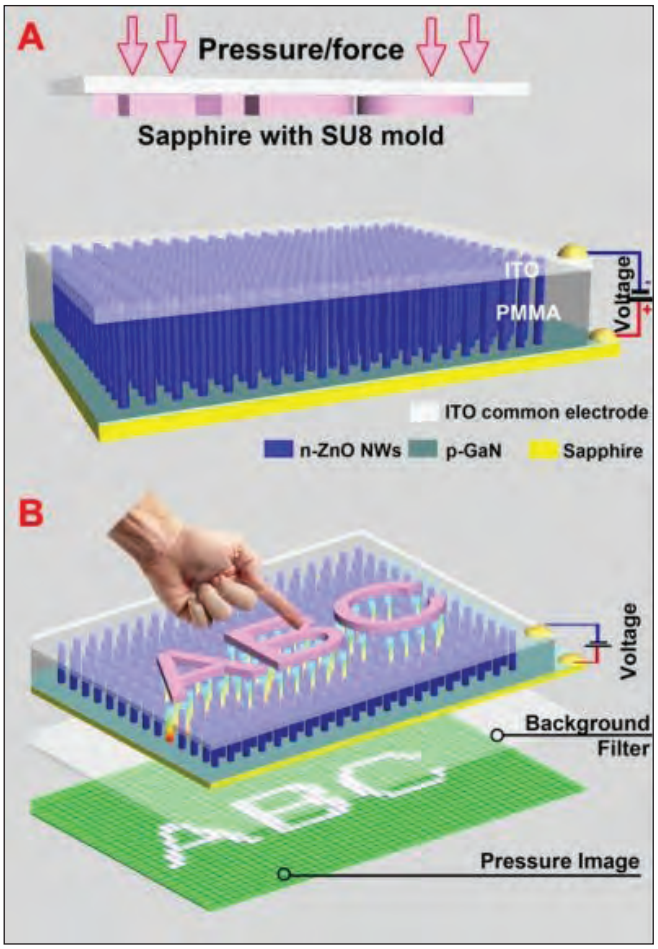
When the light emission is created, it can be detected immediately with the optical fibre.

"The nanowires stop emitting light when the pressure is relieved. Switching from one mode to the other takes 90 milliseconds or less, Wang adds.

The researchers studied the stability and reproducibility of the sensor array by examining the light emitting intensity of the individual pixels under strain for 25 repetitive on-off cycles. They found that the output fluctuation was approximately 5 percent, much smaller than the overall level of the signal. The robustness of more than 20,000 pixels was studied.

A spatial resolution of 2.7 $\mu$m was recorded from the device samples tested so far. Wang believes the resolution could be improved by reducing the diameter of the nanowires - allowing more nanowires to be grown - and by using a high-temperature fabrication process.

The researchers' study is described in detail in the paper, "High-resolution electroluminescent imaging of pressure distribution using a piezoelectric nanowire LED array," by Caofeng Pan et al in Nature Photonics (2013), published online on 11th August 2013. DOI:10.1038/nphoton.2013.191




This research was sponsored by the U.S. Department of Energy's Office of Basic Energy Sciences, the National Science Foundation, and the Knowledge Innovation Program of the Chinese Academy of Sciences.



When the light emission is created, it can be detected immediately with the optical fibre.The nanowires stop emitting light when the pressure is relieved. Switching from one mode to the other takes 90 milliseconds or less

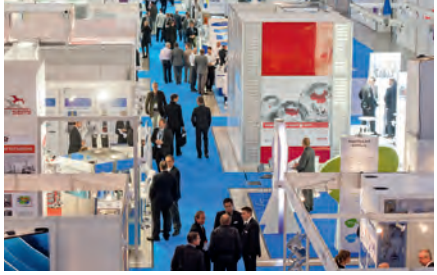
# Event Schedule

Programs and Events: 7-10 October 2013
Exhibits: 8-10 October 2013
Messe Dresden, Germany

www.semiconeuropa.org

SEMICON® Europa 2013

| | Expo | TechARENA 1<br>Free Participation - Hall 1 | TechARENA 2<br>Free Participation - Hall 2 | MEMS | Con<br>Semicond |
|---|---|---|---|---|---|
| **Monday**<br>**7 October** | | | | **International MEMS/MST Industry Forum**<br>Taking MEMS to the next level | **17th Fab M**<br>Networkin |
| **Tuesday**<br>**8 October** | **Exhibition**<br>10:00 – 17:00 | **Packaging**<br>Exhibitor Presentations<br>**Plastic Electronics**<br>Exhibitor Presentations | **Emerging Research Materials Session 1**<br>Graphene and 2D | **International MEMS/MST Industry Forum**<br>Taking MEMS to the next level | **17th Fab M**<br>Wafer Fab<br>with incre<br>novel ener |
| | | **MEMS**<br>Exhibitor Presentations<br>**Secondary Equipment Session**<br>- Invited Speakers<br>- Panel Discussion<br>- Exhibitor Presentations | **Emerging Research Materials Session 2**<br>New Trends in Epitaxy and Atomic Layer Processing | | **15th Europ**<br>Test Confer<br>A Reactive |
| **Wednesday**<br>**9 October** | **Exhibition**<br>10:00 – 17:00 | **Market Briefing** | **Silicon Photonics Session**<br>Interconnecting at light speed | **MEMUNITY MEMS Testing and Metrology Workshop** | **15th Europ**<br>Test Confer<br>A Reactive |
| | | **Test**<br>Exhibitor Presentations<br>**Best of APC Silicon Saxony**<br>**Night of Knowledge** | **3D TSV Session:**<br>The best of European 3D TSV Summit<br>- Invited Speakers<br>- Exhibitor Presentations | **MEMUNITY MEMS Testing and Metrology Workshop** | **450mm Se**<br>450mm: t<br>cooperatio |
| **Thursday**<br>**10 October** | **Exhibition**<br>10:00 – 16:00 | **Lithography Session**<br>- Invited Speakers<br>- Exhibitor Presentations | **Workshop on Equipment Assessment & Equipment Performance Improvements**<br>- Invited Speakers | | **450mm Se**<br>450mm: t<br>cooperatio |
| | | | **Process Control, Metrology, Automation and Software**<br>- Invited Speakers<br>- Exhibitor Presentations | | |


| ferences | | Business & Market | PE 2013 CONFERENCE | Standards | Training |
|---|---|---|---|---|---|
| ductor & Test | Packaging | | www.plastic-electronics.org | Free Participation | |
| anagers Forum<br>g Evening | | | | **PV Materials**<br>**PV Automation** | |
| anagers Forum<br>s - Fit for the future<br>ased flexibility and<br>gy concept | | | | **Gases & Liquid Chemicals** | |
| ean Manufacturing<br>rence (EMTC)<br>or Proactive Industry? | **Advanced Packaging Manufacturing Conference**<br>The Power of Packaging | **Press Conference**<br>**7th Executive Summit and Reception**<br>**SAXONY! - Get Together** | **Plastic Electronics Conference**<br>Plenary Session<br>Parallel Sessions<br>- OLED's for Displays and Lighting<br>- Flexible Photovoltaics<br>- Integrated Smart Systems | **Gases & Liquid Chemicals**<br>**Silicon Wafer** | |
| ean Manufacturing<br>rence (EMTC)<br>or Proactive Industry? | **Advanced Packaging Manufacturing Conference**<br>The Power of Packaging | **Market Briefing**<br>TechARENA 1 | **Plastic Electronics Conference**<br>Plenary Session | **Equipment Automation**<br>**Compound Semiconductor** | |
| ession<br>owards a global<br>on | **3D TSV Session:**<br>The best of European 3D TSV Summit<br>TechARENA 2 | | **Plastic Electronics Conference**<br>Parallel Sessions<br>- OLED's for Displays and Lighting<br>- Flexible Photovoltaics<br>- Integrated Smart Systems<br>- Microdisplay | **Compound Semiconductor** | |
| ession<br>owards a global<br>on | | **SEMI Members and Exhibitors Breakfast**<br>**EU Funding Opportunities Workshop**<br>What will the 10/100/20 strategy bring me?<br>Understanding upcoming EU funding mechanisms | **Plastic Electronics Conference**<br>Parallel Sessions<br>- OLED's for Displays and Lighting<br>- Flexible Photovoltaics<br>- Integrated Smart Systems<br>Plenary Session | **HB-LED**<br>**EHS**<br>**HB-LED**<br>**Silicon Wafer** | |

**CEI-Europe Courses in Advanced Technology**
Courses organized by CEI www.cei.se | www.semiconeuropa.org/courses

*Schedule is subject to change.*

imec · SPIL 矽品精密 Siliconware · TOKYO ELECTRON · NY Nanotech MARCY Nanocenter at SUNYIT · novaled · semi

# Era of atomic-scale semiconductor devices

University develop new technique for creating high-quality semiconductor thin films at the atomic scale.

RESEARCHERS AT NORTH CAROLINA STATE UNIVERSITY have developed a new technique for creating high-quality semiconductor thin films at the atomic scale -- meaning the films are only one atom thick. The technique can be used to create these thin films on a large scale, sufficient to coat wafers that are two inches wide, or larger.

"This could be used to scale current semiconductor technologies down to the atomic scale -- lasers, light-emitting diodes (LEDs), computer chips, anything," says Dr. Linyou Cao, an assistant professor of materials science and engineering at NC State and senior author of a paper on the work. "People have been talking about this concept for a long time, but it wasn't possible. With this discovery, I think it's possible."

The researchers worked with molybdenum sulphide (MoS2), an inexpensive semiconductor material with electronic and optical properties similar to materials already used in the semiconductor industry.

However, MoS2 is different from other semiconductor materials because it can be "grown" in layers only one atom thick without compromising its properties. In the new technique, researchers place sulphur and molybdenum chloride powders in a furnace and gradually raise the temperature to 850 degrees Celsius, which vaporizes the powder. The two substances react at high temperatures to form MoS2. While still under high temperatures, the vapor is then deposited in a thin layer onto the substrate.

"The key to our success is the development of a new growth mechanism, a self-limiting growth," Cao says. The researchers can precisely control the thickness of the MoS2 layer by controlling the partial pressure and vapour pressure in the furnace.

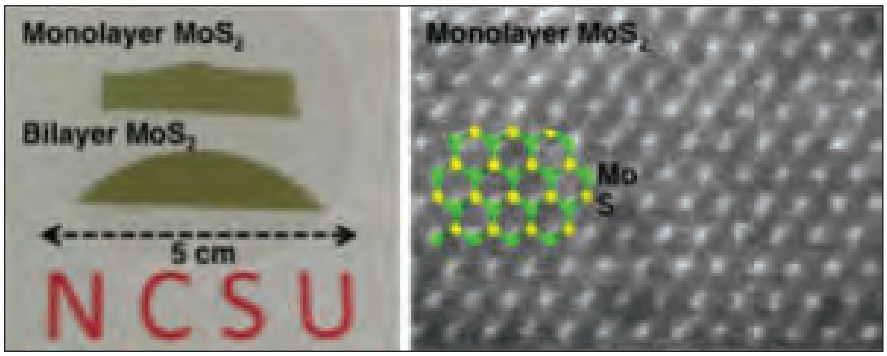
Partial pressure is the tendency of atoms or molecules suspended in the air to condense into a solid and settle onto the substrate. Vapour pressure is the tendency of solid atoms or molecules on the substrate to vaporize and rise into the air.

To create a single layer of MoS2 on the substrate, the partial pressure must be higher than the vapour pressure. The higher the partial pressure, the more layers of MoS2 will settle to the bottom. If the partial pressure is higher than the vapour pressure of a single layer of atoms on the substrate, but not higher than the vapour pressure of two layers, the balance between the partial pressure and the vapour pressure can ensure that thin-film growth automatically stops once the monolayer is formed. Cao calls this "self-limiting" growth. Partial pressure is controlled by adjusting the amount of molybdenum chloride in the furnace -- the more molybdenum is in the furnace, the higher the partial pressure.

"Using this technique, we can create wafer-scale MoS2 monolayer thin films, one atom thick, every time," Cao says. "We can also produce layers that are two, three or four atoms thick."

Cao's team is now trying to find ways to create similar thin films in which each atomic layer is made of a different material. Cao is also working to create field-effect transistors and LEDs using the technique. Cao has filed a patent on the new technique.






Molybdenum sulfide. (Credit: Linyou Cao)

**Journal Reference:**
Yifei Yu, Chun Li, Yi Liu, Liqin Su, Yong Zhang, Linyou Cao.Controlled Scalable Synthesis of Uniform, High-Quality Monolayer and Few-layer MoS2 Films. Scientific Reports, 2013; 3 DOI: 10.1038/srep01866
North Carolina State University (2013, May 22). New technique may open up an era of atomic-scale semiconductor devices. ScienceDaily.

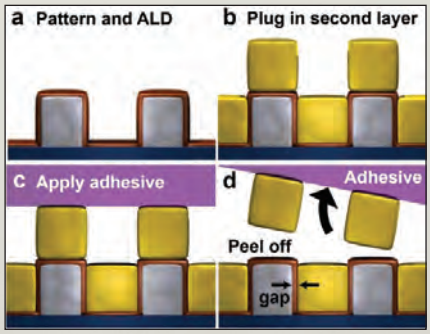
# Scotch tape makes electronic devices smaller and better

Atomic layer lithography has the potential to create ultra-small sensors with increased sensitivity using Scotch tape.

AN INTERNATIONAL GROUP of researchers from the University of Minnesota, Argonne National Laboratory and Seoul National University have discovered a technique in manufacturing nanostructures that has the potential to make electrical and optical devices smaller and better than ever before. A surprising low-tech tool of Scotch Magic tape ended up being one of the keys to the discovery.

The research is published in online research journal Nature Communications. Combining several standard nanofabrication techniques - with the final addition of the Scotch Magic tape- researchers at the University of Minnesota created extremely thin gaps through a layer of metal and patterned these tiny gaps over the entire surface of a four-inch silicon wafer.

The smallest gaps were only a nanometre wide, much smaller than most researchers have been able to achieve. What's more, the widths of the gaps could be controlled on the atomic level. This sceintists say this work provides the basis for producing new and better nanostructures that are at the core of advanced electronic and optical devices. One of the potential uses of nanometre-scale gaps in metal layers is to squeeze light into spaces much smaller than is otherwise possible. Collaborators at Seoul National University, led by Dai-Sik Kim, and Argonne National Laboratory, led by Matthew Pelton, showed that light could readily be squeezed through these gaps, even though the gaps are hundreds or even thousands of times smaller than the wavelength of the light used.




Researchers are very interested in forcing light into small spaces because this is a way of boosting the intensity of the light. The collaborators found that the intensity inside the gaps is increased by as much as 600 million times.

"Our technology, called atomic layer lithography, has the potential to create ultra-small sensors with increased sensitivity and also enable new and exciting experiments at the nanoscale like we've never been able to do before," says Sang-Hyun Oh, one of the lead researchers on the study and a professor of electrical and computer engineering in the University of Minnesota's College of Science and Engineering. "This research also provides the basis for future studies to improve electronic and photonic devices."

An image showing the new patterning technology, atomic layer lithography, based on a layering technique at the atomic level, is shown at the top of this article. A layer of metal fills the nano-patterns over an entire wafer and simple Scotch Magic tape was used to remove the excess metal on the surface and expose the atomic scale nano-gaps. One of the most surprising outcomes of the research is that Scotch Magic tape was one of the keys to the discovery.

Etching one-nanometre-wide gaps into metals is not feasible with existing tools. Instead, the researchers in Oh's team constructed the nano-gaps by layering atomic-scale thin films on the sides of metal patterns and then capping the structure with another metal layer.

No expensive patterning tools were needed to form the gaps this way, but it was challenging to remove the excess metals on top and expose the tiny gaps. During a frustrating struggle of trying to find a way to remove the metal films, University of Minnesota Ph.D. student and lead author of the study Xiaoshu Chen found that by using simple Scotch Magic tape, the excess metals could be easily removed.

"The Scotch tape works nicely, which was unexpected," says Oh. "Our technique is so simple yet can create uniform and ultra-small gaps like we've never been able to do before. We hope that it will rapidly be taken up by many researchers."

The research was funded by the U.S. Department of Defence (DARPA Young Faculty Award and the ONR Young Investigator Program), the U.S. Department of Energy and the National Research Foundation of Korea with capital equipment funding from the Minnesota Partnership for Biotechnology and Medical Genomics.

# Die and flip-chip bonding striving for ultra high precision

Cost-effective surface mounting of complex stacked die using TSV interconnect calls for ultra-high-precision die and flip-chip bonders. Consequently, back-end equipment vendors and process designers must come up with modular concepts to accommodate a broad scope of micro-assembly tasks. Dr Johann Weinhändler, Managing Director of Amicra Microtechnologies GmbH, talks about how the company is delivering on these challenges.

AMICRA WAS ESTABLISHED IN 2001 on the premise of delivering state-of-the-art micro-electronics manufacturing and test equipment for the semiconductor and optoelectronics back-end, fiber optics and optical sensors, LED and MEMS industries. The company operates on a solid stock of technology know-how in its chosen fields: products and services in high-precision processing and handling. The portfolio has since grown to cover a wide and impressive scope of micro-assembly cells and wafer-ink systems, customized laser lift-off, silicone gel dispensing, LED test and lens inspection systems.

The company took the global stage in 2009 by engaging a young and innovative management team led by Johann Weinhändler, Horst Lapsien, Stefan Wolf and Rudolf Kaiser (Figure 1).


Figure 1: The Amicra management team. Left to right: Rudolf Kaiser (Managing Director), Stefan Wolf (CFO), Johann Weinhaendler (Managing Director) and Horst Lapsien (Managing Director).
Source: altrofoto.de (Mittelbayerische Zeitung)

This team set Amicra on its current program: the high end, leading-edge segment of high-precision assembly equipment, software development, design of customized machine controls including vision and image processing – with an extra weight put on efficient handling, gripping and feeding systems with elaborate overlapping motion control algorithms.

Earlier this year Amicra received a new round of major private equity financing in view of the growing importance of the innovative AFCPlus and NovaPlus platforms. This is being used to further expand the company's presence at its home base and worldwide including the recently opened corporate offices in Sunnyvale, California, located right in the heart of the Silicon Valley and Singapore for the operations in Asia.

Last year, Amicra generated sales of about 8 million euros. Within the next five years Amicra expects to reach an annual sales volume of 50 million euros, with an estimated employee base of around 200 worldwide, says Dr. Johann Weinhändler.

This promising outlook is possible due to the rapidly evolving smartphones and communication devices, with their insatiable demand for memory space, touch sensors and LED displays, and their associated transport infrastructure and server farms. The explosion of these markets has just begun. Dr. Weinhändler says "Our vision is to grow from technology leader also to market leader in our field."

## Ultra-high-precision now is the marching order

With our latest product developments for flip-chip and die attach applications, such as the AFCPlus (Figure 2) and the flagship NovaPlus (Figure 3), Amicra is fully committed to the optimization of bond processes for all kinds of miniaturized


Figure 2: The ultra-high precision AFCPlus bonding system realizes a placement accuracy of +0.5µm at 3 Sigma

and highly demanding devices and their stringent requirements for relentless cost reduction in the back-end packaging processes.

The current company product focus is providing the highest micro-assembly placement accuracy in the 0.5 mm to 2.5 µm range, possible-being best-in-class, as well as offering fully automated wafer inking systems that are coupled with highly flexible customization and fulfilling the latest requirements in vertical 3D stacking and horizontal SoC assembly, points out Dr. Weinhändler. Amicra has acquired a substantial number of important customers in the U.S. and Asia – with the understanding that few are willing to be named in public.

An exception is a leading Taiwanese contract manufacturer, which has recently installed one of Amicra's Nova Plus systems for a large fan-out application with a panel size of 370 x 470 mm. Back in Europe, a major LD manufacturer has reportedly also selected the NovaPlus die-attach and flip-chip machine for its high-volume HDD assembly.

In another on-going customer project a NOVAPlus is used in a WLP packaging application, which attaches 20-mm diameter Au dies with 5/10µm-pitched CuSn microbumps per flip-chip on 8-inch wafers. The temperature of the (vacuum) thermo-compression is 150 to 225 °C, at a bond force of 1 to 2 kilograms. Parts are pre-fixed at 80 °C by epoxy dispensing (which evaporates during thermo-compression).

The dies are placed at a temperature range of 65 to 95 °C. With our broad product line of semi-automatic and fully automatic wafer ink systems, Amicra is currently setting industry standards at a dot size down to 70µm, as well as the inking of diced or undiced wafers. Amicra's AIS system enables inking of up to 12-inch (300mm) diameter wafers.

## Die and flip-chip processing of die stacks and 3D ICs

Amicra's high-accuracy NOVA and AFC die- and flip-chip bonders and wafer-ink systems are well suited for today's die and flip-chip processing including 3D-IC and stack-die, because they cover the full scope of high-volume micro and nano assembly applications, and they are offering optional flip-chip bonding, wafer mapping, and post-bond inspection as well.

The ultra-high-precision AFCPlus die and flip-chip bonding system is one of Amicra's well received state-of-the-art systems. It is laid out in a modular concept for flexibility and customer accommodation and it realizes a placement accuracy of +0.5µm at 3 Sigma for die and flip-chip attach. At a cycle time of <15 sec, it is well suited for processing micro-optic and micro-mechanic components, with eutectic bonding via diode laser or heating plate. AFCPlus offers auto loading of wafers and substrates, wafer mapping, epoxy stamping and dispensing.

Active alignment is also provided on request, while post-bond inspection is included; UV curing is featured as an option. The NOVAPlus die-attach and flip-chip bonder, introduced in 2010, currently is the industry-leading platform in terms of precision and productivity.

Figure 4 offers a glimpse of its inner workings. The machine was first field-approved as a basic platform in 2007 to combine extremely high accuracy (+2.5µm at 3 Sigma) with high-speed processing at a very low cycle time of <3 sec. Figure 5 shows its dual bond head concept.

Auto-loading is provided for wafers up to 12 inch (300 mm) diameter and up to 450 mm substrate wafers, 370x470 mm fan-out panels or even larger substrates up to 600 x 600 mm.

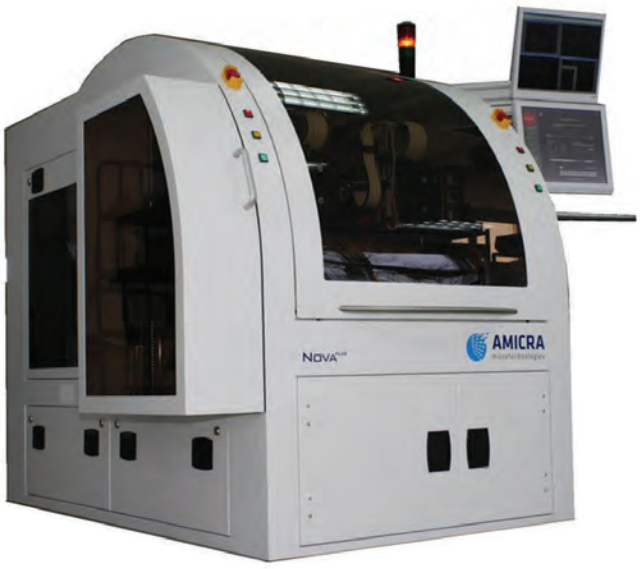



Figure 3: The die-attach and flip-chip placement system NOVAPlus combines high accuracy of +2.5µm at 3 Sigma with a very low cycle time of <3 seconds


Figure 4: NOVAPlus opened

The machine also features active bond force control, at a bond force of up to 5 kilograms. These specs make the NOVAPlus well suited for eutectic, epoxy, and laser bonding. Alignment is passive. Post-bond inspection and measurement is also a standard feature.

## Accommodating very large panel sizes

The NOVAPlus modular concept aims at micro-assembly applications in various segments of advanced semiconductor packaging, including TSV and eWLB, 3D-IC, complex die stacking, WLP and AuSn processing.

This is especially valuable for the placement of large fan-out panels of up to 370 x 470 mm, at an accuracy of +/- 2.5µm as realized for one of the largest Taiwanese Assemblers (Figure 6).

According to Dr. Weinhändler, the NOVAPlus currently is the only machine on the market for such a process that offers this kind of accuracy combined with a very large substrate working area for a panel size of up to 600 x 600 mm.

## NovaPlus accuracy test in a live environment

An accuracy test at a real working NOVAPlus machine is given in Figure 7, taken after the bond measurements. The cyancoloured frame shows the +/- 2.5µm target area. All parts with less epoxy material are inside this processing window. Those with more epoxy show a much larger distribution and offset in the Y direction: About 10 percent of them are outside the +/- 2.5µm window.

Both the AFCPlus and the NOVAPlus were exhibited at the recent Semicon Taiwan and at Semicon West in San Francisco, Next stop on the high-accuracy Amicra die bonding solutions will be Productronica 2013 in Munich, Germany and Amicra looks unstoppable.



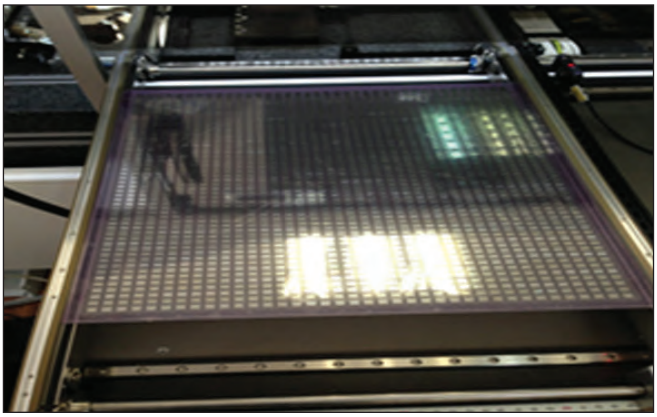


Figure 6: NOVAPlus configured for very large substrates up to 600 x 600mm

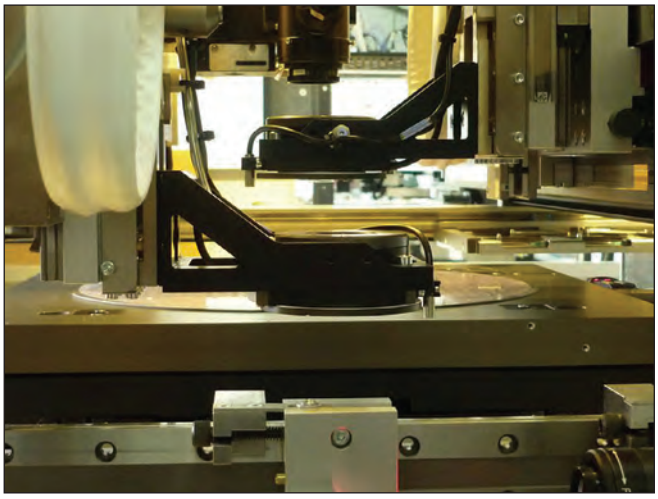


Figure 5: The dual bond head concept

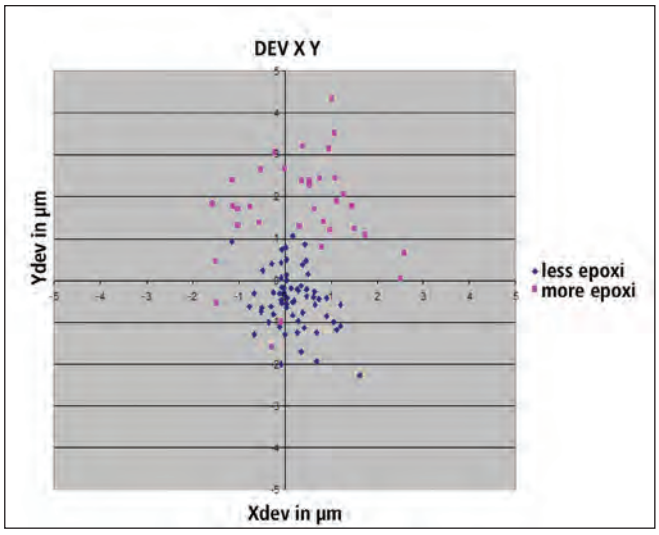



Figure 7. NOVAPlus accuracy test after bond measurements

# Optimum surface quality on Silicon based substrates

Semiconductor organisations worldwide realise the benefits of Logitech Precision Systems for the preparation of substrates from hard materials such as Silicon, Silicon Carbide, Sapphire and CVD Diamond.

Logitech Limited has invested heavily in the last year to advance system technologies within key product areas. A high level of success has been achieved in the areas of:

- Superior load and controllability for increased material removal rates, while maintaining low surface damage
- Enhanced plate flatness monitoring and higher accuracy jig control for superior flatness and TTV
- Development of user friendly, industry standard software platforms.

In response to client and market demand Logitech has developed a High Speed Lapping and Polishing System, primarily for hard materials. This benchtop solution is ideally suited to research laboratories and small scale production, due to its flexibility, reliability and low cost of ownership. The system is perfect for the processing and pilot production analysis of Silicon and Silicon based substrates.

An array of advanced in-situ sensors constantly provide the operator with real-time process information. Monitored parameters include Coefficient of Fricton, slurry and pad/plate interface temperatures. All of which are paramount for optimal performance. The High Speed Lapping and Polishing system can process substrates, wafers and part wafers up to 100mm/4" diameter quickly and easily due to the 300rpm variable plate speed and higher sample load capability. The user friendly interchangeable plate/pad design ensures that the High Speed system maintains maximum efficiency across the complete process. This is further highlighted with the high level of automated system operations and programmability, allowing full processes or sub processes to be run with minimal intervention.

Key applications for Logitech Lapping and Polishing Systems include:

- Wafer polishing to sub-nm levels
- Removal of epi-layers with nanometer level precision
- Capability to delayer up to 100mm (4") diameter wafers
- Polishing accuracy to nanometer levels for fault isolation
- Preparation of substrates for use in electronic device manufacture

Further information on Logitech technology, system solutions and material processing can be found at www.logitech.uk.com or by contacting our team on: +44 (0) 1389 875444.

# Meeting next-generation advanced packaging geometries through material advancements

The boom in the mobile market with increasing demands for smaller geometries has created the need for novel and innovative chemistries to overcome the limitations of existing materials. Jianwei Dong, Wataru Tachikawa, Richard Chen and Joon-Seok Oh at Dow Electronic Materials discuss how material advancements can meet the needs of next-generation wafer-level, 2.5D and 3D packaging technologies.

THE EXPLODING MOBILE MARKET is driving feature requirements for next-generation semiconductor devices to increasingly smaller geometries. As a result, there is increased risk of wafer stress due to more delicate features, thinner wafers to handle, and in the case of 3D IC technologies, higher density through silicon vias (TSVs) and the need to accommodate microbump structures. Equipment and processes can only go so far with existing material sets initially developed for the last generation of packages before they hit process limitations. The task has fallen largely on the shoulders of material science to tackle these limitations with novel and innovative chemistries.

Fortunately, as the entire semiconductor packaging ecosystem has entered a new age of cooperation and transparency, collaboration with R&D centers and partnerships with equipment suppliers have resulted in significant developments across the spectrum of advanced packaging materials to meet these new challenges. This article will present a number of recent technology breakthroughs including compatibility of metallurgies for tin silver (SnAg) capped copper (Cu) pillars; advancements in temporary bond/debond adhesives that allow for clean debond from active device wafers at room temperature; pre-applied underfill for die stacking that addresses the fine pitches required for stacking logic system-on-chips (SoCs) with TSVs; and low stress, high performance dielectrics that address increased stress and wafer bow resulting from thinner substrates. These material advancements began with either new material formulations or proven materials that have been optimized to address the emerging requirements of next-generation devices.

## SnAg-capped cu pillars

With mobile device manufacturers clamoring for higher density, fine-pitch ICs, a trend to replace conventional flip chip solder bumps with Cu pillar bumps capped with SnAg solder has emerged. This is because SnAg capped Cu pillars enable the higher density interconnects and lower profiles needed for emerging 2.5D interposer and 3D packaging applications. Devices that have made the transition to SnAg capped Cu pillars include high-end graphics processors, FPGAs, power amplifiers, MEMS and HB-LEDs.

In particular, silicon interposers and fine-pitch Cu pillar micro-bumps represent the two technologies that have come to define a 2.5D packaging approach. Cu pillars provide the short, low inductance, efficient interconnections between ICs in vertical stacks as well as between an IC and the silicon interposer. Capping Cu pillars with SnAg allows for improved reflow with the silicon interposer, achieving <40$\mu$m pitches. Together, micro-bumps and silicon interposers provide a high-speed and high-bandwidth communication highway for side-by-side die (and stack) placement.[1]

When selecting materials that will result in high-yield, reliable electroplated Cu pillar and Cu $\mu$pillar capped structures, it is important to consider the interface between metal layers, particularly as Cu pillar cap diameters shrink to $\mu$pillar dimensions (<30$\mu$m diameter). Additionally, interfacial properties and intermetallic compounds (IMCs) must be understood and controlled. The plating chemistry has significant influence on the compatibility of each layer, as well as control of IMC-growth, micro-void formation and overall stack reliability.

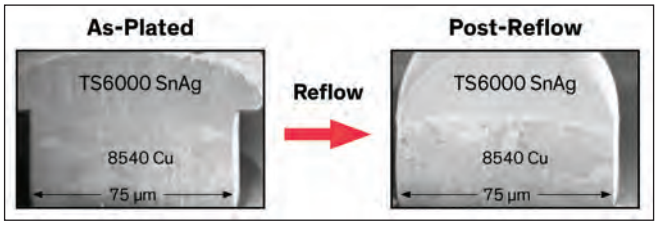



Figure 1: Left, Cu $\mu$pillar with SnAg cap as plated. Right, Cu $\mu$pillar with SnAg cap post reflow

In designing chemistries, the compatibility of the Cu and solder materials is of critical importance. This compatibility is evidenced by such characteristics as a smooth, continuous IMC layer formed after reflow of Cu pillar and Cu $\mu$pillar with SnAg solder caps (Figure 1). The dominant IMC formed is $Cu_6Sn_5$ between the Cu and SnAg interface after reflow. IMCs make up a significant fraction of the SnAg cap for Cu $\mu$pillar bump. Additionally, no interfacial voiding should be observed after reflow.

Further, industry needs for higher throughput, smaller, finer pitch features and low cost of ownership (COO), in addition to requirements for flatter pillars with smooth surface and good uniformity, is driving further development work on next-generation Cu pillar and SnAg chemistries.

The most recently developed formulations have satisfied all key design criteria including highly uniform Cu pillars (within die (WID) < 5%); a flat pillar profile (total indicated runout (TIR) < 5%); smooth surface morphology; and compatibility with SnAg capping (Table 1).

| *Deposit Property (Relative)* | Legacy Formulation Cu Pillar | Formulation A Cu Pillar |
|---|---|---|
| Surface profile | Domed (TIR>0) | Flat (TIR~0) |
| Surface morphology | Smooth | Smooth |
| Organic incorporation in bulk Cu | Relatively low (<20ppm total) | Relatively low (<20ppm total) |
| Compatibility with SnAg capping | Compatible | Compatible |

Table 1: Comparison data between a commercially available product and a new Cu Pillar formulation

Additionally, a compatible SnAg counterpart to the Cu pillar chemistry has been developed, resulting in a formulation that demonstrates high speed plating (>3μm/min); highly uniform SnAg deposits; (WID <±5% for challenging fine-pitch die designs); macro and micro void-free performance (X-ray); smoother surface morphology (as-plated and post-reflow) and a smoother, void-free interface with Cu pillar compared with its predecessors. Overall, this material exhibits the widest process window with the most robust process flexibility and a competitive COO.

## Temporary bond/debond

In 3D IC development, the temporary bond and debond step has provided ongoing obstacles and continues to be considered a roadblock to commercialization. Materials must meet temperature stability and chemical resistance requirements due to the various process steps that a bonded wafer pair undergoes -- from the time of application to the process wafer, through the backside thinning and processing, debonding and cleaning.

The adhesive used to create a temporary bond should have certain attributes to be considered practical. For example, the adhesive has to survive several processes that will inflict environmental extremes. The bond has to be strong enough to support the wafer through the thinning process, but easily debonded when needed without damage to the wafer or the electronic devices. The debonding must be gentle since the wafer is so fragile and any remaining residue needs to be easily removed.[2]

While many materials on the market have achieved many of these attributes, the gating technical issue has been with the debonding step. One solution that has recently been developed is based on a well-established permanent bonding adhesive. This benzocyclobutene (BCB) material offers inherently attractive material properties such as high thermal stability (withstanding temperatures up to 300°C), high chemical resistance and low temperature curing. It has been successfully modified to make it easily releasable from various surfaces, allowing it to be used effectively as a temporary bonding adhesive.

Clean debonding is critical, and this one requires no additional process steps for removal from the active die surface, such as laser/UV ashing or solvent soaks. Rather, an adhesion promoter is spin-coated onto the carrier wafer so that when it is debonded

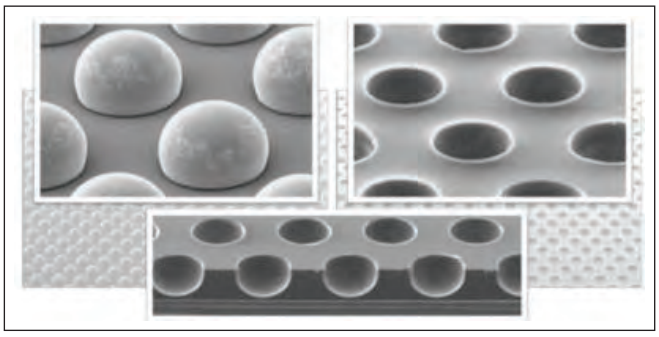


Figure 2: Even dense, C4-bumped wafers debond cleanly: SnAg solder bumps after debonding (left), BCB-based temporary bonding adhesive film after debonding (right, below)

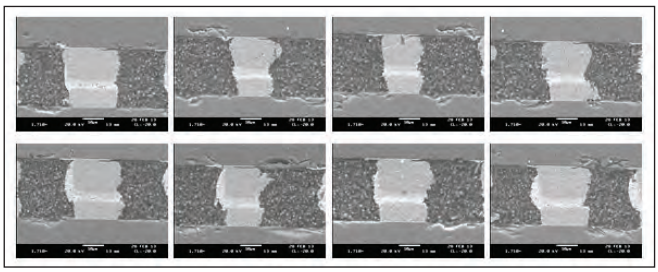


Figure 3: 100 % electrical joining of 1600 solder joints per daisy chain

using mechanical lift-off at room temperature, the adhesive goes with the carrier and leaves the device wafer free of adhesive material (Figure 2). In the event of bumped wafers, a solvent rinse may be required to remove any minor residue.

Another advantage of the modified BCB material is that while it withstands high temperatures (>300oC/1 hr), it bonds at low temperatures, which eliminates bonder/heater time and increases wafer throughput. Final cure is then performed in a batch oven process outside the bonder with no alignment shift, for increased throughput and reduced COO.

## Pre applied underfill

Underfilling 3D IC stacks is critical to help control TSV-induced stress and also to help control warpage of these ultra-thin stacks caused by CTE mismatch between the device and its substrate. In fact, thermal modeling and simulation studies show that underfill, substrate and mold compound thermal strains play important roles in the warpage evolution.[3]

After backside processing, thin devices must be assembled into stacked-die structures. Current underfill technologies required for assembly have issues with voiding and have been known to result in filler entrapment during bonding. Additionally, there have been issues with bleed and creep of underfill around the die, particularly with today's finer pitch geometries.

Alternatively, pre-applied underfills allow for simultaneous electrical and adhesive die bonding. One such material has performed well when applied as a wafer-level underfill for bonding Cu pillars with 25μm diameter and 50μm pitch on thinned die.

When applying via vacuum lamination to 300mm wafers, the result is good uniformity and thickness. It also addresses the fine pitches required for stacking logic SoCs with TSVs; an application where capillary underfills fall short. Test vehicles have demonstrated 100 % electrical joining after thermocompression bonding (Figure 3).

## Low stress high performance dielectrics

As previously mentioned, increased stress and wafer bow is also an issue due to the thinner substrates required for vertical integration in TSV and 3D packages. In addition to underfill materials and molding compounds, cured dielectric materials also contribute to the condition. Recent developments extending the thermal, electrical and chemical stability of BCB-based materials have resulted in a lower residual stress prototype of a photodielectric that is currently used in high-volume manufacturing

The new polymer is modified to allow compatibility with conventional tetramethyl ammonium hydroxide (TMAH)-based developers, vs. the traditional solvent-based BCB photodielectric. The new aqueous-developable BCB photodielectric material can easily produce patterned features to 5$\mu$m and below, with aspect ratios of 2:1 (Figure 4).

In addition to lower COO and the aforementioned lower residual stress, this photodielectric material also exhibits desirable properties such as low-temperature cure, high thermal stability with low outgassing to withstand SnAg reflow temperatures and excellent mechanical properties needed to survive integration and meet the needs for improved elongation.

## Conclusion

Materials suppliers increasingly find themselves in the role of developing solutions to overcome known challenges or limitations of existing processes and equipment. The surest and most efficient approach to address the emerging requirements of next-generation devices is to innovate new technologies that leverage and optimize proven materials when possible. Therefore, combining the known performance of existing material sets with the enhanced capabilities of new chemistries is ideal for accelerating the transition to future manufacturing nodes.

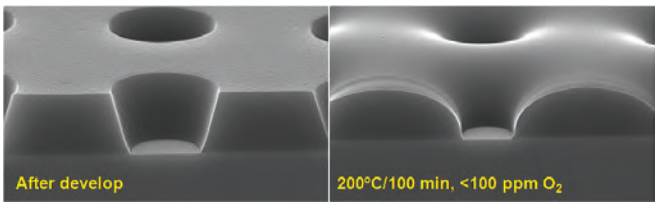



Figure 4: 70ºtilt cross sections SEM of XP120201 depicting 5 $\mu$m, 1:2 contact holes after develop (left) and after soft cure (right).

As a result, a full suite of compatible chemistries is now ready to meet the needs of next-generation wafer-level, 2.5D and 3D packaging technologies.



**References**

1. D. Patterson, "2.5/3D Packaging Enablement through Copper Pillar Technology", Chip Scale Review, July/Aug 2012, p20
2. J. A. Sharpe, M. B. Jordan, S. L. Burkett, and M. E. Barkey, "Analyzing the Behavior and Shear Strength of Common Adhesives used in Temporary Wafer Bonding" Proc., 2013 Electronic Components Technologies Conference, pp 94-95
3. K. Karaminal, "A Comparative Simulation Study of 3D Through Silicon Stack Assembly Processes", Proc. 2013 Electronics Components Technology Conference p. 1

# Europe's semiconductor industry can become a global force again

The European Commission's decision to spend up to 10 billion euros for R&D activities will create a level playing field against competition from around the world.

SEVERAL MONTHS AFTER THE EUROPEAN COMMISSION'S historic decision to take measures to hoist the European chip industry back into the world league, managers and experts of this industry come together for the SEMICON Europa trade fair and congress. The event will reflect the spirit of optimism that is spreading across Europe's chip-makers and suppliers.

Last spring as an initiative of EC vice president Neelie Kroess, the European Commission agreed to spend as much as 10 billion euros for R&D activities in the semiconductor industry. The move was intended to create a level playing field against competition from around the world and to leverage further 100 billion euros of investments into this industry segment. Such a huge sum of money was deemed necessary to enable the European chip industry to compete against their Asian and American counterparts at eye-level.

The upcoming SEMICON Europa (October 8 to 10) exhibition is the first major industry meeting after this landmark decision and offers a good opportunity to compare the high-flying expectations with the reality of the industry in Europe. While it is certainly be too early to judge if the EC's measure bears fruit, the tone for SEMICON Europa reflects an industry determined to seize the opportunity and to take the steps necessary towards implementing the technologies associated with the next generation of semiconductor manufacturing.

The EC move focused on fostering the 450mm wafer technology as well as on further miniaturization ("More Moore") and on integrating additional functionality and materials into the chips (More than Moore).

All these aspects and several more are reflected in the SEMICON Europa agenda. The congress offers a plethora of presentations from 450mm wafer processing to MEMS, FDSOI, and Advanced Packaging, providing the attendees valuable insights into the EU investments and program participation. Over 40 presentations provide insights into current trends, technologies and processes in next-generation semiconductor manufacturing and testing. "The industry has reached a historic turning point", summarizes SEMI Europe president Heinz Kundert. "The impact of 450mm wafer processing as well as other business challenges in semiconductor and related micro and nano-electronics industries will be at the heart of SEMICON Europa".

Under the aspect of next-generation semiconductor manufacturing, the two-day special program under the title "450mm: Towards a Global Cooperation" certainly will be of special interest for managers and industry leaders involved in the preparatory works to establish this technology. It is the place to discuss European and global achievements in 450mm wafer processing and how consortia, OEMs and IDMs need to collaborate to achieve the transition to this productivity-boosting manufacturing new world.

High-level experts such as the CATRENE program director Denis Rousset, Eniac executive director Andreas Wild or Bernie Caprano, the program manager for the EU Research at Intel share their experience, insights and estimation about future developments in this industry.

Rousset's presentation will focus on automation aspects of 450mm wafer processing. Based on the observation that manual batch handling has reached physical limits, he considers how a fully-automated 450mm wafer fab can look like. The answer is robotics. To gather the experience and knowledge to implement such a robotized landscape, Rousset proposes a two-steps approach, with first implementing test beds and then pilot lines. A number of EU-funded research projects are currently compiling the required expertise.

Frank Bornebroek from ASML will provide an overview on the 450mm program. He will discuss the progress the lithography equipment manufacturer has made since last year- including the challenges for lithography systems with regard to the transition to larger wafers and smaller geometries. Another track of presentations that can be expected to receive attention are "Taking MEMS to the next level". With MEMS currently a successful commercial branch of the semiconductor industry, future technology development directions are key to market developments.


The versatility of these MEMS devices gives birth to an ever-increasing number of different applications. This, in turn, fuels a technology differentiation process within the MEMS world. Accordingly, the presentations at the congress cover topics as diverse as MEMS microphones (Ulrich Krumbein, Infineon), micro optical systems (Basaam Saandany, Si-Ware Systems) or bio-medical sensors (Frederic Breussin, Yole Développement). The presenters' interest also lies with high-volume MEMS production, 3D TSVs, testing and packaging with special focus on rough automotive application environments.

SEMICON Europa also hosts the popular Fab Manager Forum where real-world managers exchange experiences and views on relevant issues in this industry including the "Night of Knowledge" Topics include an ITRS roadmap update, and a selection of current industry issues followed by a networking reception.

In addition to all these "classic" semiconductor topics, the event co-locates with another conference focusing on one of the most promising relatives to the traditional semiconductor technology: Organic electronics, aka Plastic Electronics.

The PE 2013 is one of the most prestigious meetings of this aspirant industry branch. After many years of research this technology is now clearly approaching the stadium of commercialization. Hence, manufacturability is the current buzzword throughout this young industry.

Topics which are creating interest are OLEDs for display and lighting applications, flexible PV devices as well as organic and hybrid-based integrated smart systems. The conference attracts high-profile speakers from companies such as Nokia, Plastic Logic, Philips Lighting and Panasonic, to name just a few.

# MUF and wafers get new acoustic tools

Modifications of production processes and changes in device dimensions require new non-destructive techniques to inspect for reliability. Tom Adams, consultant, Sonoscan, Inc. discusses recent advances in the acoustic microscope imaging of molded underfill flip chips and 200mm and 300mm silicon wafers.

BEFORE THE INTRODUCTION OF MOLDED UNDERFILL, the attachment of a flip chip to its substrate was imaged acoustically by a transducer that scanned the exposed silicon back side of the chip. The transducer pulsed ultrasound into the chip thousands of times a second as it scanned, and received the return echoes. Silicon is an excellent propagator of ultrasound; very little of the ultrasound is absorbed by the silicon during its fast passage to the underfill material and solder bumps that are the objects of interest.

Ultrasound is reflected at material interfaces - chip face to underfill, chip face to solder bump, and others. The most highly reflective interfaces are those between a solid (silicon, solder, underfill) and the air or vacuum in a gap. Some common gaps in flip chips are cracks within bumps, voids in the underfill, and non-bonding of bumps to their pads. These are the items that will determine whether a flip chip passes or fails.

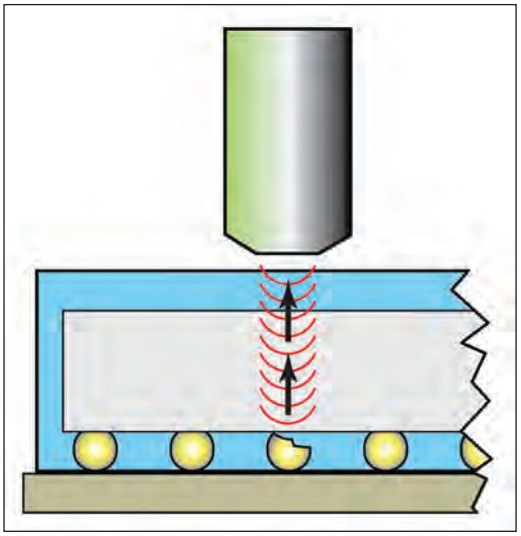


Figure 1. Ultrasound (red) pulsed into a molded underfill flip chip must travel through the attenuating underfill (blue) to image the solder bumps

When scanning the silicon back side of a flip chip, Sonoscan's personnel could use C-SAM® acoustic microscope systems equipped with very high frequency transducers because of the high acoustic transparency of silicon, and because some of the die were quite thin. Transducer frequencies could be 230, 300 or even 400 MHz. These transducers are all designed and manufactured by Sonoscan. Higher frequencies give better spatial resolution in the acoustic image. Higher frequencies are also absorbed more rapidly when traveling through materials, but silicon absorbs so little silicon that penetration of the pulse is only mildly affected.

The introduction of molded underfill gave manufacturers the ability to simplify production processes: instead of first underfilling the flip chip, and then later perhaps overmolding it, they could accomplish both functions in a single operation. But it also meant that overmolded flip chips could no longer be imaged at the high frequencies used on bare chips.

The problem is in the encapsulant material. The materials used in molded underfill are more absorbing of ultrasound than the overmold that is applied to bare-silicon flip chips as a separate process after acoustic imaging. The

MUF material contains a polymer matrix that absorbs ultrasound, and filler particles that scatter ultrasound. Typically a lower acoustic frequency having lower resolution must be used to image flip chips having MUF.

In a flip chip having molded underfill, the ultrasound must travel twice - as a downward-moving pulse, and later as an upward-moving echo - through the encapsulant material on top of the silicon [Figure 1]. (The encapsulant material in the attachment layer, changed by the capillary flow process, is less absorbing than this layer.)

Sonoscan's laboratories have seen hundreds of molded underfill samples. Most can be imaged acoustically, generally with a lower-resolution transducer, but with good results. A few flip chips are encapsulated with an underfill material that is especially attenuating, but these can usually still be imaged with meaningful results, and have been very useful in giving clues about transducer design changes that can provide both good penetration and good resolution. A few mold compounds have proved to be so attenuating that meaningful details may not be observed.

Broadly speaking, however, considerable success has been achieved in finding methods to image molded underfill flip chips. In part, success has been a matter of designing a new transducer with the right parameters to image a given molded flip chip design. Sonoscan routinely designs and manufactures customized transducers to meet the specific requirements of customer parts of all kinds that need something other than a standard transducer. The company develops and produces all of its transducers above 50 MHz. Knowing how to turn out a transducer to meet given parameters has been useful in imaging molded underfill samples; in turn, these samples have provided new insights into transducer design.

## Inspecting diverse 200mm and 300mm wafers

As of mid-2013, 300mm wafers are used in producing chips for Silicon on Insulator (SOI), Chip-on-Wafer, and Backside Illumination (BSI), the latter for camera applications. There are numerous applications for 200mm wafers. The most exciting may be MEMS applications, many of which use the 200mm diameter. The versatile nature of MEMS devices is evident in their recent use in medical sensing applications, including DNA sequencers.

As die sizes and feature sizes shrink, the critical dimensions of the structural defects such as cracks and bubbles also shrink. For 200mm and 300mm wafers today, acoustic micro imaging tools need two chief capabilities: high spatial resolution in the acoustic data collection process, and high throughput rate to image large numbers of high-population wafers. (In roughly four years, when 450mm wafers come on line, these capabilities will be even more important.)

Figure 2. Sonoscan's AW system can image 200mm and 300mm wafers and find defects down to 5 microns in size

To meet this challenge, Sonoscan has developed a multi-diameter automated wafer inspection system having multiple ultrasonic transducers and multiple stages. The AW system, shown in Figure 2, handles both 200mm and 300mm wafers. A single machine can have stages for both 200mm and 300mm wafers, and can image two wafers simultaneously. The system has a library of recipes for the various wafer types it may be required to image. It can operate as a stand-alone unit, or can be controlled by the host computer through its SECS/GEM interface.

Two wafers are scanned simultaneously on the system's two stages. A robotic arm unloads the wafers from one or more loadports containing FOUPs or other carriers. During the scanning process, the robotic arm performs other pre- and post-scan functions on individual wafers. These functions are designed to achieve maximum overall throughput.

The accelerometers, pressure sensors and other sensors made with MEMS technology typically have an internal cavity as well as a bondline around the cavity to ensure its hermeticity. The key interest is in the bondline, which may contain voids or channels that could leak and destroy the cavity's hermeticity. Even though the bondline on some newer MEMS designs is as thin as 6 microns, discontinuities and interruptions in the bondline are still imaged.

Figure 3 is the acoustic image of a portion of a bonded MEMS wafer. The dark regions are the bondline surrounding and sealing the cavity.

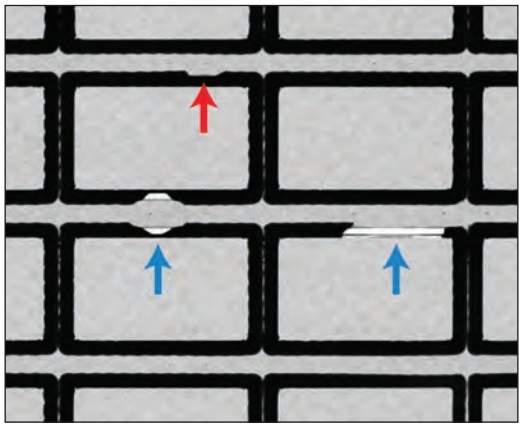


Figure 3. Acoustic image of a small area of a MEMS wafer. Blue arrows indicate separations of the bondline from the substrate; the red arrow points out thinning of the bondline

The blue arrows indicate areas where the seal is not bonded to one of its substrates - a condition that destroys the integrity of the cavity. The red arrows indicates an area where the bondline has been thinned laterally. There is no breach, but the bondline may be expected to be thinner and more vulnerable to stresses at this point.

Two new SEMI standards make it easier to evaluate the hermeticity of a MEMS bondline. SEMI MS8-0309 ("Guide to Evaluating Hermeticity of MEMS Packages") provides guidelines for evaluating bondline integrity with acoustic micro imaging. SEMI MS10-0912 ("Test Method to Measure Fluid Permeation Through MEMS Packaging Materials") describes how to measure the permeability of various bondline materials, and how to measure acoustically the thickness of a bondline to determine its long-term reliability.

Single wafers that will be used in SOI, BSI and other applications are sometimes imaged before bonding in order to spot surface cracks and subsurface damage. The ultrasound pulsed by the systems sends back return echoes from material interfaces. The strongest echoes are returned by the interface between a solid (silicon) and the air in a gap (meaning a crack, non-bond, void, bubble, etc.), even when the gap is as thin as 200Å. In a single polished wafer without metallization, such defects and anomalies are typically the only material interfaces within the bulk of the silicon.

Figure 4. Acoustic image of one portion of a direct bonded wafer pair shows size variation in the voids between the wafers

The defects most frequently imaged in wafers bonded for SOI and BSI applications are bubble-like voids, (Figure 4) contaminants or particles between the two wafers. A particle causes local upward curvature of one wafer; both bubbles and particles can cause the silicon above the defect to collapse during wafer thinning.

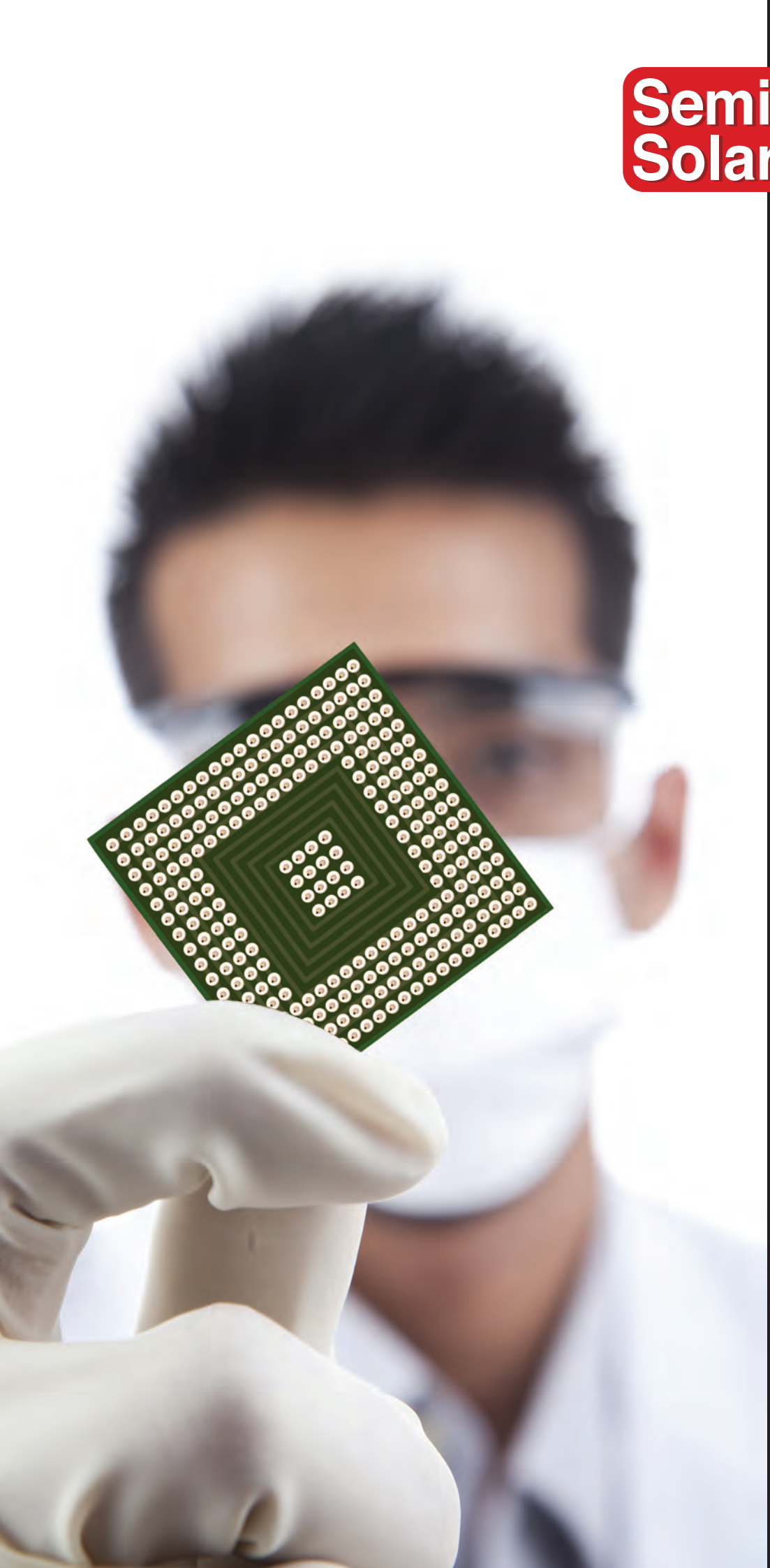
The contact bonding of these wafer pairs can also be evaluated earlier, after bonding but before annealing. Because the AW system uses a non-immersion system to couple the transducer to the wafer, there is reduced danger of water ingression between the wafers; unannealed wafers can thus be imaged and, if the contact bonding is not acceptable, separated and reprocessed.

300mm wafers for 2.5 D devices (including chip-on-wafer assemblies with interposers) are widely imaged on the AW system, and present their own challenges. The typical chip on wafer arrangement consists of a flip chip connected by its solder bumps to an interposer, which is in turn is connected by larger solder ball to the substrate.

The two layers of underfill tend to attenuate ultrasound, meaning that a lower frequency transducer is in order. Lower frequency means lower resolution, but the deeper solder balls are larger than the solder bumps above, and respond well to a lower frequency.

When an AW system has finished scanning a wafer, the output takes two forms: the quantitative data enumerating the anomaly/defect locations, and an acoustic image of the whole wafer. The acoustic image may be referred to, but it can hardly be viewed in its entirety because it displays defects down to 5 microns in size in a wafer that may be 300,000 microns in diameter.

Engineers may look at a specific region of the image because (for example) there is a history of the tool touching this region and causing contamination. If the quantitative data for a wafer type has previously proven to be reliable, that data alone is generally used as the guide for removal of defect die.



Semi Solar jobs.net

From the lab to the fab and to boardrooms all around the globe – one recruitment portal can fill your vacancy today

Reaches professionals from the silicon semiconductor, compound semiconductor and solar industries

Over 100,000 qualified professionals globally will see your vacancy

If you are recruiting and need a professional with the right experience to fit into your company, contact

**semisolarjobs.net**

# 4th CS International Conference
# Keynote Speakers Announced!

## 7 themes and 30 inspiring presentations*

**Gain a comprehensive overview of the entire compound semiconductor industry at the leading international conference.**

The 4th CS International conference will be held at the Sheraton Frankfurt Airport Hotel, Germany over two days on Tuesday 18th & Wednesday 19th March 2014.

Delegates will have the unique opportunity to network with the world's top executives in compound semiconductor technology. Hear about the breakthroughs in device technology; insights into the current status and the evolution of compound semiconductor devices; and details of advances in tools and processes which could help boost fab yields and throughputs.

This event is held once a year and brings together the best in class of the compound semiconductor industry, book your place before the 30th November 2013 and take advantage of our early bird discounted rate.

Chaired by: **Dr Andrew Nelson, IQE**

### 1. Front Ends for Mobile Devices

Handset front-ends are becoming more complex, due to an ever-increasing number of bands used for mobile communication. Will this trend play into the hands of GaAs chipmakers? Or is silicon CMOS technology going to grab market share?

**Keynote presentation: Jeremy Hendy**
Envelope Tracking - transforming the performance of CMOS and GaAs PAs

### 2. Wide Bandgap RF Devices

GaN and SiC have a great set of attributes that make them very promising materials for producing RF devices. But are they now fulfilling their potential and netting substantial sales?

**Keynote Presentation: Andrew Barnes**
Overview of GaN reliability improvement activities at the European Space Agency

### 3. LEDs

LEDs are the dominant source for backlighting screens of all size. So, to penetrate new markets and grow revenues, can chipmakers now trim the cost-per-lumen of the LED or equip the device with additional features?

**Keynote Presentation: Young Soo Park**
Slashing LED costs with 200 mm Silicon substrates

* All speakers and presentations are subject to change.

## 4. Solar

Triple-junction solar cell efficiencies are increasing steadily. Will this help to spur rapid growth in the concentrating photovoltaic sector, or will it be more valued by those requiring a power source for satellites?

**Keynote Presentation: Vijit Sabnis**
Setting a new benchmark for space solar cell performance

## 5. Laser and PICs

Rocketing levels of internet traffic are putting greater and greater strain on optical networks and data centres. Can this be addressed by advancing the performance of conventional lasers, or does the market need to turn to greater use of PICs?

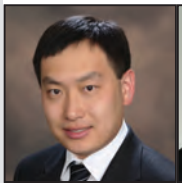
**Keynote Presentation: Michael Lebby**
OEICs for 100G and beyond datacentre opportunity using indium phosphide

## 6. Power Electronics

Silicon has dominated the power electronic market, wide bandgap semiconductors will soon replace this material. What's the primary role for SiC, and where will GaN feature?

**Keynote Presentation: Ming Su (Ford - Right)**
Can GaN or SiC make an impact in electric vehicles?

**Keynote Presentation: Mike Briere (International Rectifier - far right)**
Revolutionary performance and commercialization of GaN-on-Si based power devices



## 7. Integration of CMOS and III-Vs

Silicon is running out of steam, and the future is widely tipped to be high-mobility channels made from germanium and III-Vs. But how will these materials be introduced in the world's leading silicon foundries?

**Keynote Presentation: Dr Jean Fompeyrine**
Wafer bonding for III-V and Germanium CMOS

# Book your place NOW

Please visit **www.cs-international.net** for further information

Platinum Sponsors

Gold Sponsors

Delegate Bag Sponsor

Lanyard Sponsor

Portfolio Sponsor

**CS INTERNATIONAL CONFERENCE**

Connecting the leading compound semiconductor industry insiders

# Testing modern power semiconductor devices requires modern curve tracers

Researchers are looking to new semiconductor materials for enhanced performance. To quantify the performance advantages, devices must be thoroughly characterized. The traditional curve tracer has significant limitations when it comes to testing modern power semiconductor devices. The Source Measure Unit (SMU) offers a more capable test solution; David Wyban, Applications Engineer at Keithley Instruments tells us why.

CURVE TRACERS have been widely used in the electronics and semiconductor industries since the late 1950s, originally for characterizing vacuum tubes, later for characterizing transistors. A curve tracer incorporates power supplies for stimulating the device under test, a scope-like display for visualizing the collected data, a knob for real-time adjustment of the peak voltage across the device, and a test fixture for making connections to packaged devices both safely and easily. A curve tracer is relatively simple in design (Figure 1). It has two power supplies for stimulating the device under test (DUT). A step generator stimulates the device's control terminal with either DC current or DC voltage; the collector supply stimulates the device's channel with DC voltage. Two amplifiers monitor the voltage across and the current through the device and put a charge on the vertical and horizontal deflection plates to move the electron beam on screen and thus display different readings. Two 10-bit ADCs read the voltage from the amplifiers and convert them into a digital reading.


Curve tracers allow rapid characterization of two- and three-terminal semiconductor devices like diodes, BJTs, MOSFET, IGBTs, etc. They can be used to create characteristic current-voltage (I-V) curves on these devices using high current and high voltage. Once the curves have been traced, the built-in on-screen cursors allow extracting device parameters.

Curve tracers allow extracting parameters ranging from the reverse breakdown voltage on a diode to the family of curves on a MOSFET to the DC current gain on a BJT. Although some form of parametric analysis is required at every stage of the semiconductor device design, development, and fabrication sequence, traditional curve tracers are primarily used for device-level characterization in device development, failure analysis and for incoming inspection.

Unfortunately for power IC manufacturers, the rate of technology improvements derived from silicon-based devices is continuously decreasing. In order to meet today's higher efficiency goals, researchers are increasingly looking to new semiconductor materials, including gallium nitride (GaN) and silicon carbide (SiC), wide bandgap materials with several performance advantages over traditional silicon. The use of these materials has allowed designing devices with lower leakage currents (for better switching performance), lower ON resistances (which increases energy efficiency by reducing the power consumed by the device and delivering more to the load), higher power density (so they can deliver more power using less physical space), and finally, higher safe operating temperatures (which reduces the end product's cooling requirements).

In order to quantify the performance advantages these new designs offer, devices must be thoroughly characterized, a task that was traditionally performed with a curve tracer. Today, however, that has some problems, not the least of which is that production of curve tracers ceased in 2007. This has left test engineers hanging on to their instruments and struggling to keep them operational for as long as possible. However, the still bigger problem is that the traditional curve tracer has several significant limitations when it comes to testing modern power semiconductor devices. Fortunately, the Source Measure Unit (SMU) offers a more capable test solution. SMUs combine the source capabilities of a precision power supply with the measurement capabilities of a high accuracy digital multimeter (DMM) to create a single instrument that can both source and measure. SMUs offer all the features required for testing today's semiconductor devices, including power, dynamic range, accuracy and flexibility.

## SMUs and power

Modern semiconductor devices are capable of handling extremely high power levels and characterizing these devices demands test equipment capable of delivering those same high levels. Testing them in the ON-state requires instruments that can deliver power at very high currents; testing devices in the OFF-state requires instruments that can deliver power at very high voltages. A traditional curve tracer has two separate supplies for testing at these high levels of current and voltage. Today, there are SMUs capable of reaching these high levels as well.

Testing devices in the ON-state requires delivering a lot of current to the device. Figure 2 compares the power envelope of one traditional curve tracer's high current supply with that of a pair of high current SMU instruments wired together in parallel. Together, the pair of SMUs covers most of the power envelope of the curve tracer. The curve tracer's high current supply can put as much as 30V across the device at 0A, but this maximum voltage decreases as current increases. The curve tracer can output up to 400A, but it can only do this if there is 0V across the device. When a voltage is put across the device, the maximum current output is reduced. This phenomena is known as the load-line effect, which is caused by resistance in the output of the supply creating a voltage drop as current flows out of the supply.

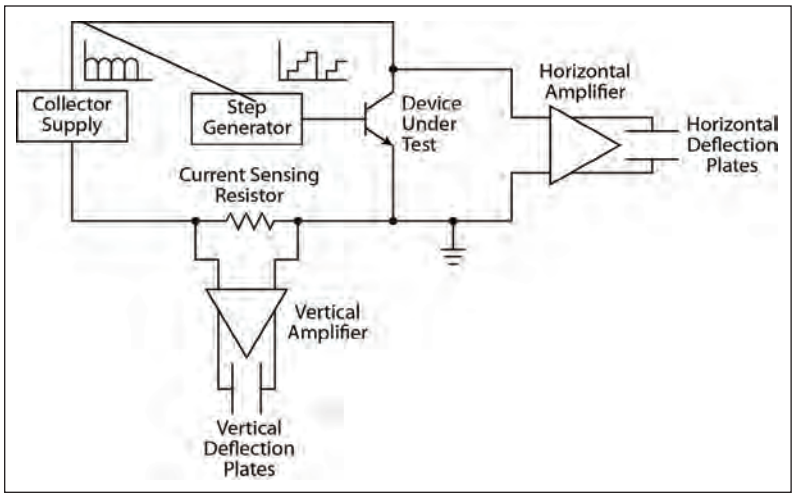



Figure 1. Traditional curve tracer block diagram

This resistance has been put into the output of the curve tracer's supply intentionally as a way to sense how much current is flowing. The effects of this resistor can be seen in the data collected by the curve tracer in the characteristic I-V curves of a transistor (Figure 3). Note how as current increases in each curve, the maximum voltage reached at that end of the curve decreases. Even

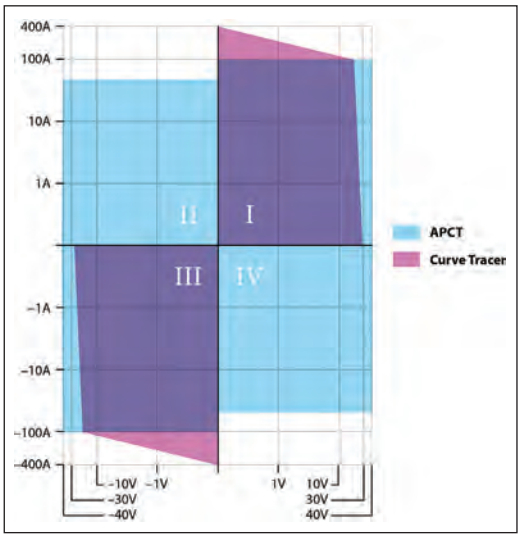
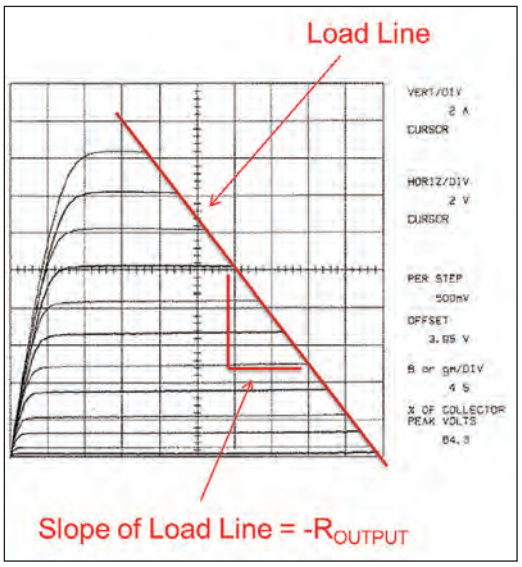



Figure 2. Power envelope of a traditional curve tracer's high current supply vs. that of a high current SMU

Figure 3. Load-line effect




though the curve tracer sweeps up to the same programmed peak value in every curve, the maximum voltage that actually reaches the device is different. If one were to draw a line across the ends of these curves, the line would be straight. This represents the load-line. When the slope of this line is measured, it is equal to the negative of the resistance in the output.

In contrast with the curve tracer, a pair of high current SMUs wired together in parallel can output up to 40V at up to 100A. Unlike the curve tracer, they do not experience the load-line effect because they use an active feedback loop to monitor their output rather than a series resistor. This loop only pulls back the voltage when it senses the programmed current limit has been reached. This allows all curves to reach the same peak voltage despite the increasing current. That allows them to output their maximum current all the way up to their maximum voltage, thereby providing more coverage in the power envelope. It's also worth noting that the power envelope of the SMU extends into quadrants II and IV, also known as the sink quadrants.

In these quadrants, power from the device is transferred into the SMU and the SMU acts as an electronic load. This expands the use of SMUs to testing additional devices like DC-DC converters and solar cells. Curve tracers have long been used to perform forward transconductance ($g_{fs}$) tests (Figure 4). SMUs' lack of load-line effect is invaluable for this test, in which the drain to source voltage ($V_{DS}$) must remain higher than a minimum level throughout the test to get valid results. In this test, the gate voltage is swept, causing the current through the drain to increase. As this current increases, the voltage output from the curve tracer will start to drop due to the load-line effect. If the peak voltage was not set high enough, the drain to source voltage will drop below the minimum $V_{DS}$ level required for valid results.

Let's consider the difference the choice of instrument will make for a test in which $g_{fs}$ has been specified at a $V_{DS}$ of 10V and an $I_{DS}$ of 30A. If the resistance in the output of the curve tracer is 75mΩ, then at 30A, we can expect a voltage drop within the supply of 2.25V. This means the peak voltage knob of the supply must be set to 12.25 V in order to get 10V at the DUT at 30A. In reality though, extracting $g_{fs}$ requires sweeping past 30A of current in order to place the function line cursor tangent with the trace, so the peak voltage knob actually needs to be set even higher.

In contrast, when using an SMU, there's no load-line effect to worry about, which simplifies the testing procedure. The $V_{DS}$ can simple be set at exactly the specified voltage and that voltage will stay the same even as the drain current increases. Programmable current limits are one of the advantages SMUs have over the curve tracer that make them a better fit for testing modern power semiconductor devices. On an SMU, when voltage is swept across the device, the current can be limited to avoid causing device damage. On the curve tracer, the only current-limiting device is the series output sense resistor, which helps protect only the power supply, not the device.

SMUs have another major advantage over traditional curve tracers: their ability to source current or voltage, which is particularly important when making ON-state resistance ($R_{ds(on)}$) measurements. Manufacturers are always trying to reduce the ON-state resistance of devices because less resistance means less power consumed by the device, increasing the efficiency of power delivery by the device.

Today, devices with an $R_{ds(on)}$ of less than 10mΩ are common. When testing devices with resistances this low, a very minor change in voltage can cause a major change in current.

For example, for a device with an $R_{ds(on)}$ of 2mΩ, a 10mV change in voltage will create a 5A current change in current. Considering that the curve tracer's high current supply only has a programming resolution of 30mV, if one ignores the load-line effect, that would mean a 15A change in current for each click of the knob!

Although curve tracers can only source voltage, SMUs have the ability to source both voltage and current. Sourcing current allows SMUs to make extremely accurate $R_{ds(on)}$ measurements

Consider another example, of a power MOSFET with an $R_{ds(on)}$ of 1.5mΩ specified at 30A $I_{DS}$. A calculation based on Ohm's Law (V = I×R) reveals that only 45mV of voltage is required to reach 30A on this device (V = 30A ×1.5mΩ = 45mV). Given that a curve tracer typically only has a programming resolution of 30mV, sourcing 45mV would be pretty tough. To be fair, sourcing 45mV accurately, particularly at these high current levels, is difficult for any instrument; in contrast, measuring 45mV is relatively easy, so it's generally highly preferable to source current and measure voltage when measuring low resistances.

Although curve tracers can only source voltage, SMUs have the ability to source both voltage and current. Sourcing current allows SMUs to make extremely accurate $R_{ds(on)}$ measurements. SMUs like the Keithley Model 2651A can source current with resolution as small as 2pA and its high sensitivity voltmeter can measure with resolution as small as 1μV. This allows for highly accurate resistance measurements, even at the sub-milliohm level.

ON-state testing requires sourcing high current; OFF-state testing requires sourcing extremely high voltage. Today's devices are commonly capable of withstanding >1200V and IGBT devices capable of 2500V are readily available. The traditional curve tracer is capable of sourcing up to 3000V, so it's still suitable for breakdown testing of modern devices. SMUs like the Keithley Model 2657A High Voltage System SourceMeter instrument are also capable of sourcing 3000V, but unlike a curve tracer, it can deliver a large amount of current at high voltage. At 3000V, the amount of current that the curve tracer can deliver is miniscule. The Model 2657A can deliver up to 20mA at 3000V or up to 120mA at 1500V, expanding its capability. Like the high current SMU, the high voltage SMU is capable of operating in quadrants II and IV, which not only expands its capabilities but increases test system safety. Devices in the OFF state have very high impedance and therefore very low leakage.

These devices also have some capacitance as well. In OFF-state testing, this capacitance gets charged to a very high voltage, but due to the very low leakage of the device, this charge remains on the device for a significant amount of time after the test voltage is removed. The SMU's ability to sink current increases test system safety because it allows the SMU to discharge the device at the end of the test very quickly, preventing shocking an operator who comes in contact with the device too soon after testing.

## SMUs and dynamic range

Characterizing a device accurately demands test equipment capable of measuring both large and small currents precisely. For example, Figure 5 shows the characteristic curve for a typical diode.

In the regions between the reverse breakdown voltage ($V_{br}$) and the forward voltage ($V_f$), currents are very small. However, in the regions below $V_{br}$ and above $V_f$, the currents are several orders of magnitude larger, especially in the forward region. An instrument with an extremely wide dynamic range is essential to characterize this device accurately, and SMUs offer some of the widest dynamic ranges in the T&M industry.

Forward or ON-state testing of a device is usually performed with a high current supply. In the forward region of a diode (below the forward voltage), the level of current is very small. The device has not turned on yet and so the current flowing through it may be just nano-amps or less. Above the forward voltage, the current quickly gets much larger, reaching several amps or even tens of amps. For an SMU, measuring over this range of currents is no problem. For example, the Model 2651A offers a measurement capability that stretches from 50 amps (or 100 amps if two units are connected in parallel) all the way down to 1pA or 14 decades of current. In sharp contrast, the high current supply of a curve tracer only has about 4 decades of current measurement capability and can only measure with far less resolution.

Reverse or OFF-state testing is usually performed with a high voltage supply. In the reverse region of the diode, at voltages smaller than the breakdown voltage, currents are very small. At and above the breakdown voltage, they rapidly become several orders of magnitude larger. In today's devices, OFF-state leakage currents can be down in the pico-amp range, but the generally accepted breakdown current is 250 micro-amps.

Accurate characterization requires an instrument capable of measuring the extremely small currents found before the breakdown with sufficient dynamic range to measure the larger currents that occur at breakdown. With the ability to measure currents as low as 1fA and as high as 120mA, the

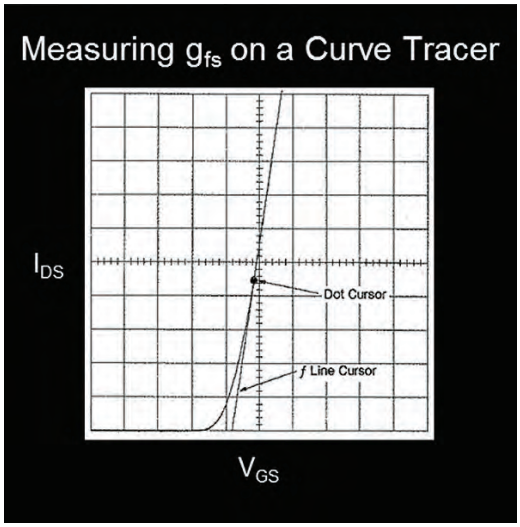



Figure 4. Curve tracer $g_{fs}$ measurement results

Model 2657A's measurement capability spans 14 decades, making it easy to measure off-state currents. In contrast, the curve tracer offers far less resolution. With this limited low current measurement capability, the curve tracer is really only suitable for finding the breakdown voltage and is unable to measure picoamp-level leakage on today's devices.

## SMUs and flexibility

SMUs offers the high flexibility needed to perform tests that would be difficult or even impossible with a curve tracer. Gate leakage measurements are difficult to do on a curve tracer but very easy to perform with SMUs. Measuring gate leakage requires sourcing a voltage on the gate terminal with the drain and source terminals grounded, then measuring the current into the gate. A curve tracer's step supply (to which the gate terminal is traditionally connected) does not support measurements, so the connections to the device must be changed so that the gate is connected to the curve tracer's collector/drain supply terminal and the drain and source terminals are connected to common.

However, this doesn't work very well because measuring gate current requires measuring low currents. Accessing the lowest current ranges on the curve tracer requires using the high voltage supply, but the highest resolution setting on the high voltage supply is 50V/division. Given that most gate leakages are measured at 20V or less, this isn't very practical. Sourcing only 20V or less is easy to do if the high current supply is used, but the lowest current measure range is 500mA/division, which is much too large to measure any kind of leakage current. In contrast, with an SMU-based power device characterization system, the gate terminal is connected to an SMU so it can make measurements.

By putting today's lowest current SMU on the gate terminal, users can source the gate voltage precisely and measure the leakage current with resolution down to 100aA. Creating Gummel plots is another test where SMUs offer a clear advantage over traditional curve tracers. This test, performed on BJTs, requires sweeping the voltage and measuring the current on the base and collector terminals in unison. This test absolutely cannot be performed using a curve tracer, but thanks to the flexible sweep configurations SMUs offer, this task is trivial.

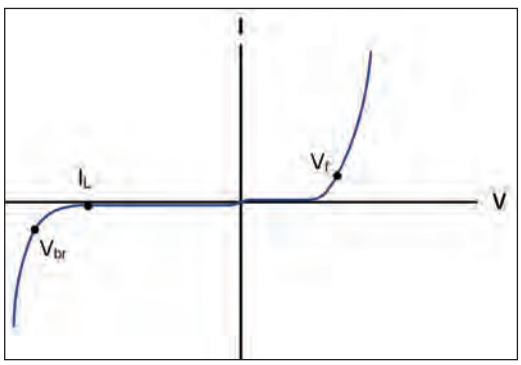



Figure 5. Characteristic curve for a typical diode

## SMUs and PCTs

As capable as SMUs are and as many advantages as they offer over traditional curve tracers, they are not the whole solution for testing advanced power semiconductor devices. Increasingly, engineers are turning to a new concept known as a parametric curve tracer or PCT, which combines the simplicity of a curve tracer with the high precision of a parametric analyzer. A PCT includes SMU instruments, cables, a test fixture, software, and test libraries to provide measurements at up to 3000 volts and up to 100 amps. As new test needs evolve, a PCT can be upgraded easily in the field, providing a solution that is both scalable and reconfigurable.

Parametric curve tracers offer two modes of operation: trace test mode and parametric test mode. Trace test mode presents an interface similar to the controls and display found on a traditional curve tracer. It allows for rapid generation of device characteristics and for interactive operation based on viewing the results in the graph. It incorporates knowledge of many device types and tests, which speeds and simplifies test setup. An on-screen slider provides real-time control and acts like the knob found on the traditional curve tracer. Trace test mode is very handy for quickly testing whether a device is good or bad or finding its boundaries. This mode is often used during device development or failure analysis.

Parametric test mode offers access to all of the advanced capabilities of the SMUs within the PCT, allowing users to specify exactly how a test is to be performed. Built-in test libraries provide support for all of the most common device and test types; a vector math formulator supports accurate parameter extraction on these devices. Once configured, an entire suite of tests can run autonomously without operator intervention. This mode is often used in device qualification, process monitoring and datasheet generation applications.

## Conclusion

Device engineers have long considered the traditional curve tracer their go-to instrument for device characterization, but dwindling availability and new device challenges are making it an increasingly unworkable solution. Fortunately, SMU instruments have assumed many of the roles in the lab that the curve tracer once played. With the extended capabilities that parametric curve tracers add to those provided by SMU instruments, engineers can be assured their evolved characterization needs won't be left unaddressed.

# CORPORATE PARTNERS DIRECTORY

## Automation/Wafer Handling



## Furnaces



## Materials, Processes and Equipment



## Vacuum Equipment



## Fan Filter Units



## Liquid Nitrogen Piping



## MFCs



## Wafers



## Furnaces



## Material Processing



## Solder Rework



## Wet Benches

EVG®

invent
innovate
implement

www.EVGroup.com

# PHOTOLITHOGRAPHY FOR TSV AND 3D-IC

- Conformal Coating in Vertical Vias
- Exposure with Proximity Lithography
- In-Via Resist Development

EVG®150 Resist Processing System

Via processed on EVG® systems

**GET IN TOUCH** To Discuss Your Manufacturing Needs: **www.EVGroup.com**