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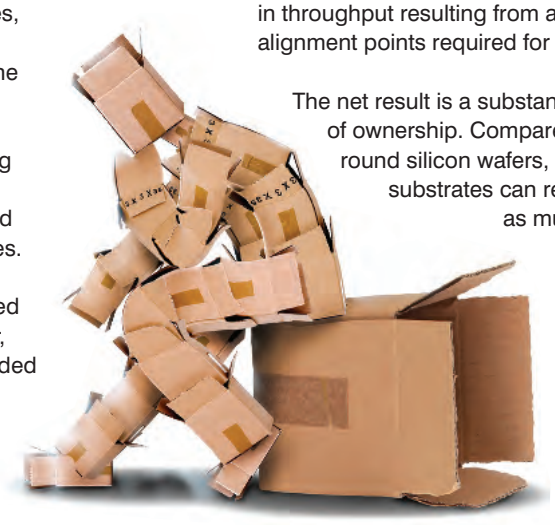
executiveview

by Rich Rogoff, Vice President and General Manager, Lithography Systems Group, Rudolph Technologies, Inc.

We must think **"outside of the box"** for new approaches in advanced packaging

AS SEMICONDUCTOR DEVICES have continued to shrink in size and grow in complexity, manufacturers have had to develop advanced packaging techniques to accommodate the rapidly increasing number and density of connections required to communicate with the outside world. Often these technologies have developed as adaptations of front-end methods. While there is certainly value to be found in using these well characterized processes, we must be careful not to carry along old baggage that may prove unnecessary in the new application.

For instance, while front-end manufacturing has historically been tied to round silicon wafers, this may not be the ideal shape and material for advanced packaging substrates. Embedded die, fan-out and interposer based packages can often be manufactured more conveniently and efficiently on larger, rectangular substrates made of glass, molded or organic panels. Our ability to think "outside of the box" for new approaches in advanced packaging will enable economy of scale efficiency gains and cost savings in the future.



Moving from round wafers to rectangular substrates in back-end advanced packaging saves corner space, delivering a roughly 10% improvement in surface utilization. In the case of lithography, the larger size of the substrate and the improved fit between the reticle and substrate can reduce the handling and processing overhead by a factor of five. These productivity improvements more than offset any potential reduction in throughput resulting from an increase in the number of alignment points required for these larger substrates.

The net result is a substantial reduction in lithography cost of ownership. Compared to a 1X stepper exposing round silicon wafers, processes based on rectangular substrates can reduce lithography cost per die by as much as 40%.

Clearly, there are many aspects of these new processes that must be addressed before they gain broad acceptance. However, if we as an industry are able to think outside of the box, we will see that the potential economic benefits of rectangular substrate processing can be significant.

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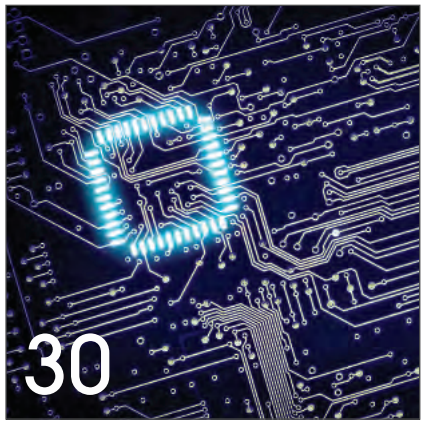
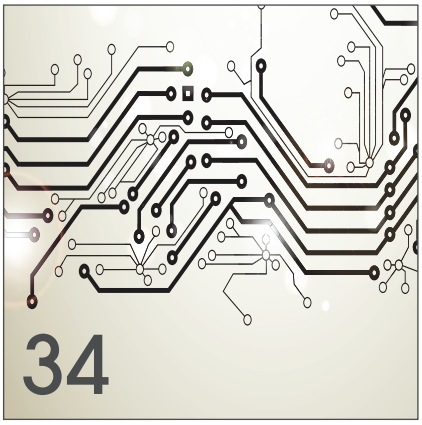
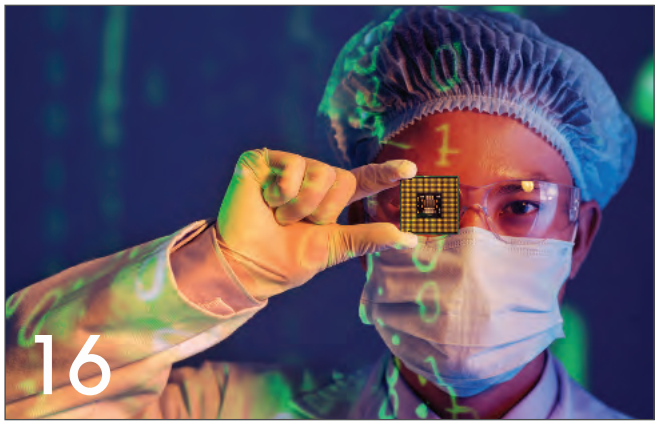
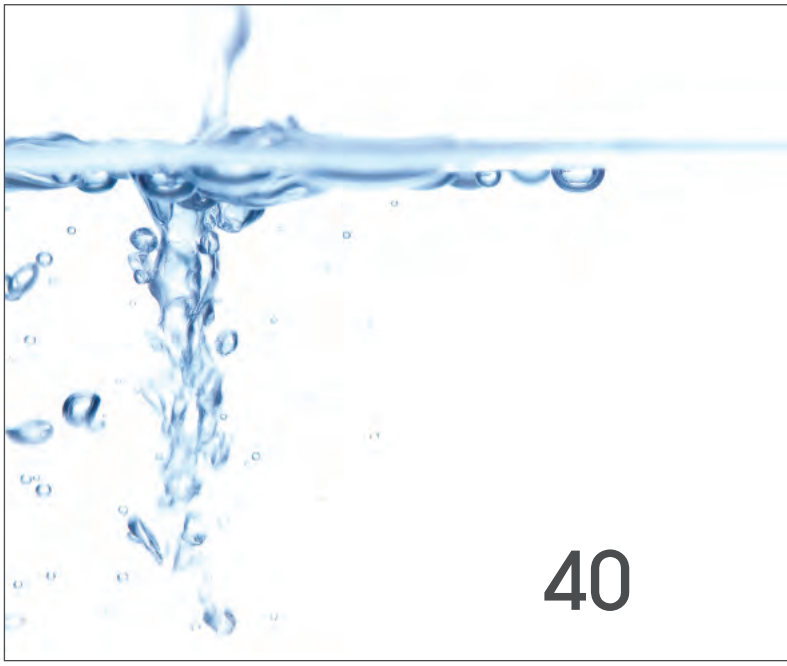
features









Synopsys, ST and Samsung to accelerate 28-nm FD-SOI adoption

SYNOPSYS has extended its collaboration with STMicroelectronics to include Samsung Electronics, enabling broader market adoption of ST's 28-nm FD-SOI technology for SoC design.

Synopsys says its Galaxy Design Platform is production-proven on multiple designs based on ST's 28-nm FD-SOI technology. This collaboration extends the Galaxy design flow to Samsung in support of its strategic agreement to offer dual sourcing of ST's 28-nm FD-SOI technology.

Developed over a multiyear collaboration with ST, the design flow enables concurrent area, power and timing optimisations to enable engineers to optimise their designs for the ST 28-nm FD-SOI process.

"The close collaboration between ST design teams and Synopsys led to advanced silicon-proven design enablement solutions that fully leverage the performance and power promise of FD-SOI technology and provide the foundation needed to meet tight time to market windows," says Philippe Magarshack, executive vice president, Design Enablement and Services, STMicroelectronics.

"Our close collaboration with Synopsys has already enabled many successful tapeouts with mutual customers using Synopsys' Galaxy Design Platform and Lynx Design System."

The Synopsys design flow for ST's 28-nm FD-SOI is compatible with the Lynx Design System, a full-chip design environment providing innovative automation and visualisation capabilities that enable higher designer productivity and faster design closure.

A technology plug-in using ST's 28-nm FD-SOI Process Design Kit (PDK), standard cells and memories, adapts the production-proven Galaxy Design Platform-based RTL-to-GDSII flow for 28-nm FD-SOI SoC designs, accelerating project setup and execution.

Lynx automation simplifies and accelerates many critical implementation and validation tasks, including back-bias management across the flow, special connection checks, In-Design physical verification for well connections and UPF supply set management for n-wells and p-wells.

Galaxy advanced design enablement features like the IC Compiler tool's concurrent clock and data optimization, layer-aware optimization, physical datapath and comprehensive support for hierarchical and low power design features can also be directly accessed by Lynx users for high-performance and low power CPU and GPU design.

"28-nm FD-SOI is an ideal solution for customers looking for extra performance and power efficiency at the 28-nm node without having to migrate to 20-nm," says Shawn Han, vice president of foundry marketing, Samsung Electronics.

"Our close collaboration with Synopsys and ST will enable designers to reduce risk, accelerate time-to-market, minimise power and maximise performance to expand 28-nm FD-SOI adoption."

Nordson MARCH unveils plasma tool for flexible substrates

NORDSON MARCH is introducing its new FlexVIA-Plus Plasma Treatment System that delivers single-stage plasma processing - including etchback and desmear - of up to 30 panels (panel size 500 x 813 mm/ 20 x 32 inch) per cycle.

This enables a rate of as much as 200 units per hour (UPH) for the manufacture of flexible electronic PCBs and substrates.

The FlexVIA-Plus System's advanced horizontal electrode design, with integrated rack, provides optimum material alignment for industry-leading plasma treatment uniformity. V

ersatile horizontal racks allow for processing of various flexible PCB sizes and make loading easy. The efficient design with its economical gas consumption and small footprint contributes to a low cost of ownership.

Specifically designed for the processing of flexible PCBs, the new FlexVIA-Plus Plasma System delivers patented, plasma technologies that provide excellent surface activation, etchback, and desmear process uniformity on both sides of the flex material.

The desmear and etchback technologies remove epoxies, polyimides, high Tg blends, mixed materials and other resins more effectively than traditional methods of etching and desmearing.

The descum capabilities effectively remove resist residue from inner layers and panels as well as residual solder mask bleed for better bonding and solderability. Temperature-controlled electrodes ensure consistent process repeatability.

"The new FlexVIA-Plus Plasma System performs similarly to our ProVIA system, but in a horizontal form-factor, which is ideal for processing flexible PCBs," says Jonathan Doan, director of marketing, Nordson MARCH. "This system meets the demands of today's high-throughput flexible circuit board manufacturing operations."

Samsung 32-layer 3D V-NAND flash first in mass production

SAMSUNG has begun mass producing what it says is the industry's first three-dimensional (3D) V-NAND Flash memory using 32 vertically stacked cell layers. This is the firm's second generation V-NAND offering.

The firm's 32-layer 3D V-NAND - or Vertical NAND - requires a higher level of design technology to stack the cell arrays than the previous 24-layer V-NAND, yet delivers much greater production efficiency. This is because Samsung can use essentially the same equipment it used for production of the first generation V-NAND.

In addition, Samsung has just launched a line-up of premium SSDs based on its 2nd generation V-NAND Flash memory with 128 gigabyte (GB), 256GB, 512GB and 1TB storage options. After introducing 3D V-NAND-based SSDs to data centres last year, Samsung is now extending its V-NAND SSD line-up to high-end PC applications, in expanding its market base.

"We increased the availability of our 3D V-NAND by introducing an extensive V-NAND SSD line-up that covers the PC market in addition to data centres,"

says Young-Hyun Jun, executive vice president, memory sales and marketing, Samsung Electronics. "Look for us to provide a consistent, timely supply of high-performance, high-density V-NAND SSDs as well as core V-NAND chips for IT customers globally, contributing to fast market adoption of 3D NAND technology."

The new 3D V-NAND-based SSDs have approximately twice the endurance for writing data and consume 20 percent less power, compared to planar (2D) MLC NAND-based drives. Later this year, Samsung will introduce additional premium 3D-based SSDs based on this 2nd generation V-NAND memory with even higher reliability and higher-density in satisfying a diversity of customer needs.

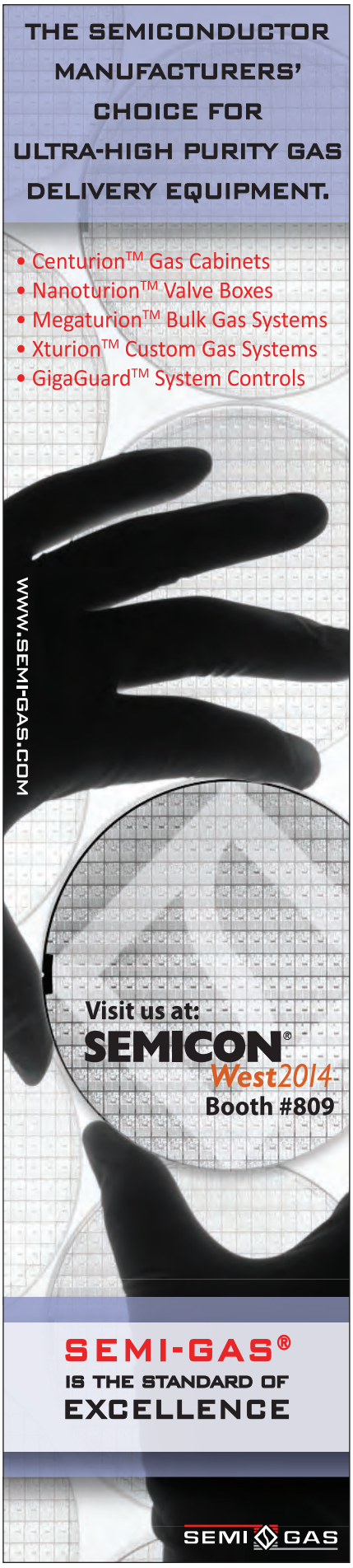
Equipment spending soars 22.5 percent in April 2014

NORTH AMERICA-BASED manufacturers of semiconductor equipment posted $1.44 billion in global orders in April 2014 and a book-to-bill ratio of 1.03, according to the April EMDS Book-to-Bill Report published by SEMI.

This was based on a three-month average. A book-to-bill of 1.03 means that $103 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in April 2014 was $1.44 billion. The bookings figure is 10.8 percent higher than the final March 2014 level of $1.30 billion, and is 22.5 percent higher than the April 2013 order level of $1.17 billion. The three-month average of worldwide billings in April 2014 was $1.40 billion. The billings figure is 14.1 percent higher than the final March 2014 level of $1.23 billion, and is 28.7 percent higher than the April 2013 billings level of $1.09 billion.

"Sales of semiconductor manufacturing equipment from North American producers continue to demonstrate strong sequential and year-over-year growth," says Denny McGuirk, president and CEO of SEMI. "The data through the first quarter reflects momentum in memory, foundry, and back-end spending."



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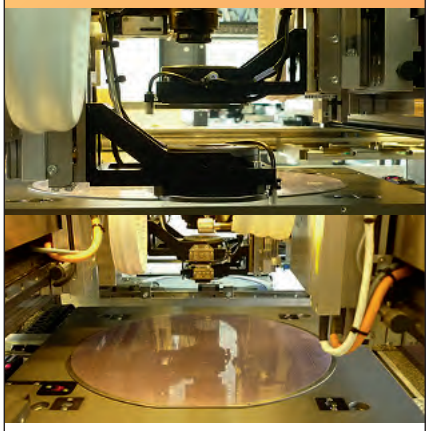

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MORE THAN PRECISION

Soitec and Simgui to provide China with 200mm SOI wafers

SOITEC and Shanghai Simgui Technology Co., Ltd. (Simgui), a Chinese materials company, have formed an international partnership.

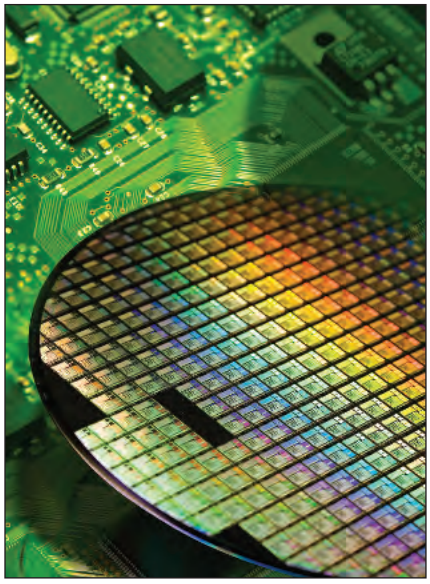
They will address both China's growing demand and limited worldwide production capacity for 200 mm silicon-on-insulator (SOI) wafers used in fabricating semiconductors for radio-frequency (RF) and power applications. In addition to giving Soitec its first wafer production capability in China, the agreement boosts the industrial manufacturing capacity of SOI wafers to meet increasing worldwide usage and represents the first step in establishing a SOI ecosystem in China.

The newly signed deal includes a licensing and technology transfer agreement under which Simgui will manufacture Soitec's 200 mm SOI wafers using Soitec's proprietary Smart Cut technology. Simgui will establish a high-volume SOI manufacturing line to directly supply the Chinese market.

In addition, Simgui will manufacture Soitec's 200 mm SOI wafers for the global market outside China, expanding Soitec's supply to customers worldwide. Beyond this initial cooperation, the two companies plan to expand their collaborative efforts in the future to take advantage of their synergies.

"We are very pleased to announce this partnership with Simgui which amplifies the ecosystem using Soitec's technology and reinforces our competitive offer," says Paul Boudre, COO of Soitec. "While paving the way for future cooperation between our two companies, it also reinforces Soitec's global leadership position in SOI and immediately bolsters our presence in the Chinese market."

Commenting on the announcement, Bernard Aspar, general manager of Soitec's Communication and Power Business Unit, says, "In addition to Soitec's SOI product volume for the RF market doubling in the last two years, the products themselves are becoming the preferred solutions for RF switches embedded in smart phones and tablets. This collaboration with Simgui



will allow us to respond to the fast-growing demand we are seeing from our customers."

"Considering that China takes over a 60 percent market share of the worldwide semiconductor market, to have a strategic collaboration with Soitec is very important to us," notes Xi Wang, Chairman of Shanghai Simgui Technology Co., Ltd. "This will enable us to grow our current SOI market share and address new opportunities as we help to develop China's SOI ecosystem." "The access to Soitec technology is an accelerator for Simgui to become a key player in thin SOI manufacturing," adds Feng Zhang, General Manager of Simgui. "On the other hand, this partnership will complete Simgui's capabilities such as Simbond, which will further strengthen both parties' SOI competitiveness."

This strategic partnership enables both Soitec and Simgui to strengthen their positions in the high-growth markets for RF and power semiconductors. While applications for power ICs include automotive electronics, lighting and power supplies, RF semiconductors are key drivers of 4G smart phones. China is the world's largest smart phone market. Soitec's RF-SOI products are already used in manufacturing by most of the leading RF foundries and have been adopted as the preferred substrates for 4G and LTE mobile computing and communication applications.

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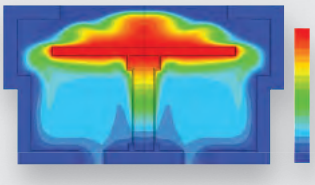

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AMAT Introduces big materials change

APPLIED MATERIALS, INC. has announced the Applied Endura Volta CVD Cobalt system, a tool capable of encapsulating copper interconnects in logic chips beyond the 28nm node by depositing precise, thin cobalt films. The two enabling applications, a conformal cobalt liner and a selective cobalt capping layer, provide enclosure of the copper lines. The introduction of cobalt, as a metal encapsulation film, marks the most significant materials change to the interconnect in over 15 years, the company says.

"The reliability and performance of the wiring that connects the billions of transistors in a chip is critical to achieve high yields for device manufacturers. As wire dimensions shrink to keep pace with Moore's Law, interconnects are more prone to killer voids and electromigration failures," said Dr. Randhir Thakur, executive vice president and general manager of the Silicon Systems Group at Applied Materials. "The Endura Volta system builds on Applied's precision materials engineering leadership by delivering CVD- based cobalt liner and selective cobalt capping films that overcome these yield-limiting issues to enable our customers to scale copper interconnects to beyond the 28nm node."

The Endura Volta CVD system, with two new process steps, represents technology extension for copper interconnects beyond 28nm. The first step involves the deposition of a thin, conformal CVD cobalt liner to increase the gap fill window of copper in narrow interconnects. This process improves the performance and yield of the device by integrating the pre-clean, PVD barrier, CVD cobalt liner and copper seed processes under ultra-high vacuum on the same platform. The second step, a new "selective" CVD cobalt capping step, is deposited after CMP* to encapsulate the copper lines for enhanced reliability performance.

Complete envelopment of copper lines with cobalt creates an engineered interface that demonstrates over 80x improvement in device reliability the company says.

Breakthrough defect reductions in EUV mask blanks

SEMATECH has announced that researchers have reached a significant milestone in reducing tool-generated defects from the multi-layer deposition of mask blanks used for extreme ultraviolet (EUV) lithography, pushing the technology another step toward readiness for high-volume manufacturing (HVM).

Following a four-year effort to improve deposition tool hardware, process parameters and substrate cleaning techniques, technologists at SEMATECH have, for the first time, deposited EUV multilayers with zero defects per mask at 100 nm sensitivity (SiO2 equivalent). Eliminating these large "killer" defects is essential for the use of EUV in early product development. These results were achieved on a 40 bi-layer Si/Mo film stack and measured over the entire mask blank quality area of 132×132 mm^2.

In addition, by subtracting out, incoming substrate defects, SEMATECH has demonstrated that the multilayer deposition process itself can achieve zero defects down to 50 nm sensitivity. Coupled with novel improvements to the mask substrate cleaning process to remove incoming defects, this represents the capability to both extend EUV to future nodes by eliminating smaller "killer" defects, and as a step to reducing smaller defects (which can be mitigated) to a level where improved yield and mask cost make EUV a more cost-effective HVM technology. Defects are generally created by the deposition process or formed by decoration of substrate defects during the multilayer deposition process. These types of defects have prevented the quality of mask blanks from keeping pace with roadmap requirements for the production of pilot line and high-volume manufacturing EUV reticles. Reducing defects in the EUV mask blank multilayer deposition system is one of the most critical technology gaps the industry needs to address to enable cost-effective insertion of this technology at the 16 nm half-pitch.

"A low defect density reflective mask blank is considered to be one of the top two critical technology gaps for the commercialization of EUV," said Frank Goodwin, manager of SEMATECH's Advanced Mask Development program. "Through sophisticated defect analysis capabilities and processes, the goal of our work is to enable model-based prediction and data-driven analysis of defect performance for process improvement and component learning. We then use these models to feed into the new deposition tool design."

SEMATECH's Advanced Mask Blank Development program is located at the SUNY College of Nanoscale Science and Engineering (CNSE) in Albany, New York to develop defect-free EUV blanks.

Brewer Science commercialises megasonic developer for MEMS

BREWER SCIENCE has announced the first commercial placement of a Cee 300MXD megasonic developer. This innovative developer was commissioned by MicroChem Corp.

The Brewer Science Cee 300MXD megasonic developer applies uniform acoustic energy to spinning substrates to gently dissolve and remove films and residues without damaging fragile device structures.

This precision handling results in stable dimensional control of vertical profiles uniformly across the wafer surface, enabling fabrication of high-aspect-ratio structures for the MEMS, display, compound semiconductor, and advanced packaging markets. Applications include radio-frequency (RF) power, MEMS, sensors, and acoustic wave devices used for wireless communication.

"MicroChem is very pleased to team with Brewer Science on what we believe could be an enabling technology for the future," said Michael Stan, Applications Engineering Manager for MicroChem Corp. "As the MEMS industry and integrated packaging technology continue to demand higher-aspect-ratio structures for TSV and RDL layers, enhanced development techniques will likely become mainstream. The cost-effective approach being pioneered by Brewer Science gives a supplier such as MicroChem Corp. the advantage of being able to rapidly prototype formulations and processes to meet these demands," he added.

"The Cee 300MXD developer features state-of-the-art technology that creates a viable pathway for our customers to decrease process cycle times, reduce cost of ownership, and accelerate time to market," said Justin Furse, Brewer Science Equipment Technology Strategist.

The Cee 300MXD megasonic developer gives customers an ideal bridge from the lab to production by allowing them to avoid significant capital investment.

Our semi-automated equipment delivers quality and precision comparable to automatic multimillion-dollar tools and is suitable for low-volume prototyping with a seamless transition to high-volume manufacturing.

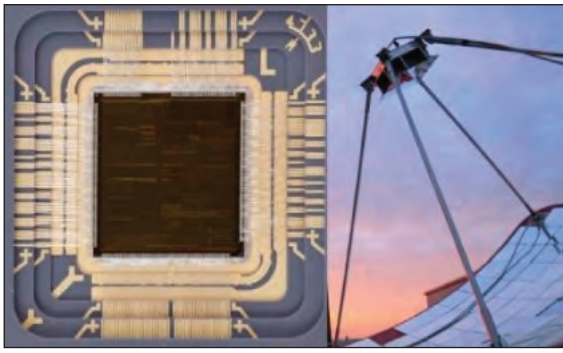
AIT unveils advanced 20 micron die-attach film

AI TECHNOLOGY (AIT) says it has solved one of the technically more challenging problems in wafer level semiconductor packaging.

The company says it can achieve conductive die-attach film adhesive (DAF) of 20 microns (μm) thickness. While die-attach film adhesive (DAF) at the wafer level is becoming more prevalent in die-attach for memory modules in precision bonding and thin packages, thermally conductive and electrically conductive die-attach film is more limiting because of the challenging handling and performance issues for the thinner conductive DAF.

The picture shows 20μm thick conductive DAF used for high power devices and concentrated solar die-attach applications. AIT's conductive DAF is built on the same self-supporting die-attach film (DAF) adhesive technology that the company pioneered in the 1990's. AIT is now able to produce ESP8660-HK in 20μm thickness for power devices from microprocessors to concentrated solar die-attach modules. This new thickness marks an improvement over AIT's 50μm thick ESP8660-HF which was first produced in 2005.

ESP866-HF can be produced in wafer-shape die-cut format and pre-laminated on dicing tape (DDAF) format up to widths of 450mm and lengths of 100 metres in AIT's clean room manufacturing environment housed in the company 's 16 acres facilities in Princeton Junction, New Jersey. Not only is ESP8660-HK available in 20μm thickness, it is also developed for high glass transition requirements to facilitate faster wire-bonding at temperatures as high as 250ºC. ESP8660-HK is also molecularly



engineered to reduce stress and ultimately improve the reliability of multi-chip module (MCM) and system in package (SIP) devices. In addition to achieving one of the lowest thermal resistances with thermal conductivity of over 8 W m/ºK, ESP8660-HK maintains its bond strength after 85%RH/85ºC and demonstrates reliability test results after thermal cycling an d shock that are not common even for traditional paste die-attach adhesives.

Semiconductor market for vehicles to quadruple

THE GLOBAL SEMICONDUCTOR MARKET for active-control systems in the autonomous vehicle will grow nearly fivefold in just seven short years, according to a new report from IHS Technology. This expansion will be driven by an increasing shift from cars simply providing alerts in hazardous situations to direct intervention in order to avoid accidents.

WORLDWIDE REVENUE for active-control systems in vehicles is set to reach $883.9 million in 2020, up from $187.3 million last year. The increase of nearly $700 million from 2013 to 2020 equates to a compound annual growth rate of 25 percent for the seven-year period. This year alone, revenue is projected to climb a robust 31 percent to $246.1 million, as shown in the attached table.

Active-control mechanisms can be distinguished from their passive-warning counterparts - older systems that have been around much longer - by the degree of driver involvement in both systems.

“Passive mechanisms in the autonomous vehicle help identify potentially hazardous conditions, but the driver is still fully responsible for avoiding an incident,” says Akhilesh Kona, analyst for automotive semiconductors. “In active-control systems, however, the mechanism takes over if the driver does not react to warnings so that the vehicle can avoid an accident or minimise the impact of a collision.”

An example of a passive mechanism is lane-departure warning, which monitors the lane markings on a roadway and alerts a driver when a car starts veering out of its lane if the turn signals are not being used. In this case, the driver must still take control of the car and steer the vehicle back to its proper lane.

But in an active-control mechanism such as lane-keep assist, the car acts in more proactive fashion: if the driver does not respond after an initial warning from the car, the car itself typically takes action to keep the vehicle from drifting.

Another example of an active-control mechanism is automatic emergency braking (AEB), which uses forward-looking radar and video systems to detect the relative speeds of vehicles to determine if a collision is imminent. If a potential collision is detected, the vehicle applies full or partial braking power to stop the car or slows it down significantly in order to mitigate the severity of the collision.

“Overall, active-control systems are growing faster than passive-warning mechanisms. Compared to the phenomenal growth of the active-control semiconductor market, the chip market for passive-warning systems is projected to grow at a less furious pace from 2013 to 2020,” notes Luca DeAmbroggi, principal analyst for automotive semiconductors at IHS.

“The semiconductors used for active-control systems need to be compliant with stringent safety certifications, such as Automotive Safety Integrity Level (ASIL), or ISO 26262,” DeAmbroggi adds. “Since safety considerations are of paramount importance to active-control semiconductors throughout their life cycle, ASIL systems will require compliant chips that will typically cost more than the standard ASIL counterparts used in passive systems.”

ASIL-compliant microcomponents (MCU) will enjoy even faster growth than overall semiconductors for active-control systems, with ASIL revenue growing to $450 million in 2020 from $70 million in 2013. These findings are contained in the report, “ADAS Semiconductor Market Tracker H1-14,” from the Automotive & Transportation research area of IHS. Automotive radar sensors are highly effective in implementing active-control functions such as AEB or automatic cruise control, but an alternative approach is also possible through the use of optical sensors along with powerful processors. Ultimately, the vehicle manufacturer’s preference is the deciding factor for the type of sensor used in the application.

In general AEB can be implemented with just one type of sensor, but implementation also depends on the ASIL targeted for the system deployed. For higher levels of ASIL certification, the preferred solution is a radar sensor, backed by an optical sensor as a redundant approach. AEB is likely to be promoted in the near future as a mandatory feature for light vehicles, which would provide a higher level of protection in affordably priced cars.

In Europe, the New Car Assessment Program (NCAP) is encouraging car makers to implement AEB for pedestrian detection and to help vehicles avoid collisions with other vulnerable road users, including cyclists and animals. Vehicle manufacturers are already planning for their cars to support AEB systems, with the aim of obtaining a five-star rating from the European program. Based in Brussels, Belgium, the NCAP is patterned after the American model created by the U.S. National Highway Traffic and Safety Administration, evaluating new vehicle designs for safety and performance threats.

Given the European program’s call to action, global semiconductor revenue for pedestrian-detection systems is projected to climb as well in the coming years, rising from just $2 million in 2013 to $400 million in 2020. The next 20 years will require an entire ecosystem for autonomous vehicles to be in place in order to be successful, IHS believes. Specifically, mandates, regulations and legislations will need to be shared among different countries, and infrastructure surrounding vehicles must also figure into the equation.

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Apple and Samsung top MEMS **microphone** buyers

Microelectromechanical systems (MEMS) microphones, used in best-selling devices like Apple's iPhone, face a resonant future as the market keeps climbing in the coming years, according to a new report from IHS Technology.

GLOBAL REVENUE FOR MEMS microphones is forecast to reach $1.04 billion this year, up a robust 24 percent from $836.9 million in 2013.

Less than a decade was needed for the MEMS microphone market to cross the billion-dollar threshold. While this year continues the galloping growth the industry has seen during the last few years, the rate of expansion is slowing as revenue has expanded.

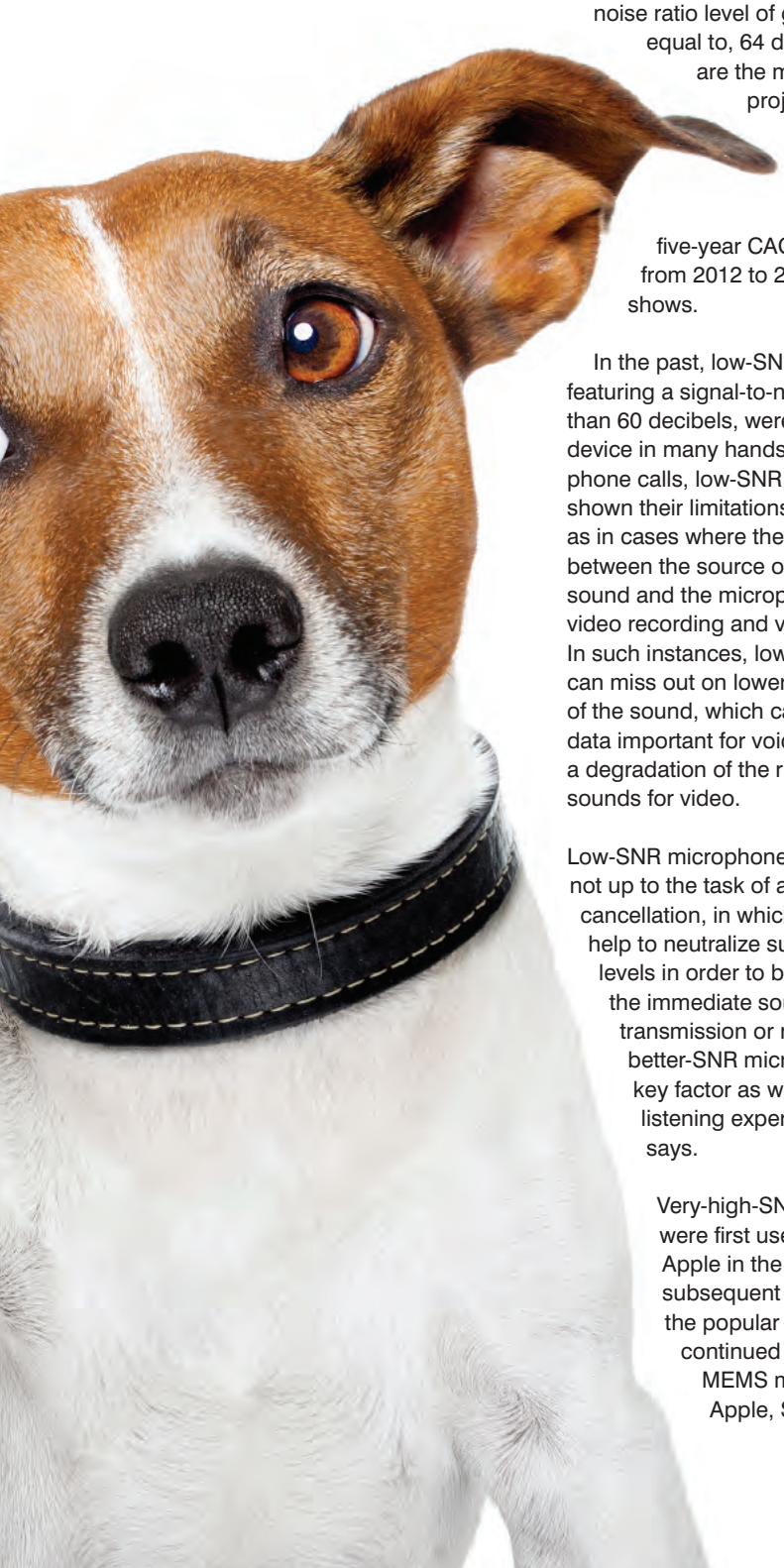
Even so, the next few years will continue to yield solid results for the business, and revenue by 2017 will amount to a projected $1.37 billion, equivalent to a five-year compound annual growth rate (CAGR) of 18 percent from 2012 to 2017. Shipments at the end of the forecast window will equal 5.4 billion units, up from 1.9 billion in 2012.

"The MEMS microphone segment has successfully capitalised on the value delivered by audible improvements in microphones to propel the industry forward," says Marwan Boustany, senior analyst for MEMS & sensors at IHS. "Especially in an age in which devices are increasingly uniform, sound can be a real and important differentiator, in features such as voice command or crystal-clear audio in high-definition

videoqualities that are possible only through high-performance MEMS microphones."

Handsets and tablets account for the majority of MEMS microphone consumption, and Apple and Samsung are the biggest buyers at present, Boustany noted.These findings are contained in the report, "MEMS and Sensors Report – Microphones – 2014," from the Semiconductors & Components service of IHS.

Two of the main measures for MEMS microphone quality are signal-to-noise ratio (SNR) and the maximum sound-pressure level (SPL). These define the lowest and highest sound levels, respectively—or dynamic range—that can be gauged by a microphone with a linear response. The measures apply to both analog and digital MEMS microphones, and have been used as the basis for microphone quality in marketing by firms such as Nokia and HTC.



At the top performance level, very-high-SNR microphones feature a signal-to-noise ratio level of greater than, or equal to, 64 decibels. These are the microphones projected to have the greatest growth in the coming years, with an estimated five-year CAGR of 40 percent from 2012 to 2017, IHS analysis shows.

In the past, low-SNR microphones, featuring a signal-to-noise ratio of less than 60 decibels, were the standard device in many handsets. Acceptable for phone calls, low-SNR microphones have shown their limitations in performance, as in cases where there is some distance between the source of the recorded sound and the microphone, such as for video recording and voice commands. In such instances, low-SNR microphones can miss out on lower volume elements of the sound, which can result in a loss of data important for voice commands and a degradation of the richness in recorded sounds for video.

Low-SNR microphones are also not up to the task of ambient-noise cancellation, in which the microphones help to neutralize surrounding noise levels in order to better focus on the immediate sound intended for transmission or reception. Here, better-SNR microphones are the key factor as well to an improved listening experience, Boustany says.

Very-high-SNR microphones were first used in 2012 by Apple in the iPhone 5, and subsequent generations of the popular smartphone continued to utilize these MEMS microphones. After Apple, Samsung joined in, using very-high-SNR MEMS microphones in its S4 and Note 3 flagship handsets. Together the two brands made up 96 percent of revenue for the very-high-SNR MEMS microphone market in 2013.

Another advantage of very-high-SNR microphones is enhanced support for voice commands, helpful for Apple's Siri or Google Now. The Motorola Moto X, for instance, includes multiple very-high-SNR microphones that improve the handset's ability to capture voice commands.

Between the very-high-SNR and low-SNR categories sits a third class of MEMS microphones, the high-SNR devices with a signal-to-noise ratio between 59 and 64 decibels, which will be what lower midrange devices may choose to transition from low-SNR microphones. Growth of this segment during the next few years will be lower than that of very-high-SNR types, but higher than in the low-SNR segment that is headed for decline.

MEMS microphones are deployed the most in handsets and tablets, which last year accounted for 93 percent of revenue in very-high-SNR microphones. Apple and Samsung each have up to three microphones for their handsets that could possibly climb to four, and the multiple numbers no doubt help increase overall revenue for MEMS suppliers.

The rapidly growing tablet space is also a vigorous market driver, with the Apple iPad product line now outfitted with two microphones and with Samsung also adding multiple microphones to some of its tablets.

Very-high-SNR microphones are making inroads into hearing aids, too. The ReSound LiNX, for instance, uses two such devices, for noise cancellation and improved performance, with an additional beneficial capability that ties in Bluetooth connectivity with an iPhone - enabling the hearing aid to act as a headset as well.

High-performance MEMS microphones will also become increasingly prominent in the automotive space, helping support voice commands and hands-free calling. Harman has announced the use of two MEMS microphones for such use in Germany's Daimler vehicles, to start in 2016.

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Samsung, Intel & TSMC
to top spending in CapEx

ACCORDING TO IC Insights Samsung and Intel are both forecast to spend at least $11.0 billion this year, and TSMC slightly less than $10.0 billion on capex. Collectively the three companies are forecast to account for 51.8 percent of total semiconductor industry capex this year.
As amazing as that number is, it is a decrease from the 55.5 percent share these three companies held in 2013. Among the top 10, six companies are forecast to spend at least $3.0 billion in 2014, and nine suppliers are forecast to spend more than $1.0 billion. After keeping their combined spending essentially flat in 2013, the top 10 spenders are forecast to boost capex spending by 10 percent in 2014.

After chopping its capital spending by 28 percent in 2012 and 12 percent in 2013, SanDisk is forecast to show the largest capital spending percentage increase (86 percent) among the top 10. The company stated that this large increase is needed to expand production of advanced 3D NAND flash memory with its manufacturing partner Toshiba.

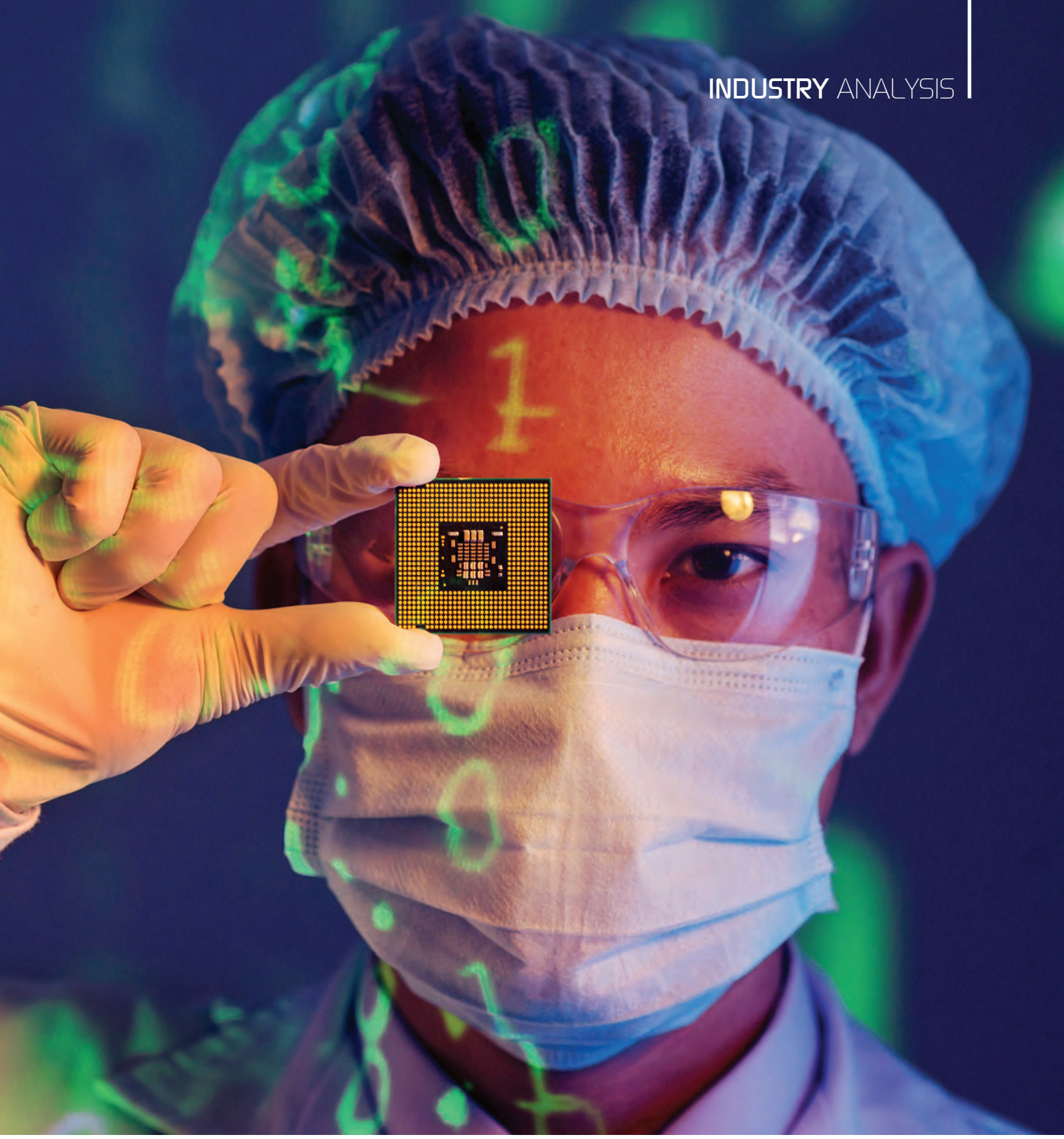
While SanDisk's capital spending level is expected to be much higher than in 2013, this increased spending is not expected to result in a significant boost to its NAND Flash capacity levels. It is worth noting that the combined capex spending increase of Toshiba and SanDisk (on account of their joint venture partnership to build flash memory) is forecast to be $1.06 billion in 2014.

Capital spending budgets are forecast to increase by $1.0 billion or more at two companies. Micron is expected to be very aggressive by increasing its spending $1.12 billion in 2014.

Still, this 58 percent jump in spending is forecast to be less than the 88 percent jump in sales revenue the company logged in 2013 (after the inclusion of Elpida's sales).

Also, pure-play foundry GlobalFoundries is expected to increase its semiconductor capital spending by $1.0 billion as well this year. SK Hynix is expected to display an 18 percent increase in spending in 2014. However, given the company's excellent sales performance in 2013 (43 percent growth) and its aggressive rebuilding program for its fire-damaged China DRAM fab, IC Insights believes there is potential upside to this estimate.

Some of the most eye-catching numbers are the massive amounts of spending expected by Samsung and Intel over the



2012-2014 time period.
Over this three-year period, Samsung is forecast to spend $35.3 billion, with about 60 percent of this amount targeting memory production.

Intel is forecast to be second to Samsung in total outlays over this same time with $32.6 billion in dedicated to capital expenditures.

These huge levels of spending are enough for each company to construct and equip eight or nine $4.0 billion leading-edge 300mm wafer fabs. Nine of the top 10 semiconductor industry capital spenders are expected to increase their semiconductor capital expenditures in 2014. In contrast, only four of the top 10 capital spenders increased their spending levels in 2013.

Meanwhile, capex spending among "other" suppliers is expected to grow at a much slower 3 percent rate this year, but that is a marked improvement from the 15 percent decline registered by the "other" segment in 2013.

In the long run, IC Insights believes that "other" companies will likely increase their spending at a lower rate, or decrease their spending at a higher rate, as compared to the top 10 companies as they implement the fabless or "fab-lite" business models for their IC production.

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SEMI: Fab equipment spending recovering

AFTER TWO YEARS OF DECLINE in terms of equipment spending, 2015 may reach or even surpass historic record year 2011 (about US $39.8 billion).

For the May 2014 SEMI World Fab Forecast publication, SEMI tracked more than 200 major projects involving equipment spending for new equipment or upgrades, as well as projects to build new facilities or refurbish existing facilities. In the last three months, 265 updates were made to the database. The latest data is shown in the table below.

In 2014, the three largest regions for fab equipment spending will be Taiwan with over US $10.3 billion, the Americas with over US $6.8 billion, and Korea with over US $6.3 billion. In 2015, these same regions will lead in spending. Taiwan is anticipated to spend over US $11 billion, Korea over US $8 billion, and the Americas almost US $7 billion. Although in sixth in regional equipment spending this year, the Europe/Mideast region will show the strongest rate of growth, about 79 percent compared to the previous year. The same region will continue to grow fast in 2015, with an increase of about 20 percent.

Worldwide installed capacity is very low for both 2014 and 2015 and the SEMI data does not suggest that this will change over the next four years. Because of the increased complexity of leading-edge nodes, such as more process steps and multiple patterning, fabs experience a decline in capacity as the same fab space produces less.

Worldwide, installed capacity grew by less than 2 percent in 2013 and is expected to grow just 2.5 percent in 2014 and 3 percent in 2015. SEMI's detailed data predict that Foundry capacity continues to grow at 8 to 10 percent yearly (a steady pace since 2012) and Flash is up 3 to 4 percent for 2014. Although DRAM equipment spending is expected to grow by 40 percent in 2014 as many fabs upgrade to a leading-edge process, installed capacity for DRAM is expected to stay flat or even drop 2 percent.

SEMI's reports also cover capacity changes for other product segments: MPU, Logic, Analogue/Mixed signal, Power, Discretes, MEMS, and LED and Opto.

The SEMI World Fab Forecast uses a bottom-up approach methodology, providing high-level summaries and graphs, and in-depth analyses of capital expenditures, capacities, technology and products by fab. In addition, the database provides forecasts for the next 18 months by quarter. These tools are invaluable for understanding how the semiconductor manufacturing will look in 2014 and 2015, and learning more about capex for construction projects, fab equipping, technology levels, and products.

The SEMI Worldwide Semiconductor Equipment Market Subscription data tracks only new equipment for fabs and test and assembly and packaging houses. The SEMI World Fab Forecast and its related Fab Database reports track any equipment needed to ramp fabs, upgrade technology nodes, and expand or change wafer size, including new equipment, used equipment, or in-house equipment.

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2014 Top 10 Suppliers' Semiconductor Capital Spending Forecast

2014F Rank	Company	2012 ($M)	2013 ($M)	13/12% Change	2014F ($M)	14/13 % Change	2012-2014F ($M)
1	Samsung	12,225	11,560	-5%	11,500	-1%	35,285
2	Intel	11,000	10,611	-4%	11,000	4%	32,611
3	TSMC*	8,341	9,709	16%	9,750	0%	27,800
4	GlobalFoundries	3,800	4,500	18%	5,500	22%	13,800
5	SK Hynix	3,363	3,146	-6%	3,700	18%	10,209
6	Micron	2,184	1,935	-11%	3,050	58%	7,169
7	Toshiba	1,137	1,630	43%	1,950	20%	4,717
8	SanDisk	979	859	-12%	1,600	86%	3,438
9	UMC*	1,770	1,098	-38%	1,200	9%	4,068
10	SMIC*	499	651	30%	880	35%	2,030
—	Top 10 Total	45,298	45,699	1%	50,130	10%	141,127
—	Others	13,742	11,731	-15%	12,100	3%	37,573
—	Total Cap Spending	59,040	57,430	-3%	62,230	8%	178,700

Source: IC Insights, Company Reports *Foundry


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Taiwan tops semiconductor equipment sales again

SEMI has reported that worldwide sales of semiconductor manufacturing equipment hit $31.58 billion in 2013 compared to $36.93 billion in sales posted in 2012. This represents a year-over-year decrease of 14 percent.This is cited in the “Worldwide Semiconductor Equipment Market Statistics (SEMS) Report,” by SEMI. Categories covered include wafer processing, assembly and packaging, test, and other front-end equipment. Other front-end includes mask/reticle manufacturing, wafer manufacturing, and fab facilities equipment.

Spending rates declined for all the regions tracked in the WWSEMS report, except for China and Taiwan. For the second year in a row Taiwan remained the region with the highest amount of spending with $10.57 billion in equipment sales. The North American market surpassed South Korea to claim the second place with $5.26 billion in sales; South Korea fell to the third position with a regional decrease of 41 percent.

The global other front end equipment segment decreased 34 percent; the assembly and packaging segment decreased 26 percent; total test equipment sales decreased 24 percent; and the wafer processing equipment market segment decreased by 11 percent.

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PacTech doubles capacity in Asia

PACTECH GMBH has announced that subsidiary PacTech Asia (Penang, Malaysia) is now doubling capacity for electroless Ni/Au and Ni/Pd wafer level plating services. The additional clean room area is now ready for installation of a new PacLine 300 automatic electroless plating system.

Manufactured by PacTech, the PacLine 300, pictures above, is suitable for both aluminium and copper pads on 200mm & 300mm wafers, and creates additional capacity of 20,000 to 30,000 wafers per month

Thorsten Teutsch, President and COO of PacTech USA and COO of PacTech Asia comments, “We are experiencing huge success in MOSFET, RFID, LED, MEMS, and other key product areas with both major IDM’s and fabless customers. PacTech Asia and PacTech USA work closely together to insure their mutual success! Over 80 percent of the volume demand results from our successful qualifications and product transfers from PacTech USA to PacTech Asia.

Additionally, PacTech Asia continues to invest in more automation, inspection and test capabilities, including wafer back metal services growing to 10,000 wafers per month.”

PacTech USA’s Silicon Valley facility located in Santa Clara, California is not only PacTech’s Equipment Sales and Demonstration Centre for the Americas, but also provides support on new designs and early production volume demands.

Expedited chip design cycles on first silicon and multi-project wafers are critical to successful design wins with key end customers. Once proven, customers are ready to ramp up production volumes, and rely on their Asia-based external foundry management teams. The “Copy Exact” process transfer from PacTech USA to PacTech Asia intends to insure the seamless transition handover. Heinrich Lüdeke, CEO of PacTech - Packaging Technologies GmbH says, “We continue to commit more investments in 2014 - 2015, supporting both our advanced equipment manufacturing unit and foundry services operations. Plans include electroplated copper capabilities, embedded die packaging solutions, and next generation high-speed solder jetting machines, as well as laser-assisted bonding equipment.”

He concludes, “With over 800 production machines in the field and over 115 patents granted, the combination of PacTech’s technologies allows our three locations to provide the widest product offering in the industry; servicing the ASIC, Foundry, Government, Medical, Aerospace, Consumer, Telecommunication, Memory, MEMS, Probe Card, and Hard Disc Drive industries.”

Plasma-Therm tool enhances NASA’s fabrication capability

Plasma-Therm’s VERSALINE Deep Silicon Etch system was recently installed at NASA’s Jet Propulsion Laboratory (JPL) to expand its silicon deep-etching resources.

The new etching system targets silicon-based applications that include MEMS, sensors, and resonators. JPL’s Microdevices Laboratory (MDL) serves users with many different requirements, and the system’s mask selectivity, uniformity, vertical profiles, sidewall smoothness, and silicon-on-insulator capabilities will be used to meet their device fabrication needs.

The tool will complement JPL’s existing suite of Plasma-Therm equipment, which has been used to make mission-critical components for NASA explorations.
JPL scientists utilised Plasma-Therm systems to help fabricate sensors for the Planck and Hershel missions to map infrared and sub-millimetre cosmic radiation and the spectrometer grating installed on the moon-mapper to detect water.

Tuneable diode lasers to sense methane and other metabolic products from possible past life forms, part of the planetary exploration project involving the Mars Rover, were also made with the assistance of Plasma-Therm technology.

A recent report describes new cosmic microwave background polarization measurements, providing strong confirmation of the Big Bang theory and insight into the first moments of a rapidly expanding universe. The low-noise, superconducting and bolometer-based detectors were fabricated using Plasma-Therm systems that are part of the key process tool set at MDL.

“It is inspiring knowing that Plasma-Therm systems are used not only to develop sensors and optical devices for observing our terrestrial world, but also to contribute to the exploration of our solar system, other galaxies, and the early universe,” says David Lishan, Plasma-Therm Principal Scientist and Director, Technical Marketing.

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STMicro automotive accelerometer can make emergency calls

STMICROELECTRONICS says it has added another "world's first" device to its portfolio of motion sensors.
The new device targets automotive telematics, black box, and emergency calling.

The firm claims the new AIS3624DQ, a 3-axis accelerometer with digital output, is the first to provide a full-scale range of ± 24g (acceleration of gravity) while meeting the automotive industry's demanding AEC-Q100 reliability stress tests.

Automotive suppliers are developing an important application to automatically contact emergency services in the event of a collision or vehicle problem. The application can supply potentially life-saving details such as the location of the vehicle and the estimated severity of the problem or accident to emergency service operators. Examples of these services include Onstar (USA), eCall (Europe), and ERA Glonass (Russia).

"In addition to all of the amazing safety innovations already built into today's vehicles, this tiny sensor may play a vital role in protecting the car's occupants," says Fabio Pasolini, General Manager of the Motion MEMS Division, STMicroelectronics. "ST's long-standing interest in augmenting peoples' lives and our leadership in Micro-Electro-Mechanical Systems (MEMS) have again come together in an important sensor that could potentially help consumers."

The major parameters in estimating the severity of a collision include the decelerations that occurred in all three dimensions at the moment of impact; for instance, the ERA Glonass specification for the Russian market requires that longitudinal accelerations up to ± 24g must be measurable with sufficient accuracy. The AIS3624DQ brings all the benefits of ST's stacked-chip technology to the automotive market. STMicroelectronics solution is based on its 8" manufacturing of MEMS products and offers a more competitive solution than the others who produce on 6".

DelfMEMS secures $7.4 million funding

DELFMEMS has secured 5.4M€($7.4M) in round C funding for the development of RF MEMS switches.
bpifrance Investissement, Iris Capital, Capitalaria, VIVES as well as previous investors (A2D Invest, Finovam, Rhône-Alpes-Création, Eurekap!, Helea Financiere and business angels) have participated to this round C of funding.

The new investment will be used to support the company's growth in the next generation, wireless front-end modules for mobile devices such as smart phones and tablets that need multi-standard, multi-mode mobile telephony.

The move to multiple wireless standards to meet the requirement of always on data access creates the need for high speed RF switching. DelfMEMS technology uses a new, integrated, micro-mechanical building block that is based on a strong, totally new, IP portfolio that includes seven major patents.

The switch is an anchorless and push-pull mechanical device that is deflected by electrostatic forces to switch RF signals based on the principle of current electro-mechanical relays/switches. It solves past issues and substantially improves insertion loss, linearity, integration, hot switching behaviour, switching time and power consumption to simplify RF architectures. The benefits of DelfMEMS RF MEMS switches are claimed to include improved receiver sensitivity leading to fewer dropped calls and better call quality together with optimal carrier aggregation switching for massively improved data rates.

Combined with high levels of RF integration, this also results in a lower bill of materials cost for the RF Front-End module, and significantly longer battery life by reducing the power consumption of the RF module by up to 20 percent.

Guillaume d'Eyssautier, DelfMEMS CEO, says, "The progress that we have made in turning RF MEMS switches into reality has really impressed our investors. The test silicon has shown that we have cracked the problems that have caused many MEMS companies to fall by the roadside. This is creating a lot of interest in the industry especially as we will have samples for customers to evaluate in a few weeks. This latest round of financing will be used to consolidate the organisation and be ready for production ramp-up by the end of 2014."

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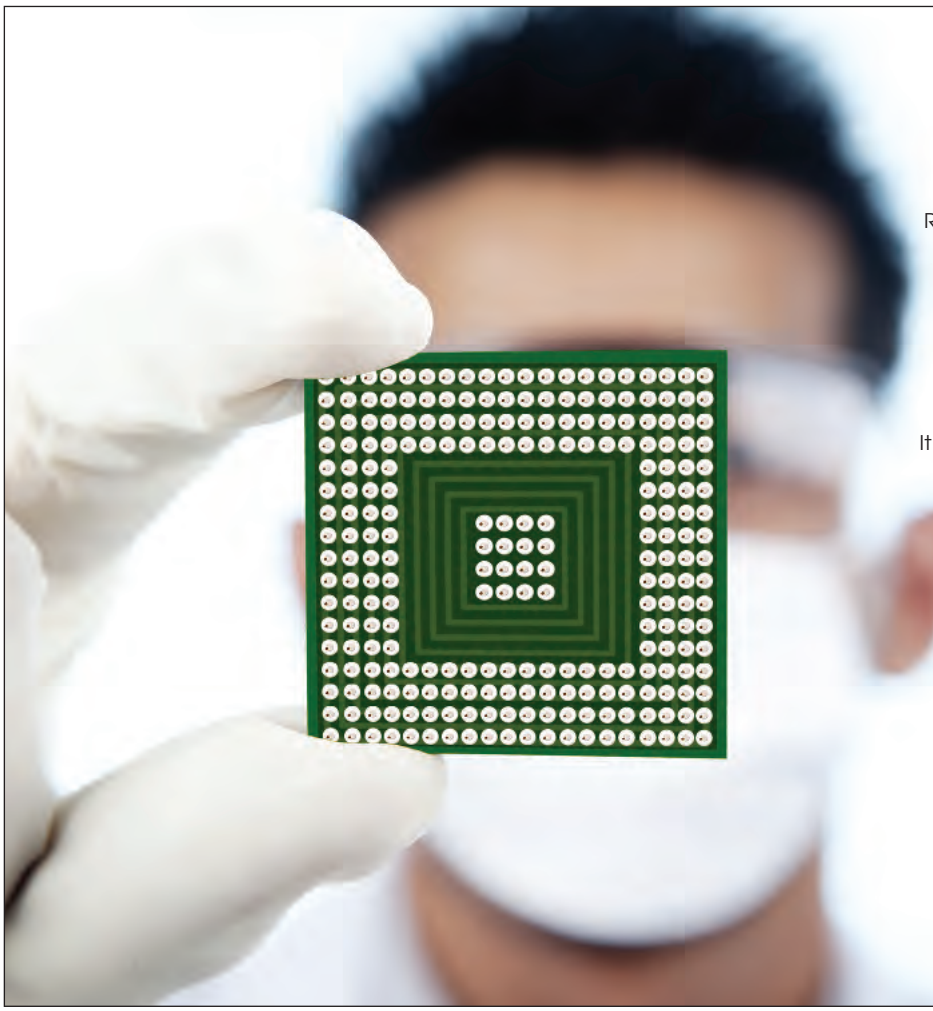

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Innovation
in materials recovery

Paul Stockman, Technology Manager at The Linde Group explores the complex procedures deployed to sustain a secure and reliable supply of material in the electronics Industry.

THE UNMATCHED TECHNOLOGICAL PROGRESS demonstrated in the semiconductor manufacturing industry has ultimately been made possible through an industry norm of constant technical and engineering innovation.

In this fiercely competitive and diverse market, the constant drive for progress has driven manufacturing complexity. Production of semiconductor devices such as microprocessors and memory is becoming increasingly sophisticated, requiring manufacturers to optimise process performance with increasing levels of resolution and accuracy. For materials suppliers, the portfolio of materials required continues to grow, and as a result, so does the supply chain complexity and quality requirements.

This pressure is exacerbated by a number of factors: a scarcity of key materials, such as the well documented reduction in the supply of helium and complex supply chains. To stay ahead of the curve and reduce operating costs, ensuring a secure and reliable supply of materials is vital.

In fact, it is becoming increasingly important to consider exactly where materials are coming from to ensure consistent quality, stable supply and ultimately the lowest overall cost of ownership. Electronics manufacturing plants are not always located in the optimum position for material supplies, making it vital to think about how materials could potentially be recovered, purified and re-used on site, saving both shipping costs and reducing logistics risks.

Three Recovery Options

To meet current industry demands we presently operate three main types of materials recovery solutions – tailored to individual customer requirements. Firstly, there is the on-site, closed loop approach where waste materials are recovered and returned into the customer manufacturing process via purification and quality control systems.

This solution can be used for materials such as helium and argon. Another alternative is on-site, open loop recovery. In this case, materials are recovered on-site but then removed and re-used for other applications – for substances like sulphuric acid. The final option is off-site recovery, which is mainly used for high cost materials. Here, the materials are recovered before shipping off-site for recovery and purification, for example, in the case of xenon.

All types of recovery can offer numerous benefits including cost reduction, supply chain security and a lower carbon footprint. Let's now take a look at these three options in more detail, and in relation to helium, sulphuric acid and xenon which are so vital to electronics manufacturing.

Helium: Finite resource and specialised recovery

Firstly, let's take Helium which is recovered via the on-site, closed loop approach.

Even though helium is an abundant element in the observable universe, on earth it is a relatively rare and non-renewable resource, found in the ground and co-located with some natural gas deposits.

In electronics manufacturing, helium is used at hundreds of points in the fab for cooling, plasma processing, and leak detection – however, its recovery is not straightforward. Helium is recovered as part of the natural gas extraction process and is not economically viable to be produced on its own.

To combat this issue, we have been closely involved in the design and manufacture of equipment to


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separate, purify, and liquefy helium to a temperature of -269˚C. Only in its pure, liquid state can helium be economically transported across the globe. By combining several core technologies, we have created a hybridized plant design to extend helium recovery to electronics applications, where the waste streams are often more dilute and contaminated.

Consequently, groups of large fabs clustered in one major site will be able to receive the real benefits of this helium recovery system, benefitting in terms of cost.

Sulphuric acid: Fresh water and logistics

The recovery of Sulphuric acid falls under the second category of materials recovery: on-site, open loop recovery. The drivers for sulphuric acid recovery are very different from that of the previously discussed Helium. The benefits here are reduction of disposal costs and associated demands for fresh water and waste water volumes.

Sulphuric acid is used in electronics manufacturing to remove sacrificial materials, to dissolve stray particles, and to otherwise clean semiconductors. Disposing of the used acid involves first neutralizing and then diluting the waste until it is acceptable for general waste water discharge to local standards.

The Linde Group joint venture, AUECC, is recovering sulphuric acid from the waste material, reducing costs and community waste flows. Using proprietary exchange technology enables the recovery of a high percentage of sulphuric acid from a customer's waste material each time. The material can be purified for re-use in the electronics or other industries.

At the largest semiconductor sites, the logistics of delivering fresh sulphuric acid and removing liquid waste can lead to congestion of delivery vehicles and large storage facilities. Therefore, by moving in acid recovery, the logistics traffic and facilities can be significantly eased. The result: reduced disposal costs, lower environmental impact, lighter traffic.

Xenon: Rarity and recovery

Finally, let's turn to Xenon, which is recovered off-site. Xenon is a particularly rare gas, with approximately only one part in 10 million in the atmosphere.

In electronics manufacturing, xenon is used in small amounts in lithography lasers, and in higher amounts and concentrations in etch applications. In fact, sometimes xenon is used as itself in plasma etching, and alternatively as the fluorinated compound XeF_2.

Xenon is obtained from large ASUs as a 1:13 crude mixture with krypton and this mixture is then separated, purified, and packaged at one of our global rare gas manufacturing centres. Due to the low starting concentration, only about 10 million litres of Xe are made each year.

So, how does the process work? Xenon is captured in proprietary vessels, shipped back to the global rare gas centres for re-purification. The original customer receives a credit for the xenon recovered at their site.

Recovering xenon in this way can have real tangible results. Ultimately, being able to recover molecules of xenon enables expansion of supply for customers, and stabilises the cost of the material for larger users.

Processes for a sustainable future

In a world dependent upon manufacturing processes requiring the use of limited resources, coupled with an ever increasing demand for electronic goods, finding innovative solutions to increase the sustainability of manufacturing is not an easy feat.

The responsibility falls on companies within the manufacturing industries to employ technologies that reduce waste, increase productivity, recycle and purify, and lift the strain on natural resources.

These are now being achieved in ways that contribute towards lower costs, provide flexible logistical solutions, and benefit the environment for a sustainable manufacturing future.

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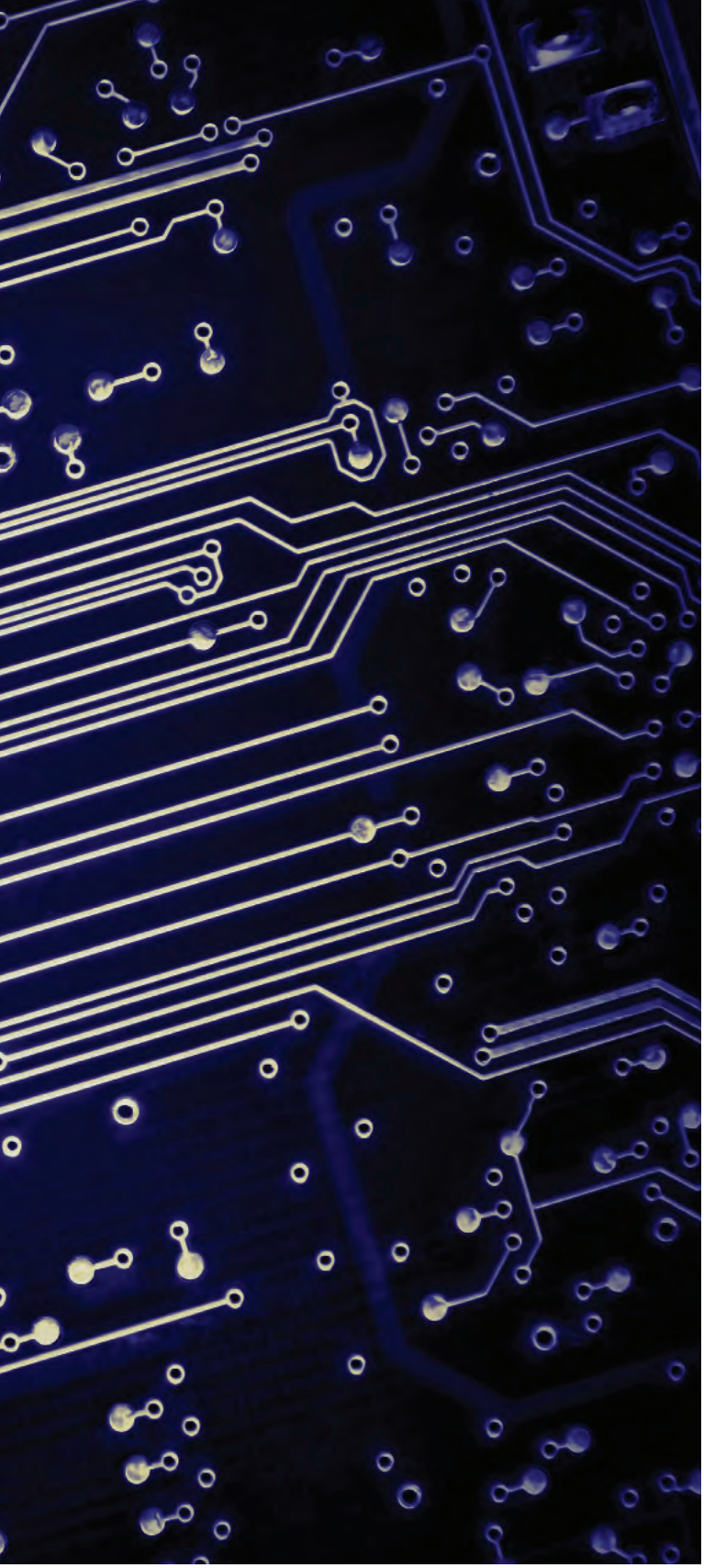
DSA: the next-generation patterning technology?

Directed self-assembly or DSA has become an attractive technique for generating fine lithographic patterns in chip manufacturing processes. But is the technique ready for chip manufacturing? And will it ever replace conventional optical lithography? Roel Gronheid, Principal Scientist at imec and DSA expert, throws more light on the current status and future of DSA.

DIRECTED SELF-ASSEMBLY or DSA is an alternative patterning technology which promises to extend conventional lithography beyond its current limits. Traditionally, the semiconductor industry uses optical lithography to pattern structures on a silicon wafer.

By decreasing the wavelength of light used for exposure and/or by increasing the numerical aperture of the equipment, the litho community succeeded in printing ever smaller features. In recent years, we saw the introduction of 365nm lithography, 248nm lithography, 193nm lithography, 193nm immersion lithography and finally extreme ultraviolet (EUV, 13.5nm) lithography. Recently there has been a growing interest in using DSA as a means to further reduce the pitch of the final printed structure. The concept of DSA is different from what we are used to. DSA is a bottom up technology that relies on the self-assembly of block copolymers (BCPs). A BCP is a special kind of a copolymer, made up of blocks of different polymerized monomers (A and B). When a thin film of such a BCP is coated on a wafer, a phase separation on the microscopic (or



more precisely: nanoscopic) level occurs between the two components. This results in different morphologies, depending on the volume fraction of components A and B. For patterning, two morphologies are of interest: lamellae (volume fraction 50/50) and cylinders of the minority block in a matrix of the majority block (30/70).

To be useful for making electronic circuits, these structures must be oriented and put in a location where we want them: directed self-assembly. The orientation of the structures (e.g., assembling parallel or perpendicular to the substrate) can be influenced by controlling the surface properties of the wafer. To guide the patterns in the desired direction, we make use of pre-patterns. Two different approaches are used for creating these pre-patterns: grapho-epitaxy and chemo-epitaxy. Grapho-epitaxy makes use of topographic features (e.g. trenches pre-formed by conventional lithography) to guide the orientation of the BCP microdomains. Chemo-epitaxy employs a surface with a chemically heterogeneous pattern (e.g. hydrophobic and hydrophilic) to align the BCP pattern through surface-polymer interactions. The dimension (for grapho-epitaxy) or periodicity (for chemo-epitaxy) of the pre-pattern should equal an integral time the periodicity of the BCP – a condition which is called commensurability.

What are the disadvantages of using DSA compared to optical lithography?

With DSA, pattern parameters such as pitch, critical dimension (or CD, i.e., the dimension of the smallest feature which can be formed) and uniformity are no longer dependent on the lithographic tool conditions, but on the polymer material itself. This holds both an advantage and a disadvantage. A major advantage is the superior uniformity that can be achieved. And, by choosing the right polymer, a phenomenally small resolution can be reached. In academia 6nm pitch (or 3nm half pitch) has already been demonstrated.

But the dependence of pattern parameters on the material properties also holds a disadvantage. Once you have your BCP, you cannot adjust the dimensions of your structures. If your supplier gives you a BCP with slightly different properties, you have to close down the whole process. This will impose new requirements to the way quality control is carried out at the material supplier. Therefore, a close collaboration with our suppliers is extremely important.

Will DSA ever replace conventional lithography?

In my opinion, DSA will never be a competitor to advanced optical lithography, EUV lithography or e-beam lithography: they will be complementary. True, DSA will be the champion when it comes to resolution. And it will be very suitable for making large

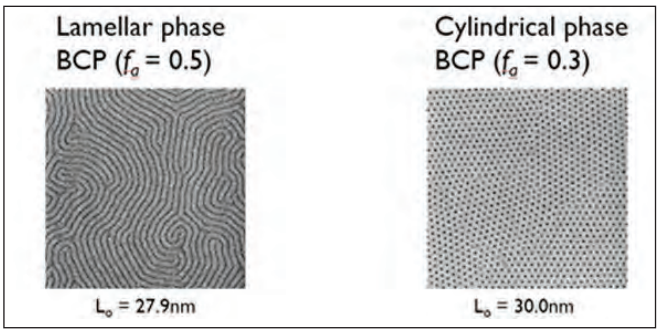


Fig 1: Examples of BCP structures: lamellar phase and cylindrical phase.

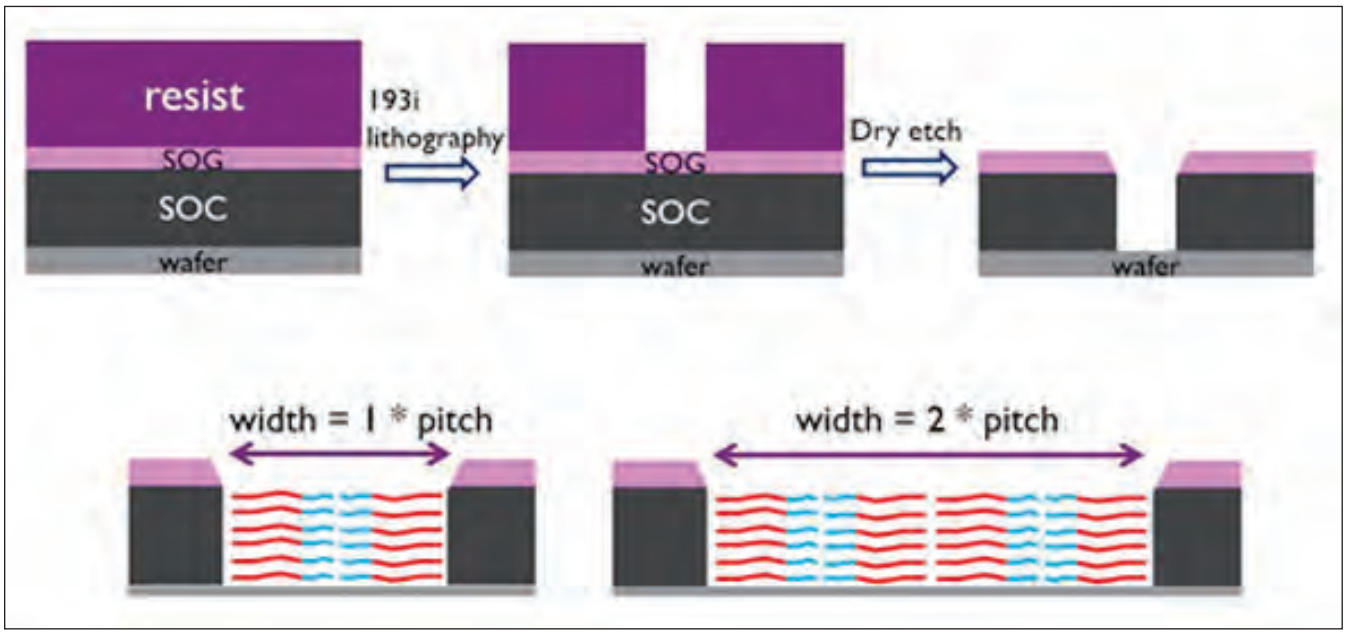


Fig 2: Schematic of grapho-epitaxy for pre-pattern generation.

regular patterns. But generating random patterns will be more difficult. This is more easily done with conventional lithography and EUV. In chip manufacturing, we will need both regular and random patterns. Also, the availability of EUV for generating pre-patterns would be very advantageous to DSA; and DSA would help to push the resolution of EUV even further, or could improve its uniformity. So, if the technology becomes mature for chip manufacturing, we will use DSA in combination with projection lithography.

What are the challenges to implement DSA in a chip manufacturing process?

I see two major challenges. First, there is the design aspect: how to design a chip that will be patterned by using DSA? It will need appropriate software. This work is currently in progress and is not expected to cause any major problems. We know how to do it. Secondly, for widespread DSA implementation, lower defect levels of DSA structures are required.

For chip manufacturing, very few errors are allowed on a wafer. For DSA, this translates into a defectivity level that is about two orders of magnitude lower than what we have today. Therefore, we need the right metrology to measure 3D structures in a BCP and to quantify defects over a relative large distance (order of centimetres). Also, we need a dedicated defect reduction strategy. Although there is still a lot of work to do, we are making significant progress. Every six months, we have consistently reached about a tenfold reduction in defectivity.

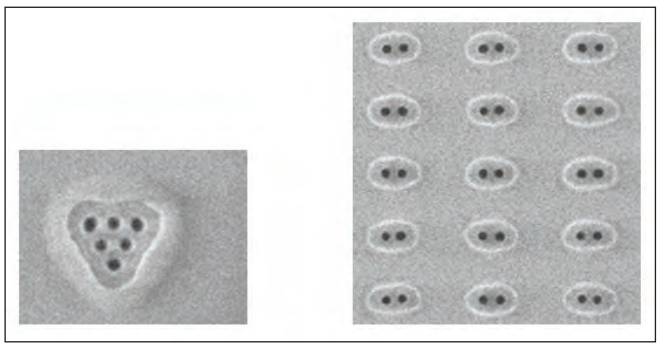


Fig 3: The SEM images demonstrate how different arrangements of hole patterns may be achieved.

Fortunately, the introduction of the polymer material itself does not pose any contamination issues. Polymers have been used in chip manufacturing since the very beginning. The most widely studied BCP material for DSA, poly(styrene-block-methyl methacrylate) (PS-PMMA), is comprised of monomers that are similar to the backbone material for chemically amplified resists.

When can we expect the first application of DSA?

Ongoing developments are progressing at a rapid rate. At imec, we are working towards including DSA into the 7nm logic technology node. Last year at the SPIE Advanced Lithography Symposium, we demonstrated the first electrical functional via chains made with DSA. In this work, we used blended polymer systems to shrink pre-patterned contact holes.

Contact holes are among the most difficult structures to resolve through traditional lithographic means. With our approach, we were able to shrink from ~53nm post-lithography CD to ~20nm holes after transfer into siliconoxide..

This year at SPIE Advanced Lithography, we reported progress on DSA material and process optimization, defect mitigation, defect metrology and inspection, and design decomposition. We also presented a 7nm compatible fin patterning technology using DSA. The fin layer of an invertor test cell based on a 4 fin, 3 gate test cell was patterned successfully.

The DSA community is working hard to prepare DSA for preproduction. Without further roadblocks, this can be expected by the end of this year or at the beginning of 2015. The first application will most probably be the patterning of contact holes

by shrinking prepatterns. This is the most simple application for which we don't need a whole new design approach.

What is imec's contribution to the DSA developments?
Certainly our work on defectivity is one of our strengths. We started working on DSA four years ago, after it was claimed that DSA was ready to move from lab to fab. The potential of DSA has been studied for a long time in the academic world and defectivity has always been unknown. Universities do not always have the right metrology to gather defect information over larger areas, which is needed for chip manufacturing.

So we needed to make the processes that have been developed in universities compatible with a manufacturing environment. At imec, we have specialized equipment to study defectivity, and we set up a dedicated process.

Another of our strengths is the ability to combine DSA with immersion lithography and EUV. With this unique toolset, we can make rapid progress in DSA development.

At this moment, we have a team of 15 researchers who work on DSA, several of them are students. And we have a unique partnership with the group of Prof. Paul Nealey from the University of Chicago. From the beginning, we had a very close collaboration and they helped us to speed up our DSA developments. We also closely collaborate with other partners, like AZ Electronic Materials, Tokyo Electron, and KLA-Tencor.

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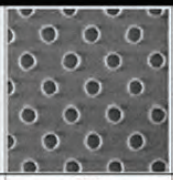
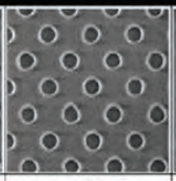
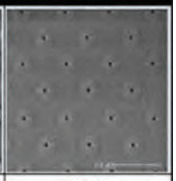
	Pst-Litho	Pst-Hardbake	Pst-DSA + Wet Dev
SEM image			
CD (nm)	53.8	58.9	14.5
Change (nm, %)	--	+5.1, +9.5%	-44.4, -75.4%
Net Shrink (nm, %)	--	--	-39.3, -73.0%
CD Range (nm)	3.4	3.3	0.5

Fig 4 a: Illustration of the DSA hole shrink application.

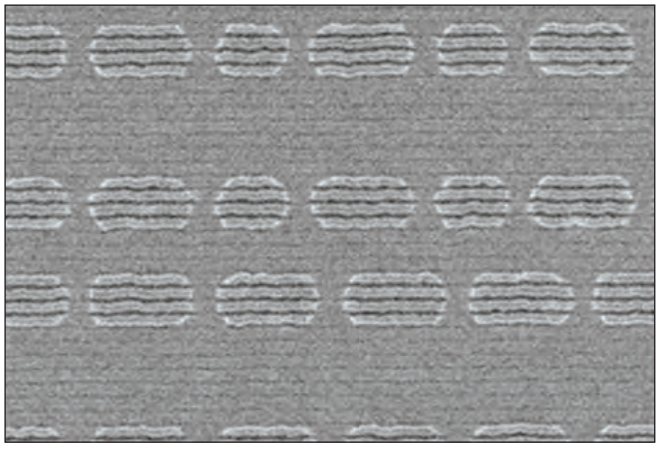


Fig 4 b: N7 compatible 28nm pitch fin layer patterned with DSA.

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Inspection of **directed self-assembly** defects

One of the challenges for translating DSA into high volume manufacturing is to achieve low defect density in the DSA patterning process. The defect inspection capability is fundamental to defect reduction in any process, particularly the DSA process, as it provides engineers with information on the numbers and types of defects. KLA-Tencor Corporation, University of Chicago and imec discuss how to accelerate the path to reduce DSA defectivity and improve the DSA process.

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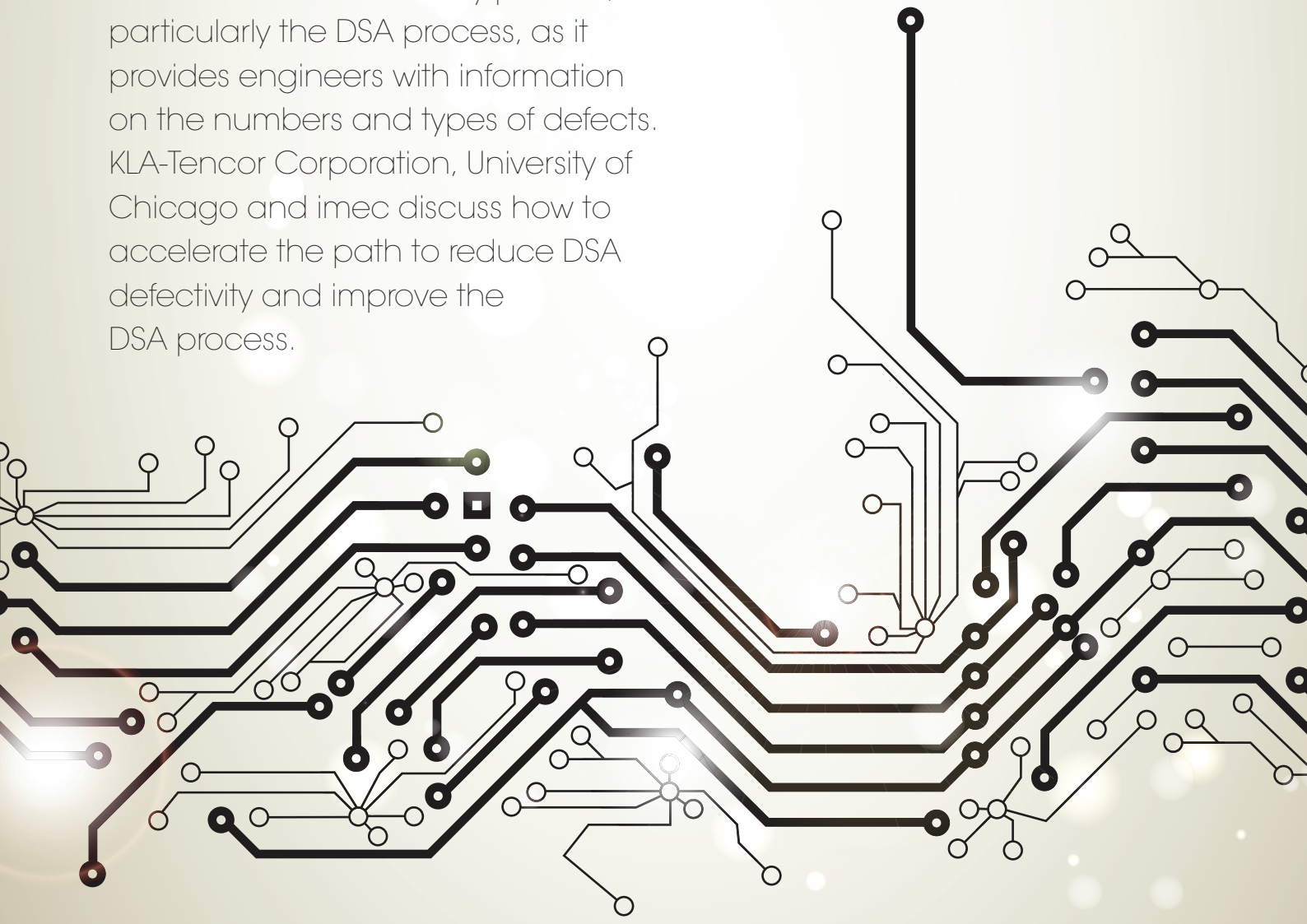


DIRECTED SELF-ASSEMBLY (DSA) is considered a potential patterning solution for future generation devices but to reach high volume manufacturing, low defect density in the DSA patterning process must be achieved.

The defect inspection capability is fundamental to defect reduction in any process, particularly the DSA process, as it provides engineers with information on the numbers and types of defects. While the challenges of other candidates of new generation lithography are well known (for example, smaller size, noise level due to LER etc.), the DSA process causes certain defects that are unique. These defects are nearly planar and in a material which produces very little defect scattering signal. These defects, termed as “dislocation” and “disclination” have unique shapes and have very little material contrast. While large clusters of these unique defects are easy to detect, single dislocation and disclination defects offer considerable challenge during inspection with conventional methods.

The concept of pattern transfer of a low signal producing layer into a more high scattering material was first explored by Kyoung-Yong Cho et al [1] for EUV lithography. In this work, a method to enhance DSA defect signal and Signal-to-Noise ratio (SNR) by etching into a silicon (Si) substrate is studied. The main purpose of this investigation is to determine the best inspection parameters to use in order to detect these subtle DSA defects using KLA-Tencor’s 2915 broadband plasma inspector. We first use a Rigorous Coupled-Wave Analysis (RCWA) method for solving Maxwell’s equations to simulate the DSA unique defects and calculate inspection parameters, such as illumination and collection apertures, wavelength band, and pixel size. Next, using the simulation, we compare SNR between “post-SiN etch” and “post-SiN+Si-substrate etch” steps. Finally, we compare the simulated SNR to actual inspection results on single dislocation type defects.

Simulation

The top view of the DSA pattern is a simple line and space array as shown on the top right of Figure 1. The critical dimension (CD) of the line is 14nm and the pitch is 28nm, with a line/space ratio of 1:1. This clip represents the typical pitch multiplication pattern (post guide pattern formation). The details of DSA pitch multiplication and etch process can be found in references 2, 3 and 4.

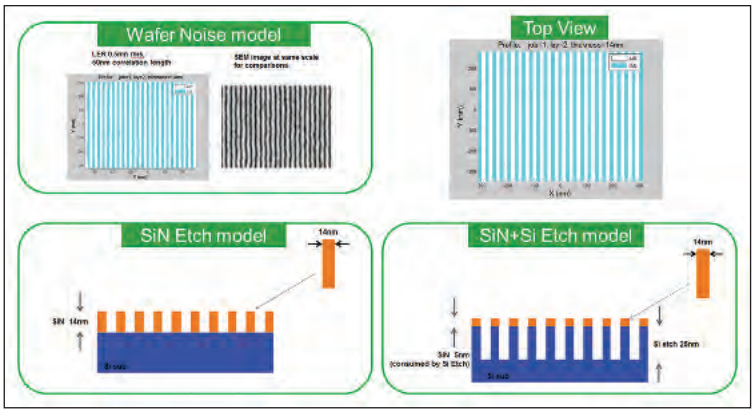


Figure 1. Stack and wafer noise model.

Prior to starting the simulation, we prepared models of the nominal pattern, layer thicknesses, a line edge roughness (LER) wafer noise model, and defect shapes. Each of these has parameters of material n/k across the wavelengths used with the 2915 wafer inspector. The RCWA code first solves the electro-magnetic fields in the wafer and outputs the amplitude and phase in the farfield. Then we apply the 2915 tool properties for inspection, such as wavelength band, light budget, numerical aperture (NA), apertures, polarization, pixel size, inspection speed, tool noise, and so on, to calculate optical images of nominal pattern, wafer noise, and defects by applying these optics and inspection tool conditions. After processing the images, we can calculate the expected signal and SNR for possible inspection tool parameters.

The bottom of Figure 1 shows the film stack model after the DSA pattern transfer into a 14nm thick SiN layer which is etched. Then the next process step is to use the SiN pattern and etch into the Si substrate to a depth of 25nm. In this etch process, the SiN is partially consumed and we assumed the remaining depth as 5nm.

The top left of Figure 1 shows wafer noise model which we based on SEM observation of the etched wafer. The model we use generates a random LER pattern with statistics of a 0.5nm line-edge roughness and a 50nm correlation length. We used the same LER model for the SiN etch and the SiN/Si etch simulations even though the etch process may smooth out

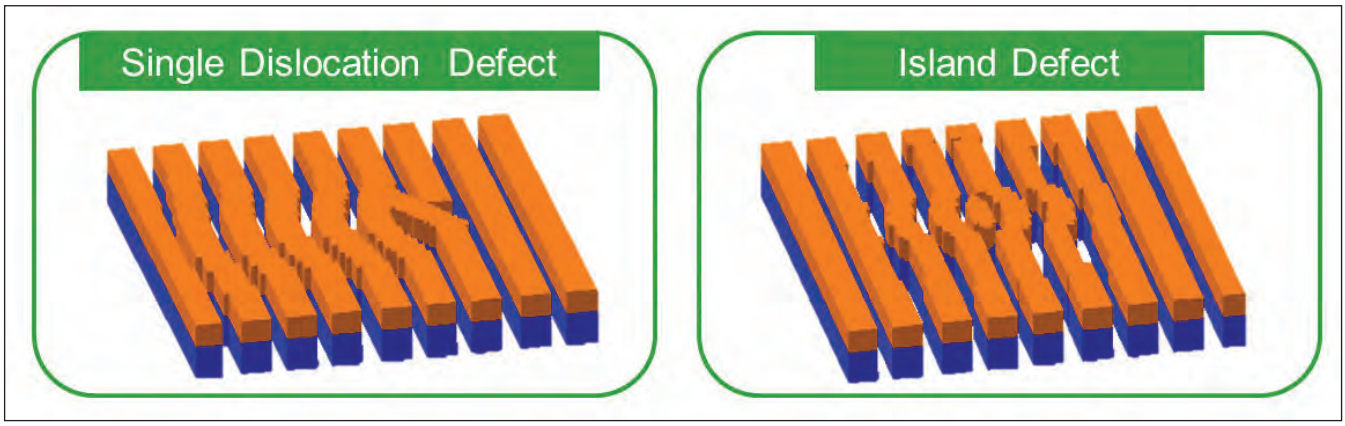


Figure 2. Defect model.

the roughness to some extent. For the SiN/Si etch simulation, the same LER profile is applied for both SiN and Si layer as we did not have enough data on LER for these layers.

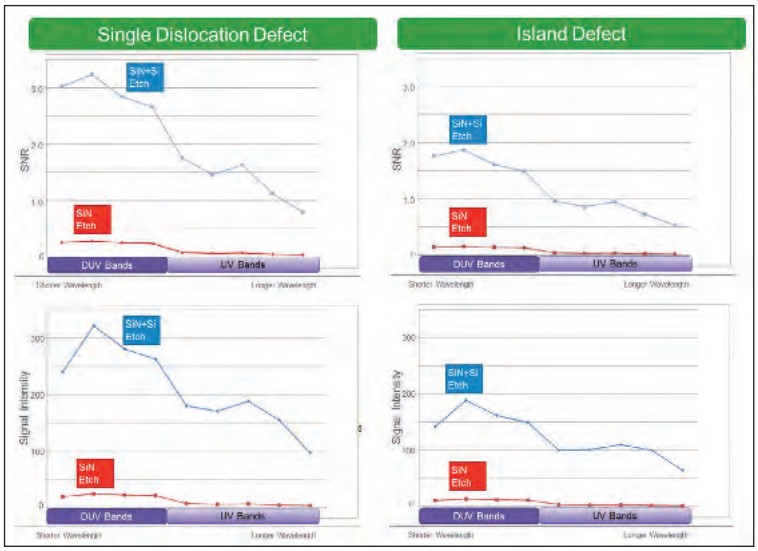
Figure 2 shows the defect models for the single dislocation and the island defect after the Si substrate etch. These models are developed from SEM images (not shown). On our wafers we noticed a defect which is neither dislocation nor disclination and hitherto not discussed in the DSA literature. We named it an 'island defect' which is shown in the right hand side of Figure 2. The detection of island defect is as challenging as single dislocation.

We attempted to duplicate the full nature of the DSA defects that spread to adjacent lines well beyond the center of the defect by bending these lines. While these simulations are specific to these exact shapes, we expect that the results will identify inspection parameters that are useful for other shaped defects as generally the layer materials and thickness are most important for the inspection parameters. We used the same shapes for the etched SiN and the etched into Si substrate.

Simulation results

Signal-to-Noise Ratio (SNR) is one of major parameters to evaluate defect detectability. A comparison of SNR between "Post SiN etch" and "Post SiN +Si substrate etch" indicates how much improved detectability can be expected between the two processes. Our simulation results, shown in Figure 3, indicate that the SNR (as a function of wavelength) is dramatically improved by >10 times for the "etched Si substrate" compared to the "SiN only etch". The SNR reached the detectable level which is SNR > 1.3 for the 2915 wafer inspection tool operating in the brightfield optical mode. Defect signal intensity also shows improvement >10 times as shown in the bottom charts of Figure 3. This means we can separate defect signal and noise easily. The simulator predicts that the shorter wavelength bands on the 2915 should be the most effective.

Figure 3. Defect SNR comparison (top) and signal intensity comparison (bottom) between post SiN etch and SiN+Si etch on each defect type.



Aperture and pixel size are key factors to define inspection sensitivity. The 2915 inspector has a range of available apertures and pixel sizes to optimize inspection sensitivity. Figure 4 compares simulation of apertures and pixel sizes for the single dislocation and island defects. The simulation predicts that "aperture 6" with a 50nm pixel size has the best SNR on both of defect types. Inspection results using this mode are reported later in this paper.

Wafer inspection

The post-etch wafer inspection was performed with the 2915, a broadband plasma patterned wafer defect inspector. Second-generation laser pumped plasma technology on this inspector produces higher light intensity which can help with detection of subtle defects on low contrast materials. On small DSA-dislocation defects, under equivalent optical conditions, the 2915 demonstrated high capture rate because of the improved SNR (4.8 on 2915 vs. 2.1 on the previous-generation 2835 inspector). The new apertures and inspection modes, together with flexible apertures enable detection of very small defects and their unique wafer signatures.

The typical methodology used in inspection recipe setup on defect inspection tools is to identify "candidate defects" using a sensitive pre-inspection built from knowledge base. A higher percentage of false defects is acceptable at this stage since the purpose is to find candidate defects. Using defect review SEM the wafer is analyzed thoroughly and

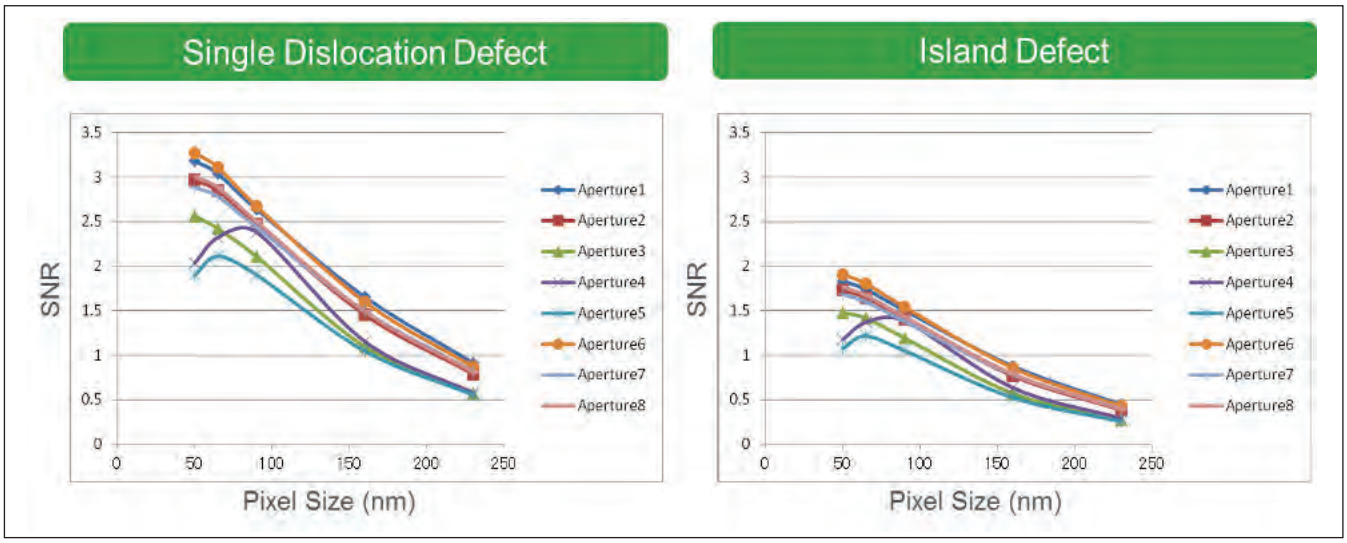


Figure 4. Aperture types and pixel size evaluation.

candidate defects are selected and identified through their unique defect coordinates.

On this initial inspection, we identified two single dislocation-type defects. The single dislocation we would like to detect is very close in appearance to these defects and therefore we performed detailed "optics characterization" on these two defects. It is our belief that if we identify optical parameters that will enhance detection of these two candidate defects, the probability of detection of single dislocation and disclination is very high, considering the fact that our post-etch signal strength and SNR are 10X greater. The signal strength and SNR were extensively studied using multiple wavelength bands, apertures, polarization, pixel size, focus and scan speed and the optimum settings were determined.

Our simulation tool has the capability of predicting SNR for the tool's various wavelength bands (as shown in the left-hand side of Figure 5). The optimum settings determined from experiment shown in the right-hand side of Figure 5 matches quite well simulation results. It appears that SNR is better in DUV band compared to UV band in simulation and experiment.

An inspection recipe was generated with the best optical mode obtained from simulation and the full "SiN + Si etch wafer" was inspected. Review was performed using KLA-Tencor's eDR-7000 review SEM. Due to high defectivity we reviewed a single row where 939 defects were classified. We were able to successfully find single dislocation defects (Defect ID 6285 and 6459). The patch images from the 2915 for these two defects show clear defect signals, as seen in Figure 6.

The reviewed defects were also classified and a defect Pareto was generated (Figure 7). In addition to dislocation defects and clusters, this mode also detected "single open" defects that are very small and of unknown origin. As shown in the Pareto, only two single dislocations were captured. The patch image on 2915 showed very strong signal as shown in the right-hand side of the Figure 6. From this we conclude

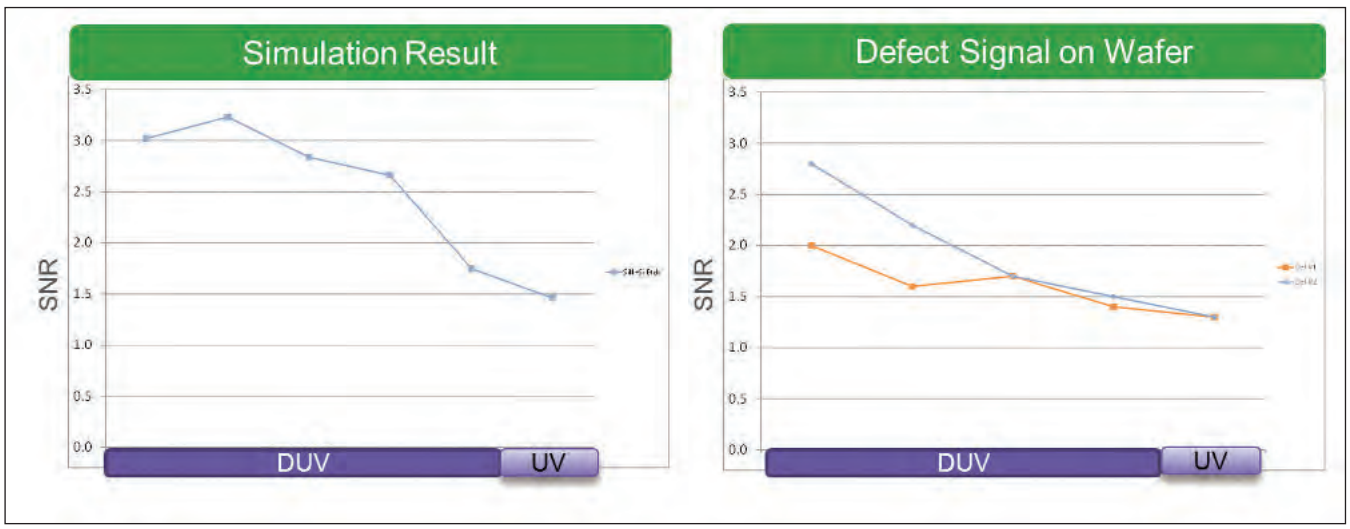


Figure 5. Simulation result for single dislocation defect and wafer-level tool data comparison on comparable defect.

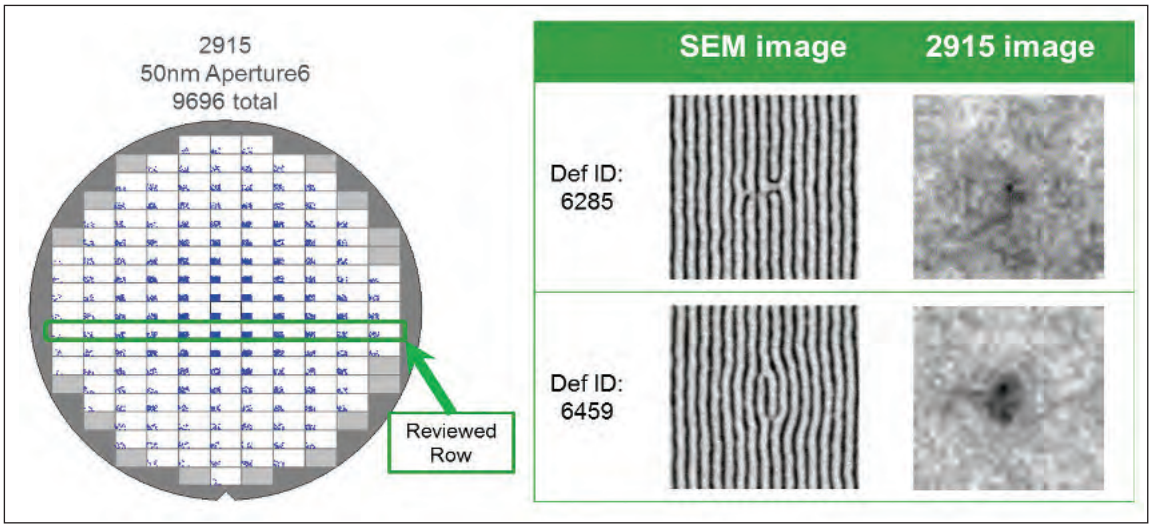


Figure 6. Wafer inspection result using the best inspection parameters as determined by simulation.

that our recipe has enough sensitivity and would have captured more if there were any more dislocation defects in the dies we classified. The dislocation pair and dislocation clusters are easily captured as shown in the Pareto. Other defects of interest are pattern collapse and line waving/bending. For reference, the inspection results from the 2915 are compared to the previous-generation wafer inspection tool, KLA-Tencor's 2835 which utilized a similar aperture to Aperture6 of the 2915. The 2915 detects 54 more defects compared with the 2835.

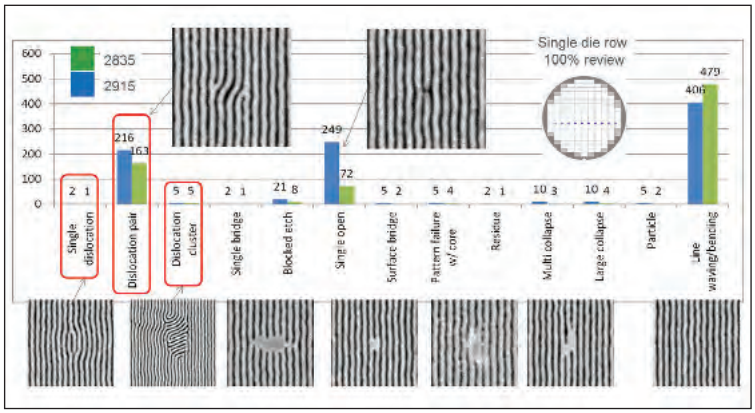


Figure 7. Defect Pareto resulting from review of 2915 inspection results.

Summary

Etching the DSA pattern into a Si substrate to a depth of 25nm is very effective for improving defect SNR to facilitate wafer inspection for DSA unique defects that are small, on a thin, low scattering material. This decoration effect boosts the inspection signal strength and improves the defect SNR of small dislocation defects >10 times compared to the DSA pattern just etched into SiN. The simulations we ran predicted this dramatic improvement, and the simulated SNR demonstrated good correlation to the 2915 broadband plasma inspection results for the single dislocation type defect. Using the best combination of aperture and pixel size from the simulation, the 2915 detected single dislocation and other DSA defects which helped us understand the defectiveness of the DSA process. In this experiment, the inspected area (single row) is equal to 3.66cm2. We found 939 defects and reviewed 100% of the defects. We found only 223 defects are DSA-specific. Hence our conclusion is that the defect density of dislocation-type DSA defects in the current process = [223/ 3.66] = 61 defects per cm^2. This information will help accelerate the path to reduce DSA defectivity and improve the DSA process.

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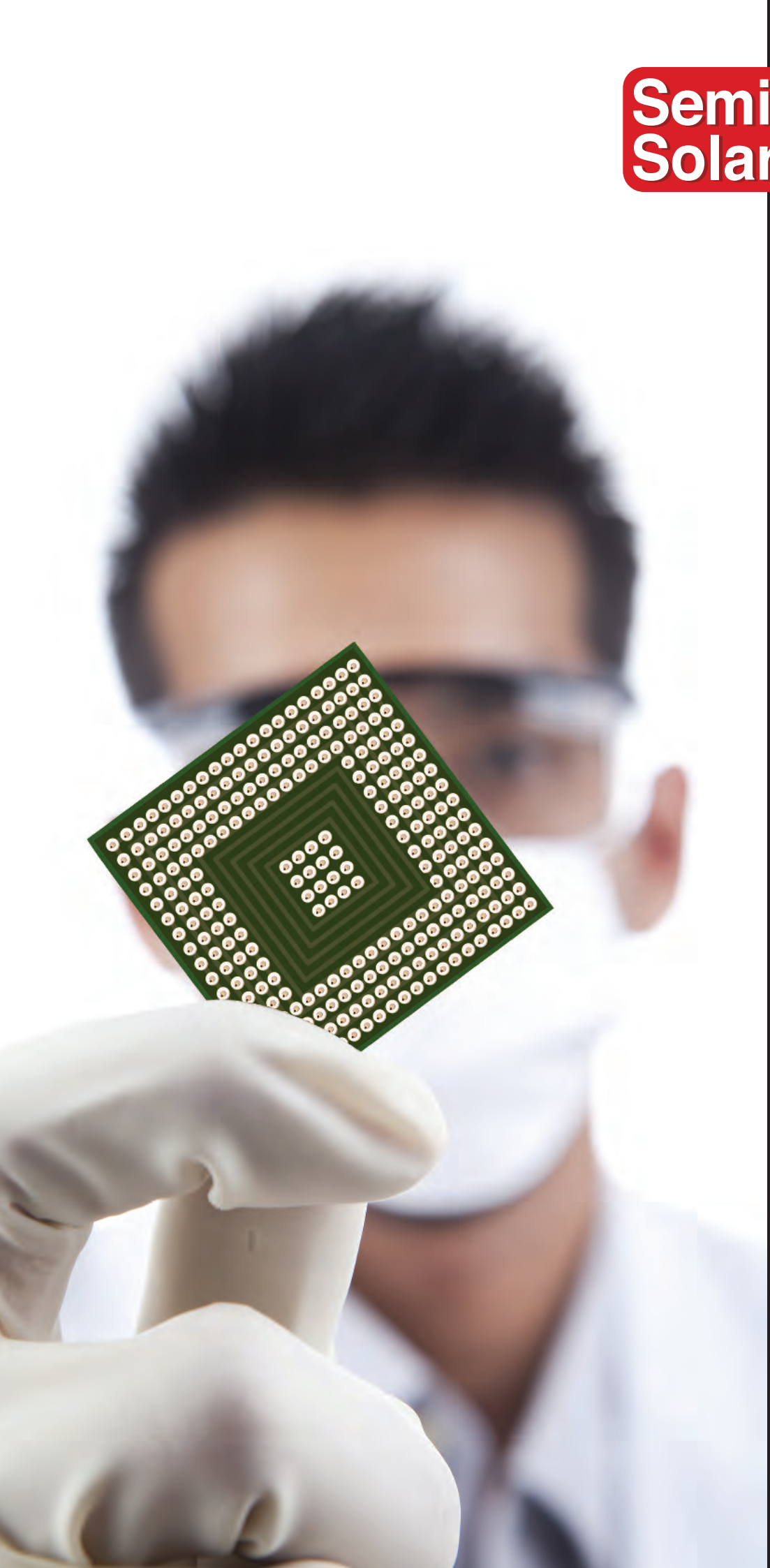
References

[1] Kyoung-Yong Cho; Joo-On Park; Changmin Park; Young-Mi Lee; In-Yong Kang; Jeong-Ho Yeo; Seong-Woon Choi; Chan-Hoon Park; Steven R. Lange; SungChan Cho; Robert M. Danen; Gregory L. Kirk; Yeon-Ho Pae "The analysis of EUV mask defects using a wafer defect inspection system" Proc. SPIE 7636 (2010)

[2] Paulina Rincon Delgadillo, Ryota Harukawa, Mayur Suri, Stephane Durant, Andrew Cross, Venkat R. Nagaswami, Dieter Van Den Heuvel, Roel Gronheid, Paul Nealey "Defect source analysis of directed self-assembly process (DSA of DSA)" Proc. of SPIE Vol. 8680, 86800L (2013).

[3] Roel Gronheid, et al "Defect Reduction and defect stability in IMEC's 14 nm half pitch chemo-epitaxy DSA flow" Proc. of SPIE (2014)

[4] Paulina Rincon Delagadillo et al "Kinetics of defect annihilation in DSA of BCP using chemically nanopatterned surfaces" Proc. of SPIE (2014)



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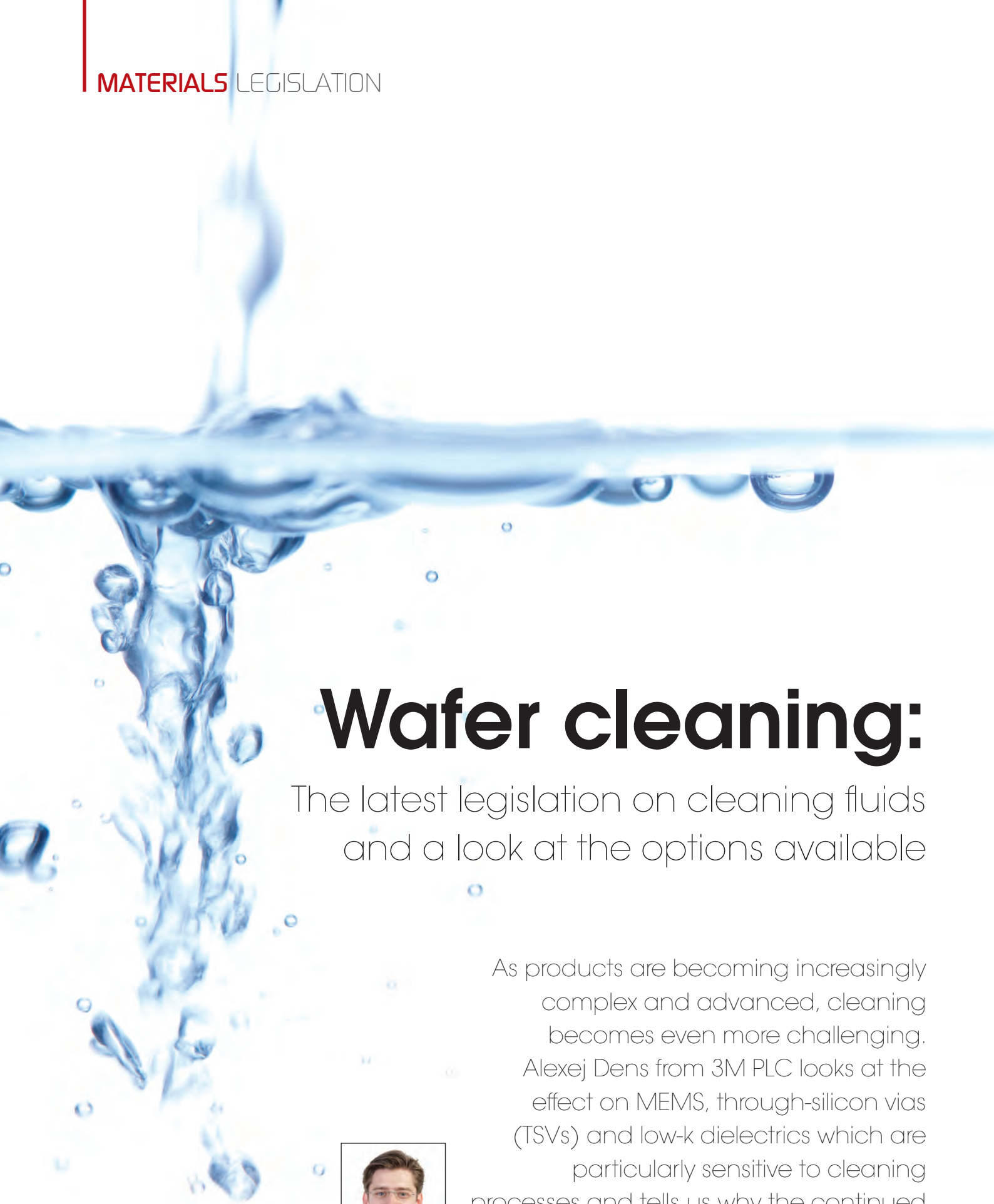

Wafer cleaning:

The latest legislation on cleaning fluids and a look at the options available

As products are becoming increasingly complex and advanced, cleaning becomes even more challenging. Alexej Dens from 3M PLC looks at the effect on MEMS, through-silicon vias (TSVs) and low-k dielectrics which are particularly sensitive to cleaning processes and tells us why the continued reduction in size components means contaminants can no longer be ignored.

IN RECENT YEARS some of the traditional precision cleaning fluids that have been widely used in the industry in the past decades have become subject to scrutiny due to their environmental sustainability, as well as health and safety properties.

The future of hydro fluorocarbons (HFCs) is in question, as part of the F-Gas Regulations (Regulation EC No 842/2006), which has a primary objective to reduce the emissions of fluorinated greenhouse gases covered by the Kyoto Protocol and thus to protect the environment. However, it's not just HFCs that are under the spotlight: Trichloroethylene (Trike) and n-Propyl Bromide (nPB), two very popular cleaning fluids, are prominent examples. The sunset date for Trike is 2016, but if users want to apply for an exception, then they must apply by the end of this year. Again, exceptions are expected to be limited and at a cost.

Similarly, nPB has been listed as a Substance of Very High Concern (SVHC) by the European Chemicals Agency (ECHA) since 2012 and is currently under further review by that organisation. The ECHA's verdict on that review is expected imminently, but further restrictions – if not an outright ban of nPB – are very possible.

nPB is already classed as 'Carcinogenic, Mutagenic or Reproductive Toxin (CMR) under the Solvent Emissions Directive 1999-13-EC (more commonly known as the SED). The SED specifies that consumption of nPB be restricted to less than one tonne per year.

While methylene chloride and perchloroethylene aree used less these days for precision cleaning, they are still in use. However, like Trike, nPB and HFCs, they are already subject to limitations under the SED: they are both classed as CMR; use is restricted to one tonne per annum; substitution is required in the shortest time; and users must comply with the emission limit of 20mg/m3.

So what are the next steps?

Clearly, for companies using these cleaning fluids, there is pressure to start looking at alternatives. While some of the target times for the implementation of restrictions may sound like a long way off, users need to allow time to thoroughly evaluate the alternatives, carry out detailed tests, and develop a business case that looks not only at performance but also at cost and future maintenance. All this can typically take many months - sometimes years - to achieve.

Fortunately, some fluids are not affected by the latest wave of legislation. So, before we look at what steps companies should take to evaluate alternatives, let's examine the main proven options that are not facing the same legislative pressures. There are really two categories of fluids, aquaeous based solutions and low toxicity solvents such as hydrofluoroethers (HFEs).

Both have low global warming potential, zero ozone depletion, no flammability and do not contain volatile organic compounds, hence they are within the bounds of any current or foreseeable legislation or guidelines from the ECHR, the SED or the F-Gas Regulations.

Both approaches have their different features and benefits. Being based on water, aqueous systems do, of course, have the advantage that the water itself is never going to be subject to legislation, although some of the detergents used to increase the solvency might. Water-detergent combinations are typically low-cost and suitable for a wide variety of cleaning machines and applications.

The downsides are that aqueous systems are by necessity larger, more complex and labour-intensive than solvent-based systems. Energy consumption is typically twice that of HFE based systems, plus large amounts of water are used, which must be processed with de-ionisation or reverse osmosis equipment prior to use. Extra cost is also associated with the disposal of contaminated waste-water.

Finally and very importantly for wafer cleaning in particular, while the quality of aqueous systems has improved, there is the substantial risk of 'spotting' or residue remaining on components.
So what do HFE-based cleaning systems have to offer? In terms of performance, they are designed to efficiently dissolve light hydrocarbons, silicon and halogenated oils and greases or any other particles prior to assembly processes. Low heat vaporisation means that drying is fast and residue free while their low surface tension makes them ideal for penetrating tight clearance in complex parts.

Any limitations?

The up-front cost of HFE fluids is more expensive than water-detergent solutions, however the cost of ownership of HFE-based systems is often comparable, because fluid consumption is typically lower (depending on the vapour containment technology) and less energy is used to run equipment.
Here are a few points to bear in mind when deciding on the fluid-equipment combination:

- **Quality of cleaning –** how efficient is removal of residue? Is a trial available?
- **Drying time –** is this within your manufacturing or assembly requirements?
- **Energy consumption –** often a hidden cost, so it is important to ask this question
- **Impact on existing equipment –** will you have to replace existing equipment, or can it be modified (or even a replacement fluid dropped in)?
- What is the anticipated level of consumption per annum?
- What about storage and waste disposal?

The latest restrictions around fluids for precision cleaning represent probably the biggest shake-up we've seen in the industry for some years. While they dos put pressure on users to seek alternatives, they also represent an opportunity to re-evaluate the latest developments in cleaning technology and to potentially take advantage of even better processes than were previously been used.

The key thing to bear in mind is that the deadlines for change are not that far away in real terms, so now is the time to start thinking about the future and act.

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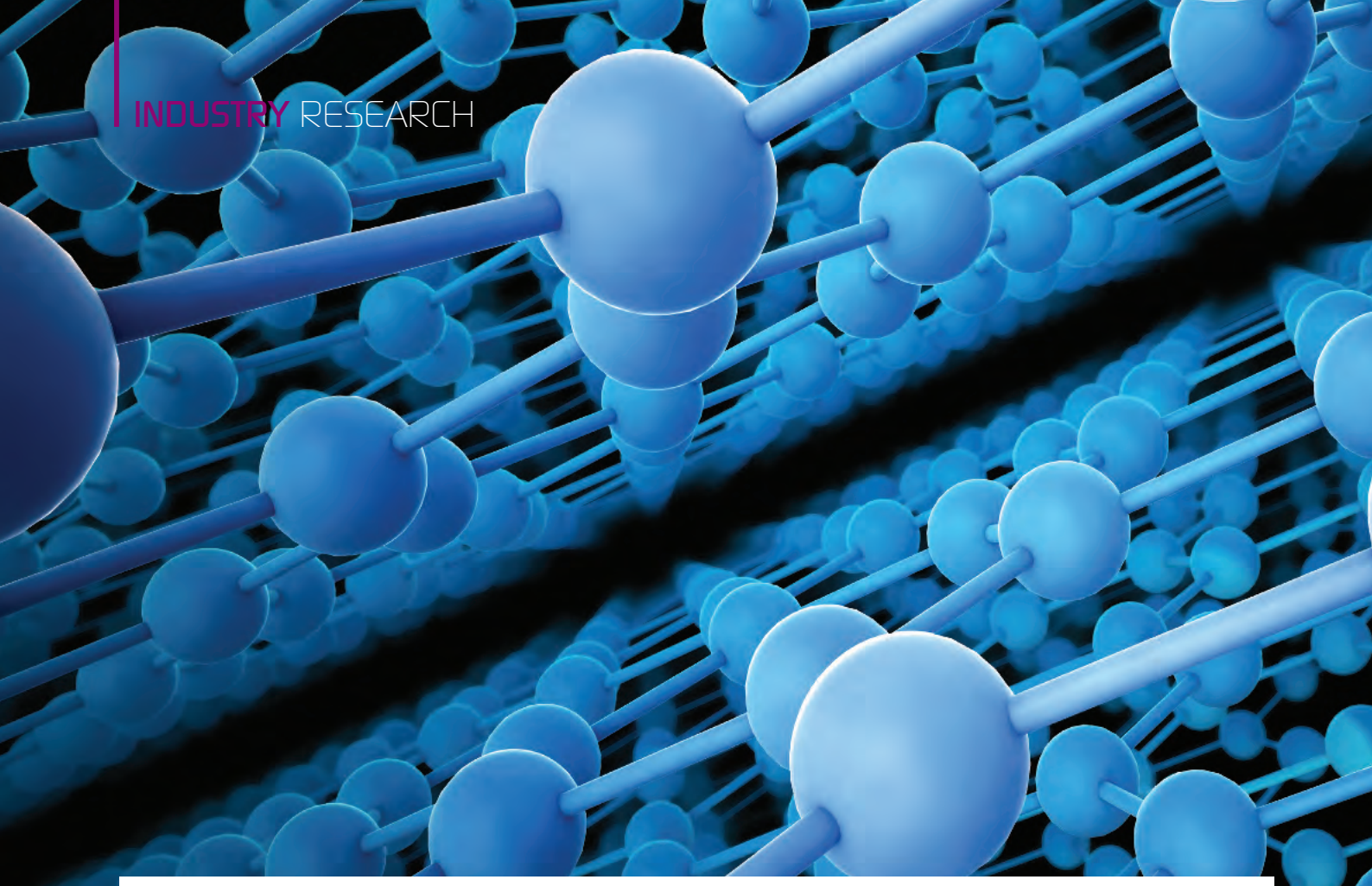


2D self-assembling material may produce transistors

RESEARCHERS around the world have been working to harness the unusual properties of graphene, a two-dimensional sheet of carbon atoms. Graphene lacks one important characteristic that would make it even more useful: a property called a bandgap, which is essential for making devices such as computer chips and solar cells.

Now, researchers at MIT and Harvard University have found a two-dimensional material whose properties are very similar to graphene, but with some distinct advantages - including the fact that this material naturally has a useable bandgap.

The research, published online in the Journal of the American Chemical Society, was carried out by MIT assistant professor of chemistry Mircea Dinc_ and seven co-authors. The new material, a combination of nickel and an organic compound called HITP, also has the advantage of self-assembly; its constituents naturally assemble themselves, a "bottom-up" approach that could lend itself to easier manufacturing and tuning of desired properties by adjusting relative amounts of the ingredients.

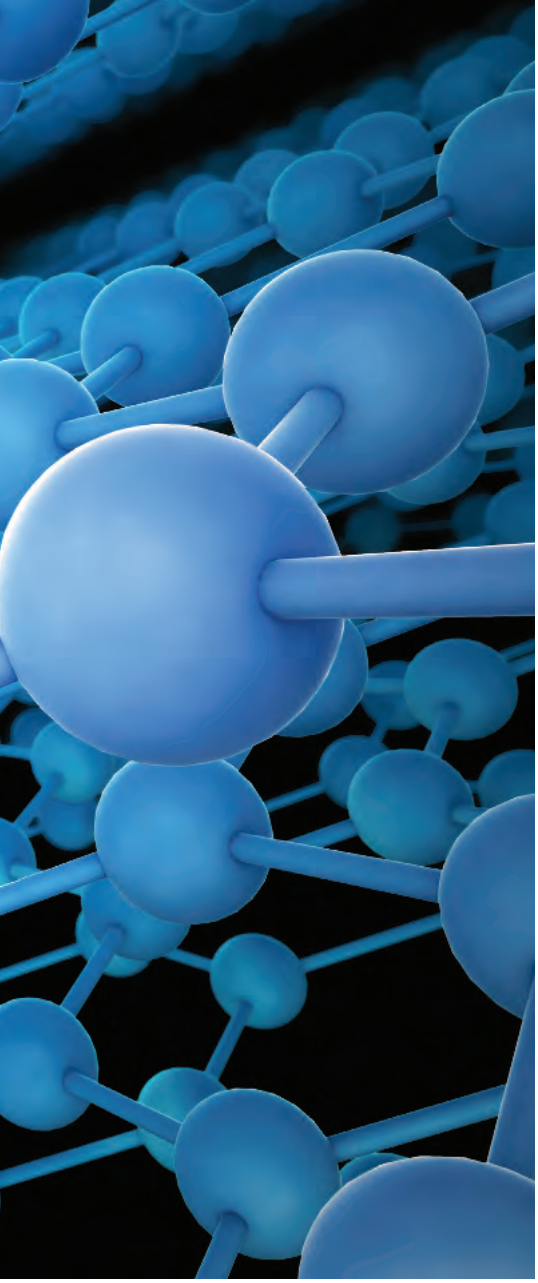
Research on such two-dimensional materials, which often possess extraordinary properties, is "all the rage these days, and for good reason," Dinc_ says.

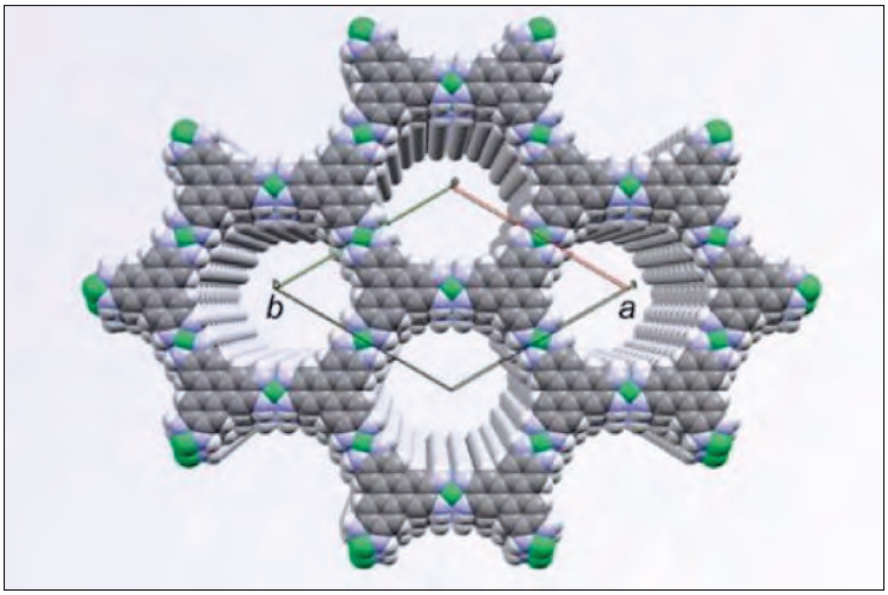
Graphene, for example, has extremely good electrical and thermal conductivity, as well as great strength. But its lack of a bandgap forces researchers to modify it for certain uses - such as by adding other molecules that attach themselves to its structure - measures that tend to degrade the properties that made the material desirable in the first place.

The new compound, Ni3(HITP)2, shares graphene's perfectly hexagonal honeycomb structure. What's more, multiple layers of the material naturally form perfectly aligned stacks, with the openings at the centres of the hexagons all of precisely the same size, about 2 nanometres across.

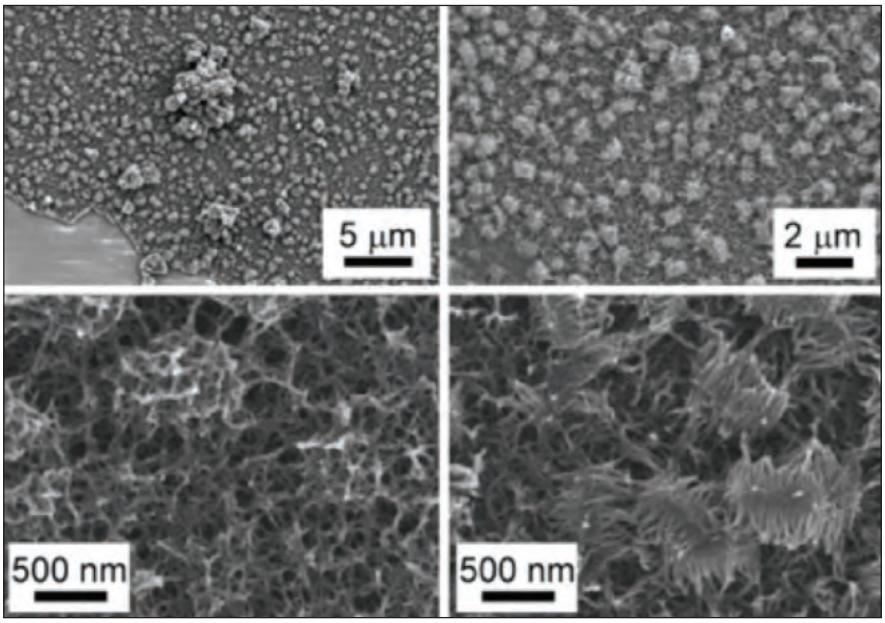
A diagram of the molecular structure is pictured at the top of this story. The new material shows how it naturally forms a hexagonal lattice structure, and its two-dimensional layers naturally arrange themselves so that the openings in the hexagons are all perfectly aligned. The image is courtesy of the researchers.

In these initial experiments, the researchers studied the material in bulk form, rather than as flat sheets; Dinc_ says that makes the current results - including excellent electrical conductivity - even more impressive, since these properties should be better yet in a 2-D version of the material. "There's every reason to believe that the properties of the particles are worse than those of a sheet," he says, "but they're still impressive."
What's more, this is just the first of what





$Ni_3(HITP)_2$ shares graphene's hexagonal honeycomb structure for flat semiconductors and has a useable bandgap



could be a diverse family of similar materials built from different metals or organic compounds. "Now we have an entire arsenal of organic synthesis and inorganic synthesis," Dinc_ says, that could be harnessed to "tune the properties, with atom-like precision and virtually infinite tuneability."

Such materials, Dinc_ explains, might ultimately lend themselves to solar cells whose ability to capture different wavelengths of light could be matched to the solar spectrum, or to improved supercapacitors, which can store electrical energy until it's needed.

In addition, the new material could lend itself to use in basic research on the properties of matter, or to the creation of exotic materials such as magnetic topological insulators, or materials that exhibit quantum Hall effects. "They're in the same class of materials that have been predicted to have exotic new electronic states," Dinc_ says. "These would be the first examples of these effects in materials made out of organic molecules. People are excited about that."

Scanning electron microscope images show the particles of Ni3(HITP)2 material at various levels of magnification. While the material in this study was in the form of nanoparticles, the analysis show that these particles are actually formed of collections of two-dimensional flakes (Image courtesy of the researchers) Pingyun Feng, at the chemistry department at the University of California at Riverside who was not involved in this work, says the approach used by this team is "novel and surprising," and that "the quality of this work, from the synthetic design strategy to the probing of the structural details and to the discovery of exceptional electrical conductivity, is outstanding." She adds that this finding "represents a major advance in the synthetic design of novel semiconducting materials."

The work was supported by the U.S. Department of Energy and the Centre for Excitonics at MIT.

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2D transistors take on silicon to speed up electronics

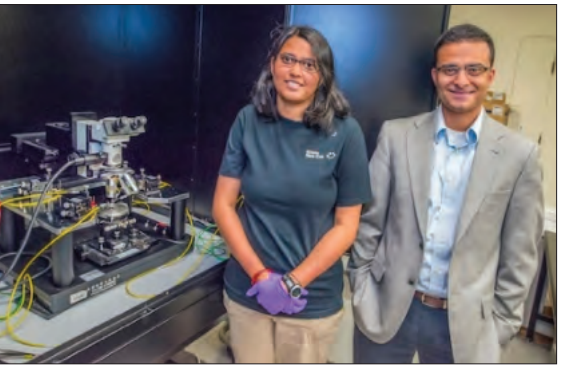
BERKELEY LAB RESEARCHERS say they have fabricated the first fully 2D field-effect transistor from layers of molybdenum disulphide, hexagonal boron nitride and graphene held together by van der Waals bonding.

Faster electronic device architectures are in the offing with the unveiling of the two-dimensional field-effect transistor (FET) by researchers with the Lawrence Berkeley National Laboratory (Berkeley Lab).

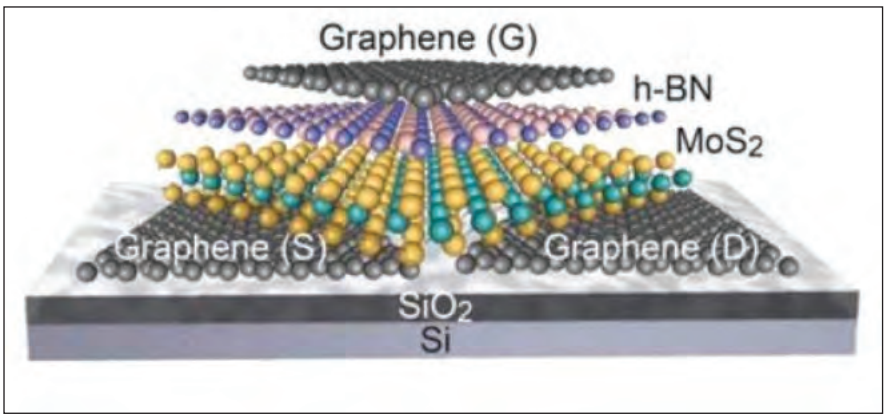
Unlike conventional FETs made from silicon, these 2D FETs suffer no performance drop-off under high voltages and provide high electron mobility, even when scaled to a monolayer in thickness.

Ali Javey, a faculty scientist in Berkeley Lab's Materials Sciences Division and a UC Berkeley professor of electrical engineering and computer science, led this research in which 2D heterostructures were fabricated from layers of a transition metal dichalcogenide, hexagonal boron nitride and graphene stacked via van der Waals interactions.

"Our work represents an important stepping stone towards the realisation of a new class of electronic devices in which interfaces based on van der Waals interactions rather than covalent bonding provide an unprecedented degree of control in material engineering and device exploration," Javey says. "The results demonstrate the promise of using an all-layered material system for future electronic applications."



Tania Roy and Ali Javey fabricated a 2D field-effect transistor that provides high electron mobility even under high voltages and scaled to a monolayer in thickness. (Photo by Roy Kaltschmidt, Berkeley Lab)



Javey is the corresponding author of a paper describing this research in ACS Nano. Co-authors are Tania Roy, Mahmut Tosun, Jeong Seuk Kang, Angada Sachid, Sujay Desai, Mark Hettick and Chenming Hu.

FETs, so-called because an electrical signal sent through one electrode creates an electrical current throughout the device, are one of the pillars of the electronics industry, ubiquitous to computers, cell phones, tablets, pads and virtually every other widely used electronic device.

All FETs are comprised of gate, source and drain electrodes connected by a channel through which a charge-carrier - either electrons or holes - flow. Mismatches between the crystal structure and atomic lattices of these individual components result in rough surfaces.

These are often with dangling chemical bonds - that degrade charge-carrier mobility, especially at high electrical fields.

"In constructing our 2D FETs so that each component is made from layered materials with van der Waals interfaces, we provide a unique device structure in which the thickness of each component is well-defined without any surface roughness, not even at the atomic level," Javey says. "The van der Waals bonding of the interfaces and the use of a multi-step transfer process present a platform for making complex devices based on crystalline layers without the constraints of lattice parameters that often limit the growth and performance of conventional hetero-junction materials."

Javey and his team fabricated their 2D FETs using the transition metal dichalcogenide molybdenum disulphide as the electron-carrying channel, hexagonal boron nitride as the gate insulator, and graphene as the source, drain and gate electrodes.

All of these constituent materials are single crystals held together by van der Waals bonding. For the 2D FETs produced in this study, mechanical exfoliation was used to create the layered components. In the future, Javey and his team will look into growing these heterogeneous layers directly on a substrate.

They will also look to scale down the thickness of individual components to a monolayer and the lengths of the channels to molecular-scale dimensions.

This work is described in detail in the paper, "Field-Effect Transistors Built from All Two-Dimensional Material Components," by Tania Roy et al in ACS Nano. DOI: 10.1021/nn501723y.

Creating nanowires three atoms wide with an electron beam

JUNHAO LIN, a Vanderbilt University Ph.D. student and visiting scientist at Oak Ridge National Laboratory (ORNL), has found a way to use a finely focused beam of electrons to create some of the smallest wires ever made.

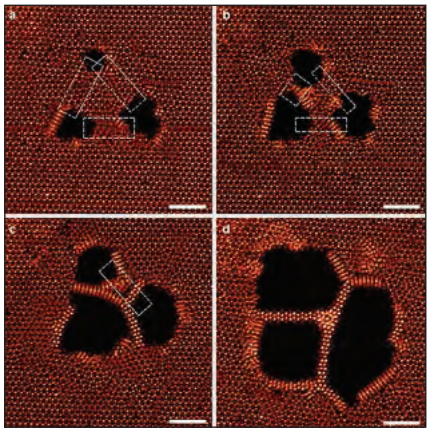
The flexible metallic wires are only three atoms wide: One thousandth the width of the microscopic wires used to connect the transistors in today's integrated circuits.

Lin's achievement is described in an article published online on April 28th in the journal Nature Nanotechnology. According to his advisor Sokrates Pantelides, University Distinguished Professor of Physics and Engineering at Vanderbilt University, and his collaborators at ORNL, the technique represents an exciting new way to manipulate matter at the nanoscale and should give a boost to efforts to create electronic circuits out of atomic monolayers, the thinnest possible form factor for solid objects.

"Junhao took this project and really ran with it," says Pantelides. Lin made the tiny wires from a special family of semiconducting materials that naturally form monolayers. These materials, called transition-metal dichalcogenides (TMDCs), are made by combining the metals molybdenum or tungsten with either sulphur or selenium.

The best-known member of the family is molybdenum disulphide, a common mineral that is used as a solid lubricant. Atomic monolayers are the object of considerable scientific interest these days because they tend to have a number of remarkable qualities, such as exceptional strength and flexibility, transparency and high electron mobility.

This interest was sparked in 2004 by the discovery of an easy way to create graphene, an atomic-scale honeycomb lattice of carbon atoms that has exhibited a number of record-breaking properties, including strength, electricity and heat conduction.



Series of still scanning electron micrographs (a to d) show how the electron beam is used to create nanowires. (Junhao Lin / Vanderbilt)
The nanowire fabrication was carried out at ORNL in the microscopy group that was headed until recently by Stephen J. Pennycook, as part of an ongoing Vanderbilt-ORNL collaboration that combines microscopy and theory to study complex materials systems. Junhao is a graduate student who pursues both theory and electron microscopy in his doctoral research.

Despite graphene's superlative properties, experts have had trouble converting them into useful devices, a process materials scientists call functionalisation. So researchers have turned to other monolayer materials like the TMDCs.

Other research groups have already created functioning transistors and Flash memory gates out of TMDC materials. So the discovery of how to make wires provides the means for interconnecting these basic elements.

Next to the transistors, wiring is one of the most important parts of an integrated circuit. Although today's integrated circuits (chips) are the size of a thumbnail, they contain more than twenty miles of copper wiring. Because this technique uses electron irradiation, it can in principle be applicable to any kind of electron-based instrument, such as electron-beam lithography.

"This will likely stimulate a huge research interest in monolayer circuit design," Lin says. "Because this technique uses electron irradiation, it can in principle be applicable to any kind of electron-based instrument, such as electron-beam lithography." One of the intriguing properties of monolayer circuitry is its toughness and flexibility.

It is too early to predict what kinds of applications it will produce, but "If you let your imagination go, you can envision tablets and television displays that are as thin as a sheet of paper that you can roll up and stuff in your pocket or purse," Pantelides comments.In addition, Lin envisions that the new technique could make it possible to create three-dimensional circuits by stacking monolayers "like Lego blocks" and using electron beams to fabricate the wires that connect the stacked layers.

His primary microscopy mentor has been ORNL Wigner Fellow Wu Zhou. "Junhao used a scanning transmission electron microscope (STEM) that is capable of focusing a beam of electrons down to a width of half an angstrom (about half the size of an atom) and aims this beam with exquisite precision," Zhou says.

The collaboration included a group headed by Kazu Suenaga at the National Institute of Advanced Industrial Science and Technology in Tsukuba, Japan, where the electrical measurements that confirmed the theoretical predictions were made by post-doctoral associate Ovidiu Cretu. Other collaborators at ORNL, the University of Tennessee in Knoxville, Vanderbilt University, and Fisk University contributed to the project.

Primary funding for the research was provided by the Department of Energy's Office of Science grant DE-FG02-09ER46554 and by the ORNL Wigner Fellowship. The work was carried at the ORNL Centre for Nanophase Materials Science user facility. Computations were done at the National Energy Research Scientific Computer Centre.

Domain walls in nanowires enhance data storage

RESEARCHERS at Johannes Gutenberg University Mainz (JGU) say they have achieved a breakthrough in the development of methods of information processing in nanomagnets.

Using a new trick, they have been able to induce synchronous motion of the domain walls in a ferromagnetic nanowire. This involved applying a pulsed magnetic field that was perpendicular to the plane of the domain walls. “This is a radically new solution,” explains Mathias KlŠui of the Institute of Physics of Johannes Gutenberg University Mainz.

“It enables us to move domain walls synchronously over a relatively large distance without them returning to their original position.” This is essential for permanent data storage, because data would otherwise be lost if domain walls were not collectively displaced in a controlled manner.

The research was carried out in cooperation with the working groups of Stefan Eisebitt at TU Berlin and Gisela SchŸtz of the Max Planck Institute for Intelligent Systems in Stuttgart. The results were published in the journal Nature Communications at the end of March. Magnetic nanowires have small regions of uniform magnetisation called domains, which can be used as storage units (bits).

The site where domains of different alignment meet each other is called a domain wall. Information can be stored in the domain, and read and processed by means of the movement of the domain walls.

The method has the great advantage that the information - as in the case of magnetic data storage in general - cannot be easily lost. This contrasts with semiconductor-based storage systems, such as RAM in PCs, which lose all stored information without power. In addition, no fragile moving parts are required such as the read/write head of a hard disk. It has not previously proved possible to induce the required controlled and synchronised movement of multiple domain walls using magnetic fields. The most obvious approach would be to apply a magnetic field in the direction in which the magnetisation runs in the tiny nanowires.

However, this has been shown to be ineffective, as there is loss of data. Mathias KlŠui and his group took a radically new path. They decided to apply a pulsed magnetic field perpendicularly to the in-plane magnetised domain walls.

As the Mainz researchers found in their model system, it is possible to customise the asymmetric field pulses that provide the forward- and backward-oriented forces that act on domain walls. Data can thus be moved within the storage medium in a controlled manner.

The participating physicists at Mainz University first tried out their concept in the context of micromagnetic simulations and then tested it experimentally.

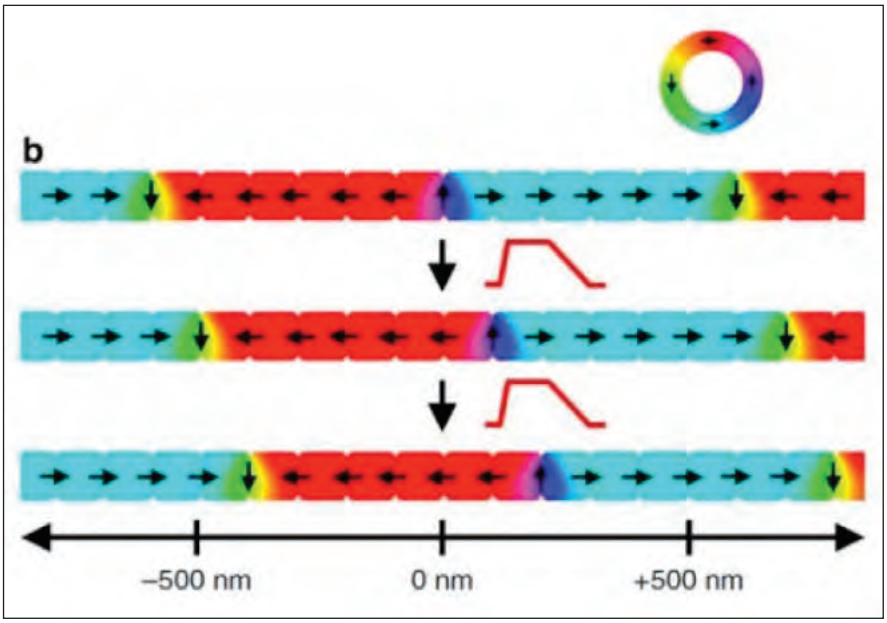
For this purpose, they recorded images of the magnetic arrangement in the tiny nanowires with the help of the electron storage ring BESSY II of the Helmholtz Centre Berlin for Materials and Energy (HZB). As expected from the simulation, they observed displacement of the domain walls in a direction that was consistent with the model.

The scientists also calculated the energy that would be necessary for the experimentally observed domain wall motion and came to the conclusion that the energy consumption of the proposed system would be quite cost-effective compared with the best components currently available.

“The results are very promising. We assume that the necessary paradigm shift will be facilitated by this new approach and it will prove possible to develop a method of efficient and controlled synchronous motion of the domain walls in nanowires,” says KlŠui.

This would pave the way for the development of non-volatile spintronic components of the next generation, which could be used in a wide range of applications for data storage as well as logic and sensor modules.

The research is documented in the paper, “Synchronous precessional motion of multiple domain walls in a ferromagnetic nanowire by perpendicular field pulses,” by Kim, J.-S. et al in Nature Communications, 5:3429. DOI:10.1038/ncomms4429



The image at the foot of this story is an illustration of synchronous displacement of several domain walls over larger distances by means of customised perpendicular field pulses. (Credit : KlŠui-Lab, Institute of Physics).

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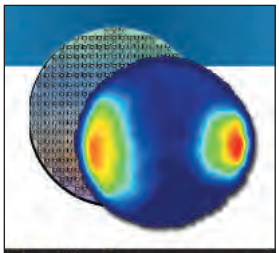
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