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executiveview

by Bertrand Loy, CEO, Entegris, Inc

Acquisition brings broader solutions for solving difficult challenges in semiconductor and electronics manufacturing

LAST YEAR, Entegris, Inc. completed its acquisition of ATMI, Inc., bringing together two industry-leading companies with complementary technologies; Entegris is a provider of a wide range of products for purifying, protecting and transporting critical materials used in processing and manufacturing in semiconductor and other high-tech industries, while ATMI develops and manufactures advanced materials and materials protection/delivery systems for semiconductor manufacturing. This marriage of materials expertise and handling/filtration technologies is unique to the industry and was driven by the need for innovative and integrated solutions that can solve a new wave of yield issues.

Process control and purity requirements are becoming more critical as manufacturers continue to develop increasingly complex processes to produce next-generation technologies. This applies to a variety of markets, including compound semiconductor, data storage, PV/solar and life sciences.

Solving these technical challenges is requiring new, more holistic innovations in materials science and an ability to translate these discoveries more quickly than ever before into real-world solutions.

With its increased scale and unique combination of technologies, Entegris is now well-suited to address these challenges. As a larger business, it can sustain investments in both fundamental materials science and new products and chemistries. This is evidenced by the opening this year of the i2M (Ideas to Market) Center for Advanced Materials Science in Bedford, MA. This $55 million facility is dedicated to researching, developing and manufacturing the world's most advanced filtration membranes and coatings technologies. Yet, technology innovation is only one piece of the puzzle.

The pressure of time-to-yield and the costs of downtime are leading the world's prominent manufacturers to demand more specialized technical applications support on a local level. As a combined entity, the new Entegris is continuing to invest to support its customers.

For example, Entegris has new and ongoing investments in Asia, specifically in Taiwan and Korea, for additional analytical services, product and materials development and manufacturing capabilities.

For suppliers like Entegris, investing in added capabilities is a strategic priority. Solving the next generation of yield challenges will not be easy, but now, as one of the industry's largest providers of yield-enhancing process solutions, Entegris is excited to meet these challenges and to continue making meaningful contributions to the industry.

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NXP and Freescale in $40 billion merger

NXP SEMICONDUCTORS N.V. and Freescale Semiconductor, Ltd have entered into a definitive agreement under which NXP will merge with Freescale in a transaction which values the combined enterprise at just over $40 billion. The merger creates a high performance mixed signal semiconductor industry leader, with combined revenue of greater than $10 billion. The merged entity will become the market leader in automotive semiconductor solutions and the market leader in general purpose microcontroller (MCU) products. The combined company will capitalize on the growing opportunities created by the accelerating demand for security, connectivity and processing.

"Today's announcement is a transformative step in our objective to become the industry leader in high performance mixed signal solutions. The combination of NXP and Freescale creates an industry powerhouse focused on the high growth opportunities in the Smarter World. We fully expect to continue to significantly out-grow the overall market, drive world-class profitability and generate even more cash, which taken together will maximize value for both Freescale and NXP shareholders," said Richard Clemmer, NXP Chief Executive Officer. Mr. Clemmer will continue to be the President and Chief Executive Officer of the merged company.

"We believe this merger, which combines two highly successful and complementary companies, will create significant value for Freescale's and NXP's shareholders, customers and employees. Both companies have built leadership positions and have a sharp focus on delivering superior value to customers. Our combined scale, size and global reach will position our new company to deliver sustainable above market growth. It will also serve to accelerate the strategic plans both companies have invested in, enabling us to deliver more complete solutions to customers," said Gregg Lowe, Freescale Semiconductor President and Chief Executive Officer.

The transaction is expected to be accretive to NXP non-GAAP earnings and non-GAAP free cash flow. NXP anticipates achieving cost savings of $200 million in the first full year after closing the transaction, with a clear path to $500 million of annual cost synergies. Under the terms of the agreement, Freescale shareholders will receive $6.25 in cash and 0.3521 of an NXP ordinary share for each Freescale common share held at the close of the transaction. The purchase price implies a total equity value for Freescale of approximately $11.8 billion (based on NXP's closing stock price as of February 27, 2015) and a total enterprise value of approximately $16.7 billion including Freescale's net debt.

The transaction is expected to close in the second half of calendar 2015. NXP intends to fund the transaction with $1.0 billion of cash from its balance sheet, $1.0 billion of new debt and approximately 115 million NXP ordinary shares. Post transaction, Freescale shareholders will own approximately 32 percent of the combined company.

Dale Ford, VP of IHS Technology commented "From a buy side perspective this definitely has important implications. When Renesas and NEC merged, many companies were left looking for another second source supplier, and they turned to Freescale and NXP. Now with the merger of these two companies there are pluses and minuses - first - the combined company should have greater resources to devote to support the significant pick-up of customers they took from Renesas / NEC when they went looking for another second source. But, second, the industry consolidation just became that much greater meaning there are fewer viable alternatives of major suppliers for vendors to choose from.

The new company will become the 7th largest semiconductor supplier overall based on preliminary market share data for 2014. Both companies started to outperform the overall market in the past 2 years prior to the merger announcement (2013 to 2014). Before that growth for each company was below overall market growth since 2008."

Lattice Semiconductor closes acquisition of Silicon Image

LATTICE SEMICONDUCTOR CORPORATION, a provider of programmable connectivity solutions, has announced the close of its acquisition of Silicon Image, Inc., a leading provider of wired and wireless connectivity solutions, and the results of the related tender offer.

For the first time in the semiconductor industry, a single company now combines the design flexibility and time to market benefits of FPGAs, with the highly integrated, function and cost optimization benefits of ASSPs. The all-cash acquisition, valued at approximately $606.6 million (or approximately $466.6 million on an enterprise value basis), is expected to be immediately accretive to EPS on a non-GAAP basis.

Darin G. Billerbeck, Lattice Semiconductor's President and Chief Executive Officer, said, "Today marks an exciting day for Lattice, as we close our transformative acquisition of Silicon Image. We have significantly expanded our Company's capabilities, with the addition of MHL, HDMI and 60 GHz Intellectual Property, enhanced our business prospects and financial profile, and further diversified our global customer base. We will move forward quickly in order to realize the compelling revenue and operating synergies created by our increased economies of scale.

Our team has put in place a well thought through, comprehensive consolidation plan for an efficient integration and the achievement of our targeted cost synergies. We plan to work relentlessly over the coming years to rapidly deleverage through our increased free cash flow, and to achieve the full benefits of this major acquisition for our customers, shareholders and employees."

Globalfoundries joins imec to develop RF Solutions for IOT applications

GLOBALFOUNDRIES, a provider of advanced semiconductor manufacturing technology has announced a partnership with imec, a leading nanoelectronics research center, for joint research on future radio architectures and designs for highly integrated mobile devices and IoT applications.

A key challenge for next-generation mobile devices is controlling the cost and footprint of the radio and antenna interface circuitry, which contain all of the components that process a cellular signal across the various supported frequency bands. Today, a typical mobile device must support up to 28 bands for worldwide 2G, 3G, 4G, LTE network connectivity, and more complex carrier aggregation schemes and additional frequency bands are expected for future generations.

These challenges are driving the need for an agile radio that integrates many of the separate components into one piece of silicon, including power amplifiers, antenna switches, and tuners and provides a solution which is both flexible and low cost.

Globalfoundries will closely collaborate with technical experts from imec to investigate low-power and compact high-performance agile radio solutions that will enable a broad range of radio architecture design--targeting improvements in area, performance and power consumption. Globalfoundries will also partner with imec to develop innovative ultra-low power IC design solutions leveraging Globalfoundries' CMOS technology to address the demanding requirements of tomorrow's IoT devices. Ultimately, the partnership aims to build a technology and design infrastructure that will enable future RF architectures while minimizing critical interface requirements for radio power consumption and performance.

"This collaboration expands our relationship with imec, and we're eager to leverage their R&D expertise in RF technology to accelerate time-to-volume of designs and deliver leading-edge RF technology to our customers," said Peter Rabbeni, director RF Segment Marketing at Globalfoundries . "This relationship further reflects our commitment to find RF design implementations that will efficiently extend the range of wireless communication applications without increasing the form factor or cost."

"There are advanced chip technology challenges the industry needs to address to enable a higher level of integration and lower power consumption for future wireless communication," said Harmke de Groot, senior director Perceptive Systems for the Internet of Things.

Samsung introduces 128-Gigabyte universal flash storage, for smartphones

SAMSUNG ELECTRONICS CO., LTD., a pioneer in advanced memory technology, has announced it is mass producing the industry's first 128-gigabyte (GB) ultra-fast embedded memory based on the much-anticipated Universal Flash Storage (UFS) 2.0 standard for next-generation flagship smartphones. The new embedded memory's UFS 2.0 interface is the most advanced JEDEC-compliant, next-generation flash memory storage specification in the world.

"With our mass production of ultra-fast UFS memory of the industry's highest capacity, we are making a significant contribution to enable a more advanced mobile experience for consumers," said Jee-ho Baek, Senior Vice President of Memory Marketing, Samsung Electronics.

"In the future, we will increase the proportion of high-capacity memory solutions, in leading the continued growth of the premium memory market."

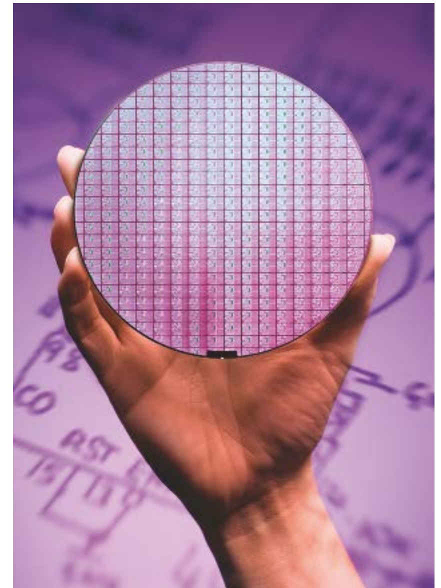
UFS memory utilizes "Command Queue," a technology that accelerates the speed of command execution in SSDs through a serial interface, significantly increasing data processing speeds compared to the 8-bit parallel-interface-based eMMC standard.

As a result, Samsung UFS memory conducts 19,000 input/output operations per second (IOPS) for random reading, which is 2.7 times faster than the most common embedded memory for high-end smartphones today, the eMMC 5.0. It also delivers a sequential read and write performance boost up to SSD levels, in addition to a 50 percent decrease in energy consumption. In addition, the random read speed is12 times faster than that of a typical high-speed memory card (which runs at 1,500 IOPS), and is expected to greatly improve system performance.

In the future, Samsung anticipates that UFS will support high-end mobile market needs, while eMMC solutions remain viable for the mid-market, value segments.

For random writing of data to storage, the blazingly fast UFS embedded memory operates at 14,000 IOPS and is 28 times as fast as a conventional external memory card, making it capable of supporting seamless Ultra HD video playback and smooth multitasking functions at the same time, enabling a much improved mobile experience. Samsung's new UFS embedded memory comes in 128GB, 64GB and 32GB versions, which are twice the capacity of its eMMC line-up, making it today's optimal memory storage solution for high-end mobile devices.

Gartner predicts 5.4 percent increase in 2015



WORLDWIDE semiconductor revenue is forecast to reach $358 billion in 2015, a 5.4 percent increase from 2014, but down from the previous quarter's forecast of 5.8 percent growth, according to Gartner Inc. The market is being driven by strong growth in application-specific standard products (ASSPs) in smartphones, along with DRAM and NAND flash in ultramobiles and solid-state drives (SSDs).

"Semiconductor revenue growth in 2015 is expected to slow from the 7.9 percent growth experienced in 2014 as DRAM returns to more traditional price reductions and the industry burns off excess holiday inventory," said Jon Erensen, research director of Gartner. "DRAM pricing was unusually firm in 2014 due to short supply, which propelled DRAM to be the fastest-growing device type in 2014 with 31.7 percent revenue growth.

DRAM supply and demand will be in line in 2015, driving bit pricing down a more traditional 16.8 percent and reducing annual DRAM revenue growth to 7.7 percent."

From an application point of view, smartphones, SSDs and ultramobiles will see the largest dollar increases. In 2015, compute applications will continue to be the largest market for semiconductors, followed by wireless and consumer applications. Combined, these three device categories represent more than two-thirds of total semiconductor revenue and have the most influence on the overall strength of the semiconductor market.

However, in 2015, the industrial electronics segment is expected to outperform overall semiconductor market growth and other electronic application categories with revenue growth of 9.1 percent. The growth will be driven mainly by LED lighting applications for industrial and residential purposes and smart city projects. In addition, the Internet of Things (IoT) will continue to drive very strong unit growth in 2015 and beyond.

Following industrial applications, wireless applications — driven mainly by mobile phones — will be the next biggest growth market for semiconductors in 2015. However, the 2015 revenue growth forecast for wireless applications, and specifically mobile phones, remains the same as the previous quarter's forecast.

"While mobile phone semiconductor sales will remain robust, driven by the accelerating shift to smartphones and 4G Long Term Evolution, there is concern that weak sell-through for other electronic equipment categories will result in higher inventory levels and drag down semiconductor sales in the first quarter of 2015," Erensen said.

Ghent University, imec and collaborators extend the spectrum of frequency comb light sources

SCIENTISTS from Ghent University and imec have joined forces with the Max Planck Institute in Garching to realise a frequency comb light source in the mid-IR wavelength band. These frequency comb light sources with an extended spectrum can be used for real-time, extremely high resolution spectroscopy, e.g. to measure the presence and concentration of gas molecules in analytes.

A frequency comb source is a light source with a spectrum containing thousands of laser lines. The development of these sources has been revolutionary for fundamental science. It has allowed the construction of a link between the optical part of the electromagnetic spectrum and the radio frequency part. As such, it has allowed researchers to determine optical frequencies with an unprecedented precision. Amongst others, frequency comb light sources have been used in optical clocks enabling precise time keeping. The enormous impact of frequency comb light sources on science was highlighted in 2005, when the Nobel Prize for physics was awarded to Prof. T. Haensch and Prof J. Hall for their work on optical frequency metrology using frequency combs.

Lately, frequency combs have been used to target more real life applications. In several experiments, it has been shown that the specific properties of the sources can be used to do fast, high-resolution spectroscopy over a broad spectrum. However, traditional comb sources are not at the right wavelength spectrum for doing spectroscopy.

Ghent University, imec, the Max Planck Institute for Quantum Optics in Garching and the Auckland University in New Zealand have developed mid-infrared frequency combs, working in the mid-infrared molecular fingerprinting region of the electromagnetic spectrum. In this wavelength region, many molecules have specific absorption bands that can be used in spectroscopy to determine the presence and concentration of these molecules in samples.

The researchers successfully realized the broad frequency combs, by combining the strong light-matter interaction in silicon with its broad transparency window. By fabricating so-called nanowire silicon photonics waveguides to confine the light in a very small area waveguide, they further enhanced the strong light-matter interaction allowing them to broaden the spectrum of the frequency combs into the mid-infrared.

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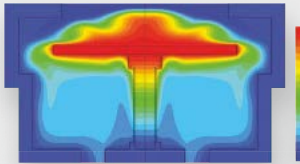

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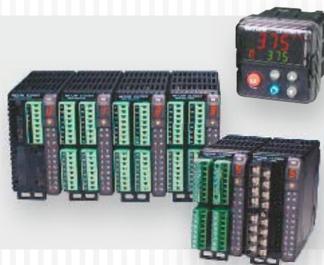

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Strong fab equipment spending expected in 2015

SEMI has announced an update of the SEMI World Fab Forecast report which updates outlooks for 2015 and 2016. The SEMI report reveals that fab equipment spending in 2014 increased almost 20 percent and will rise 15 percent in 2015, increasing only 2-4 percent in 2016. Since November 2014, SEMI has made 270 updates on its World Fab Forecast report, which tracks fab spending for construction and equipment, as well as capacity changes, and technology nodes transitions and product type changes by fab.

The SEMI World Fab Forecast and its related Fab Database reports track any equipment needed to ramp fabs, upgrade technology nodes, and expand or change wafer size, including new equipment, used equipment, or in-house equipment and spending on facilities for installation.

Fab spending, such as construction spending and equipment spending, are fractions of a company's total capital expenditure (capex). Typically, if capex shows a trend to increase, fab spending will follow. Capex for most of the large semiconductor companies is expected to increase by 8 percent in 2015, and grow another 3 percent in 2016.

These increases are driven by new fab construction projects and also ramp of new technology nodes. Spending on construction projects, which typically represents new cleanroom projects, will experience a significant -32 percent decline in 2015, but is expected to rebound by 32 percent in 2016.

Comparing regions across the world, according to SEMI, the highest fab equipment spending in 2015 will occur in Taiwan, with US$ 11.9 billion, followed by Korea with US$ 9 billion.

The region with third largest spending, the Americas, is forecast to spend about US$ 7 billion. Yet growth will decline in the Americas, by 12 percent in 2015, and decline by 12 percent in 2016 again.

Fourth in spending is China, with US$ 4.7 billion in 2015 and US$ 4.2 billion in 2016. In other regions, Japan's spending will grow by about 6 percent in 2015, to US$ 4 billion; and 2 percent in 2016, to US$ 4.2 billion. The Europe/Mideast region will see growth of about 20 percent (US$ 2.7 billion) in 2015 and over 30 percent (US$ 3.5 billion) in 2016. South East Asia is expected to grow by about 15 percent (US$ 1.3 billion) in 2015 and 70 percent (US$ 2.2 billion) in 2016.

2015 is expected to be the second consecutive year in equipment spending growth. SEMI's positive outlook for the year is based on spending trends tracked as part of our fab investment research. The "bottom's up" company-by-company and fab-by-fab approach points to strong investments by foundries and memory companies driving this year's growth.

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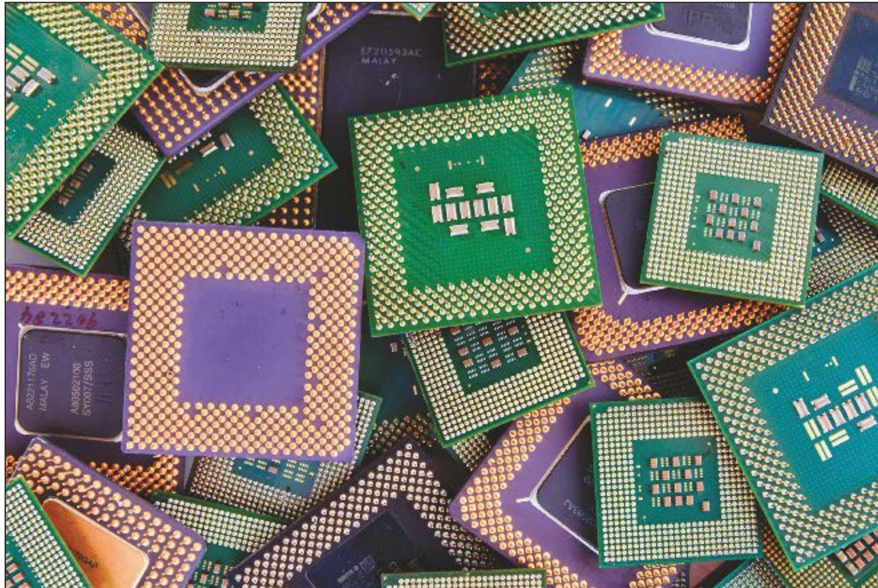
Global semiconductor industry posts record sales



THE Semiconductor Industry Association (SIA), has announced that the global semiconductor industry posted record sales totalling $335.8 billion in 2014, an increase of 9.9 percent from the 2013 total of $305.6 billion. Global sales for the month of December 2014 reached $29.1 billion, marking the strongest December on record, while December 2014 sales in the Americas increased 16 percent compared to December 2013. Fourth quarter global sales of $87.4 billion were 9.3 percent higher than the total of $79.9 billion from the fourth quarter of 2013.

Total sales for the year exceeded projections from the World Semiconductor Trade Statistics (WSTS) organization's industry forecast. All monthly sales numbers are compiled by WSTS and represent a three-month moving average.

"The global semiconductor industry posted its highest-ever sales in 2014, topping $335 billion for the first time thanks to broad and sustained growth across nearly all regions and product categories," said John Neuffer, president and CEO, Semiconductor Industry Association. "The industry now has achieved record sales in two consecutive years and is well-positioned for continued growth in 2015 and beyond."

Several semiconductor product segments stood out in 2014. Logic was the largest semiconductor category by sales, reaching $91.6 billion in 2014, a 6.6 percent increase compared to 2013. Memory ($79.2 billion) and micro-ICs ($62.1 billion) – a category that includes microprocessors – rounded out the top three segments in terms of sales revenue. Memory was the fastest growing segment, increasing 18.2 percent in 2014. Within memory, DRAM performed particularly well, increasing by 34.7 percent year-over-year. Other fast-growing product segments included power transistors, which reached $11.9 billion in sales for a 16.1 percent annual increase, discretes ($20.2 billion/10.8 percent increase), and analog ($44.4 billion/10.6 percent increase).

Annual sales increased in all four regional markets for the first time since 2010. The Americas market showed particular strength, with sales increasing by 12.7 percent in 2014. Sales were also up in Asia Pacific (11.4 percent), Europe (7.4 percent), and Japan (0.1 percent), marking the first time annual sales in Japan increased since 2010.

"The U.S. market demonstrated particular strength in 2014, posting double-digit growth to lead all regions," continued Neuffer. "With the new Congress now underway, we urge policymakers to help foster continued growth by enacting policies that promote U.S. innovation and global competitiveness."

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Cool silicon sets international standards

RESEARCH RESULTS from a collaborative project between NaMLab (TU Dresden), the Fraunhofer Institute for Photonic Micro Systems (IPMS) and GLOBALFOUNDRIES are being included in the current version of 'The International Technology Roadmap for Semiconductors', the technical guide for the semiconductor branch.

The development project was achieved at 'Cool Memory', a sub-project of Cool Silicon, the leading edge cluster for energy efficient micro-and-nanoelectronics funded by the Federal Ministry for Education and Research. Based on doped Hafniumoxide, the team has developed a cost-effective, energy-efficient ferroelectric non-volatile memory chip that requires low write voltage, can be produced at small structural width and whose production can easily be integrated in common semiconductor manufacturing processes.

Dr. Thomas Mikolajiick, Professor for Nanoelectronic Materials and Director of the NaMLab at TU Dresden, as well as the coordinator for Cool Silicon says the project's inclusion in the International Technology Roadmap is a confirmation of the success of the team's innovative work.

"For an innovation made in Dresden to become part of the International Technology Roadmap guidelines, is certainly not commonplace," Dr. Mikolajiick says. "We are very proud of this accomplishment because the roadmap is followed closely by members of the international semiconductor industry."

The new technology is a result of the Cool Silicon sub-project called 'Cool Memory', developed by participating partners searching for innovative ways to manufacture non-volatile memory.

"Typical technologies currently used for non-volatile memory are based on the principle of charge-storage," Mikolajick says. "This has several disadvantages. Writing, for instance, requires high voltage and is very energy intensive. Due to the high voltage, certain circuit parts for controlling memory cannot be reduced to desired sizes, which renders such memory inefficient for small and medium storage densities."
Therefore, the Dresden scientists rely on a different technology. They store data in ferroelectrics, a material that can be brought into two different polarization states by means of electric charge and switching requires very little energy.

"This is nothing fundamentally new," Mikolajick says. "The approach has been used since the 1950s. Up until now, the problem has been that manufacturing required complicated materials like lead zirconium titanate (PZT).

For chip manufacture, this has posed two challenges: manufacturing requires measures that are very intrusive to typical semiconductor processes; and scaling below 120 nanometers is impossible."

In order to realize the dream of a scalable and cost-effective ferroelectric memory chip, Cool Memory relies on hafnium oxide, a material which is already standard in the 28-nanometer production in the factories of project partner GLOBALFOUNDRIES where it is used as a high-k-material (high-k-dielectric). Using doping, the Dresden scientists were able to turn hafnium oxide ferroelectric and they achieved it using conventional manufacturing processes.

Now, the Saxon Leading Edge Cluster is able to produce non-volatile memory chips that enable more energy efficient writing and require lower voltage than chips currently available. They are also much easier to integrate into CMOS (Complementary Metal-Oxide-Semiconductor) processes than conventional ferroelectrics. (CMOS is a technology for constructing integrated circuits.) Doped hafnium oxide makes manufacturing at very small structural width possible.

"The fact that this innovation is being included into the ITRS shows us how large the interest is especially from the industry," Mikolajick says. "We are delighted that the work of the Leading Edge Cluster Cool Silicon has found such great international resonance."

ASE shares get a boost from Apple Watch launch

SHARES of Advanced Semiconductor Engineering Inc. (ASE), the world's largest integrated circuit packaging and testing services provider, jumped after Apple Inc. unveiled its Apple Watch. Because ASE is believed to be the sole IC packaging and testing services supplier for the Apple Watch, many expect the new device to bolster ASE's shipments, especially after the global semiconductor sector climbs out of its first quarter doldrums.

In a news conference held in San Francisco, Apple CEO Tim Cook unveiled the Apple Watch, saying that the Apple Watch is "the most personal device we have ever created."

The gadget is a miniature computer consumers can wear on their wrists, but the product requires an iPhone to be fully functional.

The Apple Watch is scheduled to go on sale on April 24 in select countries, such as the United States, Japan, Hong Kong and China, and Apple will start taking pre-orders online on April 10.

"Many market analysts expect Apple to ship about 20 million Apple Watches in the first year. Shipments could double in the second year. ASE is the sole IC packaging and testing service provider and will no doubt become one of the major beneficiaries," Hsu said.

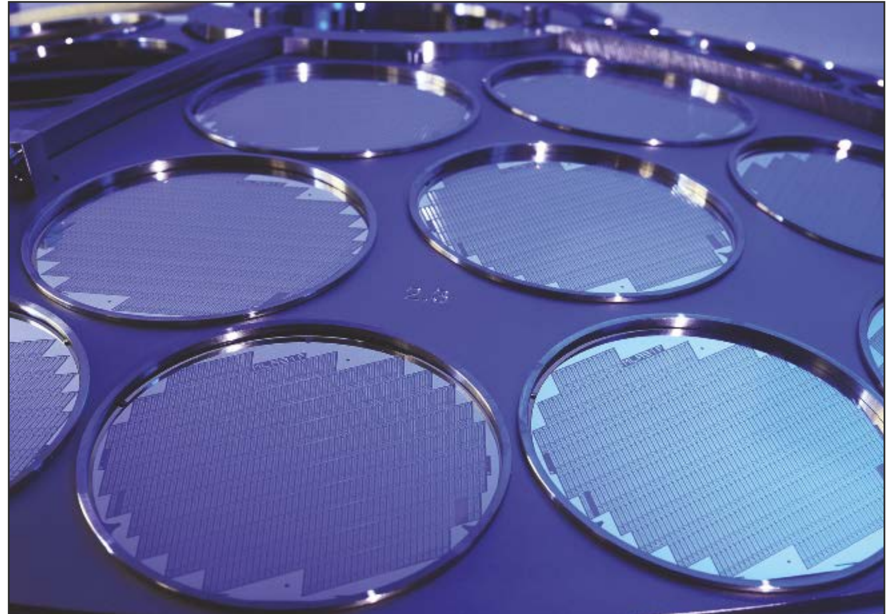
Tronics seize submicron MEMS opportunities

Tronics is capitalizing on the growing number of submicronic MEMS devices opportunities to expand its equipment and process base. Tronics has been manufacturing MEMS for 15 years with an emphasis on SOI, WLP.

Over the last 2 years, Tronics acquired advanced equipment and allocated significant resources to the development of submicron MEMS processes, which combine traditional MEMS structures and advanced Nanotechnology parts. There are a growing number of opportunities for submicronic MEMS devices in optical applications, but also in inertial and microfluidics applications.

Tronics acquired a 0.25 i-line stepper to address some of these opportunities. In the world of MEMS, this is high resolution. The stepper allows the patterning of the very small geometries necessary for many applications, such as piezoresistive inertial MEMS based on silicon nano-wires (M&NEMS), or micro mirrors for telecommunication applications. This machine is also needed to manufacture moving structures requiring very tight alignment.

Tronics also acquired equipment for nanoimprint lithography (NIL) This technique allows the creation of structures with superior resolution, as small as 50 nanometers, by embossing a resist with a stamp. This technology is cost effective for patterning large areas, once the processes have been properly developed and validated.



Tronics was one of the first European companies to bring NIL to industrial production, and is now using nanoimprint to define high-density structures on both silicon and glass substrates. With a total investment in excess of 2 million Euros in this field over the last 18 months, Tronics has demonstrated its commitment to the submicronic MEMS business. The new equipment is fully operational at Tronics and is being used for product deliveries to customers.

More than ten thousand wafers have already been processed and delivered. The range of applications requiring such tight alignment or submicronic patterns is broad and growing. Some examples are submicronic optical gratings , spectrometers, fluidic filters, piezo-resistive inertial sensors based on silicon nano-wires, micromirrors, gas sensors based on resonant silicon nano-cantilivers, and there are many others.

Pascal Langlois, CEO of the Tronics group said: "Tronics is committed to further developing the know-how required to address these opportunities, and to expanding its equipment and process portfolio. Tronics will continue to build on its solid MEMS engineering background and its ability to solve difficult MEMS manufacturing challenges, and plans to remain a leader in specialty MEMS processes."

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Nanoparticle silver ink to improve manufacturing

Genes'Ink and KELENN Technology spoke to Mark Andrews and explained how their system can improve printed electronics manufacturing.

GENES'INK and KELENN Technology recently announced co-development of a new proprietary nanoparticle silver ink for KELENN's new high speed printer, the KSCAN PE300. According to both companies, these new technologies can radically accelerate production and efficiency of printed electronics for RFID antennas, capacitors, OLED active layers and many other applications. We asked Genes'Ink and KELENN Technology to detail how their system can improve printed electronics manufacturing.

Q Speed appears a central attribute of the new KSCAN PE300, moving at 'several meters per minute' compared to only 'a few centimeters per hour' in existing systems – How do you achieve such a performance leap?

A Such performance is achieved thanks to a combination of innovations and technologies. KELENN Technology and Genes'Ink have worked together to create an industrial digital silver ink that can be used with KELENN Technology's proprietary high speed piezo jetting modules. KELENN Technology has redesigned the architecture, electronics and fluid management to be able to properly handle approximately 30 key parameters, in relation with printed electronics, such as rheology, nozzle clogging and many others.

Q Has speed been an impediment to more widespread adoption of inkjet printing of electronic circuits in the overall marketplace?

A Yes. Actually 90 percent of printed electronics is handled by screen printing. Companies are focusing on prototyping circuit design and ink formulation with low speed table top inkjet printers. However, the whole work has to be done once again when moving into industrial production scale. For the industry, before the KSCAN PE300 was announced, it was safer to put the emphasis on screen printing for production.

Q The partnership between Genes' Ink and KELENN Technology seems a natural outgrowth of a conductive ink maker working with a developer of improved electronic circuit printing technology – How do (ink and printer) complement one another to offer a better solution?

A To be able to print at fast speed, the volume of ink per droplets must be reduced compared to traditional methods. This matches perfectly with nanoparticle silver

ink, which requires less quantities for a given conductivity compared to traditional silver ink. From a consumable cost point of view, KELENN Technology's printer (uses) less ink for a given conductivity compared to screen printing. So the customer benefits from two major cost areas: improved productivity and reduced consumable costs.

Q Genes'Ink cites several applications of the new technology – active layers in OLEDs, RFID antennas, production capacitor printing. Can the technology also be used for printing the silver bus bars, lattice fingers or other elements in photovoltaic cells (printing on polysilicon wafers)?

A Yes, for example, in a very interesting case study, we have demonstrated that one litre of ink could produce approximately 1 million patterns.

Q Line accuracy seems another advantage of the new technology – Is this a benefit of the new nanoparticle ink, the printer itself, or both?

A Both technologies bring their advantages. The Nano ink specific formulation can be jetted very precisely. The printer has a native resolution of 1200 dpi with a positioning precision of the print head of up to 2 μm. But mostly, the precision is due to a number of innovations in the design of inkjet deposition that are brought to the market by KELENN Technology.

Q Ink silver content reduction (50 percent less) in your new system is another clear advantage – Can you elaborate about what enables the new printer and ink to use so much less silver?

A The (ink) formulation is a key feature. Nanoparticles of silver have the ability to coalescence and show conductivity with a very limited amount of ink and at low temperature. Reliability of inkjet deposition is a key feature as well; we are looking for a first pass yield of 95 percent. The quantity of ink waste per job has been greatly reduced by KELENN Technology compared to screen printing or other inkjet (systems).

Q The new technology mentions usage of photonic annealing in a controlled environment with a specialised atmosphere – Is the vacuum system and gas supply control self-contained, or does the manufacturer need to have out-board vacuum and gas delivery/evacuation?

A Yes, the whole technical environment is self-contained to facilitate installation and commissioning. The KSCAN PE300 is fitted with carbon filters for exhaust. In basic configurations, these filters can cope with small to medium productions. For volume production, or a more complex configuration, it is best to add external filters and output.

Q What have we not covered that is an additional benefit of the new system?

A A software package is included with the KSCAN PE300 to manage job productions; it interfaces with standard CAD electronics output vector files such as GERBER and simple image files such as TIFF, BMP and JPG. The KSCAN PE300 can also be fitted with a feeder and a stacker.

Q Do you believe the new system (ink + printer) offer decisive advantages?

A This system is opening the printed electronics market to industrial printers, not only electronics people. It is easy to use and they already use this kind of system in their plants.

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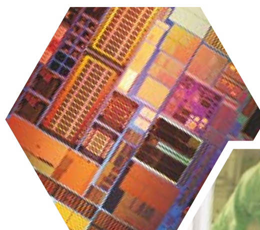

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A new step towards using graphene in electronic applications

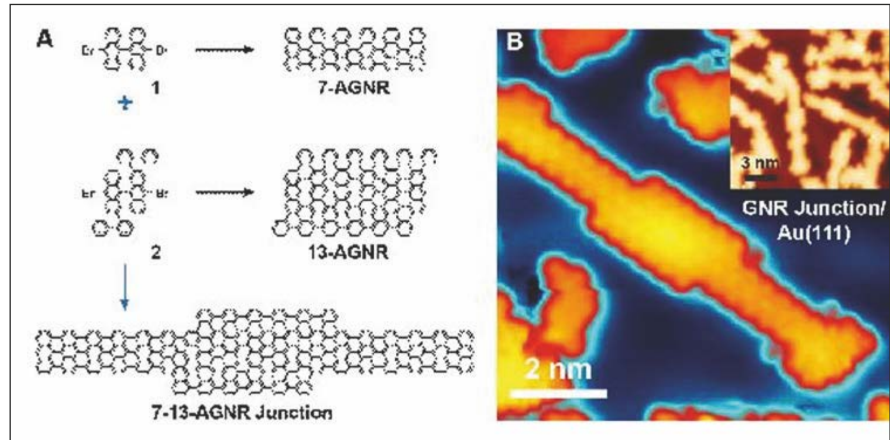
A team at the University of Berkeley and the Centre for Materials Physics (CSIC-UPV/EHU) has managed, with atomic precision, to create nanostructures combining graphene ribbons of varying widths

FEW MATERIALS have received as much attention from the scientific world or have raised so many hopes with a view to their potential deployment in new applications as graphene has. This is largely due to its superlative properties: it is the thinnest material in existence, almost transparent, the strongest, the stiffest and at the same time the most strechable, the best thermal conductor, the one with the highest intrinsic charge carrier mobility, plus many more fascinating features.

Specifically, its electronic properties can vary enormously through its confinement inside nanostructured systems, for example. That is why ribbons or rows of graphene with nanometric widths are emerging as tremendously interesting electronic components. On the other hand, due to the great variability of electronic properties upon minimal changes in the structure of these nanoribbons, exact control on an atomic level is an indispensable requirement to make the most of all their potential. The lithographic techniques used in conventional nanotechnology do not yet have such resolution and precision.

In the year 2010, however, a way was found to synthesise nanoribbons with atomic precision by means of the so-called molecular self-assembly. Molecules designed for this purpose are deposited onto a surface in such a way that they react with each other and give rise to perfectly specified graphene nanoribbons by means of a highly reproducible process and without any other external mediation than heating to the required temperature.

In 2013 a team of scientists from the University of Berkeley and the Centre for Materials Physics (CFM), a mixed CSIC (Spanish National Research Council) and UPV/EHU (University of the Basque Country) centre, extended this very concept to new molecules that were forming wider graphene nanoribbons and therefore with new electronic properties.



This same group has now managed to go a step further by creating, through this self-assembly, heterostructures that blend segments of graphene nanoribbons of two different widths.

The forming of heterostructures with different materials has been a concept widely used in electronic engineering and has enabled huge advances to be made in conventional electronics. "We have now managed for the first time to form heterostructures of graphene nanoribbons modulating their width on a molecular level with atomic precision.

What is more, their subsequent characterisation by means of scanning tunnelling microscopy and spectroscopy, complemented with first principles theoretical calculations, has shown that it gives rise to a system with very interesting electronic properties which include, for example, the creation of what are known as quantum wells," pointed out the scientist Dimas de Oteyza, who has participated in this project.

This work, the results of which are published in the journal Nature Nanotechnology, therefore constitutes a significant success towards the desired deployment of graphene in commercial electronic applications.

Dr Dimas G. de Oteyza, who was previously at Berkeley and at the CFM, is currently working at the Donostia International Physics Center (DIPC) as a Fellow Gipuzkoa.

The Fellows Gipuzkoa programme, funded by the Chartered Provincial Council of Gipuzkoa, is in fact devoted to bringing back young researchers with solid post-doctoral training in internationally prestigious groups and centres, by offering them a platform for reincorporation through contracts with a duration of up to five years, which enables them to compete in the best of conditions to obtain tenured positions as researchers in our country.

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Bibliographical reference
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Breakthrough promises

secure communications and faster computers

Scientists develop microscopic component small enough to fit onto a standard silicon chip that can generate a continuous supply of entangled photons.

UNLIKE BILBO'S MAGIC RING, which entangles human hearts, engineers have created a new micro-ring that entangles individual particles of light, an important first step in a whole host of new technologies.

Entanglement - the instantaneous connection between two particles no matter their distance apart - is one of the most intriguing and promising phenomena in all of physics. Properly harnessed, entangled photons could revolutionize computing, communications, and cyber security.

Though readily created in the lab and by comparatively large-scale optoelectronic components, a practical source of entangled photons that can fit onto an ordinary computer chip has been elusive. New research, reported in The Optical Society's (OSA) new journal Optica, describes how a team of scientists has developed, for the first time, a microscopic component that is small enough to fit onto a standard silicon chip that can generate a continuous supply of entangled photons.

The new design is based on an established silicon technology known as a micro-ring resonator. These resonators are actually loops that are etched onto silicon wafers that can corral and then reemit particles of light. By tailoring the design of this resonator, the researchers created a novel source of entangled photons that is incredibly small and highly efficient, making it an ideal on-chip component.

"The main advantage of our new source is that it is at the same time small, bright, and silicon based," said Daniele Bajoni, a researcher at the Università degli Studi di Pavia in Italy and co-author on the paper. "The diameter of the ring resonator is a mere 20 microns, which is about one-tenth of the width of a human hair. Previous sources were hundreds of times larger than the one we developed."

From Entanglement to Innovation

Scientists and engineers have long recognized the enormous practical potential of entangled photons. This curious manifestation of quantum physics, which Einstein referred to as "spooky action at a distance," has two important implications in real-world technology.

First, if something acts on one of the entangled photons then the other one will respond to that action instantly, even if it is on the opposite side of a computer chip or even the opposite side of the Galaxy. This behaviour could be harnessed to increase the power and speed of computations. The second implication is that the two photons can be considered to be, in some sense, a single entity, which would allow for new communication protocols that are immune to spying.

This seemingly impossible behaviour is essential, therefore, for the development of certain next-generation technologies, such as computers that are vastly more powerful than even today's most advanced supercomputers, and secure telecommunications.

Creating Entanglement on a Chip

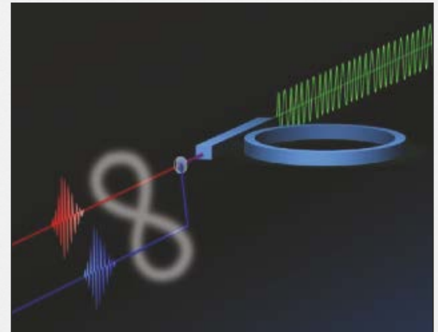
To bring these new technologies to fruition, however, requires a new class of entangled photon emitters: ones that can be readily incorporated into existing silicon chip technologies. Achieving this goal has been very challenging.

To date, entangled photon emitters - which are principally made from specially designed crystals -- could be scaled down to only a few millimetres in size, which is still many orders of magnitude too large for on-chip applications. In addition, these emitters require a great deal of power, which is a valuable commodity in telecommunications and computing.

To overcome these challenges, the researchers explored the potential of ring resonators as a new source for entangled photons. These well-established optoelectronic components can be easily etched onto a silicon wafer in the same manner that other components on semiconductor chips are fashioned. To "pump," or power, the resonator, a laser beam is directed along an optical fiber to the input side of the sample, and then coupled to the resonator where the photons race around the ring. This creates an ideal environment for the photons to mingle and become entangled.

As photons exited the resonator, the researchers were able to observe that a remarkably high percentage of them exhibited the telltale characteristics of entanglement.

"Our device is capable of emitting light with striking quantum mechanical properties never observed in an



Drawing of the silicon ring resonator with its access waveguide. The green wave at the input represents the laser pump, the red and blue wavepackets at the output represent the generated photon pairs, and the infinity symbol linking the two outputs indicates the entanglement between the pair of photons.

integrated source," said Bajoni. "The rate at which the entangled photons are generated is unprecedented for a silicon integrated source, and comparable with that available from bulk crystals that must be pumped by very strong lasers."

Applications and future technology

The researchers believe their work is particularly relevant because it demonstrates, for the first time, a quintessential quantum effect, entanglement, in a well-established technology.

"In the last few years, silicon integrated devices have been developed to filter and route light, mainly for telecommunication applications," observed Bajoni. "Our micro-ring resonators can be readily used alongside these devices, moving us toward the ability to fully harness entanglement on a chip." As a result, this research could facilitate the adoption of quantum information technologies, particularly quantum cryptography protocols, which would ensure secure communications in ways that classical cryptography protocols cannot. According to Bajoni and his colleagues,

Further reading

Paper: D. Grassani, S. Azzini, M. Liscidini, M. Galli, M. J. Strain, M. Sorel, J. E. Sipe, and D. Bajoni, "A micrometer-scale integrated silicon source of time-energy entangled photons," Optica, 2, 1, 88-94 (2015) doi: http://dx.doi.org/10.1364/OPTICA.2.000088

New solder

for semiconductors creates technological possibilities

Scientists have demonstrated how semiconductors can be soldered and still deliver good electronic performance.

A RESEARCH TEAM led by the University of Chicago's Dmitri Talapin has demonstrated how semiconductors can be soldered and still deliver good electronic performance.

"We worked out new chemistry for a broad class of compositions relevant to technologically important semiconductors," said Talapin, a professor in chemistry.

Semiconductors sit at the heart of most electronics. From computer chips to solar cells, these materials conduct electricity and make it possible to generate and control electrical current. The compounds that Talapin and his associates have developed can be used to join pieces of semiconductor. Researchers and engineers have long struggled with joining together semiconducting surfaces, which are very sensitive to impurities and structural defects.

"If you put two pieces of semiconductor next to each other, each joint will be unique and in most cases will block transport of charges," Talapin said. "You will not be able to make a reasonably good electronic circuit by simply taking different semiconductor pieces and pressing them against each other as you could do with metals."

Talapin and his associates from UChicago, Argonne National Laboratory, and the Illinois Institute of Technology published their findings in the Jan. 23, 2014, issue of Science. They have developed compounds of cadmium, lead, and bismuth that can be applied as a liquid or paste to join two pieces of a semiconductor by heating them to several hundred degrees Celsius, which is mild by industry standards.
"Our paste or our liquid converts cleanly into a material that will be compositionally matched to the bonded parts, and that required development of new chemistry," Talapin said. "We had to design special molecules that fulfill this requirement so that they do not contaminate the material." After application as a liquid or paste, they decompose to form a seamless joint.

Diverse applications

"Dr. Talapin's work is exciting because its applications are so diverse," said Eric Ginsburg, assistant director at UChicagoTech, the University's Center for Technology Development and Ventures. "We expect it to be used soon by manufacturers who need to join semiconductor parts, but it could also create new markets in the growing semiconductor industry. For example, it would enable 3-D printing of semiconductors and create possibilities for new technologies."

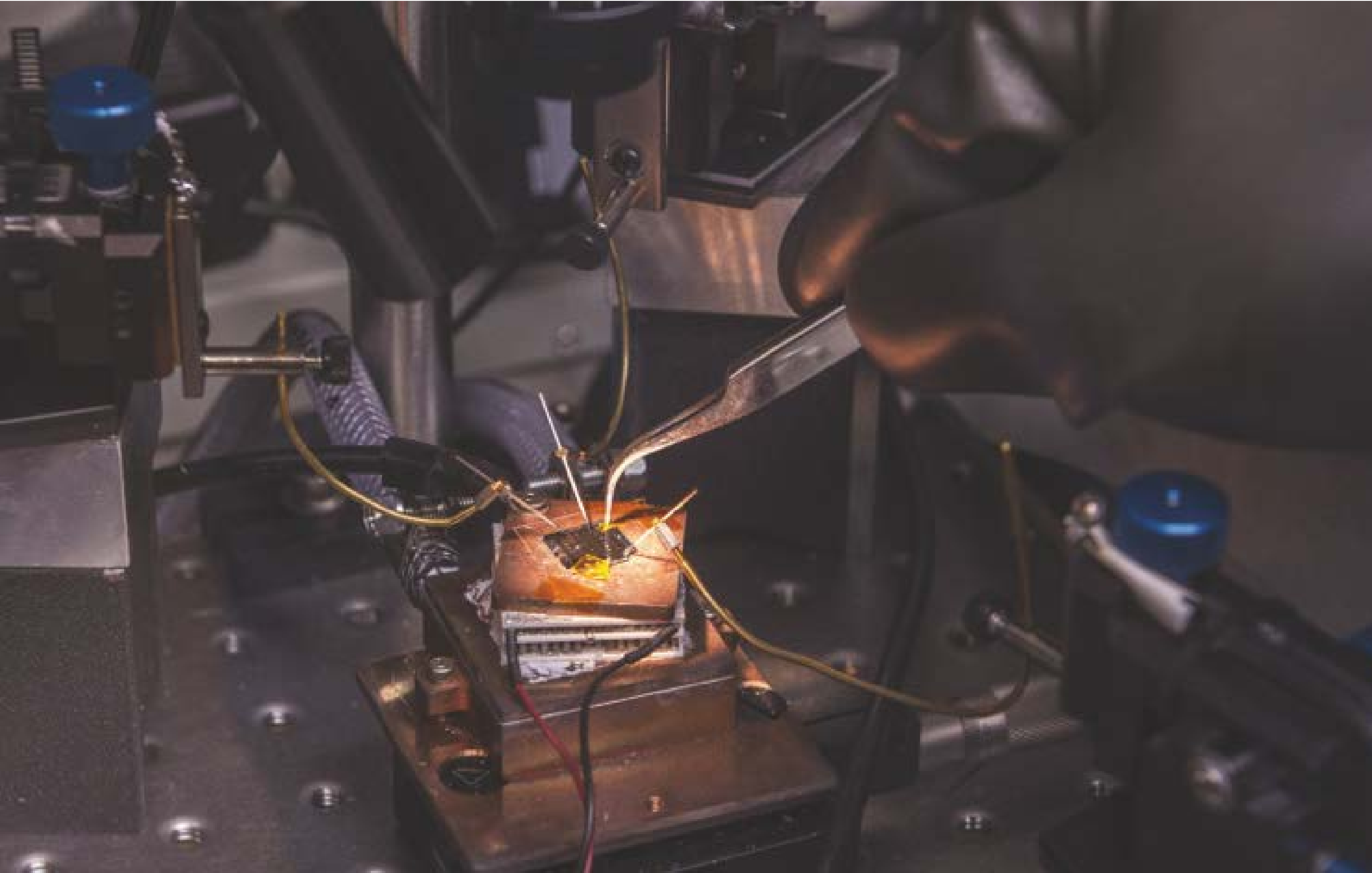
Ginsburg and Cristianne Frazer, UChicagoTech project manager, have previously helped Talapin to license his technologies. They are working closely with Talapin, industry contacts, and investors to determine a strategy for developing the new solder material.

Use of the U.S. Department of Energy's Advanced Photon Source at Argonne was critical to the project's success. "The classical, top-down manufacturing process in the silicon industry does not require soldering," Talapin said. Instead, industry engineers make a large silicon crystal, then cut, carve and etch it into the desired shapes.

Semiconductor soldering is unlikely to have a major impact on today's mainstream silicon technology, but could lead to the development of less expensive, solution-processed semiconductors needed for entry into new markets. Among these markets are printable electronics, 3-D printing, flat panel display manufacturing solar cells and thermoelectric heat-to electricity generators for the Internet of Things (IoT).

Printable electronics requires assembly of semiconductors from small pieces, putting tiny grains together like Legos. "It's like what people call additive manufacturing, when you add things and build from pieces," Talapin said. "If you want to assemble pieces, you need a solder or glue or connectors."

3-D printing is an exponentially growing market, Talapin noted. "We can 3-D print, to my knowledge, almost any class of materials, but not semiconductors." His new solder may change that.
A tiny transistor operates each pixel in current-generation flat-screen televisions. These transistors currently



Semiconductor devices like this one now can be joined electronically with a new solder developed by chemistry Professor Dmitri Talapin's research group at the University of Chicago. Credit: Rob Kozloff, University of Chicago.

are manufactured via vacuum methods, but industry experts expect that to change to printing and other less expensive solution-based manufacturing techniques.

Internet of Things

The Internet of Things is a growing network of everyday objects -- traffic lights and cars, for example -- that can communicate automatically via miniature web servers. Tiny sensors will be integrated in buildings and bridges to immediately report a crack or other structure failure. Semiconductors will be needed to convert sunlight or heat to electrical currents used to receive, process and transmit information within such a network.

"That requires very inexpensive semiconductors for electronic circuits and devices that come essentially at the price of a postage stamp," Talapin said. Printing electronics in a way similar to printing postage stamps. It is a chemistry problem to find the right "inks" for this purpose, he said. "Right now postcards and magazines are simply colourful, but there's nothing that precludes them from being colourful and electronically active, so that as ink dries it forms a film that can conduct charges. It's not sci-fi these days."

Solar cells also represent an increasingly lucrative, highly competitive, multibillion-dollar annual market, one that fuels the quest for improved solution-process manufacturing methods for semiconductors.

"Solution-processed semiconductors is a huge field. We definitely have hundreds of competitors, both in academic settings and in companies," Talapin said. "It's a very competitive area because it's now on the final approach to big money." The Science article mentioned in passing that their semiconductor soldering approach set a new record for electron mobility in solution-processed semiconductors, a measure for how quickly electrons move through the materials. The new record is almost 10 times faster than the old one. "It's mind-blowing," Talapin said.

Funding: II-VI Foundation, Department of Energy, National Science Foundation, and the Keck Foundation.

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Further reading

D. S. Dolzhnikov, H. Zhang, J. Jang, J. S. Son, M. G. Panthani, T. Shibata, S. Chattopadhyay, D. V. Talapin. Composition-matched molecular "solders" for semiconductors. Science, 2015; 347 (6220): 425 DOI: 10.1126/science.1260501

Laser-induced graphene **'super'** for electronics

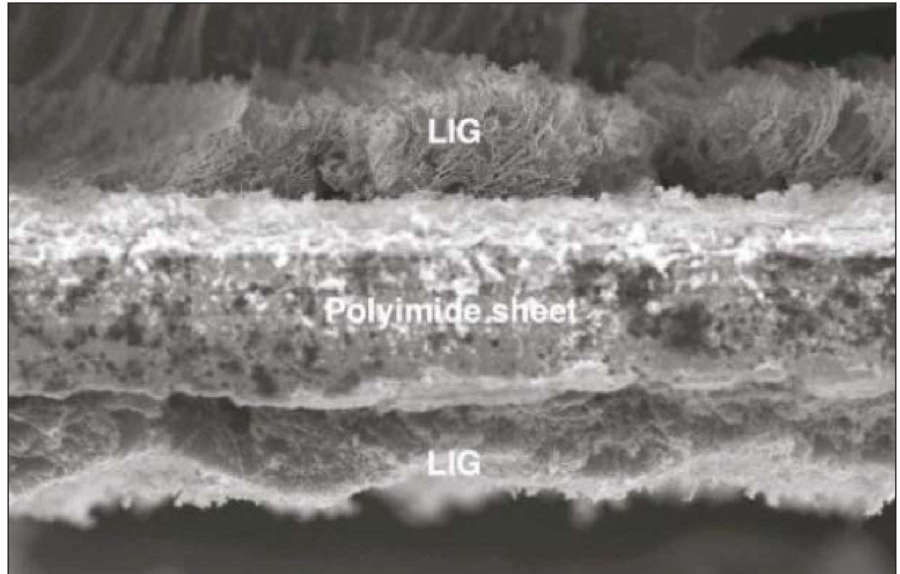
Rice University scientists advanced their recent development of laser-induced graphene (LIG) by producing and testing stacked, three-dimensional supercapacitors, energy-storage devices that are important for portable, flexible electronics.

THE RICE LAB of chemist James Tour discovered last year that firing a laser at an inexpensive polymer burned off other elements and left a film of porous graphene, the much-studied atom-thick lattice of carbon. The researchers viewed the porous, conductive material as a perfect electrode for supercapacitors or electronic circuits.

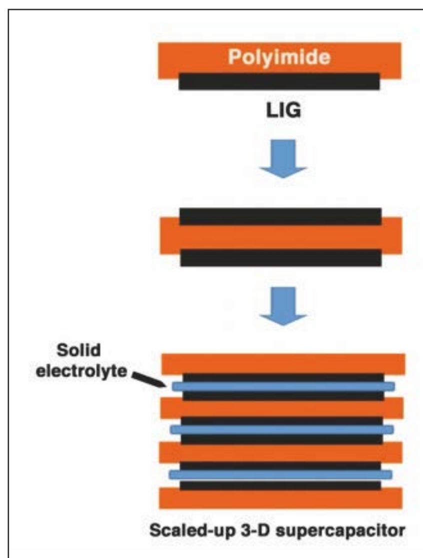
An electron microscope image shows the cross section of laser-induced graphene burned into both sides of a polyimide substrate. The flexible material created at Rice University has the potential for use in electronics or for energy storage.

To prove it, members of the Tour group have since extended their work to make vertically aligned supercapacitors with laser-induced graphene on both sides of a polymer sheet. The sections are then stacked with solid electrolytes in between for a multilayer sandwich with multiple microsupercapacitors.

The flexible stacks show excellent energy-storage capacity and power potential and can be scaled up for commercial applications. LIG can be made in air at ambient temperature, perhaps in industrial quantities through roll-to-roll processes, Tour said. The research was reported in Applied Materials and Interfaces.



An electron microscope image shows the cross section of laser-induced graphene burned into both sides of a polyimide substrate. The flexible material created at Rice University has the potential for use in electronics or for energy storage. Credit: Tour Group/Rice University. Courtesy of the Tour Group.



A schematic shows the process developed by Rice University scientists to make vertical microsupercapacitors with laser-induced graphene. The flexible devices show potential for use in wearable and next-generation electronics. Credit: Tour Group/Rice University

Capacitors use an electrostatic charge to store energy they can release quickly, to a camera's flash, for example. Unlike chemical-based rechargeable batteries, capacitors charge fast and release all their energy at once when triggered. But chemical batteries hold far more energy. Supercapacitors combine useful qualities of both -- the fast charge/discharge of capacitors and high-energy capacity of batteries -- into one package.

LIG supercapacitors appear able to do all that with the added benefits of flexibility and scalability. The flexibility ensures they can easily conform to varied packages -- they can be rolled within a cylinder, for instance -- without giving up any of the device's performance.

"What we've made are comparable to microsupercapacitors being commercialized now, but our ability to put devices into a 3-D configuration allows us to pack a lot of them into a very small area," Tour said. "We simply stack them up.

"The other key is that we're doing this very simply. Nothing about the process requires a clean room. It's done on a commercial laser system, as found in routine machine shops, in the open air." Ripples, wrinkles and sub-10-nanometer pores in the surface and atomic-level imperfections give LIG its ability to store a lot of energy. But the graphene retains its ability to move electrons quickly and gives it the quick charge-and-release characteristics of a supercapacitor. In testing, the researchers charged and discharged the devices for thousands of cycles with almost no loss of capacitance.

To show how well their supercapacitors scale up for applications, the researchers wired pairs of each variety of device in serial and parallel. As expected, they found the serial devices delivered double the working voltage, while the parallels doubled the discharge time at the same current density. The vertical supercapacitors showed almost no change in electrical performance when flexed, even after 8,000 bending cycles.

Tour said that while thin-film lithium ion batteries are able to store more energy, LIG supercapacitors of the same size offer three times the performance in power (the speed at which energy flows). And the LIG devices can easily scale up for increased capacity.

"We've demonstrated that these are going to be excellent components of the flexible electronics that will soon be embedded in clothing and consumer goods," he said.

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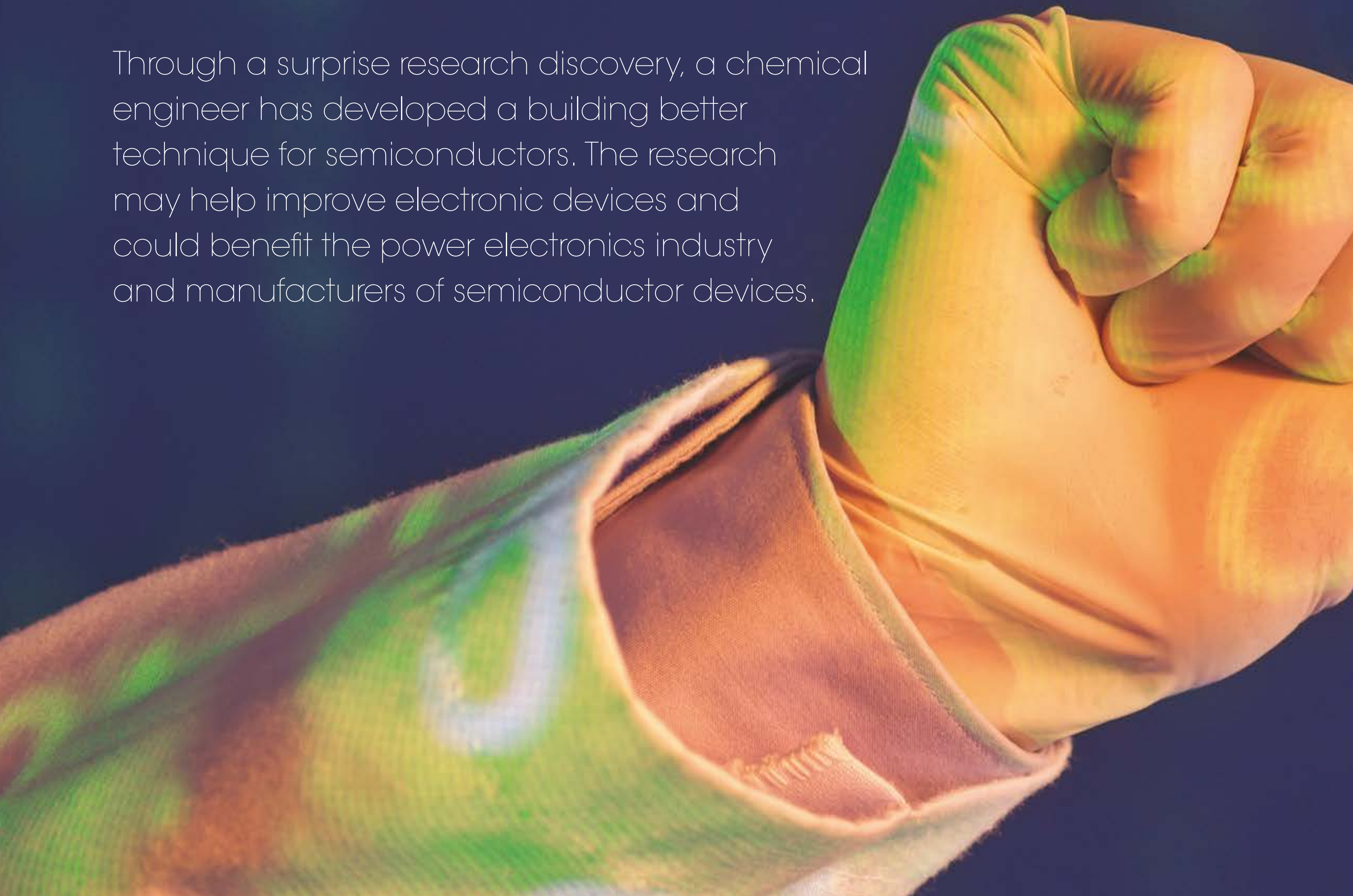
Patented process builds better semiconductors, improves electronic devices

Through a surprise research discovery, a chemical engineer has developed a building better technique for semiconductors. The research may help improve electronic devices and could benefit the power electronics industry and manufacturers of semiconductor devices.



THROUGH a surprise research discovery, a Kansas State University chemical engineer has found the icing on the cake for electronic devices.

Jim Edgar, university distinguished professor of chemical engineering, has received a patent for his invention "Off-axis silicon carbide substrates," which is a process for building better semiconductors. The research may help improve electronic devices and could benefit the power electronics industry and manufacturers of semiconductor devices.

Electronics are made of semiconductors crystals that must be layered perfectly for the electronic device to work.

"It's like a stacked cake separated by layers of icing," Edgar said. "When the layers of semiconductors don't match up very well, it introduces defects. Any time there is a defect, it degrades the efficiency of the device."

Edgar's research has developed a better way to build semiconductors and layer them to minimize potential defects -- an important discovery for manufacturers. Edgar describes the research discovery as serendipitous. Several years ago, when Yi Zhang, a 2011 doctoral graduate in chemical engineering, was working in the laboratory, she found a

substrate sample that was very smooth. Collaborative researchers at the State University of New York at Stony Brook and the University of Bristol in the United Kingdom later confirmed the layer's presence and proved that it had fewer defects than on the standard substrate.

"We have applied this process to other systems," Edgar said. "We are working on verifying that it is not just these specific materials we started with, but that it can be applied to a lot of different materials."

Some of Edgar's latest research focuses on two different boron compounds: boron phosphide and icosahedral phosphide. The researchers received support from the National Science Foundation.

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Jim Edgar, university distinguished professor of chemical engineering at Kansas State University, has received a patent for his process that can build better semiconductors and improve electronic devices.
Credit: Image courtesy of Kansas State University

THE MEMORY ROADMAP:

a paradigm shift from 2D to 3D

"There will never be enough memory": this idea has driven the continuous scaling of memory technologies. Today, DRAM and Flash, both charge-based memory concepts, represent the largest memory markets. For a long time, experts have predicted that emerging memories, such as STT-MRAM, resistive RAM and phase-change memory, all resistance based, would replace the common DRAM and Flash technologies in the Terabit era. According to Jan Van Houdt, Chief Scientist at imec and IEEE Fellow, we will first witness a paradigm shift from planar towards 3D technologies, rather than from charge-based to resistance-based memory.

IN TODAY'S ELECTRONIC SYSTEMS, a large part of the system area is consumed by memories. Jan Van Houdt: "Let's take a closer look at CPU (or central processing unit) centric systems, used in for example personal computer and server applications. Close to the CPU, on-chip, static random access memories (or SRAMs) are the dominant memories. These embedded SRAMs are volatile and excel in speed. But they consist of 6 transistors, and are therefore rather big and have a large cost per bit. Also on chip, less fast and somewhat denser, are higher cache memory levels, mostly made in SRAM or embedded DRAM technology. Off chip, farther away from the CPU, you find ROM (read only memory) or NOR Flash memories for code execution, DRAM chips for the working memory, and non-volatile Flash NAND memory chips for storage. In general, memories located farther away from the CPU are cheaper, slower, denser and less volatile."

The ever increasing performance of computation platforms and the consumer's hunger for storing and exchanging ever more data drive the need to keep on scaling memory technologies. For a long time, memory experts have been dreaming of one

unified memory, a scalable memory concept that would replace all the different memories. Jan van Houdt: "This idea has meanwhile been abandoned. Electronic systems require ever more different memories with different sizes and specifications. For the terabit era, we expect that the memory hierarchy becomes even more complex. We will soon witness the introduction of two new memory classes: storage class memory (or SCM) and embedded non-volatile memory (or e-NVM). With SCM, we fill up the gap between DRAM and Flash. It will provide an intermediate step between high-density Flash and high-performance DRAM in terms of latency, speed and cost. SCM will mainly serve the server market: Google, Yahoo, Facebook... they will benefit from this new class of memories which do not necessarily require 10 years of retention. Another newcomer, embedded non-volatile memory, is today only present in some particular applications (microcontrollers and smart cards). Current non-volatile technologies like Flash are too complex to embed in high-end CMOS technology. Especially for mobile applications, there is growing interest in a new embedded non-volatile memory technology."

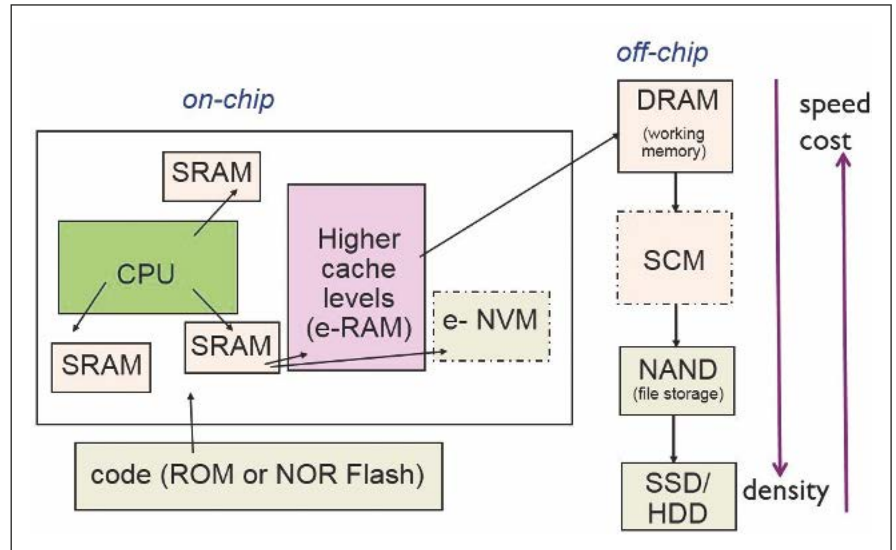
DRAM and Flash memories: scaling issues

Today, the memory market is dominated by DRAM and Flash memories. DRAM chips are now available up to 8GB densities in a 25nm technology node, while Flash has ended up at 16nm half pitch dimensions, yielding 128GB on a single chip with 2 or even 3 bits per cell. Both memories are charge based, and this generates some particular scaling issues.

Jan Van Houdt: "DRAM is structurally a very simple type of memory. It consists of one transistor and one capacitor that can be either charged or discharged. However, upon further scaling, this concept runs out of steam. One of the problems is related to periodic DRAM refreshment. Today, a DRAM memory is being refreshed about 16 times per second to deal with the slow discharge of the capacitor. When further scaled, the capacitor has to be refreshed even more frequently, hindering the performance of the memory. Scaling the capacitor not only increases the leakage, but also the aspect ratio, which has already increased to 35 for conventional double-sided crown capacitors. A new architecture, the one-pillar architecture, with new electrode materials and higher-k dielectrics, partly solves this problem. But even this pillar capacitor cannot be scaled down below 15nm." Nevertheless, DRAM scaling can continue, but not in the classical way. Jan Van Houdt: "An interesting way to scale on performance and power, is 3D stacking: stacking different DRAM dies and connecting them by using through-Si vias (TSVs).

This leads to the so-called hybrid memory cube, which also allows to take many logic functions off-(memory-) chip and optimize the chip system as a whole. A disadvantage of this solution is cost, since TSV technology is still a quite expensive technology."

With Flash, the problem is more complicated. Flash memory stores information in an array of memory cells, mostly made from floating-gate transistors. While in traditional devices, each cell stores one bit of information, more advanced concepts store 2 or even 3 bits per cell. Jan Van Houdt: "Today, a NAND Flash cell in a $4F^2$ cell layout provides the smallest dimension. But when we decrease the half pitch of the cell array, the threshold voltage shift associated with the tunneling of one electron towards the floating gate, dramatically increases towards several 100mV's. This limits programming accuracy dramatically at the 10nm technology node, and unless new smart ways around this 'single electron limit' are found, this could very well be the end of planar NAND technology. So, we are running out of electrons. The most attractive solution is to go 3D. Not by die stacking, as in DRAM, but by stacking vertical cells by using a charge trap Flash architecture. Following this 'bit cost scaling' (or BiCS) concept, the memory cell transistors are placed vertically on the chip in order to increase the density even further. This way, up to 32 cells have already been stacked in a functional device, and first products are on the market."



The classical (server-based) memory hierarchy.

What about the emerging memory technologies: STT-MRAM, PCM and RRAM?

In the past years, experts have predicted that new memory technologies, mainly resistance-based, would replace 'old' DRAM and Flash technologies in the years to come. At first, it was believed that phase change memory (or PCM) could replace NOR Flash, while resistive RAM (or RRAM) would replace NAND Flash. Spin-torque transfer memory was identified as the only technology that could potentially replace DRAM due to its high endurance.

Jan Van Houdt: "Recently, more and more experts believe that these new memory technologies may first end up in embedded applications and in storage class memory. Take STT-MRAM, for example. The core element of STT-MRAM is a magnetic tunnel junction in which a thin dielectric layer, usually 4 to 5 atomic mono-layers, is sandwiched between a magnetic fixed layer and a magnetic free layer. Writing of the memory cell is performed by switching the magnetization of this free magnetic layer. STT-MRAM is a very promising memory concept because of its non-volatility, high-speed, low-voltage switching (<1V) and almost unlimited read/write endurance. But there are some disadvantages. The memory is too large for Flash replacement, and cannot (yet) be used in a 3D configuration. Also, STT-MRAM is current driven, ending up with a high write power and large peripheral devices. The technology could potentially replace DRAM, but can at the moment not compete with the low cost of DRAM technology. Eventually, if (3D) DRAM has finally hit the wall, and STT-MRAM is able to shrink its size, this would become a possibility. On a shorter term, I expect STT-MRAM to replace embedded SRAM in higher caching levels (L3)."

Another resistance-based technology is PCM, which is based on the melting and (re-)crystallization of chalcogenide material. Jan Van Houdt: "PCM is a reasonably mature technology with a high endurance (on cell level), large programming window and non-

> "Recently, more and more experts believe that these new memory technologies may first end up in embedded applications and in storage class memory"

destructive read. The technology writes reasonably fast at low voltage. However, due to its large programming power and issues with material (in)stability, PCM is currently seen as a replacement for the declining market of NOR Flash technology."

And then there is RRAM, which relies on the formation of a conductive filament in an insulating layer. Jan Van Houdt: "Typically, an RRAM device consists of two electrodes that sandwich a thin dielectric layer. This layer serves as the ion transport and storage medium. The ionic movements and structural changes in this medium, caused by e.g. an electric field, cause a measureable change of the device resistance. RRAM comes in several flavors: oxide RAM (or OXRAM), conductive bridging RAM (or CBRAM) and vacancy modulated conductive oxide (or VMCO). In general, the concept is low cost, low voltage and can be realized with 'standard materials', like TaO_x. But although the resistive switching structures show excellent memory characteristics, implementation of high-density RRAM arrays lags behind, mainly due to sneak current issues.

To suppress the leakage paths, a non-linear selection device (or selector) is required to connect serially with each resistive switching element forming a memory cell. And that's one of the weaknesses of RRAM. In order to compete with Flash technology, I see the need for two major breakthroughs: RRAM needs to become more dense by directly going 'true' 3D, i.e., by placing cells vertically on a chip. In this configuration, there is however no space for the selector. Another breakthrough is therefore required in the development of a selector-less concept for 3D RRAM. But that's still in the future. As a first target, I see RRAM as a candidate memory technology for application in storage class memories and embedded non-volatile memories. The concept is especially interesting for Internet of Things and low-density applications."

Newcomers

Besides these charge- and resistance-based memory concepts, researchers explore other memory concepts to fill in the memory hierarchy. For example, there is the return of ferroelectrics: the FeFET. Jan Van Houdt: "FeFET is for sure not a newcomer. It has long been considered the ideal memory, but material issues, the breakdown of the interfacial layer and the bad retention characteristics have always been showstoppers. Recently however, a ferro-electric phase has been found in HfO_2, a well-known material, and this triggered new interest in this memory concept." Besides exploring new technologies, researchers also look at the system level. SRAM, for example.

Jan Van Houdt: "Memory makers do not consider this a true memory technology, since it is realized on chip in standard logic CMOS technology. But we do need a replacement for SRAM, since SRAM deteriorates with every new CMOS technology generation. And there are some interesting options that deserve further investigation. Ferro-electric tunnel junctions, for example, or spin-based domain wall switching. Spin-based concepts in general are very attractive, as they could possibly solve important issues with charge-based concepts (the decreasing number of electrons) or resistance-based concepts (which are current based)."

Conclusion: the paradigm shift

While emerging memories have been predicted to replace the common DRAM and Flash technologies in the Terabit era, the industry has clearly shifted towards a more conservative view. Jan Van Houdt: "This view focuses on the continuation of well-known concepts, even though pushing them to the required density levels is not straightforward either. The immaturity of the resistance-based concepts (mainly PCM, RRAM and STT-MRAM) has slowed down their introduction in the roadmap. We will first witness a paradigm shift from planar towards 3D technology rather than from charge-based to resistance-based memory. The resistance-based emerging memories will first show up in new application fields, like storage class memory and embedded non-volatile memory."

Jan Van Houdt received a PhD from the University of Leuven in 1994. During his PhD work, he invented the HIMOS™ Flash memory, which he transferred to several industrial production lines. In 1999 he became responsible for Flash memory at imec and as such was the driving force behind the expansion of imec's memory program. Today he is Chief Scientist of the Memory Department. He has published more than 250 papers in international journals and accumulated more than 200 conference contributions (incl. 35 invitations and 5 best paper awards). He has filed more than 50 patents and served on the program and organizing committees of 10 major semiconductor conferences. In 2014 he received the title of IEEE Fellow for his contributions to Flash memory devices.

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Beyond the curve to **foldable displays**

Lightweight, unbreakable, flexible and wearable; these are just a few of the development targets for contemporary consumer electronics. Over the past couple of years interest in flexible displays that meet these needs has increased significantly, with the market for this flexible display technology predicted to expand to more than $21billion by 2020[1]. Dr. Michael Cowin, Head of Strategic Marketing, SmartKem Ltd looks at the opportunities ahead.

FEW INDUSTRIES have the same rate of development as the electronics sector. Buoyed by consumer demand for fresh innovation and fierce industry competition, electronics development exists in a rapid cycle of continuous improvement. One of the most exciting and eagerly awaited outputs from this process is the development of bendable and flexible displays; a potentially transformative technology set to emerge over the next few years.

Curved displays are already available in the commercial space, with the more recent emergence of curved phones and television screens. Yet despite their novelty, the real 'wow' factor in the consumer experience has yet to be achieved. The value in the next generation of smart and wearable technology will come with the introduction of flexible and foldable devices such as smartphones, tablets and watches. However, this demands a new semiconductor platform with entirely new physical properties and form factor capability which in turn raises a unique set of challenges for traditional and new thin-film transistor (TFT) technologies to overcome.

Significant developments in electronic devices almost always require a corresponding advance in their functional components and materials. Leaps in processing power, for instance, have often occurred due to the emergence of increasingly smaller and denser transistors. In contrast, the rise of thin-film electronics has relied on the development of TFT technology with increasingly stable and uniform properties over wide areas.

These properties are in increasing demand; however the challenge now lies in ensuring the transistors also demonstrate true physical flexibility. This is set to become a key market driver, with organic semiconductors beginning to change the landscape of traditional TFT based platforms.

Organic semiconductors now deliver similar, and in most cases superior, properties to traditional inorganic devices, but with much improved physical flexibility.

Organic based TFTs (OTFTs) are already starting to penetrate the supply chain for the development of truly flexible Active Matrix Organic Light Emitting Diodes (AMOLED) displays and Electronic Paper Displays (EPD).

Indeed OTFT technology is now being seriously considered as a straight replacement in amorphous silicon (a-Si) lines for the manufacture of plastic, lightweight and ruggedised LCDs.

Figure 1: The evolution of flexible electronic devices has required a new approach to development, typified by the emergence of high performance organic semiconductors.

Furthermore the utility of organic semiconductors as a platform technology is set to play a pivotal role in how we see, touch and sense information in every aspect of our lives. This combined with the shift towards Big Data, The Cloud and the Internet of Things will drive flexible and adaptable technology fully into the mainstream in the form of a new generation of displays, touch screens and sensors.

Understanding organic semiconductors: Smart chemistry for smart electronics

Traditional inorganic TFT semiconductors are formed from amorphous or polycrystalline structures and as such are unable to meet the market demands of robust flexibility. In the case of Low Temperature Polycrystalline Silicon (LTPS), for example, the poly-crystalline network is partially responsible for the semiconducting properties but is also the root of the material's inflexibility.
Organic semiconductors are fabricated from small organic molecular species, polymers or a combination of both which allows them to overcome this fundamental limitation through their intrinsically flexible nature; offering the potential of ultra-flexible displays that can be folded to a sub-millimetre bend radius with no change in TFT performance.

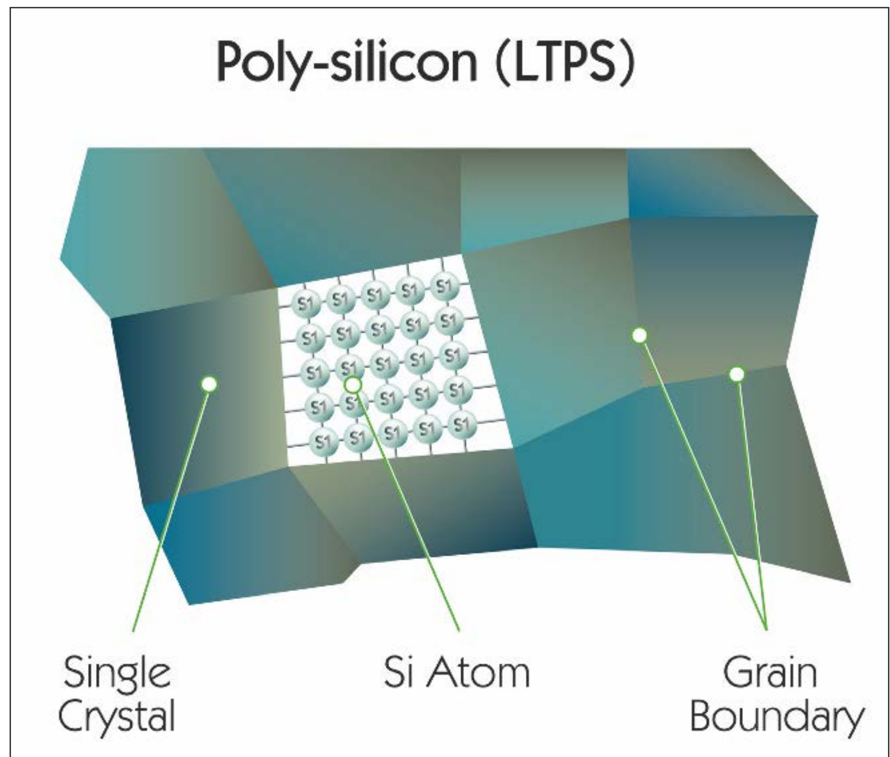

Image courtesy of AUO

This end product advantage is further complemented by a range of additional benefits such as a high mobility performance and a potential cost down proposition to manufacturers through ease of processing, higher yields and increased throughput achieved via low temperature processes such as Sheet-to-Sheet and eventual Roll-to-Roll (R2R) print techniques.

Organic semiconductor technology generally fits within two main material categories: polymeric and distinct molecular materials. A common feature of both is that they are types of conjugated systems, meaning they consist of alternating single and double bonds which lower the overall energy of the molecule and increase stability.
Efficient device operation can be ensured by matching the highest electron energy level of the organic semiconductor to the work function of a metal contact.
For high performance TFTs, high charge carrier mobility is required which naturally favours crystalline small molecule semiconductors; molecules that are closely packed with regular arrangement in a crystal lattice increase good π-bonds and therefore efficient charge carrier mobility.

A new class of organic semiconductor materials eliminate such issues by designing into solution based semiconductor 'inks' the preferred features of chemically stable, high mobility, single-crystal organic semiconductors and combining them with amorphous semiconducting polymers or 'binders'. This material combination offers the electrical performance of single crystals but with the uniform processing characteristics required for high mobility.

As such the key benefits of organic semiconductors are realised with a technology platform that offers ease of production coupled with superior physical and electrical semiconductor performance in end-product form.
Although organic semiconductors can be stable up to 300°C the ease by which these solution-based materials can be processed at low temperatures offers manufacturers a wide range of cost effective stack materials and substrates, and easier bond/de-bond and inter-

Characteristic	a-Si	LTPS	OTFT	Oxide
Flexibility & Fold Capability	✗	✗	✓✓	✗
Route to stretch-ability	✗	✗	✓✓	✗
Low Temperature Process	✗	✗	✓✓	✗
Print Compatibility	✗	✗	✓✓	✗
Mobility	✗	✓✓	✓	✓
Bias Stress Stability	✗	✓✓	✓✓	✗
Low Cost of Ownership	✓✓	✗	✓✓	✓
Established Supply Chain	✓✓	✓✓	✓	✓
Suitable for Wide Area	✓✓	✗	✓✓	✓
Reproducibility	✓✓	✓✓	✓	✗

Figure 2: The different TFT characteristics

layer alignment due to less expansion and contraction. This all adds up to significantly improving production yield (over high temperature processing) and thereby reducing production costs over any area of substrate.

One company leading the development of organic semiconductors is SmartKem with its product *tru*-FLEX™. While the electrical performance of *tru*-FLEX™ exceeds the need for applications such as AMOLED, LCD and EPD - more critically, the resulting TFTs are almost unbreakable, exhibiting flexibility down to a highly acute bend radius, thus eliminating the need for exotic and costly strain management layers. This offers original equipment manufacturers a high degree of confidence in product performance making the SmartKem *tru*-FLEX™ material a key component for highly rugged and reliable flexible display applications such as mobile and wearable devices.

Easing the printing processes

In addition to being the only truly flexible technology currently available, one of the major advantages of organic semiconductors comes from their ease of application. Solution based semiconductor inks can be applied to substrates through a range of additive processes and print production systems, including slot dye, spin coating and inkjet printing.

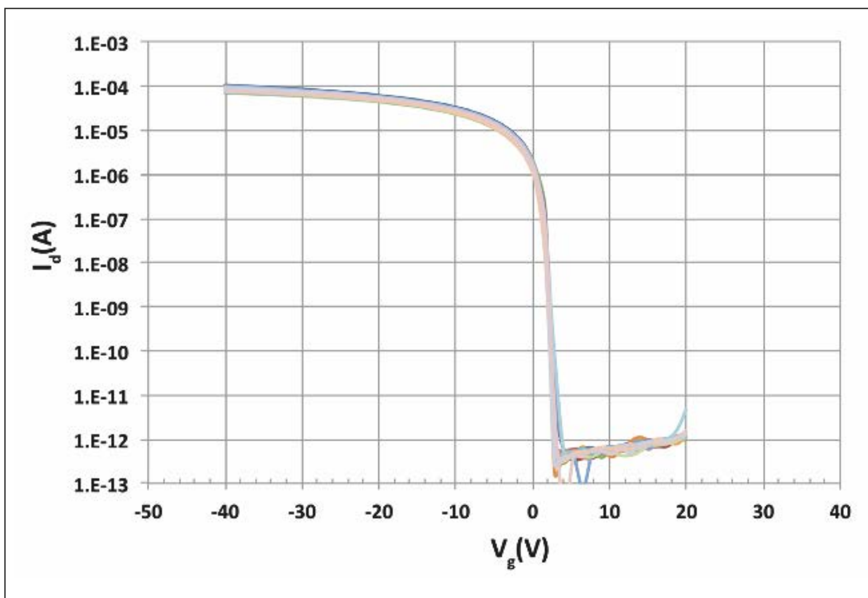

Figure 3: Typical linear transfer curves for SmartKem's tru-FLEX™ TFTs
x-axis : VG (V) y-axis : ID(A)

This application flexibility, along with the improvements in final product quality, process control and overall efficiency, make organic semiconductors an attractive prospect for manufacture. Organic semiconductor ink coatings are also compatible with R2R processing. Here, semiconductor materials are continuously or near continuously patterned onto a wide substrate area.

This high throughput process enables semiconductor fabrication and coating at a fraction of the time and cost of traditional manufacturing methods. Although still in its infancy, combining organic semiconductors with a scaled up R2R fabrication process is considered a realistic and incredibly lucrative prospect. For this reason many consider R2R processing the ultimate goal for electronics manufacture and organic semiconductors a critical component to achieving this.

The next generation of electronics

From displays and augmented touch screens to sensors, organic semiconductors are set to play a pivotal and diverse role in this new generation of electronics. Meeting the demands of this growing market requires developers of organic semiconductors to push boundaries in terms of the electrical performance and dynamic physical characteristics of these materials in TFT form. In response to this technological advancement the IEC standards for electronics are being re-written and re-defined to standardise every facet of this new industry.

Printable organic semiconductors have made the transition into pre-production and are enabling electronics manufacturers throughout the industry to make new and exciting form factor displays and products that will overhaul the current consumer world. And it's all a lot closer than you think.

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Reference

[1] Flexible Displays technology and Market Forecast Report, September 2014, DisplaySearch

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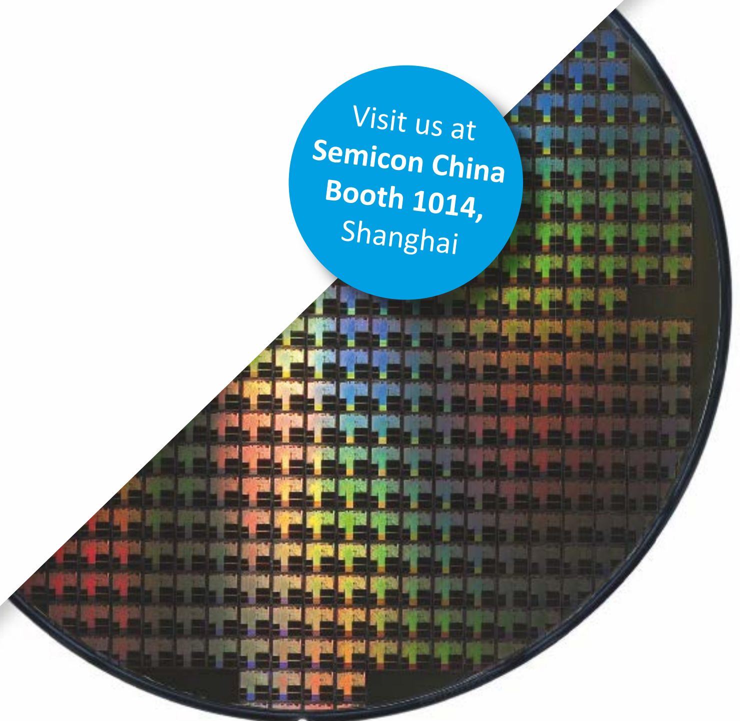


Growth!

What a welcome forecast

Indicators continue to point towards a robust 2015. Updated 2014 tallies show global Fab spending jumped nearly 20 percent. Forecasters predict semiconductor surges of nearly 10 percent this year.

COMING AFTER YEARS of lacklustre semiconductor growth, the latest market reports and projections are welcome news. 2014 saw fab spending grow 19.8 percent, according to the latest SEMI World Fab Forecast. IHS Technology analysts joined the chorus with their own results pointing to industrial semiconductor markets growing 16.8 percent in 2014. That amazing spurt led IHS to forecast overall industrial semiconductor Compound Annual Growth Rates (CGAR) of 9.7 percent for 2015 and beyond.

What's driving this growth? Are there cloudy days in the forecast?

While expansion is gladdening the hearts of semiconductor industrialists, the biggest celebrations are in optical LED boardrooms. This segment grew 23.4 percent last year, from $6.3 to $7.1 billion (USD). Discrete power transistors and related components posted significant 13.4 percent growth, from $5.5 to $6.3 billion (USD). Another technology enjoying a renaissance was dynamic random access memory (DRAM) that saw double-digit increases in both 2013 and 2014, largely making-up numerically for the lean years during global economic recession.

Most industry watchers credit this growth and predicted market expansions largely to overall global economic recovery. IHS researchers say we can thank a recovering United States economy for driving so many positive headlines in the past year. It's this same outlook that will make for a better 2015, they say.

Home secure home

The expansion of mobile devices into more aspects of daily life continues to be a juggernaut driving needs for memory circuits, screens, RF connectivity, power and control functionality, as well as software applications. Growth in the industrial semiconductor segment touches upon everything from factory automation to building control, lighting and related devices that use semiconductors to give previously 'dumb' devices wireless connectivity, memory or logic. All these have helped sales to take a steep leap skyward. LED lighting is at the forefront as well as home automation and control, surveillance and general security applications. People are buying more and they want what they buy to be efficient, connected and multi-tasking. Growing concerns for preventing all these devices from being 'hacked' is another opportunity for anyone involved in device or network-level security.

"Because of strong industrial segment growth, semiconductor companies see opportunities in these markets as never before. More devices are being used in applications that did not previously employ semiconductors," remarked Robbie Galoso, principal analyst for IHS in the company's report.

Mr. Galoso further observed that industrial segment growth has been lifted by a gradual acceleration in the global economy, which continues to boost industrial equipment demand, especially from the United States and China.

US growth is expected to continue through 2018. Economic expansion is more broadly based in the United States than in other regions. Major positive factors include the housing market, (stabilized in many areas while growing in others,) improved consumer finances and credit (thanks to jobs recovery), as well as increased capital spending. The US gross domestic product (GDP)

is expected to grow 2.4 percent in 2014, 3.1 percent in 2015 and 2.7 percent in 2016.

While the United States accounted for 30.5 percent of all semiconductors used in industrial applications in 2013, China is a sizeable second, purchasing about 14 percent of the world's output last year. IHS forecasters predict the Chinese economy will grow 7.3 percent in 2014, 6.5 percent in 2015 and 6.7 percent in 2016.

A more complete picture

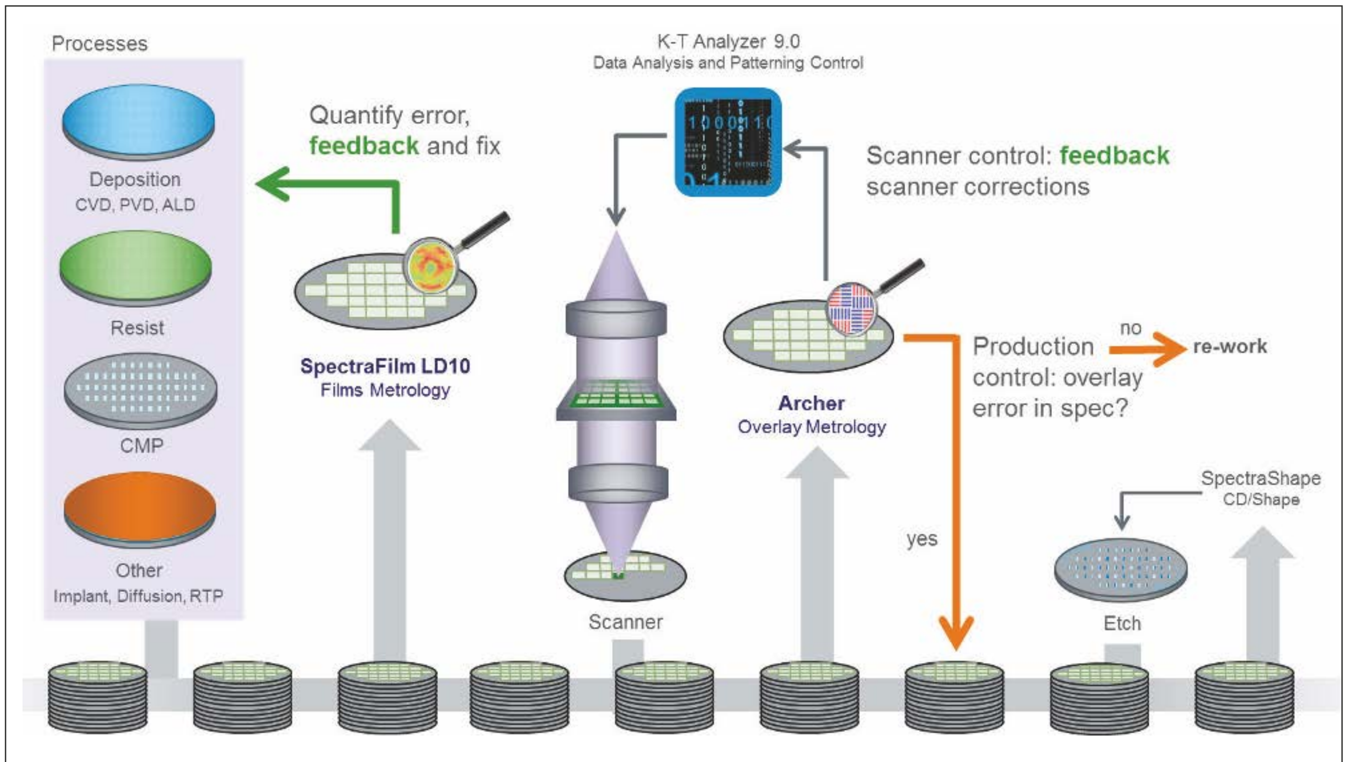
While the research points to recovering world economies as driving strong semiconductor growth, stopping there doesn't yield a complete picture. Even if more people have more secure jobs it's not guaranteed that they will part with hard-won income. Growth can be attributed in part to pent-up demand, but products have to be more amazing than ever to compete in global markets.

When one considers that the latest products in global shopping carts employ more creative design, are made with more efficient manufacturing and offer greater capabilities—all thanks to semiconductor technology—the picture of why we're growing becomes a bit more clear.

New technologies and frontiers

To keep costs at bay, improve performance, mitigate material expenses and achieve double-digit growth, there is a constant push for new and better approaches to creating more exciting products.

The frontiers of 3D NAND flash memory chips were pushed higher and higher in 2014. There were announcements by Samsung regarding its 24-layer designs early in the year. Not to be outdone by anyone but themselves, Samsung upped the ante mid-year by topping their 24-layer design with a 32-layer device. In November Intel countered by announcing the advantages of its own 32-layer approach. Some suggest the 'micro-skyscraper' rage won't end until structures with 50 or more layers emerge, but since taller isn't always better others in the industry believe different approaches to increase capacity, speed and/or performance are certain to follow. Some point that Toshiba/SanDisk could be a manufacturer to watch in 2015 after 2014 announcements seemed to lack the enthusiasm of their peers' PR.



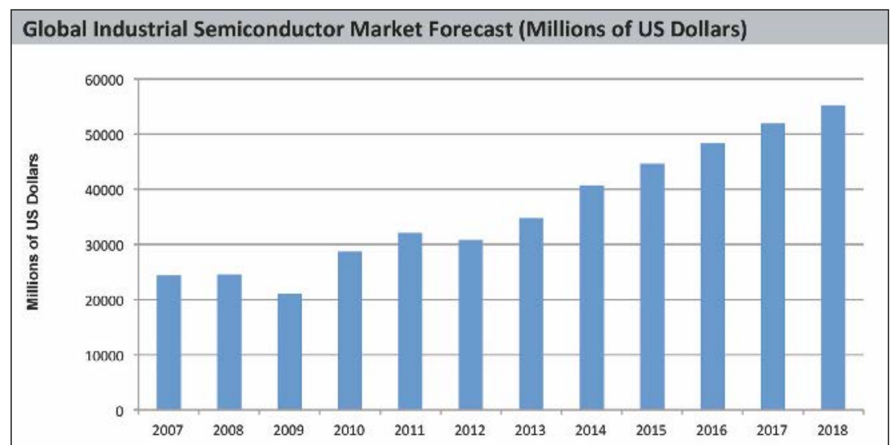
KLA-Tencor image depicts a simplified process flow in a semiconductor fab. After films are deposited on the wafer and qualified on the SpectraFilm LD10, (to ensure that thickness and uniformity meet production specifications,) they move on to the lithography cell where they are patterned by the scanner. The Archer 500LCM measures pattern overlay error—checking alignment against previous level patterns. Data collected can be used in a feedback or feed-forward capacity to improve patterning in subsequent lots or to make production decisions such as sending a wafer back for re-work or allowing it to continue down the line. Because of multi-patterning there can be many etch-deposition iterations not depicted in this overview.

One way to gain insight into directions major chip makers are headed is to take a look at some of the most advanced work of those who make the equipment that chip-makers rely upon for easier, faster, or otherwise 'better' processes.

One such leader is KLA-Tencor who aligned the official release of new products to the 2015 SPIE Advanced Lithography event in San Jose, California on 19 February. In a follow-up interview with KLA-Tencor CMO Brian Trafas, he noted that the new Archer 500LCM and SpectraFilm LD10 supported the advanced needs of manufacturers working with devices below 16nm, in particular FinFETs, 3D NAND and similar leading-edge devices. The results are improvements of up to 25 percent compared to existing systems.

As each generation reduces device size and as multi-patterning and spacer pitch splitting become more common, a new approach to metrology tools is needed to enable better qualification and monitoring of lithography films and film stacks, he indicated. Going smaller and taller (or more complex any way it's defined,) carries with it the need for better tools that will deliver greater performance while fitting into a manufacturer's current fab facility.

Trafas explained the new system (supporting overlay and films metrologies), can increase productivity as much as 25 percent. With more precise metrology tools manufacturers can receive substantially better feedback and feed-forward information, which is significant and all the more critical as device stacks increase in size and



Credit: IHS Inc.

geometries shrink even further. Beyond new hardware, the company developed new in-die targets, a new calibration method (Archer Self Calibration), new algorithms and further automated self-checks to improve performance without slowing the process or reducing yields.

The ultimate goals are to not only improve throughput of current devices but anticipate where manufacturers and designers are headed next—smaller, taller and more complex devices – all without slowing the lines while delivering improved error detection that more closely aligns with CD-SEM measured standards.

Promising research to enable 7nm geometries

At both the SPIE symposium and the International Solid State Circuits Conference (ISSCC) held in February in San Francisco, imec took the stages with advancements that again demonstrated the resilience and wide-ranging appeal of versatile silicon technology.

The SPIE conference was the first setting for a number of announcements that are moving the state-of-the-art supporting 7nm devices. Imec's Director of advanced Lithography, Kurt Ronse, highlighted presentations of interest to lithography users in a post-event discussion. Imec announced a key new processes enabling 7nm devices with partners Tokyo Electron and Merck utilizing a revolutionary new directed self-assembly (DSA) process; researchers showed they had reduced detectable defects to 24 defects/cm^2. Imec and its partners believe they're just hitting stride.

"Over the past few years, we have realized a reduction of DSA defectivity by a factor 10 every six months," stated An Steegen, senior vice president of process technologies at imec. "Together, with Merck and Tokyo Electron, providing state-of-the-art DSA materials and processing equipment, we are looking ahead at two different promising DSA processes that will further improve defectivity values in the coming months. Our processes show the potential to achieve single-digit defectivity values in the near future without any technical roadblocks lying ahead."

"Imec presented results on work with partners Murata and Huawei that detailed a new stand-alone multiband electrical-balance duplexer (RF filter) for applications including smartphones. The devices are designed using 0.18μm SOI CMOS and offer an alternative to today's standard"

It's about power

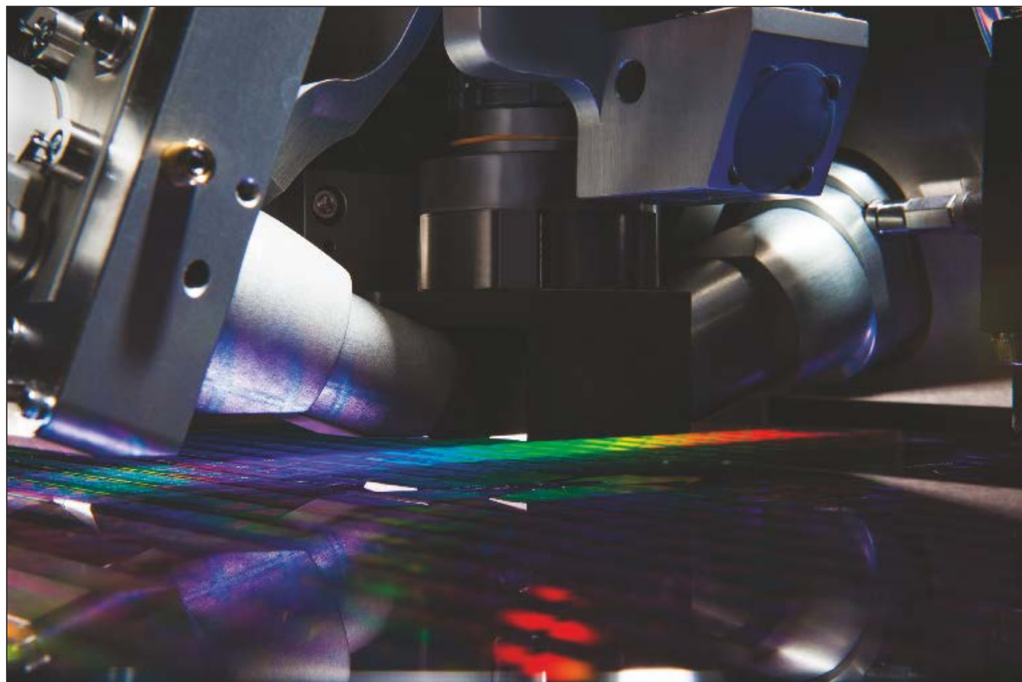
The other significant news from imec excited those interested in Extreme Ultra Violet (EUV) for practical 7nm geometries. EUV power has grown from 10W, to 40W and now to 80W and beyond; Ronse noted some participants have achieved 100W.

Even the greatest power levels are still below the 250W threshold considered necessary for full production. But while movement seemed stalled in 2014 the more recent steady increases in power levels is highly encouraging, Ronse said.

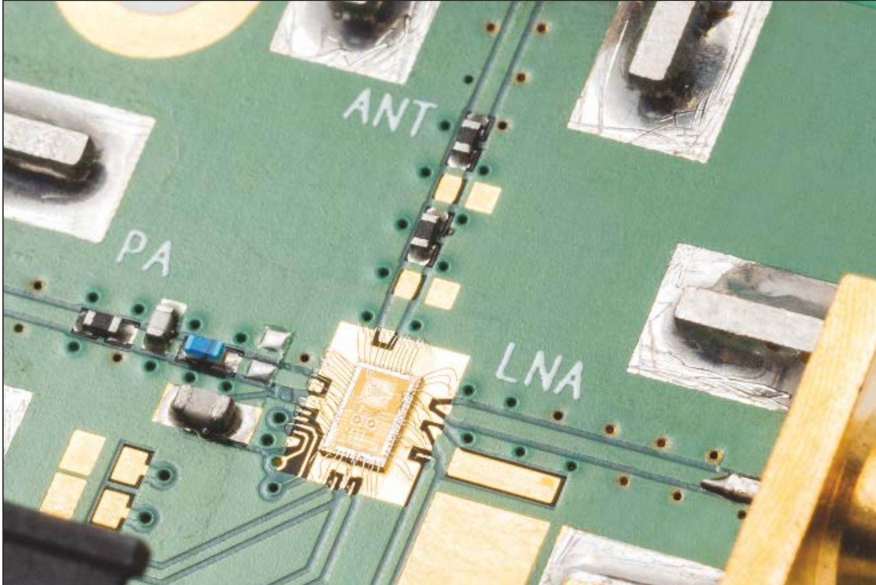
On the ISSCC stages

Imec's Harmke de Groot, Director of Perceptive I of T, said three announcements drew plenty of attention. One addressed new multi-band smartphone filter technology, while another showed it was possible to reduce power and size in Bluetooth and ZigBee radios; a third unveiled a high-performance 79 GHz radar for future generations of automotive driver assistance.

Imec presented results on work with partners Murata and Huawei that detailed a new stand-alone multiband



KLA-Tencor's metrology systems include multiple optical technologies enabling non-destructive, production-capable measurement of overlay, film thickness, critical dimension and device profile across a diverse range of IC process layers, device types and design nodes.



Imec photo of their new ultra-low power 2.4 GHz radio for Bluetooth Low Power and ZigBee standards in a test fixture.

electrical-balance duplexer (RF filter) for applications including smartphones. The devices are designed using 0.18μm SOI CMOS and offer an alternative to today's standard: fixed-frequency SAW-based duplexers mounted externally as part of Receive/Transmit chains.

Imec believes the new devices offer insertion loss and linearity comparable to SAW-based devices, but also deliver an intriguing benefit—they are tunable, opening the possibility of one CMOS filter working across multiple bands instead of one filter per band. Considering that today's smartphones have three to four or more bands to cover regional variations and needs, the potential of imec's new filter is immediately appealing so long as costs and manufacturability are competitive.

In other promising news from imec, the researchers announced work in combination with Holst Centre and Renesas for an ultra-low power 2.4 GHz short range radio for Bluetooth and ZigBee systems. The devices, made with 40nm CMOS, reduce supply voltage by 20 percent, cut power consumption by 25 percent and shrink chip area by 35 percent compared to previous 90nm RF front-end designs.

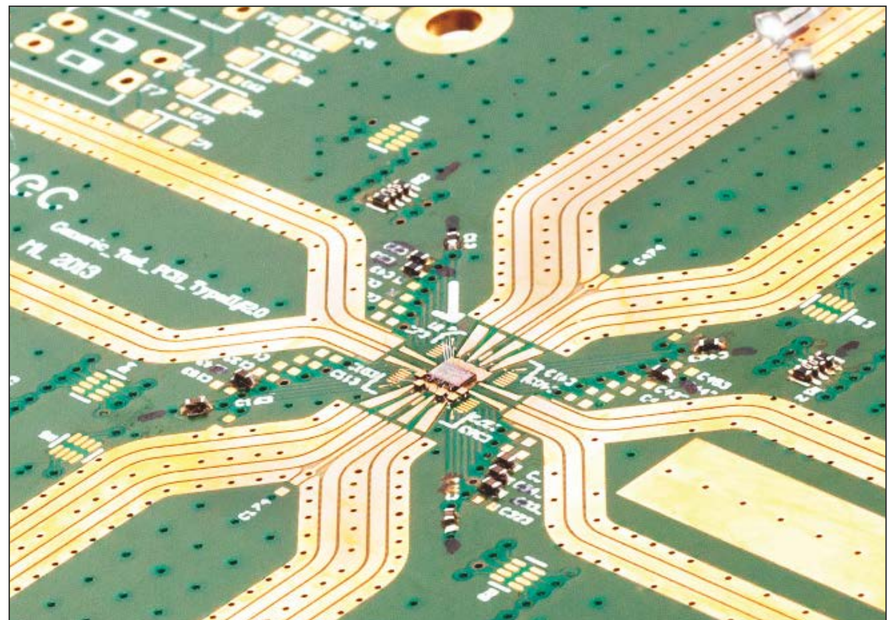
Imec partnered with Panasonic for another ISCC announcement, this time for 79 GHz automotive radar that demonstrates the potential of downscaled CMOS for inexpensive millimeter wave radars that can be accurate and precise when utilized to detect an object's presence and motion.

Current automotive high frequency radars often employ SiGe-based technologies and in addition to lower cost the new approach can be mounted 'invisibly' compared to systems that employ ultrasonic sensors. The CMOS radar system is lower-power, compact and integrated; at high volume CMOS technology is intrinsically lower-cost than SiGe.

Power, economies and innovation

2015 forecasts point to continued growth in semiconductor sectors, particularly those serving emerging markets such as LED lighting, security and wide-ranging industrial applications. As economic recovery takes place in many more places around the world, growth in the CapEx expenditures for fab equipment are expected grow even though the number of fabs may consolidate or facility expansion may slow.

Through research enabling more powerful and efficient devices, and through manufacturers creating new technology with greater efficiency and functionality, the robust international semiconductor market demonstrates that the best may still be to come.



Imec photo of their 28mm CMOS 79 GHz transceiver chip for phase-mode continuous wave auto radar.

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Maximizing productivity in the lab

Failure analysis labs typically involve lots of manual tasks performed by highly skilled operators. However, failure analysis labs are now adopting practices from the fab, such as increased automation, as the need for more and faster failure analysis feedback becomes critical to maximising yield. Todd Templeton from the FEI Company explains some of the practices and efficiencies that can be gained through automation in the modernised lab.

MOST PROCESSES found in today's advanced failure analysis (FA) labs rely heavily on skilled technicians performing a variety of tasks that require them to make hundreds, if not thousands, of small operations each day. These tasks might require operators to manually insert failed or defective components into electrical testers, grind down packaging or surface layers to expose specific circuitry, mark and navigate to suspect areas in a SEM or dual beam FIB-SEM, and set imaging or preparation conditions for SEM or TEM analysis. This sort of operation is very different from the process that occurs on the other side of the wall, in the fab. There, batches of wafers are processed according to specific recipes with very little human interaction. In most 300mm fabs, factory automation software directs the movement of FOUP (front opening unified pod) cassettes filled with wafers between process tools where recipes are automatically downloaded and run. Very few operators are required to run a fully automated, "lights out" fab. Efficiencies in operation are achieved largely because routine steps or processes have been automated and

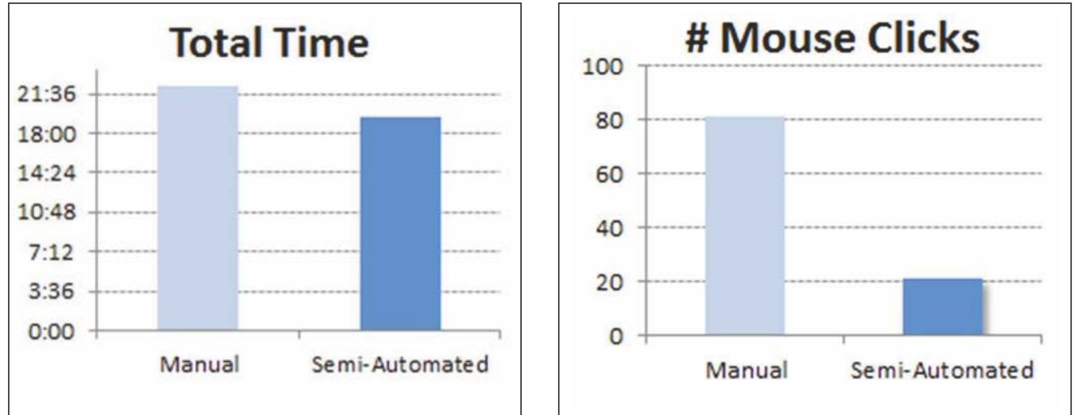


Figure 1. Throughput and mouse click comparison for making a thick lamella prepared for in-situ liftout.

the need for operator interaction minimized. This methodology is now making its way from the fab and into the FA lab as the need for more and faster failure analysis feedback becomes the bottleneck to yield ramp.

Transition from manual to automated

For many decades, the process of manufacturing semiconductor chips was managed through the use of a paper trail. Cassettes of individual wafers were batched together into lots and moved from process to process based on a printed set of instructions that accompanied the batch on the manufacturing floor. Later, as computational power increased, factory automation software was introduced into fabs to allow operators to move lots of wafers into a particular process step and determine the proper process conditions for the next manufacturing step. After manually selecting the correct conditions for the process step, the wafers were processed and then manually logged out and physically moved to the next manufacturing location.

As factory automation software became more sophisticated in the mid 1990's, operators on the factory floor were no longer required to manually enter in lot and process information. Recipes and lot tracking became more automated, reducing the number of mistakes and the amount of time wasted waiting for operators to be present. With the advent of overhead transport (OHT) systems central stockers were able to store, move, and retrieve 200mm standard mechanical interface (SMIF) and 300mm FOUP cassettes, eliminating the need for operators to interface with wafer lots and process equipment. Improved lot movement, reduced operator injuries, and fewer missed processing steps resulted from this enhanced automation.

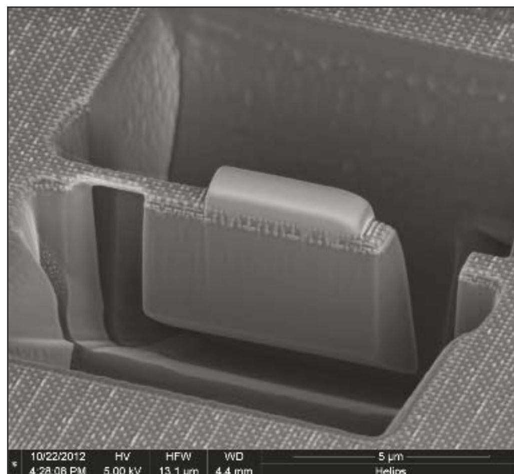


Figure 2. Thick lamella ready for ISLO.

Reducing operator strain and involvement in the more mundane aspects of failure analysis is a goal commonly vocalized by lab managers. Managers know that reserving their valuable human resources for the most critical process steps reduces operator fatigue and burnout. A method for creating recipes to automate basic, repetitive steps in the failure analysis process has been available for some time and is now showing benefits. For example, the first step in the preparation of a thin section for examination in a transmission electron microscope (TEM) is creating a thick lamella containing a specific feature or defect and preparing it to be lifted out of the bulk sample [1]. Once the operator has navigated to the location where the lamella is to be created, the next series of steps is generally the same for all samples created in that lab. Automating these steps, including automatically setting system operating parameters such as pattern sizes and locations for bulk silicon removal, FIB and SEM beam settings, and stage orientation, allows them to be executed without an operator in attendance.

Automation can significantly reduce process time and operator interaction with the tool. To illustrate this, we performed a test using an automated FIB-SEM (FEI Helios NanoLab 460F1 DualBeam with iFast automation software). The test evaluated the number of mouse clicks and time required to create a 150nm thick lamella ready for liftout, comparing a fully manual method a fully automated process. The results show that the automated recipe process was able to create the lamella 12% faster than the manual method and with nearly 75% fewer mouse clicks (Fig.1) In addition to offering ergonomic improvements to all users, the automated approach also allows novice operators to attain the quality and throughput

performance standards required in their labs more quickly. Once the thick lamella has been created, it must be extracted from the bulk sample and thinned to its final thickness – thin enough to transmit electrons and isolate the feature of interest – typically a few tens of nanometers. Extracting and manipulating a sample this size for thinning and transfer to the TEM is not trivial. One method, the in situ lift out (ISLO) process, proceeds by attaching the nearly free thick lamella (Fig. 2) to a nanomanipulator probe, cutting the lamella free, moving and attaching the lamella to a TEM grid, and finally cutting the attachment to the nanomanipulator probe. Once attached to the grid the lamella is thinned to final thickness with the FIB, and the grid, with the lamella attached, is transferred to the TEM. Because the typical dimensions for a thick lamella ready for ISLO are in the 0.5 – 2.0μm thick by 20μm wide range, the transfer process requires great precision.

The ISLO process was developed as a manual process and has been well documented [2-4]. Except for some very unique cases, nearly all TEM lamella that are extracted from bulk samples using ISLO follow an identical process, making this an ideal candidate for automation.

Challenges with automating the ISLO process include, but are not limited to: accurate movement of the nanomanipulator needle to prevent collisions, which may destroy the lamella or nanomanipulator needle; a predictable and repeatable needle shape; attaching the chunk to the TEM grid so proper final thinning and eventual zone axis alignment in the TEM can be realized; and finally, optimization of the speed and success rate at which this process can be performed. As a result of a comprehensive approach to solving these challenges a fully automated method for ISLO has been developed [5].

Increasing lab efficiency through automation

As a result of automating more and more of the process steps for creating TEM lamella, lab managers can increase the efficiency and productivity of their valuable human resources. In FA laboratories where no automation is employed, technicians must be at the dual beam preparation tool 100% of the time when creating TEM lamella. The process of selecting the target region of interest (ROI), placing the milling boxes and selecting the beam conditions to create a thick lamella, and then performing the ISLO process are all performed manually. Conversely, in labs which have adopted a more automated approach to creating lamella, technicians are able to oversee the operation multiple dual beam sample preparation tools at the same time.

An illustrative example comparing a fully manual FA lab with a more modern lab which has adopted automated system recipes for sample processing follows. In the fully manual lab, a technician can create a 100nm thick lamella and perform the ISLO process in roughly 29 minutes once the ROI has been identified. In the case where 8 lamellae from the same wafer are being prepared

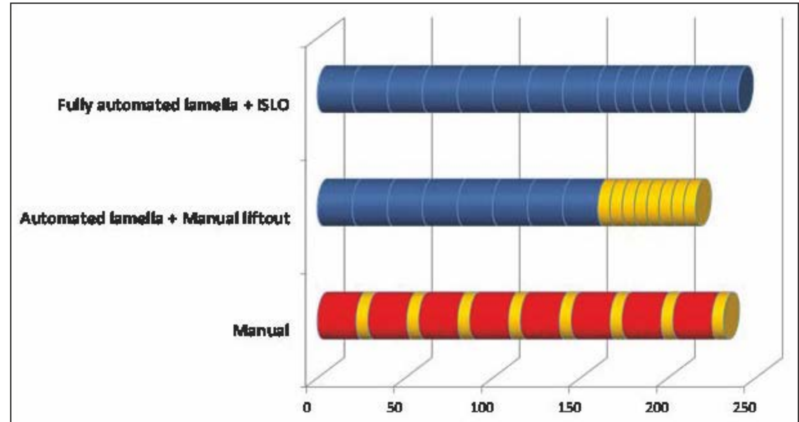
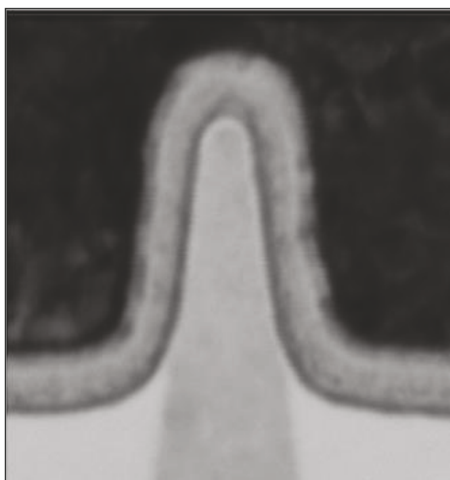
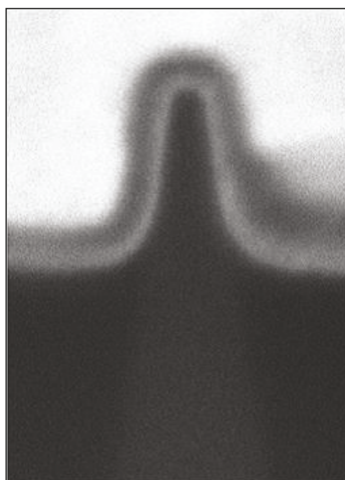


Figure 3. Comparison between manual and fully automated lamella creation and ISLO. Red represents the amount of time an operator is sitting at the instrument creating the lamella. Yellow represents the amount of time an operator is manually performing the ISLO process. Blue represents a fully automated process where there is no operator required at the instrument.





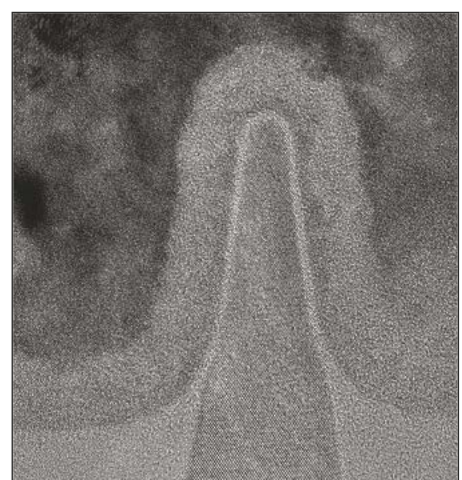


Figure 4. SEM cross-section image of a 22nm logic Fin-FET (top left), 30kV Bright Field STEM image (top right), and 200kV BF TEM image (bottom) using the in-situ liftout and transfer process.

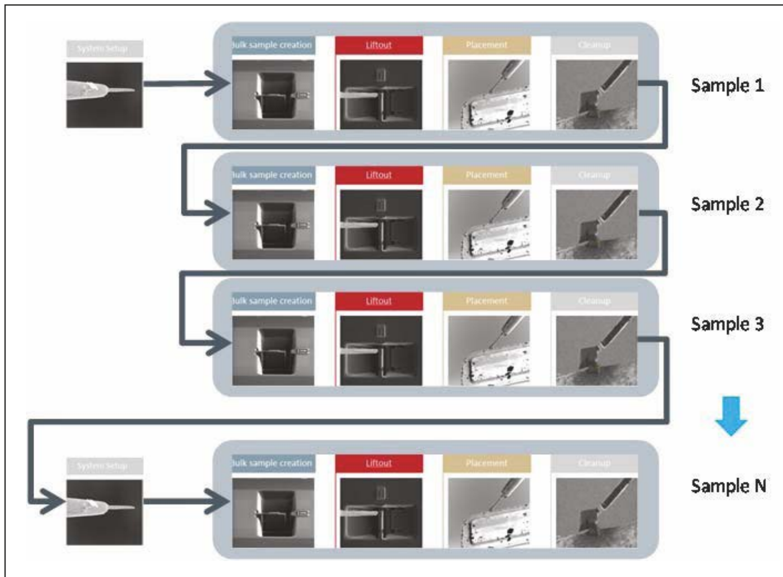


Figure 5. One possible sample process flow for lamella creation and ISLO using a fully automated recipe.

for transfer to TEM grids, the entire process can take up to 232 minutes (approximately 4 hours) assuming no breaks or interruptions. During this time, the technician is constantly interacting with the instrument. (Fig. 3)

In contrast, in high volume FA labs running fully automated recipes to create thick lamella for in-situ liftout, the time the operator is required to be in front of the instrument is greatly reduced. By using automated recipes to create the thick lamella, as previously shown in Fig. 1, the same dual beam system is able to run unattended for approximately 160 minutes.

During the nearly 3 hours that the DualBeam is running unattended, the technician can be working on an adjacent system to thin previously created lamella. In both cases, the end result of this process is a high quality, thinned lamella which will yield meaningful results in the TEM (Fig. 4)

With the addition of the capability to perform fully automated in situ lamella liftout and transfer, FA labs can gain further efficiencies by increasing the amount of time the DualBeam can run unattended. In this third scenario where even the liftout and transfer of the lamella is automated, after performing the initial setup to identify the region of interest and location on the TEM grid for the lamella, the DualBeam is able to run an entire 4 hours without operator intervention. In this case, a single technician would theoretically be able to operate two DualBeam systems, performing the final thinning on one instrument while another is automatically creating lamellae and transferring them to TEM grids.

Because these automated recipes can be configurable, one lab may choose to sequentially create all of the thick TEM lamellae and then perform the automated liftout afterwards, while another lab may choose to create and lift out each sample individually (Fig. 5). Similar to what happens with complex sample flows in the fab, labs are gaining the ability to configure and automate the process flow for each unique failure analysis sample, reducing the requirement for highly trained operators to be sitting at the tool. An additional benefit to increased automation is the ability to link data and process information at all stages of the FA process to each final image and report.

Conclusions

The development of automation software and integrated accessories for failure analysis equipment is now bringing more fab-like activities and processes into the FA lab. While highly trained technicians will always be an essential part of the FA lab, many of the tedious, repetitive tasks in the sample preparation process flow can now be handled automatically without the need for an operator at the tool. Standardizing and creating recipes for routine process steps which do not require the knowledge of trained technicians provides for a more efficient use of manpower. Labs moving to fully automated sample preparation recipes can significantly increase the number of high quality samples produced by each operator. Various automation components are now available to labs as they look to streamline the FA process to support the fab's ever increasing demand for more process data. As more and more automation moves into the FA lab one should not be surprised to see the proliferation of tools and blinking signal towers with only a few operators scattered throughout the lab.

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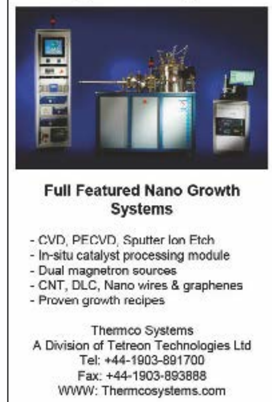

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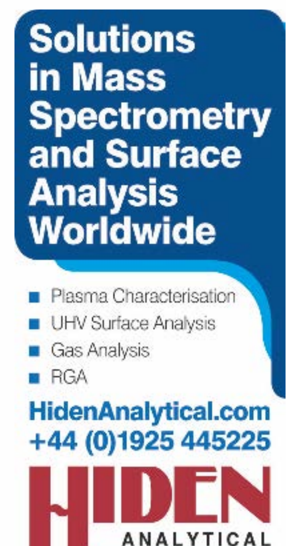

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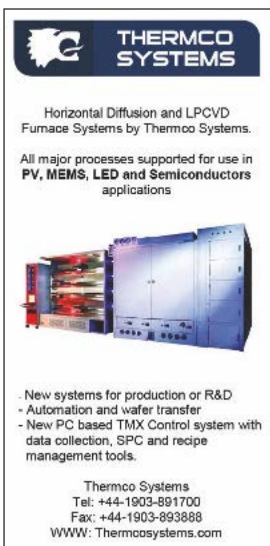

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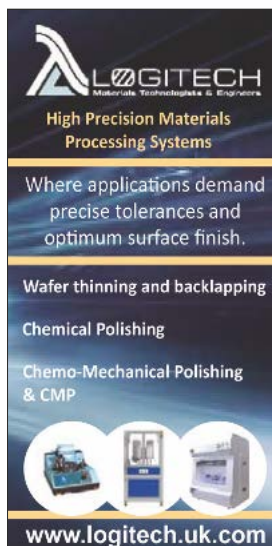

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