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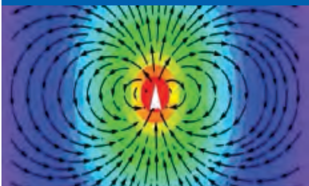

# Electroplating

An old technology for the future

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# executiveview

by Mark Andrews, USA Contributor

## Applied Materials & Tokyo Electron merger dissolves as regulators favour competition

WHO WAS SURPRISED when chip manufacturing equipment makers Tokyo Electron and Applied Materials had to call-off their engagement in April? Many market watchers said this get-together was doomed, that regulators took 18 months to formally arrive at a 'no-deal' consensus was the real surprise.

Market analysts and insiders had forecast a rocky road in part because both semiconductor companies held large market shares; combined they controlled about 25 percent. But Applied Materials and Tokyo Electron were not alone. Days after their split, the US Federal Communications Commission and Justice Department also gave a 'no-deal' stamp of disapproval to Time Warner's and Comcast's request to merge; their coupling would have created the number- one US provider of cable television, internet and related services with around 50 percent share.

On the semiconductor side, companies such as KLA-Tencor, Lam Research and ASML would have found the post-merger 'Eteris' intimidating, since its closest competitor would have only had half its share. The merger would have also given Applied Materials an insider's stake in Japanese business, which it earnestly sought. Creating a new competitive threat in Japan, still struggling to regain momentum, no doubt also concerned Japanese and American regulators. What both break-ups do signal is a 'new normal', that growing market share will depend more upon product innovation than it does buying-out the competition. These changes are occurring for two reasons.

First, major free market economies tried a 'hands-off' style of regulating that proved disastrous when the Great Recession bloomed. Second, the leaders at Applied Materials/Tokyo Electron suffered from bad timing; they decided to get together after so many others, making their hook-up less palatable from a competitive standpoint.

While the global economy is still recovering, there is a strong realization that large mergers almost always cost jobs and reduce competitors. Since these are high tech manufacturing jobs in Japan and the US, lost jobs also involve healthy salaries and benefits going away. Governments not only worry about competition-busting behemoths, but also dealing with entities that pay lower taxes due to off-shore headquarters.

One has to give Applied Materials and Tokyo Electron credit for trying to solve some of their long-term challenges while offering shareholders better earnings potential. Both companies find themselves fighting for share in a market with fewer players even through the overall pie grew about 10 percent in 2014. The leadership at Applied Materials and Tokyo Electron has seen that having a good Plan B is more critical than ever.

Having strong products and always looking for ways to innovate are central to that strategy. Mergers can and will continue—many are helpful to both consumers and business. But the 'Anything Goes' days are gone, at least for now.


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# JSR and imec partner to enable EUV lithography resist solutions

JSR CORPORATION and imec have signed a Letter of Intent to partner in enabling manufacturing and quality control of EUV lithography materials for the semiconductor industry. This partnership will be formalized by establishing a joint venture with imec as minority shareholder. The signing ceremony was held at the Embassy of the Kingdom of Belgium in Tokyo (Japan).

EUV lithography is considered as one of the main drivers to extend Moore's law towards single digit nanometer technology nodes. Imec and JSR's collaboration, will allow both companies to leverage their strengths when developing photoresist solutions for the semiconductor industry to manufacture the most advanced devices.

JSR will provide manufacturing technology to the joint venture including upgrading the facility at its wholly-owned subsidiary in Belgium, JSR Micro NV, by installing manufacturing and analytical equipment. Imec will provide expertise and services to the joint venture for quality control on materials. In addition to the manufacturing of JSR brand photoresists, the joint venture will offer toll-manufacturing capability to other material suppliers with confidentiality secured.

"JSR has been a strategic partner of imec for a long time, and I am excited with this intensified collaboration," stated Luc Van den hove, president and CEO at imec. "This collaboration strengthens our supplier hub concept, a neutral open innovation R&D platform that involves suppliers more deeply and at an early stage of process step and module development. The partnership enabled through close proximity between the JSR manufacturing facility and the imec technology platform will allow our partners to gain access to best-in-class materials for next-generation technologies."

"We know that EUV lithography is required to realize Moore's law in semiconductor manufacturing technologies and we continuously focus our R&D efforts to meet industry needs," said Nobu Koshiba, President of JSR Corporation. "JSR has successfully developed not only chemically amplified photoresists, but also newly designed chemistries with very high sensitivity and good productivity. Our strength has also extended to peripheral materials, such as multilayer materials.

The industry is requesting material suppliers to prepare manufacturing infrastructure and quality control capabilities for defect-free lithography solutions, as well as to improve photoresist performance to match EUV exposure equipment.

It is by knowing those industry needs and requirements very well, that we, two world leading organizations that have supported the semiconductor industry for a long time, come to this unique idea to form a manufacturing joint venture to support those future industry needs. This is done based on our very long, trust-worthy relationship with imec. This is a very exciting challenge for us and I have great respect for imec for their brave and challenging spirits."

# DelfMEMS RF-MEMS ohmic switch hits one billion operations milestone

DELFMEMS has announced that its twelve throw, RF-MEMS ohmic contact switch design has just passed the one billion test cycles milestone and is still going strong. Cybele Rolland, DelfMEMS CEO, explained, "Achieving the billion switch milestone is a major achievement for our FreeFlex design. Importantly, this is the first time an industrialised RF-MEMS contact switch has been show to achieve this level of performance, but this is only the beginning. Our second-generation production switches, which we will be shipping towards the end of 2016, are expected to achieve up to 50 billion operations. This ensures that they will reliably deliver the performances required for the next generation of handsets, LTE-A and beyond, with ultra-low insertion loss, outstanding isolation and superior linearity, which for end users translates to longer battery life, better call quality and massively increased data speeds."

There are key two innovations by DelfMEMS that help it achieve this breakthrough. First, although gold is currently used as the contact material, this will be replaced in the production switches by a metal compound that has been proven to be reliable for cold switching in excess of 50 billion cycles.

Second, its patented FreeFlex MEMS switch design ensures that the contact point is always changing slightly, which lengthens the life of the switch. The DelfMEMS RF-MEMS switch structure uses a new, integrated, micro-mechanical building block that is based on a robust, new IP portfolio that includes seven key patents and innovations.

It does not use a cantilever beam or bridge featuring a highly conductive electrode electrostatically actuated in order to create an ohmic contact resulting in a mechanical switching.

# Daimler and Qualcomm collaborate on connected car technologies

QUALCOMM TECHNOLOGIES, INC., a subsidiary of Qualcomm Incorporated and Daimler AG has announced a strategic collaboration focused on pioneering innovation in the connected car.

In the first phase of the collaboration, the companies will focus on transforming future vehicles with mobile technologies that enhance in-car experiences and vehicle performance such as 3G/4G connectivity, wireless charging technology for in-vehicle use and implementation of the Qualcomm Halo Wireless Electric Vehicle Charging (WEVC) technology.

In addition, the companies are jointly assessing the application of Qualcomm Technology's newly developed Automotive Solutions.

Qualcomm Technologies is collaborating with Daimler on its Wireless Power Transfer 2.0 high performance program for electric vehicles.

The Qualcomm Halo WEVC technology provides high performance and high power in a small vehicle package that could allow Daimler customers to charge their electric vehicles (EV) and plug-in hybrid EVs without ever having to plug them in. In addition, Qualcomm WiPower technology enables consumer electronics to charge wirelessly in-vehicle. "It's important that we remain on the cutting edge of technology and continue to deliver unparalleled experiences to our customers," says Prof. Dr. Thomas Weber, Member of the Board of Management of Daimler AG responsible for Group Research and Mercedes-Benz Cars Development.

"With this in mind, we are eager to jointly explore possible fields of future cooperation with an internationally leading tech firm like Qualcomm."

Qualcomm is helping the automotive industry create an entirely new landscape for communication, convenience, energy efficiency, infotainment and safety through its Qualcomm Snapdragon Automotive Solutions, while Daimler has a history of producing vehicles that embody these concepts.

Mercedes-Benz customers have come to expect vehicles equipped with numerous intelligent systems and sensors that enhance safety, convenience and comfort.

Together, the companies intend to combine automotive expertise to advance the connected car industry by delivering intelligently connected vehicles of the future that drive emission-free.

## Avago to buy Broadcom for $37 billion

AVAGO TECHNOLOGIES is acquiring the communication chip company Broadcom. The cash and stock transaction values the combined company at $77 billion. On completion of the acquisition, the combined annual revenues will be of approximately $15 billion.

Under the terms of the agreement, Avago will acquire Broadcom for $17 billion in cash consideration and the economic equivalent of approximately 140 million Avago ordinary shares, valued at $20 billion as of May 27, 2015, resulting in Broadcom shareholders owning approximately 32 percent of the combined company.

Based on Avago's closing share price as of May 27, 2015, the implied value of the total transaction consideration for Broadcom is $37 billion.

Avago intends to fund the $17 billion of cash consideration with cash on hand from the combined companies and $9 billion in new, fully-committed debt financing from a consortium of banks.

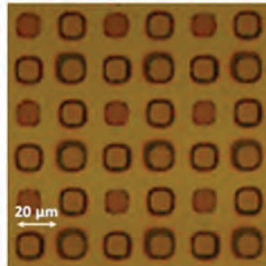
"Today's announcement marks the combination of the unparalleled engineering prowess of Broadcom with Avago's heritage of technology from HP, AT&T, and LSI Logic, in a landmark transaction for the semiconductor industry," said Hock Tan, president and COE of Avago.

"The combination of Avago and Broadcom creates a global diversified leader in wired and wireless communication semiconductors. Avago has established a strong track record of successfully integrating companies onto its platform. Together with Broadcom, we intend to bring the combined company to a level of profitability consistent with Avago's long-term target model."

# Fujifilm and imec demonstrate colour OLEDs with photoresist technology

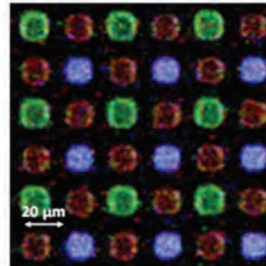
FUJIFILM CORPORATION and nano-electronics research institute, imec, have demonstrated full-colour organic light-emitting diodes (OLED)*1 by using their jointly-developed photoresist technology*2 for organic semiconductors, a technology that enables submicron*3 patterning. This breakthrough result paves the way to producing high-resolution and large organic Electroluminescent (EL) displays and establishing cost-competitive manufacturing methods.

**Enlarged images of the OLED array, whose performance has been verified this time**



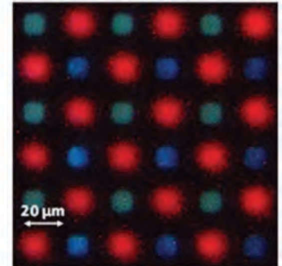

**Optical microscopic image**

The OLED array forms a pattern with subpixel pitch of 20µms to achieve a high resolution of 640ppi.




**Photoluminescent image**

The above image was taken with UV illumination on the OLED array, confirming that red, green and blue dots emit light separately.




**Electroluminescent image**

The above image was taken with voltage applied, instead of UV illumination. All the red, green and blue dots were confirmed to emit light, verifying its correct performance.

Organic EL displays are increasingly used for televisions, mobile devices including smartphones as well as wearable devices. Since they can be made thin and flexible, while also offering excellent response time and contrast ratio. It is said that today's products require organic EL displays of high pixel density, i.e. around 200ppi*4 for 4K televisions, 500ppi for full HD mobile devices and even higher density for compact displays for wearable devices. There has been active R&D for organic semiconductors to develop a high-resolution patterning method for organic EL materials to be used in these products.

In 2013, Fujifilm and imec jointly developed photoresist technology for organic semiconductors that enables submicron patterning without damaging the organic semiconductor materials, based on photolithography*5 capable of high-resolution patterning on large substrates. There is no need for additional capital investment since an existing i-line exposure system can be used for the new technology. This is why the technology has attracted wide attention since the development announcement with anticipation of a cost-effective way of manufacturing high-resolution organic semiconductor devices.

In the latest achievement, Fujifilm and imec produced full-color OLEDs with the photoresist technology for organic semiconductors and successfully verified their performance.  Red, green and blue organic EL materials were patterned, each in the subpixel pitch of 20$\mu$m*6, to create full-color OLEDs. An OLED array of 40 x 40 dots at the resolution of 640ppi was realized and illuminated with UV rays to confirm that red, green and blue dots separately emitted light. The emission of red, green and blue lights was also confirmed in a test involving the application of voltage rather than illumination, confirming its correct performance.

These results open new opportunities, such as using the novel photolithography in a multiple patterning process. An example would be creating an OLED array that adds a fourth color to red, green and blue, as well as developing previously-unseen devices such as a new sensors that integrate OLED with the organic photodetector*7.

# Infineon Technologies extends its medium voltage MOSFET portfolio

INFINEON TECHNOLOGIES has extended its medium voltage MOSFET portfolio with OptiMOS TM300 V, setting a new standard in the power MOSFET market. In doing so, the company confirms its position as market leader enabling energy efficient solutions in applications such as telecom systems, uninterruptible power supplies (UPS), motor control, industrial power supplies and DC/AC inverters.

The new OptiMOS 300 V helps system designers to increase power density and reduce cost with the highest level of reliability. Ultimately, for the end user, this translates into energy cost savings. For example, in hard switching applications such as AC/DC converters OptiMOS 300 V cuts energy losses by 50 percent. This allows for higher switching frequencies and, consequently, passive component and solution size reduction. Furthermore, OptiMOS 300 V can provide voltage spike headroom for better reliability, safety and ease of design in a 60 V telecom rectifier. The number of stages required in cascaded high voltage switch mode power supplies can also be reduced. Additionally, 110 V AC UPS can now be realized with OptiMOS 300 V.

"With 300 V blocking capability, Infineon extends the benchmark OptiMOS technology into a so far non-mainstream voltage class to support evolving applications such as multilevel converters," says Richard Kuncic, Vice President & General Manager Business Line DC/DC at Infineon Technologies AG.
"Due to superior performance of OptiMOS technology and the wide application spectrum, we expect this voltage class to become a new standard in the power MOSFET market."

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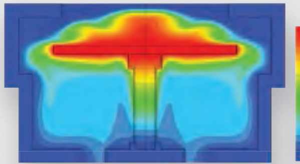
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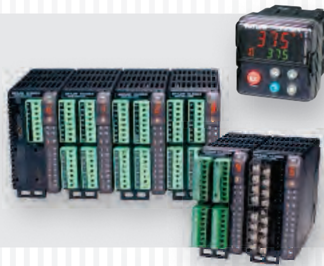
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# EV Group sees strong demand for emerging photonic applications

EV GROUP (EVG) has announced that its NILPhotonics Competence Centre—established to assist customers in enabling new and enhanced products and applications in the field of photonics—has generated strong interest from customers and resulted in multiple system orders since its launch in December 2014.

New system orders have included the company's EVG700/7000 Series UV-NIL (UV nanoimprint lithography) systems with SmartNIL technology to support high-volume manufacturing applications, including displays, light emitting diodes (LEDs) and wafer-level optics. Since its initial launch, the NILPhotonics Competence Center has also expanded the products and applications it is supporting.

These include photonic and microfluidic devices for bio-medical applications that pave the way for faster and more accurate diagnosis of diseases, as well as plasmonic structures that simultaneously carry optical and electrical signals and can be scaled to the smallest dimensions to enable new chip designs as well as better-performing devices, such as waveguides and sensors.

"The prevailing perception has been that despite the potential benefits of NIL technology, the barrier to entry for integrating it into high-volume manufacturing (HVM) is high. That simply isn't the case. EV Group has invested significant resources over many years in developing NIL technology as an HVM-capable solution for a number of applications," stated Markus Wimplinger, corporate technology development and IP director at EV Group.

"Today, we have the world's largest installed base ofmore than 200 systems at customer facilities around the globe supporting volume-manufacturing of LEDs, MEMS, optics, photovoltaics and other devices. Our NILPhotonics Competence Center allows us to more easily bring all of our process and product capabilities and expertise to bear in helping our customers enable new photonic products and applications."

EVG's NILPhotonics Competence Center leverages EVG's field-proven process and equipment know-how in NIL and other process areas such as wafer bonding to support emerging photonic applications and significantly shorten time to market through fast process implementation and optimization, as well as through customized equipment design.

In addition, EVG has a global partner network to draw from to support its customers' process integration and optimization efforts across the NIL infrastructure, including template manufacturing, resist materials and supporting equipment. As a result, EVG is able to provide consultation and support across all phases of the product lifecycle—from design for manufacturing and prototyping through process development, qualification runs, pilot manufacturing and process transfer.

# Infineon reports 31 percent revenue jump

EARLIER THIS YEAR, Infineon's CEO Reinhard Ploss said the acquisition of International Rectifier (IR) had opened a new chapter in Infineon's history, moving it into the 'fast lane'. Reporting its Q2 results (the first since IR's lines of business have been included) Infineon has recorded a very positive 31 percent revenue boost of €355 million from €1,128 million to €1,483 million.

"Business was running very well, with additional tailwinds provided by the acquisition of International Rectifier and the strong dollar", stated Reinhard Ploss, CEO of Infineon Technologies AG.
He added: "The signals we are receiving from our markets are generally positive. We are making good progress with the integration of International Rectifier. Our strategy is paying off and Infineon remains on a growth path."

The acquisition of IR, which concluded on 13th January 2015, extends Infineon's compound semiconductor technology for power electronics. In recent years, Infineon has become a leading vendor of SIC power semiconductors. IR is a globally recognised specialist for chips based on GaN, a technology that was key to the acquisition.

The integration of IR into the Infineon is proceeding according to plan, according to the company. At the latest in fiscal year 2017, IR's margin contribution is expected to be at least in line with Infineon's target of 15 percent Segment Result margin over the cycle.
Sales have been integrated into one joint team since March.

In addition, many key organizational changes have already been completed. Infineon has also started the optimization of the product portfolio. In March, the combined range of GaN products was presented at the US trade fair for power electronics - APEC 2015, for example.

Additionally, a comprehensive concept for the combined production network has been drawn up. The company will be discontinuing manufacturing operations at Techview in Singapore by the end of the year.

Production in Newport, Wales, will be running at full capacity until the end of calendar year 2016 and will then be phased out in 2017. In parallel, the company is looking for a buyer to take over and continue to operate the factory.

Based on an assumed exchange rate of US$ 1.10 to the euro, Infineon expects quarter- on-quarter revenue growth of between 7 and 11 percent in the third quarter of the 2015 fiscal year. All segments are forecast to make a contribution to the expected revenue growth. At the mid-point of the growth range, the Segment Result Margin is expected to be about 15 percent.

# Dow Corning collaborate with IBM on thermal interface material

DOW CORNING has unveiled new Dow Corning TC-3040 Thermally Conductive Gel, a next-generation thermal interface material (TIM 1). Developed through the help of IBM, this cutting-edge new material offers more effective and reliable thermal management, reduced stress and excellent under-die coverage for demanding flip chip applications the company says. Dow Corning unveiled the new product technology here at the IEEE Electronic Components and Technology Conference (ECTC 2015).

TIM-1 solutions are a class of high-purity, thermal interface materials that are applied between the chip surface and a heat spreader to help dissipate damaging heat to the exterior of a semiconductor package. However, as applications from data centers to consumer devices to automotive electronics all demand higher functioning integrated semiconductor devices with increasing processing power, the temperatures within chip packages are rapidly increasing and testing the limits of conventional TIM-1 solutions.

"A long-time member of IBM's ecosystem, Dow Corning brought decades of expertise in advanced silicone technology to help formulate this break-through TIM-1 material for high-end chip packaging," said Andrew Ho, global market segment leader, Semiconductor Packaging Materials at Dow Corning. "It is only the latest innovation on the ambitious roadmap of thermal management solutions that Dow Corning has planned for this rapidly evolving global market."

The successful efforts of IBM and Dow Corning scientists have raised the bar for TIM-1 performance. Dow Corning TC-3040 Thermally Conductive Gel delivers nearly two times the thermal performance of other industry standard TIMs, as well as high thermal conductivity targeting 4W/mK with robust reliability. As a result, it offers chip-makers broader design options for high-performing yet more reliable ICs with improved thermal management."

# Microsemi completes acquisition of Vitesse

MICROSEMI CORPORATION and Vitesse Semiconductor Corporation jointly announced that Microsemi's wholly-owned subsidiary LLIU100 Acquisition Corp. successfully merged into Vitesse, completing Microsemi's acquisition of Vitesse under Section 251(h) of the General Corporation Law of the State of Delaware (the "DGCL"), with no vote of Vitesse's stockholders required to consummate the merger.

At the effective time of the merger, each outstanding share of Vitesse (other than shares directly owned by Vitesse and its subsidiaries, Microsemi or LLIU100 Acquisition Corp. and shares held by stockholders that are entitled to and properly demand appraisal of such shares under Delaware law) was converted into the right to receive $5.28 per share in cash, without interest and less any applicable withholding taxes, the same price that was paid in the tender offer. Following the merger, Vitesse shares will cease to be traded on Nasdaq.

Headquartered in Camarillo, California, Vitesse designs a diverse portfolio of high-performance semiconductors, application software, and integrated turnkey systems solutions for carrier, enterprise and Internet of Things (IoT) networks worldwide. Vitesse's products enable the fastest-growing network infrastructure markets including mobile access/IP edge, enterprise cloud access, and industrial IoT networking.


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# Apple watch success needed for a smartwatch mega boom

THE SMARTWATCH market will grow from 3.6 million unit shipments in 2014, to 101 million shipments in 2020 according to a new report released today by IHS Inc.

"Apple Watch success will drive the overall smartwatch market," said Antonios Maroulis, analyst at IHS Technology. "The smartwatch will become a key accessory device offered by most leading smartphone manufacturers seeking to dominate this new profitable market. We forecast the ratio of smartwatch shipments to smartphone shipments will increase from 1:500 to 1:20 between 2014 and 2020."

Apple's entry into the smartwatch market will benefit all smartwatch suppliers as Apple's marketing raises consumer awareness of the category and explains the benefits clearly. The Apple Watch will leave an enormous addressable market untapped because the Apple Watch requires a modern iPhone and has a starting price of $349 USD. The two billion Android smartphone users and those Apple customers unwilling to spend so much on a smartwatch is a large target for Android smartwatch makers.

In the IHS baseline smartwatch forecast, Apple's 2015 Apple Watch shipments will hit 19 million units, or 56 percent

of the total smartwatch market. Over time, IHS forecasts Apple's share of the market will fall to 38 percent in 2020 as other smartwatch makers refine their products and successfully serve the vast Android smartphone market, which Apple chooses not to address.

Google's Android Wear will ship 96 million units over the next five years, leveraging the vast Android smartphone installed base. Should Google add iPhone support, it will increase its addressable market still further, the IHS report says.

"Should Apple stumble with its foray into smartwatches, the smartwatch market will suffer similarly. Smartwatches could then follow the fate of Google Glass. Without Apple and its marketing strength, the smartwatch category needs greater marketing spend from other smartwatch makers to overcome damage to consumer perceptions," forecasts Ian Fogg, senior director of Mobile & Telecoms at IHS. "Apple's smartwatch competitors need the Apple Watch to succeed."

"Delivering a wide range of apps will be critical for smartwatch success," Maroulis said. "Apple's and Google's success with existing smartphone application stores will give them an invaluable head start over challengers."

Apple has an advantage in smartwatches because of the quality and range of apps for iOS devices such as the iPhone and the iPad. Similarly, Google has a head start because of the Google Play Android app store. Device makers may find tactical success in the short run with proprietary OS platforms such as Pebble or niche open platforms such as Tizen which Samsung supports. But in the long term, only standard platforms that are supported by many hardware makers will deliver sufficient scale to prove attractive to app makers. Because of weak app ecosystems, IHS forecasts other smartwatch OS devices, excluding Apple and Android Wear, to amount to just 40 percent of smartwatch shipments in 2020.

# Rudolph wins lithography and inspection orders

RUDOLPH TECHNOLOGIES, INC has announced that a major outsourced assembly and test (OSAT) manufacturer has placed a $12 million order for a follow-on JetStep Advanced Packaging Lithography System and multiple NSX Inspection Systems for use in their planned capacity expansion. The tools, which will ship this quarter and next, will be used in high-performance fan-out wafer level packaging (FOWLP) applications.

"The JetStep System will be equipped with new hardware and software features that significantly increases our industry-best productivity. These upgrades will also be applied to the existing installed base, providing our customer with a significant capacity increase at a best-in-class cost-of-ownership," said Rich Rogoff, vice president and general manager of Rudolph's Lithography Systems Group. "The JetStep System continues to be the clear choice for advanced packaging fan-out wafer level processes due to its ability to handle warped wafers with varying die placement."

"In addition to lithography, we are pleased to supply the latest 2D and 3D inspection and metrology solutions for the same FOWLP applications," added Mike Goodrich, vice president and general manager of the Rudolph's Inspection Business Unit.

"Our newest NSX Systems offer the fast, reliable inspection and metrology needed for demanding advanced packaging applications, such as photoresist thickness and redistribution layer (RDL) and under bump metallization (UBM) height measurements."

Further enhancing both the JetStep System and the NSX Systems is Rudolph's Discover Yield Management Software, which enables yield improvement through real-time analysis for faster solutions, increasing the productivity of each tool and the overall fab yield. The JetStep Advanced Packaging Lithography Systems have been specifically designed to meet the challenges of back-end manufacturing.

# OKI develops mass-production technology for multi-layer printed circuit boards

OKI CIRCUIT TECHNOLOGY has successfully developed design and mass production technologies for multi-layer printed circuit boards that support high speeds and high frequencies based on copper coin insertion. The new technology achieves a 20-fold improvement in heat dissipation over existing technologies.

Mass production of printed circuit boards based on the new technology began in April 2015 for use in the latest large-volume data communication devices. Sales forecasts for this fiscal year are 200 million yen.

OKI Circuit Technology say they have successfully developed a new "T-Coin (Technology of copper Coin insert) structure" that increases the area available for heat conduction for a limited number of through-holes by inserting cylindrical copper (copper coins) into through-holes without leaving gaps using a specially-developed method

that minimizes pressure loading. "This technology improves heat dissipation performance 20-fold while ensuring high reliability and long service life.

Heat-generating components are in direct contact with large areas of copper with high thermal conductivity, ensuring high heat dissipation performance," says Masahito Nozue, President of OKI Circuit Technology. "The technology is expected to contribute to the development of products that achieve adequate heat dissipation performance, even without cooling fans or heat sinks."

The newly developed T-Coin structure was made possible by manufacturing techniques that control the shape and thickness of the copper coins to micron levels, along with machining pressure rate control techniques that prevent damage when copper coins make contact with the through-hole plating.

The technology is compatible with a wide range of copper coin diameters (3.0 mm to 6.0 mm) and printed circuit board thicknesses (1.0 mm to 2.0 mm) for ready customization and application to all stages of the process, from simulation and prototyping to mass production of printed circuit boards, for a wide range of uses.

In the lead-up to the start of mass production, OKI Circuit Technology developed and introduced a copper coin insertion apparatus based on its own specifications to ensure uniform pressure when inserting copper coins into through-holes.

# China's smartphone market contracts for the first time in six years

IDC's latest Mobile Phone Tracker shows the China smartphone market contracted by 4 percent year over year (YoY) with 98.8 million units shipped in the first quarter of 2015. This is the first time in six years that the China smartphone market declined YoY as the market continues to mature. On a quarter over quarter (QoQ) basis, the market contracted 8 percent on the back of a large inventory buildup at the end of last year.

"Smartphones are becoming increasingly saturated in China," said Kitty Fok, Managing Director at IDC China. "China is oftentimes thought of as an emerging market but the reality is that the vast majority of phones sold in China today are smartphones, similar to other mature markets like the US, UK, Australia, and Japan. Just like these markets, convincing existing users as well as feature phone users to upgrade to new smartphones will now be the key to further growth in the China market."

Apple was the top smartphone vendor in China in the first quarter of 2015, with consumers still having a strong appetite for the larger screens on the iPhone 6 and iPhone 6 Plus.

Xiaomi slipped to the second position as it faced strong competition from other vendors in the low to mid-range segment of the market, while Huawei maintained third position as it saw a good uptake in the mid-range segment. Samsung and Lenovo both led the market at least once last year, but rankings have since changed quickly, highlighting the volatility of consumers' brand preference in China. IDC expects relatively flat growth for China in 2015.

Other trends to expect in China this year include:

Multi-brand strategies. Huawei and ZTE are positioning younger sub-brands Honor and nubia, respectively, to chip away at Xiaomi's user base, and to attempt to gain a loyal fanbase. Lenovo is also getting into the mix with the Motorola acquisition, not to mention its upcoming online-focused Shenqi division.

# New understanding of electromagnetism could enable 'antennas on a chip'

New understanding of the nature of electromagnetism could lead to antennas small enough to fit on computer chips – the 'last frontier' of semiconductor design – and could help identify the points where theories of classical electromagnetism and quantum mechanics overlap.

A TEAM OF RESEARCHERS from the University of Cambridge have unravelled one of the mysteries of electromagnetism, which could enable the design of antennas small enough to be integrated into an electronic chip. These ultra-small antennas -- the so-called 'last frontier' of semiconductor design -- would be a massive leap forward for wireless communications.

In new results published in the journal Physical Review Letters, the researchers have proposed that electromagnetic waves are generated not only from the acceleration of electrons, but also from a phenomenon known as symmetry breaking. In addition to the implications for wireless communications, the discovery could help identify the points where theories of classical electromagnetism and quantum mechanics overlap.

The phenomenon of radiation due to electron acceleration, first identified more than a century ago, has no counterpart in quantum mechanics, where electrons are assumed to jump from higher to lower energy states. These new observations of radiation resulting from broken symmetry of the electric field may provide some link between the two fields.

The purpose of any antenna, whether in a communications tower or a mobile phone, is to launch energy into free space in the form of electromagnetic or radio waves, and to collect energy from free space to feed into the device. One of the biggest problems in modern electronics, however, is that antennas are still quite big and incompatible with electronic circuits -- which are ultra-small and getting smaller all the time.

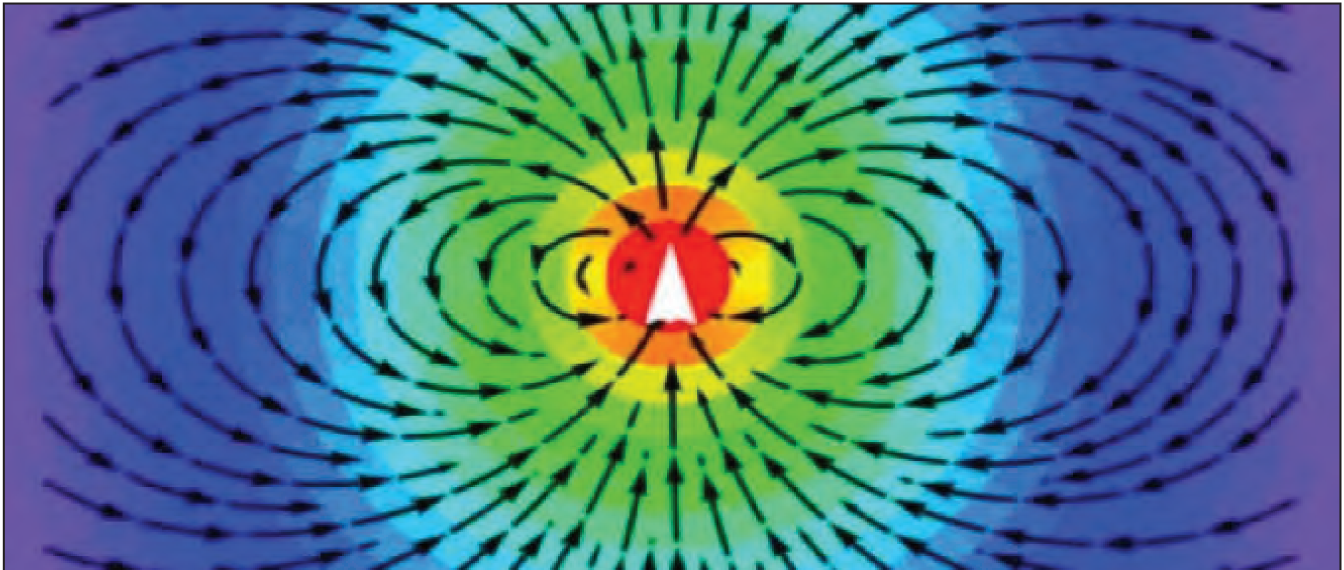
"Antennas, or aerials, are one of the limiting factors when trying to make smaller and smaller systems, since below a certain size, the losses become too great," said Professor Gehan Amaratunga of Cambridge's Department of Engineering, who led the research. "An aerial's size is determined by the wavelength associated with the transmission frequency of the application, and in most cases it's a matter of finding a compromise between aerial size and the characteristics required for that application."

Another challenge with aerials is that certain physical variables associated with radiation of energy are not well understood. For example, there is still no well-defined mathematical model related to the operation of a practical aerial. Most of what we know about electromagnetic radiation comes from theories first proposed by James Clerk Maxwell in the 19th century, which state that electromagnetic radiation is generated by accelerating electrons.

However, this theory becomes problematic when dealing with radio wave emission from a dielectric solid, a material which normally acts as an insulator, meaning that electrons are not free to move around. Despite this, dielectric resonators are already used as antennas in mobile phones, for example. "In dielectric aerials, the medium has high permittivity, meaning that the

"Antennas, or aerials, are one of the limiting factors when trying to make smaller and smaller systems, since below a certain size, the losses become too great,"

Professor Gehan Amaratunga of Cambridge's Department of Engineering



Credit: Generated using Mathematica from Wolfram Inc

The radiation pattern from a dipole antenna showing symmetry breaking of the electric field.

velocity of the radio wave decreases as it enters the medium," said Dr Dhiraj Sinha, the paper's lead author. "What hasn't been known is how the dielectric medium results in emission of electromagnetic waves. This mystery has puzzled scientists and engineers for more than 60 years."

Working with researchers from the National Physical Laboratory and Cambridge-based dielectric antenna company Antenova Ltd, the Cambridge team used thin films of piezoelectric materials, a type of insulator which is deformed or vibrated when voltage is applied. They found that at a certain frequency, these materials become not only efficient resonators, but efficient radiators as well, meaning that they can be used as aerials.

The researchers determined that the reason for this phenomenon is due to symmetry breaking of the electric field associated with the electron acceleration. In physics, symmetry is an indication of a constant feature of a particular aspect in a given system. When electronic charges are not in motion, there is symmetry of the electric field. Symmetry breaking can also apply in cases such as a pair of parallel wires in which electrons can be accelerated by applying an oscillating electric field. "In aerials, the symmetry of the electric field is broken 'explicitly' which leads to a pattern of electric field lines radiating out from a transmitter, such as a two wire system in which the parallel geometry is 'broken'," said Sinha.

The researchers found that by subjecting the piezoelectric thin films to an asymmetric excitation, the symmetry of the system is similarly broken, resulting in a corresponding symmetry breaking of the electric field, and the generation of electromagnetic radiation. The electromagnetic radiation emitted from dielectric materials is due to accelerating electrons on the metallic electrodes attached to them, as Maxwell predicted, coupled with explicit symmetry breaking of the electric field.

"If you want to use these materials to transmit energy, you have to break the symmetry as well as have accelerating electrons -- this is the missing piece of the puzzle of electromagnetic theory," said Amaratunga. "I'm not suggesting we've come up with some grand unified theory, but these results will aid understanding of how electromagnetism and quantum mechanics cross over and join up. It opens up a whole set of possibilities to explore."

The future applications for this discovery are important, not just for the mobile technology we use every day, but will also aid in the development and implementation of the Internet of Things: ubiquitous computing where almost everything in our homes and offices, from toasters to thermostats, is connected to the internet. For these applications, billions of devices are required, and the ability to fit an ultra-small aerial on an electronic chip would be a massive leap forward. Piezoelectric materials can be made in thin film forms using materials such as lithium niobate, gallium nitride and gallium arsenide.

Gallium arsenide-based amplifiers and filters are already available on the market and this new discovery opens up new ways of integrating antennas on a chip along with other components.

"It's actually a very simple thing, when you boil it down," said Sinha. "We've achieved a real application breakthrough, having gained an understanding of how these devices work."

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# Beyond the lithium ion

## Significant step toward a better performing battery

Researchers have taken a significant step toward the development of a battery that could outperform the lithium-ion technology used in electric cars such as the Chevy Volt. They have shown they can replace the lithium ions, each of which carries a single positive charge, with magnesium ions, which have a plus-two charge, in battery-like chemical reactions, using an electrode with a structure like those in many of today's devices.

THE RACE IS ON around the world as scientists strive to develop a new generation of batteries that can perform beyond the limits of the current lithium-ion based battery.

Researchers at the University of Illinois at Chicago have taken a significant step toward the development of a battery that could outperform the lithium-ion technology used in electric cars such as the Chevy Volt.

They have shown they can replace the lithium ions, each of which carries a single positive charge, with magnesium ions, which have a plus-two charge, in battery-like chemical reactions, using an electrode with a structure like those in many of today's devices.

"Because magnesium is an ion that carries two positive charges, every time we introduce a magnesium ion in the structure of the battery material we can move twice as many electrons," says Jordi Cabana, UIC assistant professor of chemistry and principal investigator on the study.

"We hope that this work will open a credible design path for a new class of high-voltage, high-energy batteries," Cabana said.
The research is part of the Joint Centre for Energy Storage Research, a Department of Energy Innovation Hub led by Argonne National Laboratory that aims to achieve revolutionary advances in battery performance. The study is online in advance of print in the journal Advanced Materials.

Every battery consists of a positive and negative electrode and an electrolyte. The electrodes exchange electrons and ions, which are usually of positive charge. Only the ions flow through the electrolyte, which is an electric insulator so as to force the electrons to flow through the external circuit to power the vehicle or device.

To recharge the battery, the exchange is reversed. But the chemical reaction is not perfectly efficient, which limits how many times the battery can be recharged.
"The more times you can do this back and forth, the more times you will be able to recharge your battery and still get the use of it between charges," Cabana said. "In our case, we want to maximize the number of electrons moved per ion, because ions distort the structure of the electrode material when they go in or leave. The more the structure is distorted, the greater the energy cost of moving the ions back, the harder it becomes to recharge the battery."

"Like a parking garage, there are only so many spaces for the cars," Cabana said. "But you can put a car in each space with more people inside without distorting the structure."

Having established that magnesium can be reversibly inserted into electrode material's structure brings us one step closer to a prototype, said Cabana.

"It's not a battery yet, it's piece of a battery, but with the same reaction you would find in the final device," said Cabana.

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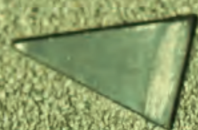

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# Materials scientists putting new spin on computing memory

As computers continue to shrink – moving from desks and laps to hands and wrists – memory has to become smaller, stable and more energy conscious. A group of researchers is trying to do just that with help from a new class of materials, whose magnetism can essentially be controlled by the flick of a switch.

This is a colorized scanning transmission electron micrograph of the LSMO / PZT interface. Using aberration-corrected electron microscopy, the authors are able to resolve small changes in atomic structure and chemistry at nearly the picometer scale. This yields a valuable and unprecedented new insight into the properties of oxide interfaces.

Ever since computers have been small enough to be fixtures on desks and laps, their central processing has functioned something like an atomic Etch A Sketch, with electromagnetic fields pushing data bits into place to encode data. Unfortunately, the same drawbacks and perils of the mechanical sketch board have been just as pervasive in computing: making a change often requires starting from the beginning, and dropping the device could wipe out the memory altogether.

As computers continue to shrink--moving from desks and laps to hands and wrists--memory has to become smaller, stable and more energy conscious. A group of researchers from Drexel University's College of Engineering is trying to do just that with help from a new class of materials, whose magnetism can essentially be controlled by the flick of a switch.

The team, led by Mitra Taheri, PhD, Hoeganaes associate professor in the College of Engineering and head of the Dynamic Characterization Group in the Department of Materials Science and Engineering, is searching for a deeper understanding of materials that are used in spintronic data storage. Spintronics, short for "spin transport electronics," is a field that seeks to harness the natural spin of electrons to control a material's magnetic properties. For an application like computing memory, in which magnetism is a key element, understanding and manipulating the power of spintronics could unlock many new possibilities.

Current computer data storage takes one of two main forms: hard drives or random access memories (RAM). You can think of a hard drive kind of like a record or CD player, where data is stored on one piece of material--a hard disk--and accessed by a magnetic read head, which is the computer's equivalent of the record player's needle or the CD player's laser. RAM stores data by encoding it in binary patterns of electrical charges called bits. An external electric field nudges electrons into or out of capacitors to create the charge pattern and encode the data.

To store data in either type of memory device we must apply an external magnetic or electric field--either to read or write the data bits. And generating these fields draws quite a bit of energy. In a desktop computer that might go unnoticed, but in a handheld device or a laptop, quality is based, in large part, on how long the battery lasts.

Spintronic memory is an attractive alternative to hard drives and RAM because the material could essentially rewrite itself to store data. Eliminating the need for a large external magnetic field or a read head would make the device less power-intensive and more rugged because it has fewer moving parts. "It's the difference between a pre-whiteout typewriter and the first word processor," said Steven Spurgeon, PhD, an alumnus whose doctoral work contributed to the team's recently published research in Nature Communications. "The old method required you to move a read head over a bit and apply a strong magnetic field, while the newer one lets you insert data anywhere on the fly. Spintronics could be an excellent, non-destructive alternative to current hard drive and RAM devices and one that saves a great deal of battery life."

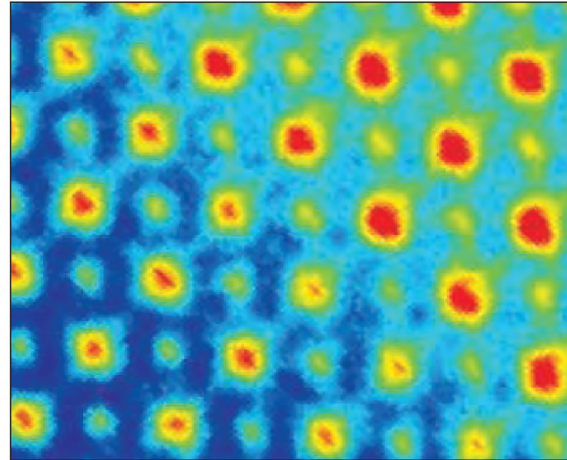
While spintronic materials have been used in sensors and as part of hard drive read heads since the early 2000s, they have only recently been explored for direct use in memories. Taheri's group is closely examining the physical principles behind spintronics at the atomic scale to look for materials that could be used in memory devices. "We're trying to develop a framework to understand how the many parameters--structure, chemistry, magnetism and electronic properties--are related to each other," said Taheri, who is the principle investigator on the research program, funded by the National Science Foundation and the Office of Naval Research. "We're peering into these properties at the atomic scale and probing them locally, in contrast to many previous studies. This is an important step toward more predictive and far-reaching use of spintronics."

Theoretically, spintronic storage could encode data by tuning electron spins with help from a special, polarized electrical current running through the material. The binary pattern is then created by the "up" or "down" spin of the electrons, rather than their presence "in" or "out" of a capacitor.

To better understand how this phenomenon occurs, the team took a closer look at structure, chemistry and magnetism in a layered thin film oxide material that has shown promise for use in spintronic data storage, synthesized by researchers at the University of Illinois--Urbana Champaign.

The researchers used advanced scanning transmission electron microscopy, electron energy loss spectroscopy and other high-resolution techniques to observe the material's behavior at the intersections of the layers, finding that parts of it are unevenly electrically polarized--or ferroelectric.

"Our methodology revealed that polarization varies throughout the material--it is not uniform," said Spurgeon, who is now a postdoctoral research associate at Pacific Northwest National Laboratory. "This is quite significant for spintronic applications because it suggests how the magnetic properties of the material can be tuned locally. This discovery would not have been possible without our team's local characterization strategy."



Credit: Drexel University

They also used quantum mechanical calculations to model and simulate different charge states in order to explain the behaviour of the structures that they observed using microscopy. These models helped the team uncover the key links between the structure and chemistry of the material and its magnetic properties.

"Electronic devices are continually shrinking." Taheri said. "Understanding these materials at the atomic scale will allow us to control their properties, reduce power consumption and increase storage densities. Our overarching goal is to engineer materials from the atomic scale all the way up to the macroscale in a predictable way. This work is a step toward that end."

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# Ultra-sensitive sensor detects individual electrons

Scientists have created an electronic device so accurate that it can detect the charge of a single electron in less than one microsecond. It has been dubbed the 'gate sensor' and could be applied in quantum computers of the future to read information stored in the charge or spin of a single electron.

A SPANISH-LED TEAM of European researchers at the University of Cambridge has created an electronic device so accurate that it can detect the charge of a single electron in less than one microsecond. It has been dubbed the 'gate sensor' and could be applied in quantum computers of the future to read information stored in the charge or spin of a single electron.

In the same Cambridge laboratory in the United Kingdom where the British physicist J.J. Thomson discovered the electron in 1897, European scientists have just developed a new ultra-sensitive electrical-charge sensor capable of detecting the movement of individual electrons.

"The device is much more compact and accurate than previous versions and can detect the electrical charge of a single electron in less than one microsecond," M. Fernando González Zalba, leader of this research from the Hitachi Cambridge Laboratory and the Cavendish Laboratory, said.

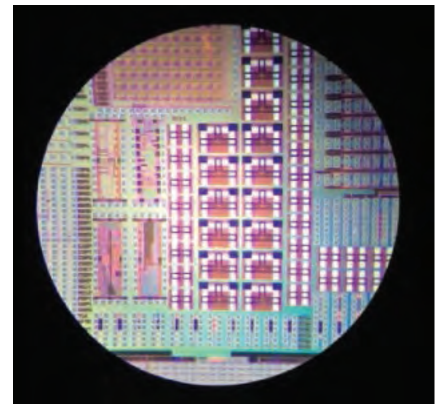
Details of the breakthrough have been published in the journal Nature Communications and its authors predict that these types of sensors, dubbed 'gate sensors', will be used in quantum computers of the future to read information stored in the charge or spin of a single electron.

"We have called it a gate sensor because, as well as detecting the movement of individual electrons, the device is able to control its flow as if it were an electronic gate which opens and closes," explains González Zalba.

The researchers have demonstrated the possibility of detecting the charge of an electron with their device in approximately one nanosecond, the best value obtained to date for this type of system. This has been achieved by coupling a gate sensor to a silicon nanotransistor where the electrons flow individually.

In general, the electrical current which powers our telephones, fridges and other electrical equipment is made up of electrons: minuscule particles carrying an electrical charge travelling in their trillions and whose collective movement makes these appliances work.

However, this is not the case of the latest cutting-edge devices such as ultra-precise biosensors, single electron transistors, molecular circuits and quantum computers. These represent a new technological sector which bases its electronic functionality on the charge of a single electron, a field in which the new gate sensor can offer its advantages.



Credit: TOLOP

A silicon chip was used for the design of the gate sensor.

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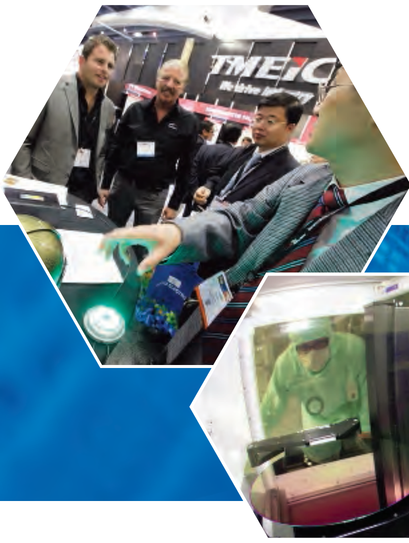
M. F. Gonzalez-Zalba, S. Barraud, A. J. Ferguson, A. C. Betz. Probing the limits of gate-based charge sensing. Nature Communications, 2015; 6: 6084 DOI: 10.1038/ncomms7084



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**What's New in Flexible Printed Electronics**—This program will examine the impact of flexible, hybrid electronics on new products and innovation, and investigate flexible hybrid manufacturing techniques. Industry leaders will discuss the latest thinking about electronics on plastic, paper, and glass, also the implications of flexible electronics designs for long-lasting and always-on IoT.

**Next Generation Non-volatile Memory: MRAM, RRAM and 3DNAND**—Learn about the state of emerging memory technologies and the challenges for high volume manufacture.

**Challenges for Getting to 5 nm, Photolithography and Transistor Scaling**—Explores high volume manufacturing solutions, including the role that EDA tools will play. Examines lithography cost and productivity issues in achieving 5 nm and below.

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# Electroplating

## An old technology for the future

Kevin Witt, ClassOne Technology Vice President, offers insight into ways that classic electroplating processes are being updated to address the industry's latest metal deposition requirements.

ALTHOUGH IT MAY SEEM counterintuitive, a great many of the industry's most advanced devices, such as compound semiconductors, MEMs and smart sensors that are used in the latest electronics applications, are not built using the most advanced process technology on the largest wafers. There are a couple of reasons for this. In many cases, such as analog devices, the desired level of functionality can be achieved using 90 nm or larger critical dimensions rather than today's leading-edge 14 nm standard. In others, it can be cost. It makes no sense to invest in a 300 mm process line if market demand can be met using 200 mm wafers.

While large semiconductor manufacturers, especially those producing large volumes of logic or memory devices, have adopted the latest in metal deposition technology, many others have found that time-tested methods of depositing metal onto substrates — such as sputtering and evaporation — have cost-effectively met their requirements. That is changing. As technologies such as wafer-level packaging are increasingly adopted, these useful and relatively inexpensive techniques are reaching their limits. This article will briefly describe some of these limitations and suggest a proven alternative that can overcome them.

### Capability limits

Sputtering and evaporation are limited in three main areas when it comes to wafer-level packaging applications: poor step coverage; limited feature fill; and poor metal lift-off for small features. Sputtering, for example, is mostly a line-of-sight process that relies on probability and randomness to uniformly deposit the desired thickness of metal on the substrate. High-aspect features, such as deep vias, the thick resist used for copper pillars, or the narrowly spaced lines found in redistribution layers cannot be properly filled. For structures that span different elevations within a die, it can be virtually impossible to achieve greater than 20-30 percent step coverage, even if continuity can be maintained. At the same time, once aspect ratios increase much beyond 3:1, filling features with metal, whether

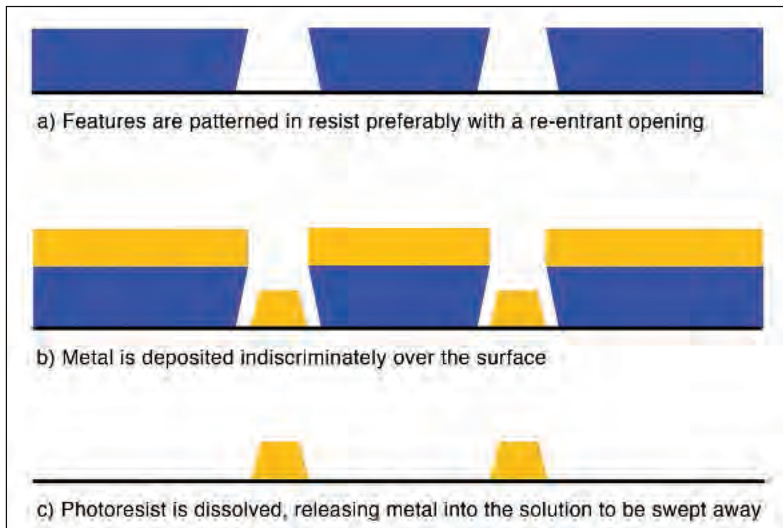


Figure 1. A simplified metal lift-off process.

via sputtering or evaporation, can be compromised by overhangs and step coverage limitations that can result in defects such as voids. Both techniques typically require the removal of excess metal from the substrate. As feature sizes become smaller, however, metal lift-off (Figure 1) becomes a problem because the features are so small they no longer adhere well to the substrate during subsequent processing. Similarly, the edges of features become less well defined and ragged, leading to an increased susceptibility to other types of defects, as well as introducing additional integration issues and challenges.

## Cost

Sputtering and evaporation both cease to be cost-effective techniques when depositing the types of thick films required to build advanced devices used in wafer-level packaging. Sputtering, for example, is a slow process that becomes extremely expensive when depositing films over a few tenths of a micron in thickness. It would cost a relative fortune and take an unreasonable amount of time to sputter the metal needed for a 90 micron copper pillar, even if the film stress could be managed.

With evaporation, waste becomes a cost issue. By the very nature of the process, the thicker the film to be deposited, the greater the amount of metal that ends up deposited off the substrate, such as inside the system. Finally, there is the raw material cost. At a minimum, the materials used in both sputtering and evaporation techniques must meet the same purity requirements as the deposited film, thereby increasing starting material costs. These very pure raw materials are, by their nature, more expensive than more commonly available, less pure counterparts.

## The Electroplating alternative

Electroplating is a nearly two-century-old process that uses an electric current from an anode to deposit metal from a solution (the electrolyte) onto a cathode (the substrate). There are typically two electroplating process flows used in device manufacturing. The first, damascene, deposits the metal into features that have been etched into a previously deposited dielectric film or layer. The second, the through-template process, deposits metal in the open areas of a patterned dielectric template, such as photoresist, which is later chemically dissolved or stripped away.

Whichever process flow is used, the basic physics are the same. As shown in Figure 2, a seed layer, which acts as the cathode, is first deposited onto the surface substrate. A resist layer is then deposited and patterned lithographically to create the desired features.

This is often the very same mask that was used for the metal lift-off process. The substrate is placed into a plating solution, voltage is applied, and metal ions are then selectively deposited following the lines of the electromotive force (voltage.) Once the wafer is removed from the bath, rinsed and dried, the resist is then stripped away using standard solvent processing. Finally, the seed layer is etched away using the deposited features as a hard mask, leaving behind the isolated patterned features.

The electroplating process offers significant advantages over sputtering or evaporation for applications such as wafer-level packaging, redistribution lines and interconnects. It can deliver nearly 100 percent step coverage with

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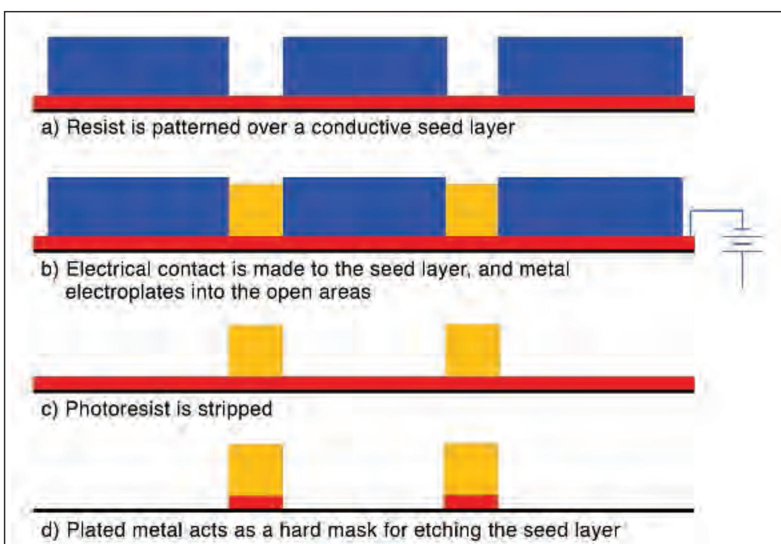
> "The idea for Solstice electroplating tools originally came from ClassOne's sister company, ClassOne Equipment. A long-time provider of quality refurbished tools, they were seeing a trend emerging, especially in small and medium-sized semiconductor manufacturers"

excellent feature fill, minimizing defect and integration issues. A simple, self-organizing process, it also offers deposition rates in excess of 4 microns per minute for some materials, making it an excellent technique for depositing the thick films required to build features such as the 90 micron copper pillars mentioned above. Its faster deposition rate also speeds wafer throughput and lowers overall cost of ownership. Electroplating offers an additional benefit since it is a purification process by nature. As a result, the raw materials need not be of the same level of purity required for sputtering or evaporation, which further lowers production costs. Finally, electroplating offers a much wider process window than the alternative processes, thereby increasing process flexibility.

As many university students have learned, making and using a small electroplating cell is simple and inexpensive. Outside of the laboratory and in the fab environment, the use of automated equipment and hazardous chemicals introduces concerns that need to be mitigated. There have been many different types of electroplating systems put into service over the years with varying degrees of success. Like most processes in semiconductor device manufacturing, electroplating makes use of potentially dangerous chemicals, so safety is a concern. Exposed or open baths of electroplating chemicals can be risky to both operations and maintenance personnel, as well as to the equipment itself. Chemicals can also pose environmental and facility contamination risks. Care should always be taken to ensure that plating equipment has integrated secondary containment and appropriate fail-safes as well as interlocks, such as those called for in the SEMI S2, CE, or FM4910 specifications. Since plating solutions tend to be corrosive, material compatibility becomes an important issue for safety as well as for maximizing asset longevity.

Figure 2. A simplified electroplating process.




Once safety guidelines and process controls are taken into consideration, choosing a plating system comes down to the performance to price ratio for the production volumes in question. Wet benches are often used for non-critical plating operations and can be either automated or manually operated, depending on production needs. For low levels of non-critical production, the variability in results that arise from manually operated equipment may not become an issue. Alternately, hand operations can become cumbersome as volume levels increase. When reproducibility and its consequent variation reduction matters, or when a high degree of uniformity is demanded, wet benches fall short and single wafer tools are desirable.

Single wafer tools fall into two general categories: fountain platers and paddle platers. Used more widely in the industry, fountain platers place a wafer face down into an overflowing pool while the wafer rotates. By comparison, paddle platers mechanically agitate the electrolyte near the surface of a static wafer. Paddle platers often can achieve higher ultimate plating rates for the same chemistry (due to a higher amount of agitation). But this benefit needs to be considered against the mechanical complexity of the chamber and necessary automation, which lead to increased costs. These tools tend to be physically larger than their fountain plater counterparts, which may be a concern for older, more space-constrained facilities.

## The future of electroplating: ClassOne Technology's solution

The idea for Solstice electroplating tools originally came from ClassOne's sister company, ClassOne Equipment. A long-time provider of quality refurbished tools, they were seeing a trend emerging, especially in small and medium-sized semiconductor manufacturers. These users were facing a technology transition from vacuum-based deposition to electroplating and needed new equipment; however, their budgets were limited. So, a new company, ClassOne Technology, was created specifically to address those needs. ClassOne's Solstice platform was designed for ≤200 mm wafers, to provide advanced electroplating capabilities at an affordable cost.

## Experience-grounded innovation

ClassOne Technology immediately brought in a team of seasoned veterans, with over 400 years of combined experience both in designing and using plating systems. They set about creating a new generation of electroplating systems to replace the aging Equinox® plating tool originally developed by Semitool in the early 1990s. Aimed at users of 200 mm and smaller wafers, the design objectives were functionality, reliability and ease of use combined with broad and advanced processing capability. To achieve ClassOne's standards of quality and performance the Solstice team utilized elegant design and best-of-breed components to deliver dependable performance while maximizing cost-efficiency. The Solstice control system employs Windows 7 and is based upon systems that have been in use for over 10 years in other industries. These elements form the basis of all three Solstice systems:

- S8: a fully-automated, cassette-to-cassette production tool with up to eight chambers;
- S4: fully automated like the S8, but with up to four chambers;
- LT: a semi-automated development tool with up to two chambers.

All Solstice tools share components, subassemblies, software and controls. This provides economies of scale and also gives users a seamless path from plating development to full automated production. Using the same chambers for all wafer sizes, for example, allows users to make changes in materials or wafer diameters by simply and quickly changing-out a few relatively inexpensive components. The Solstice ECD family is an excellent example of how an older technology can gain new life by solving emerging problems. Electroplating has significant potential to provide a cost-effective alternative to the sputtering or evaporation of metals for advanced applications. This time-tested technology is now becoming a key enabler and cost reducer for many small and mid-sized device manufacturers who have neither the need nor the budget for larger deposition systems.

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KEVIN WITT is the VP of Technology at ClassOne Technology and has worked more than 25 years in semiconductor and related high-tech industries.

Prior to ClassOne, he consulted for a variety of tech-based companies including VEECO, ESI, BioNano Genomics, TruTag, Advanced Inquiry Systems, SolarSemi Engineering, and The Thompson Group/SEMSYSCO.

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# Macronix expands flash portfolio for wearables

Serial NOR Flash Memory Series MX25R offers ultra-low power and wide voltage range, aimed at next-generation consumer wearables. Heko Arndt, Senior Field Application Engineer at Macronix Europe N.V. explains.

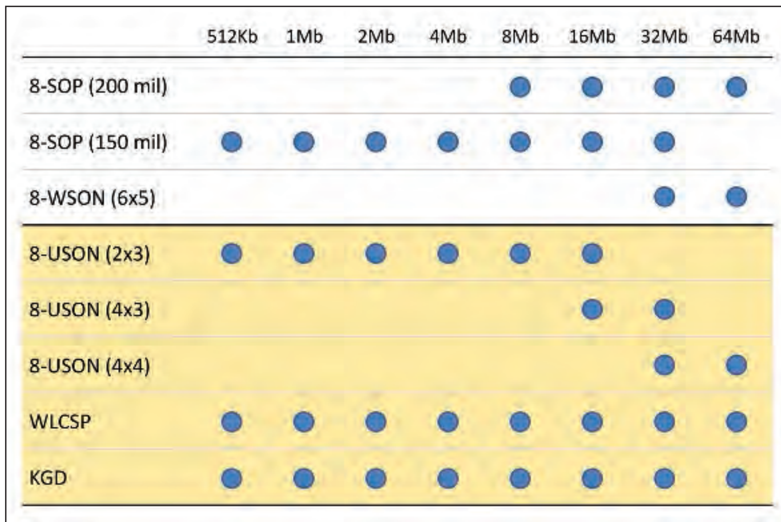
MACRONIX INTERNATIONAL CO. LTD has recently introduced its new MX25R Serial NOR flash product family. The devices are specifically aimed at next-generation consumer wearables in the context of the 'Internet of Things' (IoT). The MX25R product family features an ultra-low-power mode and densities ranging from 512Kb up to 64Mb, with plans to move up to 128Mb, 256Mb and 512Mb in the near future. Power consumption in the MX25R family is 60 percent lower than traditional solutions, with a wide Vcc span of 1.7V to 3.6V to support diverse requirements of wearable devices.  The new family fits within the Macronix portfolio of serial NOR flash products ranging from 512Kb to 1 Gb.

## Serial NOR Flash memory for wearables

Macronix's MX25R series caters specifically to next-generation consumer wearables. It supports the standard Serial NOR flash memory interface and industry-standard 8-pin layouts. With its very compact die, this allows for very small package dimensions such as the USON (Ultra Thin Small Outline No Lead), WSON (Very Very Thin Small Outline No Lead), WLCSP (Wafer Level Chip Scale Package), and also KGD (Known Good Die) solutions for stacked-die SIPs (System in Package).

The market prospects for wearables, in their first incarnations coming as sensor-enabled wristbands and rings, or smart watches equipped with fitness and location trackers, are a promising sub-segment of the IoT category of systems and services. According to new research from International Data Corporation (IDC), IoT systems and services promise a potential compound annual growth rate (GAGR) of 78.4 percent.

By 2018 annual sales for wearables may exceed a total unit volume of 112 million units according to a recent report published by US market researcher IDC. This market dynamic has encouraged Macronix to develop novel product solutions of memory devices for wearable applications to further expand its leading position as a vendor of non-volatile memory devices.



| | 512Kb | 1Mb | 2Mb | 4Mb | 8Mb | 16Mb | 32Mb | 64Mb |
|---|---|---|---|---|---|---|---|---|
| 8-SOP (200 mil) | | | | | ● | ● | ● | ● |
| 8-SOP (150 mil) | ● | ● | ● | ● | ● | ● | ● | |
| 8-WSON (6x5) | | | | | | | ● | ● |
| 8-USON (2x3) | ● | ● | ● | ● | ● | ● | | |
| 8-USON (4x3) | | | | | | ● | ● | |
| 8-USON (4x4) | | | | | | | ● | ● |
| WLCSP | ● | ● | ● | ● | ● | ● | ● | ● |
| KGD | ● | ● | ● | ● | ● | ● | ● | ● |

Figure 1. Available package formats for MX25R serial NOR flash devices.

"The key factor for wearables to gain rapid popularity is designing them with ultra-low power consumption and in a small form factor," states Min-Cheng Lin, Deputy Director of Macronix's Segment Marketing Department. "The next generation of memory devices will progress in the following directions: standardized interfaces prioritizing ease of data import, smaller and slimmer form factors and a power supply design focusing on ultra-low voltage and energy consumption."

## Internet of Things and wearables

Judged by its dominating presence at the 2015 Consumer Electronics Show (CES) in Las Vegas, NV, the 'Internet of Things' (IoT) provides a forward-looking perspective for the anticipated wide-area networking between people and things in a real-world environment. In this view, IoT should be understood as a generalized category and a driver to build a consensus for a comprehensive data network and its step-by-step implementation. The need for consensus-building results from the multitude of competing processor platforms and operating systems, in addition to the various protocols for radio interfaces and data security measures. This pertains to the consumer realm as well as to its industrial-use counterpart in the guise of 'Industry 4.0'. All these developments involve an extraordinary systems complexity.

Accordingly, Macronix sees several large, distinctive market segments for IoT devices and systems: cloud services and data centers, gateways for mobile telephony, automotive connectivity, home media, and a myriad of consumer-oriented IoT nodes for consumers in the form of ultra-compact, sensor-enabled terminal devices for data acquisition and wireless transmission over short distances to their personal base stations, such as smart phones and tablets.

Figure 2. USON and WLCSP packages for the Macronix Serial NOR Flash MC25R Series.

Most attractive from a current market perspective are the wearables, since they will establish large consumer markets. This is clearly indicated by the number of the semiconductor vendors focusing on wearables and smart home systems and the prioritization they are giving this segment. Among them are NXP, Freescale, Qualcomm, TI, Sony, MTK, Intel, Infineon and others. Of course, ARM as a licensor is heavily engaged in this realm as well.

Another market segment offering good prospects for high sales volumes, which could gain in importance in the mid-term, is smart lighting and smart metering, plus home security and home control systems equipped with thermostats and related equipment. However, this segment may attract a smaller number of device vendors since it involves different, somewhat higher demands on product quality.

Macronix is set to contribute to these emerging markets through specific incremental improvements of non-volatile memory devices, especially in regard to ultra-low power and standby modes. In stark contrast to the more broadly defined Internet of Things, with its complex infrastructure and fast transfer of large amounts of data, the wearable devices segment calls for a pragmatic system partitioning. Wearables, per definition, are the smallest possible data systems to be worn close to the human body. If they were larger they wouldn't be wearables anymore. Wearables, in contrast to smart phones and multimedia systems, don't require high memory densities and large memory spaces since they connect wirelessly with their dedicated base stations.

## Specific NOR flash configurations for wearables

Macronix's new Serial NOR flash MX25R Series was specifically designed and laid out for the relevant performance requirements of wearable devices – that is, eliminating all non-essential structures and features. Among other measures, the internal buffers were tailored to the envisioned applications, whereas a typical high-performance memory cell would comprise large internal RAMs. In wearable applications, when focusing on frequencies of just a few Megahertz, there are

further routes for optimization to reduce die size and power consumption, while maintaining all options for system designers to still utilize special 'performance modes' - at the cost of higher power consumption.

In its deep-power-down (current-saving) mode the MX25R devices offer a very favorable power budget, with savings of more than 90 percent compared to traditional solutions.

In regard to connecting the memory device with the system environment, the MX25R is compatible with the well-known and widely-used standard Serial NOR Flash Interface. This eliminates additional development efforts on the user's side and it accelerates time to market. With regard to active current, the Macronix MX25R device – drawing 4 mA (8 mA peak) - is situated at the lower end of the range available in the market. As a first estimation the active current of the MX25R device is 70 percent lower than with traditional last-generation memory solutions: in deep-power-down mode the difference goes up to more than 90 percent.

With its wide supply voltage range of 1.7V to 3.6V, the new MX25R series not only consumes less power during standard operation but enables designs to operate over the full Vcc range of the battery, thereby eliminating the need for external regulators. MX25R-based applications continue to operate even when the remaining battery capacity goes down to voltages below 2.7V. This further extends battery life by up to 50 percent.

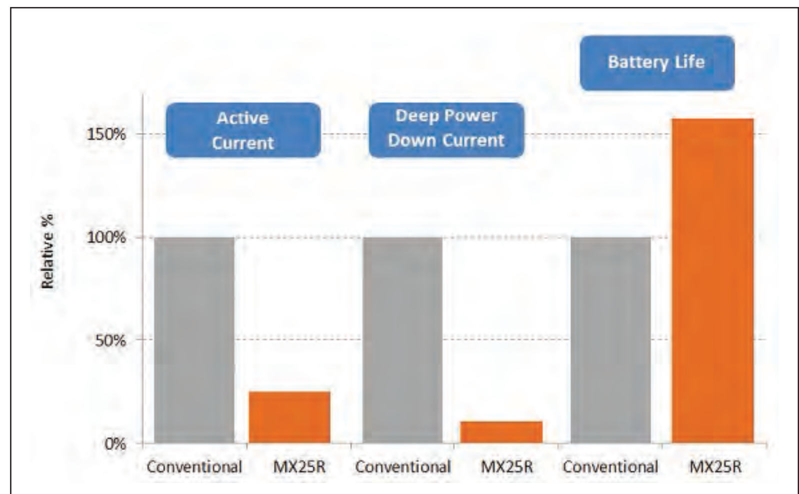



Figure 3. Performance overview of the Serial NOR Flash Series in regard to active current, deep-power-down consumption and battery lifetime in wearables.

Macronix currently offers the broadest selection of memory densities for Serial NOR flash memory devices, offering performance data tailored to the IoT sub-segment of wearables with densities ranging from 512 Kbit to 512Mbit.

## First wearable devices displayed

At the recent Electronica 2014 trade show held in Munich, Germany, Macronix displayed a full range of market-ready wearables connecting to the Internet of Things. Among its exhibits were smart watches and wristbands, medical devices, a GPS-enabled watch and GPS dog tracker, as well as examples of smart lighting applications.

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Figure 4. Inspecting a batch of memory devices at Macronix in HsinChu, Taiwan.

# With the 7nm FinFET, parasitics come into play

With every new technology generation, an understanding of the interdependencies between design and technology becomes increasingly important. A shining example is the scaling of FinFET technology beyond 10nm. Marie Garcia Bardon, Researcher at imec, talks about the options and limitations of advanced FinFET scaling.

THE CONTINUOUS EVOLUTION of systems-on-chips for smart mobile applications and their accelerated time-to-market, put severe requirements on the logic roadmap. Marie Garcia Bardon: "With each new technology generation, we try to achieve area reduction, speed improvement, power reduction and cost reduction, all at the same time.

This has so far driven the technology scaling, at device level, from 28nm planar Si devices, towards 20nm planar and finally Si-based FinFETs at the 14/16nm and 10nm technology nodes. FinFETs have been introduced because they provide a better electrostatic control over the channel and maintain the sub-threshold swing closer to ideal.

For the 7nm technology node, new disruptive solutions are possible at device level to continue performance improvement: we might replace the Si channel material with non-Si high-mobility materials. Or we might move to gate-all-around structures, either in the form of horizontal or vertical nanowires, since they offer the ultimate electrostatic channel control. However, another component became increasingly important: parasitics capacitances and resistances."

## Scaling the FinFET beyond 10nm: a parasitics-dominated era

From the 7nm node onwards, the impact of parasitics is becoming increasingly important. This means that unwanted capacitances and resistances increased due to tight dimensions and became non negligible at system level. And this substantially lowers the performance of the system in terms of speed and power. Marie Garcia Bardon: "We have to start considering parasitics that did not impact the systems performance before. At these small dimensions, we can no longer neglect the series resistances and parasitic capacitances in the back-end-of-line (e.g. parasitic capacitance between the interconnect layers) and in the front-end of line (e.g. fringe capacitances between gate and source/drain). The series resistance lowers the effective voltage on the transistor, while the parasitic capacitances eat part of the systems power and slow down its operation. If we want to meet the performance targets at the 7nm node, it will no longer be sufficient to optimize the transistor itself (channel material, gate all around etc). We have to introduce innovations that reduce these parasitic elements and their impact."

## Evaluating various technology/design options

Marie Garcia Bardon has explored the design space that allows to meet the performance target. She and her team have discussed possible solutions and have identified the main performance limiters. Marie Garcia Bardon: "We can think of several innovations which allow a reduction of the device parasitics. For example, we can improve the spacer width and the dielectric constant, e.g. by using air gap spacers. Or we can lower the contact resistivity by using wrapped around contacts. We can also optimize the back-end-of-line width and pitch, and the fin height.

At design level, we can explore solutions such as fin depopulation, i.e., reducing the number of fins per device. And we will have to evaluate, through simulations and calculations, all these new

> "One of the main objectives of technology scaling has always been an improvement of the systems speed. But for future technologies, speed might not be the main driver anymore"

parameters at the same time, and see which options are the best to meet our targets. The results of these evaluations are benchmarks of the different options in terms of power and frequency, as well as target values for the different elements. For example, what would be the optimal series resistance for a FinFET with Si channel to still meet the targets? And what speed benefit do we expect from a wrapped around contact? For each option, we can evaluate how good the performance compares to the target speed. With these results, we help the technology researchers at imec and our partners to choose between the many options and give direction to the technology roadmap."

## Dark silicon

One of the main objectives of technology scaling has always been an improvement of the systems speed. But for future technologies, speed might not be the main driver anymore. Marie Garcia Bardon: "With each new technology generation, we have been able to put more and more transistors on a chip. But the power reduction per transistor has not kept pace with this area scaling, due to the transistor leakage. This means that, with each new generation, there is a growing gap between how many transistors you can put on a chip vs. the percentage of transistors that can be powered with the same power budget.

This gap between area gains and power gains is referred to as 'dark silicon'. So, although we are still pushing area scaling, we might not be able to use the extra transistors on the chip for a certain power budget. And that's why we will also need solutions, at device level, to decrease the leakage."

## A collaborative effort

Six years ago, Marie Garcia Bardon joined the imec INSITE team, where she started modeling and evaluating the different transistor generations. Imec's INSITE program allows both product designers and technology developers to make informed decisions, based on a wide range of scenarios concerning future technology developments. Marie Garcia Bardon: "Working in the imec INSITE team is like solving a puzzle: we have to put all the pieces together and evaluate how they perform together, starting from the technology aspects all the way towards system level. This means that we have to interact with various people at imec: experts in front-end-of-line, in litho, in back-end-of-line, etc. Even within our INSITE team, we work together with modeling specialists in diverse domains. And this is one of the things I really like about my job. Our research is actually a convergence of everything we do at imec within core CMOS. We explore and optimize many parameters at the same time, and cross the traditional design-technology boundary. We take into account system requirements, and evaluate how they impact technology. And vice versa, how technology solutions impact decisions at the design level. Therefore, all these insights are the results of a collaborative effort of many people involved."

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Marie Garcia Bardon, Researcher at imec, will give an invited talk at the 2015 International Conference on IC Design and Technology (ICICDT, http://www.icicdt.org/index.php) which will take place at imec, Leuven, Belgium, from June 1-3, 2015. A global forum for interaction and collaboration of IC design and technology for 'accelerating product time-to-market'.

# How AMI tools image MEMS devices

The long-term functioning of a MEMS device depends on the integrity of the cavity; and the imaging and analysis of the seal protecting the cavity depends on acoustic micro imaging tools. Tom Adams, consultant, Sonoscan, Inc reports.

THE DEVICES known as MEMS (MicroElectroMechanical Systems) excel at collecting and reporting all sorts of data from all sorts of environments. MEMS devices collectively give us more data about the world we live in, and thus provide opportunities to live more advantageously in that world.

Blood pressure for example, was first measured a little over a hundred years ago, and since that time has been measured by fairly cumbersome mechanical equipment. Today a single MEMS device can be implanted that measures and reports blood pressure continuously. In a very different area, there's bad news for burglars: an extremely sensitive MEMS altitude/air pressure sensor can instantly report the slight but sudden change in air pressure caused by a window being opened three floors below.

Because they were made possible by the continued development of semiconductor manufacturing, MEMS devices share many features with semiconductor devices: they tend to be built in layers, they use many semiconductor materials, and they are inspected by some of the same tools, including Acoustic Micro Imaging (AMI) tools.

An AMI tool pulses ultrasound into a sample and receives the return echoes from material interfaces within the sample. A sample that consists of

a single material and that has no internal interfaces will therefore send back echoes from the top and bottom surfaces only - the top surface because it is the interface between the sample and the coupling fluid, and the bottom surface because it interfaces with what support the sample is resting on.

When a sample has (like a MEMS or semiconductor sample) multiple bonded layers, an echo will be returned from each interface between layers. If there is an anomaly in one of the layers, or between two layers, it is typically a gap-type defect such as a crack or delamination, void or non-bond.

Gaps typically return echoes of very high amplitude ( more than 99.99% of the pulse), even if the gap is as thin as 100Å. In contrast, the interface between two well bonded materials will return only a fraction of the ultrasound, while the remainder proceeds deeper into the sample.

Gaps are thus easy to see when using an AMI tool, as are well-bonded interfaces. The echo also gives information about the depth of an interface, and about its polarity (whether in crossing an interface the pulse traveled from a material having higher acoustic impedance to material having lower acoustic impedance, or vice versa).

MEMS (Micro-ElectroMechanical Systems) devices are imaged by AMI tools at any of three stages: 1) while the devices are still in wafer form; 2) after dicing; 3) in their final packaged form. And some wafers, such as SOI, are imaged after bonding to eliminate poorly bonded pairs before etching. The frequencies of ultrasound used in of MEMS range from 50 MHz to 400 MHz.

Generally, lower frequencies penetrate better through materials, while higher frequencies give better spatial resolution in the acoustic image. Because they are thin and because the materials involved are highly transmissive of ultrasound, MEMS devices can be imaged at high frequencies for maximum image resolution.

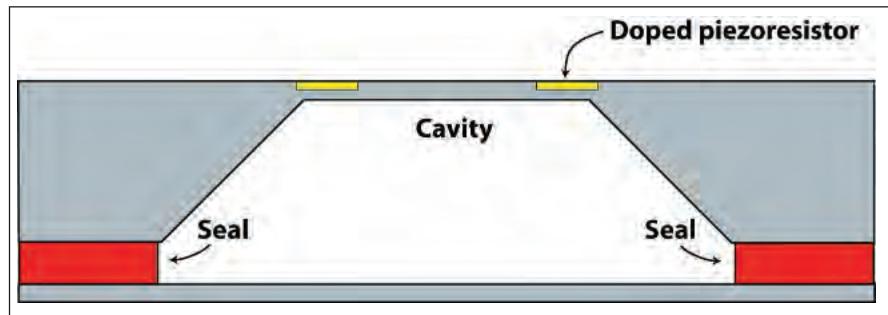


Figure 1. MEMS designs vary widely, but the seal protecting the cavity is the most frequent target of acoustic micro imaging tools.

But by far the most frequent purpose of acoustic imaging is to characterize the seal that surrounds the cavity and ensures the cavity's hermeticity. The cavity may contain a vacuum, air, or another gas. The seal may be made of glass, metal, epoxy or another material. The makers of the MEMS device want to ensure the successful functioning of the seal and of the device over the desired lifetime. Using SEMI standards, the permeability of the seal material to the external environment, and especially to humidity, can be quantified.

If the cavity contains a gas under pressure, the permeability of the seal material to the gas can also be quantified. In some MEMS pressure devices the cavity is divided into a sealed region and a region open to the outside environment. The Si membrane between the two regions deforms as the outside pressure changes, so the deformation rate, the seal quality and the permeability of the seal material all affect the functionality of the MEMS device.

What does a MEMS device look like to an acoustic micro imaging tool? Because the cavity contains gas or a vacuum, more than 99.99% of a pulse of ultrasound striking the silicon-to-cavity interface will be reflected and will create a bright white (highest amplitude) pixel in the acoustic image. All of the area of the cavity will thus be bright white, except where there may be solid features that extend from the ceiling to the floor of the cavity. These areas will be some shade of gray. Surrounding the cavity is the seal (Figure 1) that keeps the cavity intact. The seal has an interface to the silicon above and the silicon below. The cavity region will of course appear bright white, but what the operator of the acoustic micro imaging tool hopes to see around the cavity is a uniformly gray line meaning that the seal is without flaws. What he does not want to see are bright features within the seal; these would be delaminations, voids or non-bonds.

During the imaging process, the ultrasonic transducer scans the top surface of the MEMS wafer or individual device at a speed that can exceed 1 m/s. At this speed it sends several thousand pulses of ultrasound per second into the sample, and collects the return echoes from each one. Each echo becomes a pixel in the acoustic image.

Echoes from different depths within the wafer or device arrive at the transducer at different times. A time gate may be set to collect only echoes from the top to bottom of the seal.

An acoustic image of a pair of bonded wafers is shown in Figure 2. This is a fairly low resolution image of test wafers, where the purpose is to verify the reliability of the bonding process. In this case, when the two wafers were brought into contact to achieve fusion bonding, contact initiated at two locations rather than one. As the two wavefronts collided, they trapped air, resulting in the large and small bright white voids seen in the acoustic image. Regions where the two wafers are successfully bonded are black; there is no echo because there is no longer a material interface.

Figure 2. Acoustic image of two bonded MEMS wafers. White regions are voids between the wafers.

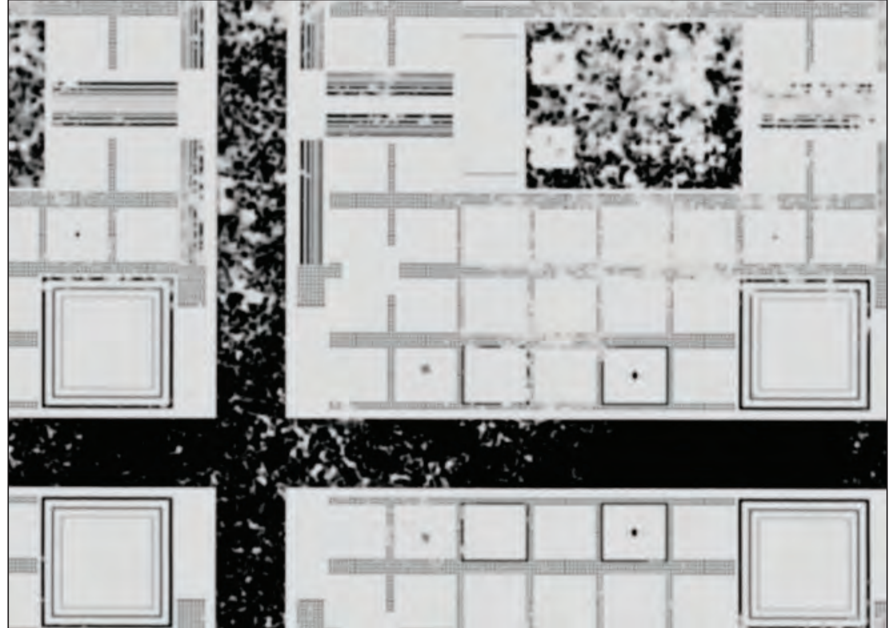

Figure 4. Large numbers of small defects (white) are present in the seal and other bonded regions of this MEMS wafer.

In development or production, higher ultrasonic resolution is used to inspect for individual voids such as those shown in the following images. Defects may be viewed by a technician who examines the acoustic image of the whole area of the wafer, or they may be found and reported by Digital Image Analysis (DIA) software.

Figure 3 is a small section of a high-resolution acoustic image showing rectangular cavities (bright areas) and the rectangular seals surrounding the cavities. Some of the seals are intact, but the circles identify locations where part of the seal is not attached to a wafer or is altogether missing. These circled defects will of course cause immediate failure of the MEMS device, but there are other, smaller anomalies that appear capable of causing eventual failure.

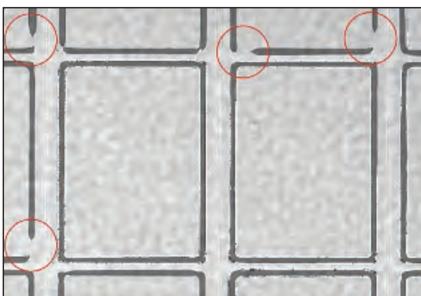

Figure 3. The cavities in this acoustic image of a MEMS wafer are bright rectangles; some of the seals are incomplete (red circles).

Figure 4 is the acoustic image of a small area of a MEMS wafer. The dark black lines are fairly wide seals along which the wafer will be cut for singulation. There are dark structures within the cavities that are bonded to one or both wafers.

But within the seal, as well as within the structures inside the cavity, are numerous small white areas which are defects. They may be areas of non-bonding on the top of the seal and other structures. Whatever their depth, some of defects on or in the seal are already large enough to compromise the hermeticity of the cavity.

The design and structure of MEMS devices vary greatly from one application to another, but the integrity of the seal around the cavity is always of critical importance. In some very recent MEMS designs, the seal may be as little as 6 microns wide, but the very high ultrasonic frequencies used to image MEMS devices, along with the high ultrasonic reflectivity of solid-to-gas anomalies, means that defects in the seal can still be imaged.

In some cases, the target of acoustic imaging may be something other than (or in addition to) the cavity seal. For example, it is important to know that the substrate wafer is free from tiny cracks that can occur during processing. The cracks are typically more or less vertical. The problem is that a nearly vertical, extremely thin crack does not reflect much ultrasound pulsed from above.

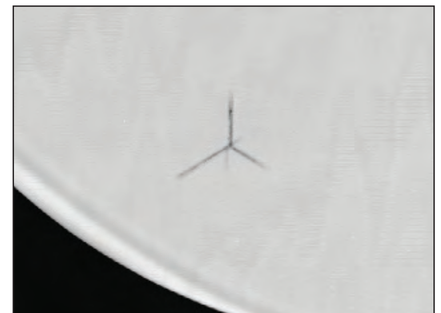

Figure 5. A crack such as this one in a single wafer may cause failure during later processes.

Figure 5 is the acoustic image of a single wafer in which a complex crack has formed. The risk is that such a crack will not survive subsequent processing, but will fail and likely destroy the wafer or wafer pair at a later stage.

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# PIC INTERNATIONAL CONFERENCE

## Photonics Integrated Circuits Conference

**Creating and strengthening links between chipmakers and network builders**

**1 - 2 March 2016, Sheraton Brussels Airport Hotel, Belgium**

**Co-located with the 6th CS International Conference**

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### Over 30 inspiring presentations

- Where should the laser go?
- Driving deployment of PICs in datacentres
- Increasing the capability of optical networks
- What's the role of the foundry?
- Do we have the tools for designing, making, packaging and testing PICs?
- A question of material: InP, silicon, or something else?

Sales of PICs are soaring, with their deployment helping to boost the capacity of networks and data centres.

To aid this industry, we are strengthening the relationships between the makers and the users of these integrated circuits by launching PIC International, a global conference dedicated to this industry. Attendees at the inaugural PIC International conference will hear industry-leading insiders delivering more than 30 presentations spanning six sectors.

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**www.picinternational.net**

# 2014: A great year for the industry

## Worldwide industrial semiconductor revenues grew by 18 percent

Global industrial semiconductor revenue in 2014 totalled $40.4 billion, up from $34.3 billion in 2013. The year-over-year increase follows solid growth of 13 percent in 2013, a decline of 3 percent in 2012 and 12 percent growth in 2011. The strong performance achieved in 2014 represents the highest annual growth rate, since the 36 percent boom in 2010.

"Gradual acceleration in the global economy, led by the United States and China, continued to lift industrial equipment demand," said Robbie Galoso, principal analyst, IHS Technology. "Broad-based growth in industrial electronics gained momentum in the semiconductor industry, especially in products used for factory automation control, commercial avionics, LED lighting, digital internet-protocol cameras, climate control, renewable energy, traction, wireless application-specific testers and oil and gas exploration equipment."

Based on the latest information from the IHS Industrial Semiconductors service, the industrial electronics category is expected to continue its strong momentum, as the top application-revenue driver in the semiconductor industry, through 2019. Industrial semiconductor revenue growth is expected to increase 7 percent in 2015, with continued growth forecast for many segments; however, more moderate growth is expected this year, due mainly to slowed growth in memory, logic and analog products used in building and home control, military and civil aerospace, and test and measurement. With improving financial results in the long term, the industrial semiconductor market is expected to be on track to reach 6 percent compound annual growth rate (CAGR) between 2014 and 2019.

Texas Instruments maintained its strong position as the largest industrial semiconductor supplier in the world, followed by STMicroelectronics and Infineon Technologies. Both Micron Technology and ON Semiconductor both made their way into the top-10 industrial semiconductor supplier ranking list in 2014.

"Micron jumped into the top 10 last year, due to the success of their product-longevity program, which reinforced their commitment to the industrial market and leveraged the company's 2013 acquisition of Elpida Memory," Galoso said. "Micron's product longevity program continued to grow quickly in 2014, which helped the company become the undisputed global industrial memory chip supplier."

The other big mover among the top 10, On Semiconductor, was boosted by its acquisition of Aptina, a leading complementary metal-oxide semiconductor (CMOS) image sensor supplier in the industrial market, which moved the merged company into tenth position in the rankings. Because both Micron and ON Semiconductor made their way into the top 10 rankings, both Maxim Integrated Products and Cree were displaced.

"Strategic acquisitions will continue to play a major role in shaping the overall semiconductor market rankings in key industrial semiconductor segments," Galoso said. "Infineon and NXP will soon upgrade their positions among the top semiconductor suppliers in 2015, due to their acquisitions of International Rectifier and Freescale Semiconductor respectively."

The combined industrial semiconductor revenues for NXP and Freescale last year would amount to $1.3 billion. A joint NXP Freescale would be ranked in sixth place, behind Analog Devices; NXP was previously ranked 16th while Freescale was ranked 17th. The combined company will catapult into the top 10 for major industrial applications, and impressive share gains will be realized -- especially in manufacturing and process automation, military and civil aerospace, power and energy and medical electronics. On the other hand, the combined Infineon International Rectifier would generate $2.3 billion in industrial semiconductor revenues, which would catapult the merged company into second place in last year's rankings.

Among the top 10 semiconductor suppliers, nine companies achieved growth in 2014 and seven of those companies posted double-digit growth. Out of the top 10 companies, only one, Renesas Electronics, suffered a decline, as the Japanese semiconductor market and suppliers continued to struggle. Optical Semiconductor delivered the strongest performance, thanks to the continued strength of the LED market.

The highest semiconductor device absolute revenue growth from 2014 to 2019 will come from LEDs, which is expected to grow from $6.3 billion to $12.6 billion—stemming from the global general lighting LED lighting boom, with most countries banning incandescent bulbs in 2014. Discrete power transistors, thyristors, rectifier and power diodes are expected to grow from $6 billion to $7.3 billion, due to the policy shift toward energy efficiency.

Microcontrollers (MCUs) are also expected to experience robust growth in the long-term, growing from $4.3 billion to $5.8 billion, because of advances in power efficiency and integration features.

Out of more than 27 semiconductor segments, 26 achieved increased year-over-year growth in 2014. All 7 major semiconductor components grew last year, led by optical, analog integrated circuits (ICs), logic ICs, discretes, microcomponent ICs, memory ICs, and sensors and actuators. Both analog ICs and logic application-specific ICs achieved the strongest turnaround in growth, moving from relatively flat growth in 2013 to over 20 percent growth last year.

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# CORPORATE PARTNERS DIRECTORY

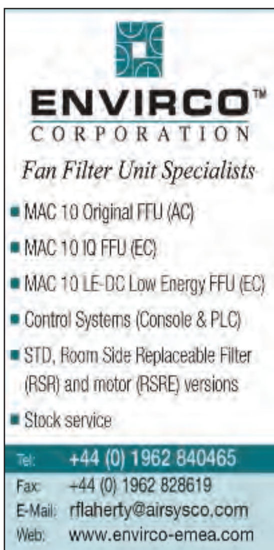
## Device Design & Packaging

## Furnaces

## Materials, Processes and Equipment

## Solder Rework

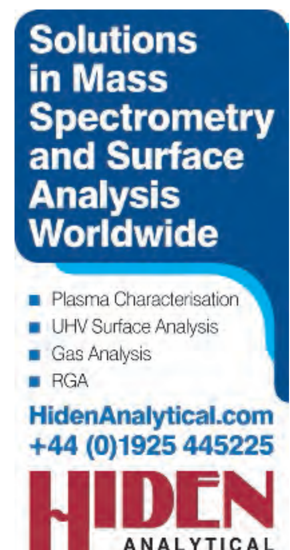
## Fan Filter Units



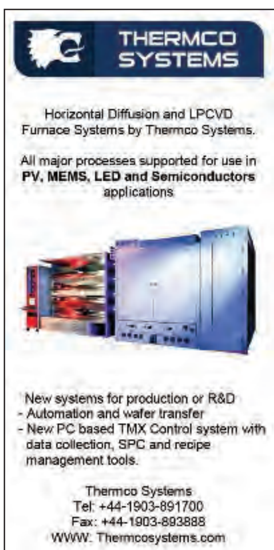

## Furnaces

## MFCs

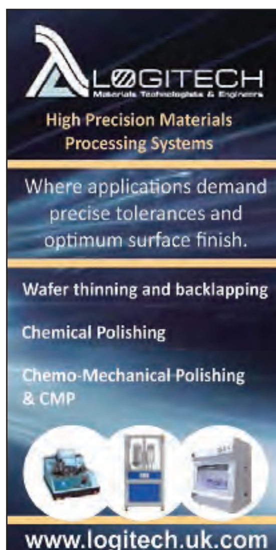
## Vacuum Equipment




## Furnaces




## Material Processing




## Pump Line Heaters

## Wet Benches

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Cu TSV

MEMS

Pads & Pillars

Patterned Ni, Cu, Au, Sn, Ag & Alloys

Cu RDL

Solder Bumps

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