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Volume 37 Issue V 2015

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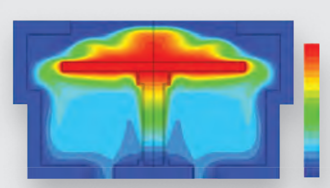

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executiveview

by Mark Andrews, Technical Contributor

The journey continues

MOVIE CHARACTERS are memorable if they're larger than life. Like a movie, the ever-changing face of semiconductor technology has its own characters that keep us watching as the storyline unfolds.

2015 started enthusiastically. Early analyst predictions foresaw 7 percent growth. But even as TSMC and other major chip makers reported strong 2014 earnings, clouds crept into forecasts. The real storm would not appear for months, so as they always do, new products came to market including advances such as ever-shrinking SoC devices, wearable's, flexible and printable electronics, sensors, radar and moves toward realising IoT expansion.

By mid-2015 the year that looked so promising shifted to a picture of something gained/something lost – when good news came, a 'Grinch' would turn gentle breezes into gales. We saw exciting new products and technologies in one hand / shrinking chip revenue in the other. And so it went.

In July the plot line followed a path signaled earlier: China's continual expansionist ambitions were overtaken by reality. Growth slowed and analysts clamored that they had, '…seen it coming for years.' Companies supplying China, buying from China or hoping for a future there inhaled sharply and forecasts slipped.

As the final days of 2015 tick away, many are looking for a happy ending. Take heart—there is one in the works. Semiconductor technology remains an industry that powers global economic optimism, even as some hoping for 7 percent growth will likely see less. Semiconductor researchers, designers and manufacturers deliver the products and technologies that consumers embrace every day. Whether it's wearable sensors, autonomous vehicles, IoT, new mobile computing solutions or renewable energy to thwart climate change, semiconductors deliver the solutions that our global community wants and needs.

The reality of semiconductors' role in the 21st century – unlike a movie plot – should give you optimism that if not today, then tomorrow the industry will see solid growth. Yet remember that all expansion reverses, just as reversals are themselves turned around.

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Silicon Semiconductor is published four times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/€158 pa (UK & Europe), £138.00 pa (air mail), $198 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2015. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing.
US mailing information: Silicon Semiconductor (ISSN 1096-598X) is published four times a year for a subscription of $198 by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. Periodicals postage paid at Rahway, NJ. POSTMASTER: send address changes to: Silicon Semiconductor, c/o Mercury International Ltd, 365 Blair Road, Avenel, NJ 07001.
Printed by: Pensord Press. © Copyright 2015. ISSN 2050-7798 (Print) ISSN 2050-7801 (Online).

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30 Taking charge of change

Handling product and process change on an industrial scale is no simple subject. But there are solutions to manage change that semiconductor manufacturers have embraced as both effective and profitable.

36 The memory roadmap: A paradigm shift from 2D to 3D

"There will never be enough memory": this idea has driven the continuous scaling of memory technologies. Today, DRAM and Flash, both charge-based memory concepts, represent the largest memory markets. For a long time, experts have predicted that emerging memories, such as STT-MRAM, resistive RAM and phase-change memory, all resistance based, would replace the common DRAM and Flash technologies in the Terabit era.

40 Beyond the curve to foldable displays

Lightweight, unbreakable, flexible and wearable; these are just a few of the development targets for contemporary consumer electronics. Over the past ouple of years interest in flexible displays that meet these needs has increased significantly, with the market for this flexible display technology predicted to expand to more than $21billion by 2020[1].

44 Maximizing productivity in the lab

Failure analysis labs typically involve lots of manual tasks performed by highly skilled operators. However, failure analysis labs are now adopting practices from the fab, such as increased automation, as the need for more and faster failure analysis feedback becomes critical to maximising yield.

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With every new technology generation, an understanding of the interdependencies between design and technology becomes increasingly important. A shining example is the scaling of FinFET technology beyond 10nm.

56 More than Precision: Meeting the challenge of accurately assembling active optical cables

No one would dispute the fact that active optical cable (AOC) and Silicon Photonics technologies are getting tremendous attention due to the need of transferring more and more data at ever faster data rates. This is putting immense pressure on the assembly equipment suppliers to offer advanced tools and processes that push the envelope of ultra-precise die placement.

61 Killer consumables: How clean are your seals?

In semiconductor manufacturing the threat of particle and especially metallic contamination to transistor integrity is a significant and potentially costly threat. This is mainly true for front end processing but, due to the high mobility of many of these contaminants, it remains a threat at all stages of the manufacturing process flow.

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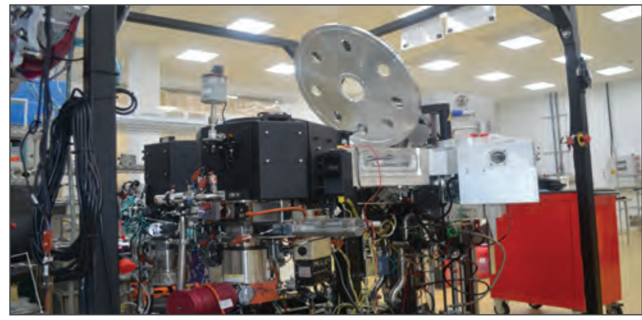
To be competitive in the IoT market, cost is key and making the successful adaptation of secondary equipment is paramount.



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Manufacturers are pooling resources to double global IC capacity. Will achieving the next milestone in silicon evolution give members a competitive edge?

2015

A year of merger mania in semiconductor manufacturing

2015 set records for merger activity as the China slowdown created global economic headwinds. While some markets contract, new opportunities are poised to strengthen 2016 growth.

2015 WAS A RECORD-SETTING YEAR across the semiconductor industry. Merger mania hit new highs, with 18 deals of $100 million or more making headlines. Mergers closing by October 31st were valued at $110 billion. Yet some major deals did not happen, as was the case with the Tokyo Electron/Applied Materials match-up. Meanwhile, the acquisition of KLA-Tencor by Lam Research Corporation announced in fourth quarter moves forward with the approval of most industry watchers even though regulators have not officially weighed-in.

Contributor Mark Andrews saw that some of the biggest headlines came from China, where the country's long-standing expansionist business climate ran into substancial headwinds that shook financial markets this past summer. World markets largely recovered thanks to infusions of capital by the Chinese central bank and the resilience of the United States' economy. Despite China's negative pull, Asia is still on-track to be the world's major producer of semiconductors by 2020.

While technological advances continue to drive product innovation, headlines in 2015 often spoke of incremental advances for many applications. That having been said, new ground was broken in memory, photonics, 5G, IoT and progress towards 450mm technologies.

As 2015 draws to a close, industry analysts remain optimistic that growth—perhaps at a slower pace—will continue in the New Year thanks to the ever-inventive minds of the world's best manufacturers, suppliers, researchers and entrepreneurs.

2015 Year in Review

January

Researchers at IC Insights got off to a busy start, forecasting seven percent growth in semiconductor manufacturing. This prediction was within the range of SEMI's forecasts as well.

While several researchers foresaw a China slowdown, none were looking for the fall-off that markets would experience by the summer.

Taiwan Semiconductor Manufacturing Company (TSMC) announced record quarterly 2014 profits, but also signalled that a slowdown might be coming. As if they heard the forecast in Taiwan and wanted to exert their own influence, leaders in Beijing signalled that China intended to fund semiconductor expansion to the tune of $10 billion (USD.) Meanwhile a new report from IC Insights listed the top 50 foundries of 2015; nine were in China. At the Consumer Electronics Show in Las Vegas (USA), Intel announced a new chip family that included 14 new designs targeting PC and notebook applications. Intel also showcased what it claimed to be the smallest wearable system on a chip (SoC) device that was clearly targeting the wearables market.

February

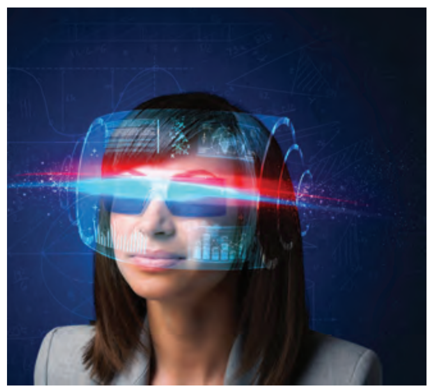
A week into leading the SEMI trade group, John Neuffer helped celebrate record setting revenues in 2014 of nearly $338 billion, up 9.9 percent over 2013. China was first on his list of stops as the world's number-two economy sought expanded roles in high-tech manufacturing, placing more emphasis on key capabilities that have up to this point typically been located elsewhere across the globe.

As China topped many analysts' must-watch lists, America's Silicon Valley again made news, this time for its continued expansion. Perhaps seeing ahead to the rocky road we'd find by mid-2015, Silicon Valley executives reported continuing expansion of the type not experienced since the 'bubble' days of the dotcom boom that burst in 2001, but of a type that they believed was more sustainable compared to the breakneck pace set before 2000-2001. February saw TSMC announcing a $16 billion investment in its plants. Spoiler Alert: That ambitious plan would be trimmed later in 2015, with capital investment falling from $10.5 to $8 billion, reflecting the reality of a shrinking market.

Even though February saw shouting matches over whose semiconductor fabs might grow the fastest, Internet of Things (IoT) technology grabbed headlines as well. Security experts at ARM outlined what they saw as the road ahead for realizing the technology's potential, putting cash into the gambit by acquiring Offspark, a company specializing in Transport Layer Security (TLS), technology that was already used widely across commerce and communications infrastructure. Elsewhere in the IoT universe, experts meeting at the Boston Embedded Systems Conference said that the competing platforms for realizing IoT secure connectivity were still sorting themselves out and would be for years to come, which could affect how quickly IoT devices are brought to market.

March

Merger mania continued in a big way on March 1st with the announcement by NXP and Freescale that they planned to combine resources, creating a $10 billion revenue machine. If finalized the merger would create the world's 9th largest chip maker, and dominate the market for automotive and general purpose microcontroller semiconductors. NXP and Freescale valued the deal at $40 billion.



As if to put an exclamation point on the issue of global fab hot spots, analyst at IC Insights said that Asia would have nearly 70 percent of all fabs by 2019, with the bulk (40 percent,) located in Taiwan and South Korea. China made the list with a forecast of 10.9 percent of global fabs by 2019.

In a move that surprised no one except those with their heads in the sand, exhibitors at Wearable TechCon noted that smart glasses from Epson, Google and Sony were resetting expectations and were turning their attentions to business applications. The appeal of Google Glass and similar products in work environments that challenge staff to maintain constant contact across multiple applications as well as 'interface' with their human counterparts seems intuitive. One has to wonder why the developers didn't seek those markets at the same time they were promoting smart glasses to mainstream consumers.

Technology news came on several fronts, with researchers at North-eastern University announcing that they had uncovered basic principles that should enable the development of quantum Wigner crystals, predicted as theoretically possible in 1934. The breakthroughs could enable ultra-high-electron mobility several orders of magnitude superior to either silicon or graphene. On the optical front the University of Washington in Seattle and California's Stanford University announced development of nano-scale lasers that could be ideal for transmitting data optically around semiconductor chips.

March ended with analysts 'cooling' to the idea of an Intel/Altera combination. Although speculation about Intel acquiring an FPGA leader has persisted for years, that market is tiny compared to Intel's primary computing markets. Analysts wondered why the chip maker would spend $13 billion for a company with perhaps $2 billion in annual revenues.

April

IoT again made headlines as EuroCPS pledged to fund as many as 30 teams across Europe with up to $25 million to underwrite a three-year initiative in fundamental and practical research. The goal was to enable greater capabilities and market growth for all things wearable tied to Internet of Things applications. The initiative particularly targets smaller research groups that often are challenged when competing against major global enterprises with deep R&D pockets.

At midpoint, engineers commemorated the entry of Gordon Moore's 'simple' assertion that transistors could double in capacity within the same area of a silicon chip every two years. While the ramifications of this idea are still being argued the impact of Moore's Law is undeniable. The successful pursuit of greater computing capacity led to not just faster and cheaper computers, but also myriad applications from communications and the Internet to smartphones, tablets and now the dawn of IoT.

April saw announcements from the Internet Engineering Task Force (IETF) about new, faster chips and the software to drive them, all tied to software-defined networking (SDN). Meanwhile, the Optical Internetworking Forum (OIF) is leading initiatives to create bonded Ethernet channels. The ultimate goal of both groups is to create 400 Gb/s channels bonded to create pipes as 'fat' as 1.6 Tb/s.

Analysts also went out on a limb to predict Intel's process technology of choice for its next two generations, driving toward 10nm devices. Analyst David Kanter (based on the contents of papers released by the company and other assorted data,) predicted Intel would rely on quantum well FETs using two new materials—indium gallium arsenide (InGaAs) for n-type transistors and strained germanium for p-type devices. Only time will tell, but if he is correct Intel could leap frog competitors one more time.

Closing out a busy April was Apple's achievement of yet another sales record: $58 billion in the second quarter compared to the same time in 2014. Although Apple declined at the time to make forecasts on its then-anticipated Watch segment, iPhone and Mac sales dropped. Nevertheless the world's largest electronics company reported a $13.6 billion profit. Not bad for a 'cooling' market.

May

We all know how frustrating it can be to find the right component for a new design, and engineer Javier Solorzano responded by co-founding a new company called Elektet that he believes will aid designers, and manufacturers searching for just the right component. This isn't your basic parametric search engine like many chip vendors have built into their websites. His approach is a 'Google-like' system that could work across the web to help engineers locate parts despite widely varying product IDs and descriptions across the industry.

It was no surprise to discover the industry heavy weights Qualcomm and Broadcom again found something to dispute, this time in how the LTE-Unlicensed (LTE-U) spectrum is being utilized alongside Licensed Assisted Access. The US Federal Communications Commission is interested in whether the two companies are sharing spectrum and not

looking into ways that incumbent Wi-Fi technologies might be infringed upon. The inquiry could potentially pit cellular network providers against the 'cable guys' as well as users of unlicensed spectrum. Stay tuned….

Infineon made additional headlines by announcing that the Munich, Germany based company was looking for a buyer to take over its Newport (Wales) wafer fab that came to the company as part of its acquisition of International Rectifier. Although seen as an eventual blow to the local economy, Infineon stated it expected work to continue in Newport through the end of 2017, indicating that demand is sufficient for a potentially protracted sales process.

News from the wearables market included opinions from the Embedded Systems Conference in California that indicated relatively modest sales figures could be tied to the fact that while devices such as Apple Watch have many capabilities, they haven't achieved the kind of data throughput that medical practitioners would need to use the devices for patient diagnoses or monitoring. One problem lies in the sensor design, which is fine for other systems today but lacks the contextual data that a doctor or other practitioner would need.

Samsung made headlines by announcing it would ramp production of its 10nm devices starting in 2016. The new node is expected to be in full production by the end of next year. International Business Strategies CEO Handel Jones said that if Samsung can achieve 10nm at production volumes, the impact could be very disruptive in the market.

June

The month began with good news for Taiwan Semiconductor Manufacturing Company (TSMC) when MediaTek announced that it would continue using the company as its leading-edge chip foundry. This announcement laid to rest fears that MediaTek might be shifting its business to TSMC rival Samsung.

Defending his company's decision to buy Altera, Intel CEO Brian Krzanich said the combined companies would ship integrated products starting in late 2016 for servers and some still-undetermined embedded systems. His message was met with some scepticism by Linley Gwennap, a principal analyst at The Linley Group and a veteran Intel analyst. Krzanich estimated new business could be "…be quite a bit bigger than a billion dollars…"

'Sanity' became the watchword at an early June conference attended by Internet of Things (IoT) experts who labelled projections of up to 50 billion IoT devices by 2020 as 'Fantasy.' A more realistic projection is 1.9 billion IoT devices shipping by 2020, according to Linley Gwennap who said he took a bottoms-up look at real world stats, such as the global middle class population (about 2 billion by 2020) and the number of homes expected to have Wi-Fi or other broadband connections (around 600 million.)

Analysts at the Computex Taipei event looking for ways to realize maximum penetration for wearable IoT devices stated that 72 million wearable devices worth $17 million will ship this year, pointing to a compound annual growth rate (CAGR) of 18 percent. They projected up to 156 million units worth $39 billion by 2019. Bruce James, director of mobile solutions for ARM, with chip designs in 90 percent of with world's smartphones, is betting on watch and watch-like wearables as emerging leaders.

By mid-month, reports were surfacing noting that demand for semiconductors was weakening in the second quarter with some assemblers in Asia suggesting double-digit fall offs compared to second quarter in 2014. The iPhone supply chain and automotive markets remained a bright spots in 2015 forecasts.

While current semiconductor shipments were falling compared to 2014, China's top foundry, Semiconductor Manufacturing International Corporation (SMIC), forged a joint venture with Huawei, Qualcomm and the imec research institute to develop its own technology for 14nm process production at a SMIC fab by 2020. Beijing had earlier committed to spending $10 billion for domestic semiconductor production, which could include the 14nm development project analysts said.

July

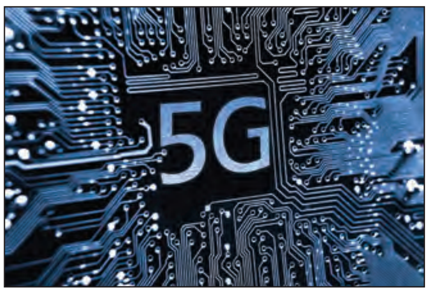
IBM and GlobalFoundries got the month off to a busy start, announcing that they had closed the deal transferring IBM's Burlington, Vermont (USA) foundry to GF. The deal was worth $1.5 billion and as a condition IBM agreed to make

"'Sanity' became the watchword at an early June conference attended by Internet of Things (IoT) experts who labelled projections of up to 50 billion IoT devices by 2020 as 'Fantasy.'"

GlobalFoundries its supplier for the next 10 years while Global also obtained ownership of 10,000 IBM semiconductor patents.

5G took another step towards becoming the next cellular communications standard when it was announced that demonstration projects, trials and specifications work would begin within months of the July announcement. 5G is expected to deliver a number of benefits compared to 4G technologies, including maximum data rates of 10- to 20 Gb/s, likely confined to dense urban areas.

Analysts at Credit Suisse in Taipei said MediaTek (the world's third largest chip designer,) is expected to continue making market share gains in the LTE market at the expense of top-rated Qualcomm because of its position in the fast-growing Chinese smartphone market. MediaTek's market share in LTE is likely to double (up to 45 percent of the China market) by December 31st.



In other news from Asia, the Tsinghua Unigroup (China) bid $23 billion to buy Micron Technology. While the deal would fill one of the biggest strategic holes in China's chip industry it was expected to raise political issues all the way to the US White House. Micron is the second largest chip maker in the US (behind Intel) with revenue of $16.8 billion in 2014.

By mid-July analysts were reporting that semiconductor sales were in a two-year slump due primarily to weak demand for PCs and some smartphones. Gartner Group reported that chip sales rose a mere 2.2 percent by the middle of 2015, with growth of just 1.3 percent predicted by year's end. At the same time, Gartner predicted that growth would return to a more typical 4-5 percent range starting in 2017, thanks to expected growth in IoT, the expansion of smartphone sales in growing markets such as India and China, and more positive momentum in other markets including Europe and the Americas.

"The Consumer Electronics Association, also presenting at the Flash Memory Summit, said that while wearables constitute the fastest growing segment they are also the smallest and most fragmented"

Taiwan Semiconductor Manufacturing Co. (TSMC), the world's largest chip foundry, said the outlook for the rest of 2015 is worse than the company previously expected because customers were digesting an inventory glut built earlier this year. While the company expected an increase in demand for computer, consumer and industrial segment devices, it expected smartphones and other handset device markets to decline.

The impact of declining growth in China was fully felt across global financial markets starting in July. Even though the official sources in Beijing reported 7 percent annual growth, outside economists and analysts pointed to the government's widely observed miscalculation of 'deflator' factors that are a broad measure of prices affecting a country's economy. Economists stated that Chinese gross domestic product (GPD) figures were wrong by up to 2 percentage points.

The vulnerability of devices linked to the internet hit home in July as car maker Jeep and its parent, Fiat Chrysler Automotive (FCA), admitted that Jeep vehicles were vulnerable to hacker attacks. FCA stated that blame for the vulnerability was shared with Sprint, FCA's system integrator, and Harmon Kardon, designer of in-vehicle infotainment systems.

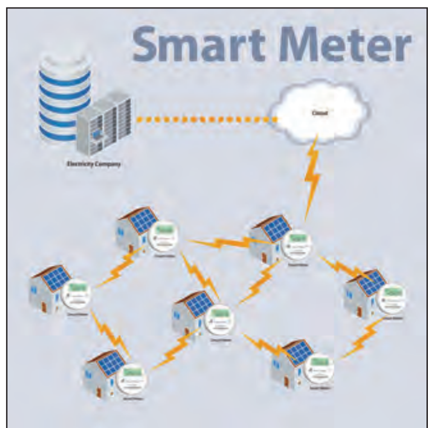
The revelation came at the end of the month when a hacker team succeeded in taking over vehicle functions by exploiting software weaknesses. A sweeping recall of 1.4 million vehicles resulted to proactively address the problem; no driver injuries were reported at the time.
NXP celebrated strong financial performance as the month drew to a close. The company reported $1.506 billion in revenue, a 12 percent increase compared to 2014. High performance mixed signal products for security, connectivity and mobility made the second quarter the 12th consecutive double-digit growth period for the company.

August

At a meeting of IoT professionals at the Embedded Systems Conference (ESC), the group conceded that Internet of Things technology will not take off until two lynchpin requirements are met: development of wide area networks and lower costs for hardware crucial to seamless connectivity. While hardware costs typically decline as deployment accelerates, the lack of networks hinders overall market development. While the group referenced good efforts to create networks by the LoRa Allience led by Semtech, and SigFox (France), the group foresaw that IoT devices would slowly enter the market since cellular networks appear to be, '…the only viable option for that kind of coverage for the next ten years….'

At the Flash Memory Summit Samsung announced solid-state drives (SSDs) and systems geared to drive 3-D NAND into mass markets. But analysts and even other vendors suggested that it may take most of 2016 before the technology is ready for mainstream implementation. The Consumer Electronics Association, also presenting at the Flash Memory Summit, said that while wearables constitute the fastest growing segment they are also the smallest and most fragmented. This led other analysts to conclude that fitness trackers and

smart watches both show signs of gaining traction with consumers, yet they have penetrated just 11 percent of US households, nowhere near the 60 percent penetration of smartphones in the US.



Altera executives seemed edgy about prospects of life under the Intel umbrella. Analysts, speaking with current senior executives and those who have already departed the company, cited fears of how well Intel integrates acquired companies given its PC-oriented leadership. Despite Intel's long-standing attempts to shed its dependence on personal computing, they cited what happened to past acquisition targets including Level One, DSP Communications, Sialogis Corporation, Giga A/S as cause for concern over how well Altera might fare. Smart meters are driving the IC market supporting IoT in utility markets. Global revenues for semiconductors used in water, gas and electric meters reached $1.2 billion in 2014, with growth standing at 11 percent according to IHS researchers. Growth opportunities remain as more public utilities change over to the technology, which better tracks customer utilization. The future points toward integrated ICs to do the work now being done by individual components; manufacturers with integration expertise are best positioned to take advantage of this growing market.

MediaTek's rapid growth in 4G smartphones is likely to be undermined by handset makers in China who are designing their own chips, according to Hong Kong based Bernstein Research. Spreadtrum Communications and Huawei are eroding MediaTek's position because the maturing market is favoring Chinese players that are backed and subsidized by the government. At the same time MediaTek is gaining market share from Qualcomm in the 4G and high-end segment.

September

Chinese upstart Phytium Technology made headlines with is aggressive 'Mars' design that was released at the Hot Chips event. The Mars architecture is designed for ARM-based servers and utilized advanced SoCs not seen before in mass market applications. But despite the fact that Phytium is only three years old, the company has deep roots in Chinese electronics—it is a subsidiary of China Electronics Corporation, one of the oldest state-run enterprises.

Gartner researchers reported that chip sales in September continued to slow largely due to stagnant sales of semiconductors headed into PCs, tablets and smartphones. They forecast that growth could dip to a fraction of one percent, but might rebound once third quarter sales figures were finalized. TSMC announced that it expected to begin early production utilizing a 10nm process later in 2015, and planned to achieve 7nm production capability by 2017. The road map that the company unveiled in Silicon Valley meetings also pointed towards a reduced cost version of its 16nm process in 2016 and a broad portfolio of specialty processes for IoT, automotive and sensor applications.

Perhaps leaping ahead of consumer acceptance and comfort, analysts at the Linley Group announced their research points to the availability of fully autonomous, self-driving cars by 2022. This new technology will help double the size of today's $10 billion automotive semiconductor market by 2025. Feedback from automotive industry insiders suggest that today's driver assistance and automation systems are mere 'appetizers' for the main course of self-driving cars.

The technology is already there and being tested, remarked Linley Gwennap, principal of the Linley Group. The researcher did not elaborate on how willing consumers will be to hand steering wheels over to microprocessors. Anyone for a replay of 'I Robot'?

October

Google's' Nest Labs announced it planned to release its Weave protocol in 2016 and will involve partners that will use it to connect smart home products such as locks, light switches and cameras. The advancement is seen by industry observers as another way that IoT devices are moving into more mainstream applications visible to a wider range of consumers.

The slump in PC market semiconductor sales was reflected in Micron Technology's report of declining sales revenue for a third straight quarter. Even though PC sales remain sluggish, the company reported healthy demand for memory chips in other end markets,

> "Analysts at the Linley Group announced their research points to the availability of fully autonomous, self-driving cars by 2022. This new technology will help double the size of today's $10 billion automotive semiconductor market by 2025"

pointing to the continued shift away from traditional computing and towards other small form factor computer options such as tablets and smartphones.

Marvell announced that it is sampling the first products based upon its MoChi approach to building modular SoCs. One of the company's two new 64-bit ARM processors is the first to implement final-level cache (FLC) technology, which aims to shrink external DRAM requirements. The MoChi design concept is Marvell's approach to creating products that operate like SoCs when interacting with application software, but may actually be composed of multiple die in one or more packages. The concept enables chips made in different processes to work together as closely as if they were grouped together on the same die.

Extreme Ultra Violet (EUV) technology got a boost from imec researchers in Belgium working with Cadence Design Systems. The two organizations partnered to create two 5nm test chips using a mix of 193i and EUV techniques. The researchers believe this approach represents the best alternative to breach the barrier limits of Moore's Law in transistor evolution.

Dell bid $67 billion to buy storage giant EMC in a mid-October acquisition proposal. The deal was billed as the largest high-tech purchase to date, but received mixed reviews from industry watchers. The analysts were unenthusiastic largely because both companies—though large and successful—are seeing flat or declining sales in their segments. Industry insiders wondered how the company would deliver growth to investors given little prospect for innovation beyond the company's existing portfolios.

The town of Bristol, England took innovation to a new height by turning itself into a 'petri dish' for experiments in communications and the Internet of Things (IoT.) Bristol received grants and gifts totally 75 million (GBP) to create wired and wireless infrastructure for a smart city. It aims to build applications ranging from assisted living programs for seniors to driverless cars and solar energy.

Taiwanese semiconductor giant TSMC reduced early-2015 planned capital expenditures of $10.5 billion to $8 billion, a 25 percent cut. The move came on the heels of slowing global demand for semiconductors.

Lam Research Corporation announced its intention to purchase KLA-Tencor, marking the start of the industry's largest merger of high performance process tool makers. The $10.6 billion deal was observed by some analysts as an effort to put the new company ahead of its arch-rival, Applied Materials. The merger was approved by both boards, but comes at a time of increasing regulatory scrutiny of M&A activity. In April Applied Materials and Tokyo Electron cancelled a planned $29 billion mega merger, citing opposition from antitrust interests at the US Department of Justice. Yet most analysts approve of the Lam/KLA deal, saying it will give the combined entity a decisive edge in global competition through pricing power it likely would not enjoy as separate companies.

November

Fears about automobiles being vulnerable to hacking led to more media coverage of the dilemmas facing car makers. While manufacturers have quietly sought to patch firmware and software holes, evidence remains that many newer car infotainment and computing systems are vulnerable to attacks that gain access through radio or cellular frequencies, or piggybacking on the short range signals from a consumer's key fob. According to the US Federal Bureau of Investigation (FBI), between April 2014 and June 2015, there were 992 'ransomeware' related complaints, with victims reporting losses totalling more than $18 million.

The Semiconductor Industry Association (SIA) reported that global chips sales declined 3 percent to $85.2 billion in third quarter. The decline followed trends from earlier reports, with declines in traditional PC sales and smartphones as leading indicators. At the same time sales picked up in September, leading some analysts to hope for a better year-end tally. Qualcomm reported to shareholders that it believed smartphone growth would continue to slow in 2016, and that prices for chips going into handsets will continue to fall, though less sharply than they did in 2015. Qualcomm also expects China OEMs will command a growing share of the market.

While Qualcomm fretted over its future with Samsung and with other key handset makers, its prospects may be looking up when it comes to printed electronics. Raghu Das, CEO or IDTechEx, hosted an industry forum on the subject in Silicon Valley, saying that the technology had matured to a point that engineers need to 'get printed electronics out of the lab and utilize their capabilities.'

Those poised to take advantage of these possibilities include Qualcomm and a handful of other companies. Qualcomm later presented new products at the forum, including a label that can gather data from a golf club and feed info to the player's smartphone. A thin-film battery maker, Blue Spark Technologies, displayed a bandage that can deliver a patients temperature information to a handset.

The strengthening US dollar compared to the position of other world currencies has taken a toll on the semiconductor industry, among many, and is forecast to lead to contraction in worldwide chips sales in 2015.

Samsung is set to make inroads into Intel's position as the world's largest chip maker in 2015, according to market forecasts compiled by researchers at IC Insights. The researchers say that Intel continues to suffer from its dependence on the weakening personal computer market and its limited success breaking into mobile phone applications. IC Insights expects Intel sales to contract 2 percent in 2015 compared to Samsung growing its chip revenue 10 percent, which should bring them in at $6 billion behind Intel's forecast of $50 billion in chip sales.
Merger mania continued in November

as Renesas Electronics became an investment target attractive to a number of suitors outside Japan, including China's Tsinghua Unigroup and Germany's Infineon Technologies. Tsinghua's ambitions in memory chips are well established since it is seeking a foothold in the logic business, especially in automotive and MCU segments.

Infineon is said to regard Renesas as an ideal fit, based on the Japanese chip vendor's strength in infotainment, head unit and digital cockpit technologies and other areas of automotive electronics where Infineon lags. It's also important that Renesas has a strong position with both Japanese and European automakers.

“A rocky 2015 did not deter Taiwanese semiconductor giant TSMC from predicting this month that it will achieve double-digit growth during the coming year and that its 10nm process is on schedule for production in 2016. The company's CEO also predicted similar results for 2015 at the end of 2014, so it remains to be seen how well the company will fare against headwinds now buffeting the industry”

December

T.J. Rodgers, outspoken CEO and President of Cypress Semiconductor, said this month that he expects 'merger mania' which is now driving consolidation across the industry may continue for another two years. The CEO cited a causal relationship between what executives see in the market and fears that not merging with a like-minded company could mean they are losing out on potential market share gains. Chip companies executed more than 18 M&A transactions worth more than $100 million in the last year; M&A activity totalling $110 billion was reported as of October 31st.

A rocky 2015 did not deter Taiwanese semiconductor giant TSMC from predicting this month that it will achieve double-digit growth during the coming year and that its 10nm process is on schedule for production in 2016. The company's CEO also predicted similar results for 2015 at the end of 2014, so it remains to be seen how well the company will fare against headwinds now buffeting the industry. TSMC also announced that its 7nm process was on track; the company could see 10nm as a transitional node leading directly into 7nm.

For only the second time in the last 25 years, business growth for the top chip manufacturers in 2015 is expected to beat the growth of top fabless companies, according to researchers at IC Insights. The change in fortunes is largely credited to Samsung's decision to use its own Exynos application processor in smartphones at the expense of Qualcomm. This growth notwithstanding, IC Insights said they also expect 2015 will be rather flat overall for the top 10 integrated device manufacturers (IDMs), while the top 10 fabless companies are expected to slip into slightly negative figures this year.

The International Electron Devices Meeting (IEDM) in Washington, DC was the setting for word from senior ARM researchers that even though it is getting harder and more costly to make chips smaller and faster, there is hope to be found in advancing Moore's Law. To combat an increasing set of design limitations, engineers will need to employ a host of remedies that could fragment and possibly dilute economies of scale.

This may result in significant sacrifices in density for the sake of schedules, combined with balancing the need for cost effectiveness with market timing. The researchers see hope in what is already being done and will be done to increase productivity and cut costs, noting as an example that multiple passes through lithography will increase costs while new steppers coming online for 7nm will be 50 percent faster than those used at 28nm.

United Microelectronics Corporation (UMC), the world's third largest foundry, said it expects to open a joint venture 300mm fab in China about two months earlier than expected. Production should begin in the third quarter of 2015. A spokesperson credited the aggressive readiness posture to faster than expected construction in China. Meanwhile, UMC arch rival, Taiwan's TSMC, also announced plans to open its first wholly owned 300mm fab in china, slated to begin production in the second half of 2018.

A Chinese government-backed firm has initiated a bidding war for chip maker Fairchild Semiconductor International. In November Fairchild accepted an acquisition offer from ON Semiconductor Corporation. The offer it accepted was for $2.4 billion, while the offer from the unsolicited bidder was for $2.6 billion. While Fairchild said it will review the new offer, its board has already accepted the ON Semiconductor bid, so it is unclear whether the Chinese company has a chance to acquire Fairchild.

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Nanoparticle silver ink to improve manufacturing

Genes'Ink and KELENN Technology spoke to Mark Andrews and explained how their system can improve printed electronics manufacturing.

GENES'INK and KELENN Technology recently announced co-development of a new proprietary nanoparticle silver ink for KELENN's new high speed printer, the KSCAN PE300. According to both companies, these new technologies can radically accelerate production and efficiency of printed electronics for RFID antennas, capacitors, OLED active layers and many other applications. We asked Genes'Ink and KELENN Technology to detail how their system can improve printed electronics manufacturing.

Q Speed appears a central attribute of the new KSCAN PE300, moving at 'several meters per minute' compared to only 'a few centimeters per hour' in existing systems – How do you achieve such a performance leap?

A Such performance is achieved thanks to a combination of innovations and technologies. KELENN Technology and Genes'Ink have worked together to create an industrial digital silver ink that can be used with KELENN Technology's proprietary high speed piezo jetting modules. KELENN Technology has redesigned the architecture, electronics and fluid management to be able to properly handle approximately 30 key parameters, in relation with printed electronics, such as rheology, nozzle clogging and many others.

Q Has speed been an impediment to more widespread adoption of inkjet printing of electronic circuits in the overall marketplace?

A Yes. Actually 90 percent of printed electronics is handled by screen printing. Companies are focusing on prototyping circuit design and ink formulation with low speed table top inkjet printers. However, the whole work has to be done once again when moving into industrial production scale. For the industry, before the KSCAN PE300 was announced, it was safer to put the emphasis on screen printing for production.

Q The partnership between Genes' Ink and KELENN Technology seems a natural outgrowth of a conductive ink maker working with a developer of improved electronic circuit printing technology – How do (ink and printer) complement one another to offer a better solution?

A To be able to print at fast speed, the volume of ink per droplets must be reduced compared to traditional methods. This matches perfectly with nanoparticle silver

ink, which requires less quantities for a given conductivity compared to traditional silver ink. From a consumable cost point of view, KELENN Technology's printer (uses) less ink for a given conductivity compared to screen printing. So the customer benefits from two major cost areas: improved productivity and reduced consumable costs.

Q Genes'Ink cites several applications of the new technology – active layers in OLEDs, RFID antennas, production capacitor printing. Can the technology also be used for printing the silver bus bars, lattice fingers or other elements in photovoltaic cells (printing on polysilicon wafers)?

A Yes, for example, in a very interesting case study, we have demonstrated that one litre of ink could produce approximately 1 million patterns.

Q Line accuracy seems another advantage of the new technology – Is this a benefit of the new nanoparticle ink, the printer itself, or both?

A Both technologies bring their advantages. The Nano ink specific formulation can be jetted very precisely. The printer has a native resolution of 1200 dpi with a positioning precision of the print head of up to 2 μm. But mostly, the precision is due to a number of innovations in the design of inkjet deposition that are brought to the market by KELENN Technology.

Q Ink silver content reduction (50 percent less) in your new system is another clear advantage – Can you elaborate about what enables the new printer and ink to use so much less silver?

A The (ink) formulation is a key feature. Nanoparticles of silver have the ability to coalescence and show conductivity with a very limited amount of ink and at low temperature. Reliability of inkjet deposition is a key feature as well; we are looking for a first pass yield of 95 percent. The quantity of ink waste per job has been greatly reduced by KELENN Technology compared to screen printing or other inkjet (systems).

Q The new technology mentions usage of photonic annealing in a controlled environment with a specialised atmosphere – Is the vacuum system and gas supply control self-contained, or does the manufacturer need to have out-board vacuum and gas delivery/evacuation?

A Yes, the whole technical environment is self-contained to facilitate installation and commissioning. The KSCAN PE300 is fitted with carbon filters for exhaust. In basic configurations, these filters can cope with small to medium productions. For volume production, or a more complex configuration, it is best to add external filters and output.

Q What have we not covered that is an additional benefit of the new system?

A A software package is included with the KSCAN PE300 to manage job productions; it interfaces with standard CAD electronics output vector files such as GERBER and simple image files such as TIFF, BMP and JPG. The KSCAN PE300 can also be fitted with a feeder and a stacker.

Q Do you believe the new system (ink + printer) offer decisive advantages?

A This system is opening the printed electronics market to industrial printers, not only electronics people. It is easy to use and they already use this kind of system in their plants.

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Electroplating

An old technology for the future

Kevin Witt, ClassOne Technology Vice President, offers insight into ways that classic electroplating processes are being updated to address the industry's latest metal deposition requirements.

ALTHOUGH IT MAY SEEM counterintuitive, a great many of the industry's most advanced devices, such as compound semiconductors, MEMs and smart sensors that are used in the latest electronics applications, are not built using the most advanced process technology on the largest wafers. There are a couple of reasons for this. In many cases, such as analog devices, the desired level of functionality can be achieved using 90 nm or larger critical dimensions rather than today's leading-edge 14 nm standard. In others, it can be cost. It makes no sense to invest in a 300 mm process line if market demand can be met using 200 mm wafers.

While large semiconductor manufacturers, especially those producing large volumes of logic or memory devices, have adopted the latest in metal deposition technology, many others have found that time-tested methods of depositing metal onto substrates — such as sputtering and evaporation — have cost-effectively met their requirements. That is changing. As technologies such as wafer-level packaging are increasingly adopted, these useful and relatively inexpensive techniques are reaching their limits. This article will briefly describe some of these limitations and suggest a proven alternative that can overcome them.

Capability limits

Sputtering and evaporation are limited in three main areas when it comes to wafer-level packaging applications: poor step coverage; limited feature fill; and poor metal lift-off for small features. Sputtering, for example, is mostly a line-of-sight process that relies on probability and randomness to uniformly deposit the desired thickness of metal on the substrate. High-aspect features, such as deep vias, the thick resist used for copper pillars, or the narrowly spaced lines found in redistribution layers cannot be properly filled. For structures that span different elevations within a die, it can be virtually impossible to achieve greater than 20-30 percent step coverage, even if continuity can be maintained. At the same time, once aspect ratios increase much beyond 3:1, filling features with metal, whether

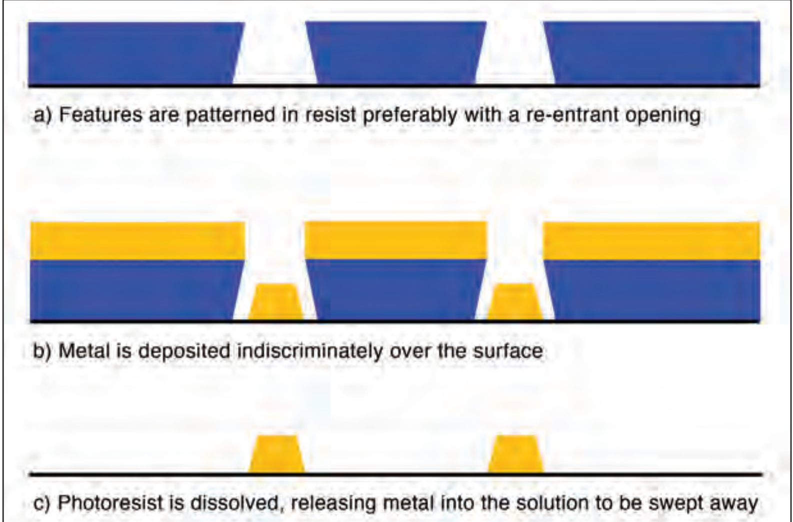

Figure 1. A simplified metal lift-off process.

via sputtering or evaporation, can be compromised by overhangs and step coverage limitations that can result in defects such as voids. Both techniques typically require the removal of excess metal from the substrate. As feature sizes become smaller, however, metal lift-off (Figure 1) becomes a problem because the features are so small they no longer adhere well to the substrate during subsequent processing. Similarly, the edges of features become less well defined and ragged, leading to an increased susceptibility to other types of defects, as well as introducing additional integration issues and challenges.

Cost

Sputtering and evaporation both cease to be cost-effective techniques when depositing the types of thick films required to build advanced devices used

in wafer-level packaging. Sputtering, for example, is a slow process that becomes extremely expensive when depositing films over a few tenths of a micron in thickness. It would cost a relative fortune and take an unreasonable amount of time to sputter the metal needed for a 90 micron copper pillar, even if the film stress could be managed.

With evaporation, waste becomes a cost issue. By the very nature of the process, the thicker the film to be deposited, the greater the amount of metal that ends up deposited off the substrate, such as inside the system. Finally, there is the raw material cost. At a minimum, the materials used in both sputtering and evaporation techniques must meet the same purity requirements as the deposited film, thereby increasing starting material costs. These very pure raw materials are, by their nature, more expensive than more commonly available, less pure counterparts.

The Electroplating alternative

Electroplating is a nearly two-century-old process that uses an electric current from an anode to deposit metal from a solution (the electrolyte) onto a cathode (the substrate). There are typically two electroplating process flows used in device manufacturing. The first, damascene, deposits the metal into features that have been etched into a previously deposited dielectric film or layer. The second, the through-template process, deposits metal in the open areas of a patterned dielectric template, such as photoresist, which is later chemically dissolved or stripped away.

Whichever process flow is used, the basic physics are the same. As shown in Figure 2, a seed layer, which acts as the cathode, is first deposited onto the surface substrate. A resist layer is then deposited and patterned lithographically to create the desired features.

This is often the very same mask that was used for the metal lift-off process. The substrate is placed into a plating solution, voltage is applied, and metal ions are then selectively deposited following the lines of the electromotive force (voltage.) Once the wafer is removed from the bath, rinsed and dried, the resist is then stripped away using standard solvent processing. Finally, the seed layer is etched away using the deposited features as a hard mask, leaving behind the isolated patterned features.

The electroplating process offers significant advantages over sputtering or evaporation for applications such as wafer-level packaging, redistribution lines and interconnects. It can deliver nearly 100 percent step coverage with

> "The idea for Solstice electroplating tools originally came from ClassOne's sister company, ClassOne Equipment. A long-time provider of quality refurbished tools, they were seeing a trend emerging, especially in small and medium-sized semiconductor manufacturers"

excellent feature fill, minimizing defect and integration issues. A simple, self-organizing process, it also offers deposition rates in excess of 4 microns per minute for some materials, making it an excellent technique for depositing the thick films required to build features such as the 90 micron copper pillars mentioned above. Its faster deposition rate also speeds wafer throughput and lowers overall cost of ownership. Electroplating offers an additional benefit since it is a purification process by nature. As a result, the raw materials need not be of the same level of purity required for sputtering or evaporation, which further lowers production costs. Finally, electroplating offers a much wider process window than the alternative processes, thereby increasing process flexibility.

As many university students have learned, making and using a small electroplating cell is simple and inexpensive. Outside of the laboratory and in the fab environment, the use of automated equipment and hazardous chemicals introduces concerns that need to be mitigated. There have been many different types of electroplating systems put into service over the years with varying degrees of success. Like most processes in semiconductor device manufacturing, electroplating makes use of potentially dangerous chemicals, so safety is a concern. Exposed or open baths of electroplating chemicals can be risky to both operations and maintenance personnel, as well as to the equipment itself. Chemicals can also pose environmental and facility contamination risks. Care should always be taken to ensure that plating equipment has integrated secondary containment and appropriate fail-safes as well as interlocks, such as those called for in the SEMI S2, CE, or FM4910 specifications. Since plating solutions tend to be corrosive, material compatibility becomes an important issue for safety as well as for maximizing asset longevity.

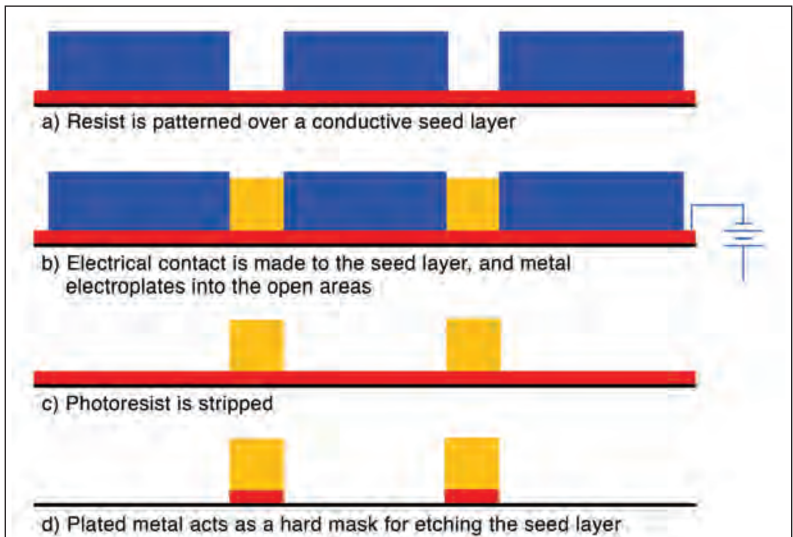

Figure 2. A simplified electroplating process.

Once safety guidelines and process controls are taken into consideration, choosing a plating system comes down to the performance to price ratio for the production volumes in question. Wet benches are often used for non-critical plating operations and can be either automated or manually operated, depending on production needs. For low levels of non-critical production, the variability in results that arise from manually operated equipment may not become an issue. Alternately, hand operations can become cumbersome as volume levels increase. When reproducibility and its consequent variation reduction matters, or when a high degree of uniformity is demanded, wet benches fall short and single wafer tools are desirable.

Single wafer tools fall into two general categories: fountain platers and paddle platers. Used more widely in the industry, fountain platers place a wafer face down into an overflowing pool while the wafer rotates. By comparison, paddle platers mechanically agitate the electrolyte near the surface of a static wafer. Paddle platers often can achieve higher ultimate plating rates for the same chemistry (due to a higher amount of agitation). But this benefit needs to be considered against the mechanical complexity of the chamber and necessary automation, which lead to increased costs. These tools tend to be physically larger than their fountain plater counterparts, which may be a concern for older, more space-constrained facilities.

The future of electroplating: ClassOne Technology's solution

The idea for Solstice electroplating tools originally came from ClassOne's sister company, ClassOne Equipment. A long-time provider of quality refurbished tools, they were seeing a trend emerging, especially in small and medium-sized semiconductor manufacturers. These users were facing a technology transition from vacuum-based deposition to electroplating and needed new equipment; however, their budgets were limited. So, a new company, ClassOne Technology, was created specifically to address those needs. ClassOne's Solstice platform was designed for ≤200 mm wafers, to provide advanced electroplating capabilities at an affordable cost.

Experience-grounded innovation

ClassOne Technology immediately brought in a team of seasoned veterans, with over 400 years of combined experience both in designing and using plating systems. They set about creating a new generation of electroplating systems to replace the aging Equinox® plating tool originally developed by Semitool in the early 1990s. Aimed at users of 200 mm and smaller wafers, the design objectives were functionality, reliability and ease of use combined with broad and advanced processing capability. To achieve ClassOne's standards of quality and performance the Solstice team utilized elegant design and best-of-breed components to deliver dependable performance while maximizing cost-efficiency. The Solstice control system employs Windows 7 and is based upon systems that have been in use for over 10 years in other industries. These elements form the basis of all three Solstice systems:

- S8: a fully-automated, cassette-to-cassette production tool with up to eight chambers;
- S4: fully automated like the S8, but with up to four chambers;
- LT: a semi-automated development tool with up to two chambers.

All Solstice tools share components, subassemblies, software and controls. This provides economies of scale and also gives users a seamless path from plating development to full automated production. Using the same chambers for all wafer sizes, for example, allows users to make changes in materials or wafer diameters by simply and quickly changing-out a few relatively inexpensive components. The Solstice ECD family is an excellent example of how an older technology can gain new life by solving emerging problems. Electroplating has significant potential to provide a cost-effective alternative to the sputtering or evaporation of metals for advanced applications. This time-tested technology is now becoming a key enabler and cost reducer for many small and mid-sized device manufacturers who have neither the need nor the budget for larger deposition systems.

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Prior to ClassOne, he consulted for a variety of tech-based companies including VEECO, ESI, BioNano Genomics, TruTag, Advanced Inquiry Systems, SolarSemi Engineering, and The Thompson Group/SEMSYSCO.

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Critical challenges in gas supply to advanced semiconductor manufacturing fabs

Shrinking device geometries challenge manufacturers to more precisely manage gases and other critical materials. Dr. Anish Tolia, Ph.D., Head of Global Marketing, Linde Electronics, explains why scale, quality, supply chain, and sustainability should dominate production planning.

RAPID CHANGES in the technical and business environment of semiconductor manufacturing have intensified challenges throughout the supply chain. Semiconductor manufacturers are pushing the limits of physics and driving a constant need for new materials. Semiconductor companies and materials suppliers must formulate mutually profitable models for developing new products to achieve continued success.

At the same time, process control and purity demands are reaching unprecedented levels due to increasing complexity of the processes and related yield challenges. Tighter production process control and advanced metrology solutions (aka 'fingerprinting') are key to addressing these issues.

On the business side, industry consolidation continues and fewer customers are building ever larger fabs, which presents materials delivery and environmental challenges. The materials supply chain is increasingly globalized; managing risk and delivering uninterrupted product is critical. Larger scale and more on-site gas generation and delivery schemes are cogent approaches to solve the problems.

Finally, as the global semiconductor industry grows, environmental concerns and limited natural resources, which include rare gases like helium, krypton, and neon become an area of increasing focus. Innovative solutions like materials recycling can be a useful tool in reducing environmental impact.

This article explores the four key factors in gas supply to advanced semiconductor manufacturing fabs – Scale, Quality, Supply Chain, and Sustainability – as well as the drivers and solutions for each factor.

SCALE - Larger fabs + more complex and smaller devices = more gases

Consumers want ever more technologically sophisticated smartphones, tablets, smart watches and other wearables, not to mention automotive, household, and medical electronics. Semiconductor companies are increasing capacity to meet this demand – a 10 percent integrated circuits upsurge worldwide in 2014.

This increase has also predicated a move from MiniFabs (monthly production of 10-30,000 wafers) to MegaFabs (30-80,000 wafers a month) to now GigaFabs (80-100,000 wafers a month). A typical logic foundry is now at 80,000 WSPM (wafer starts per month); a typical memory fab now exceeds 120,000 WSPM. Additionally, many large fabs are now concentrated in clusters (science parks).

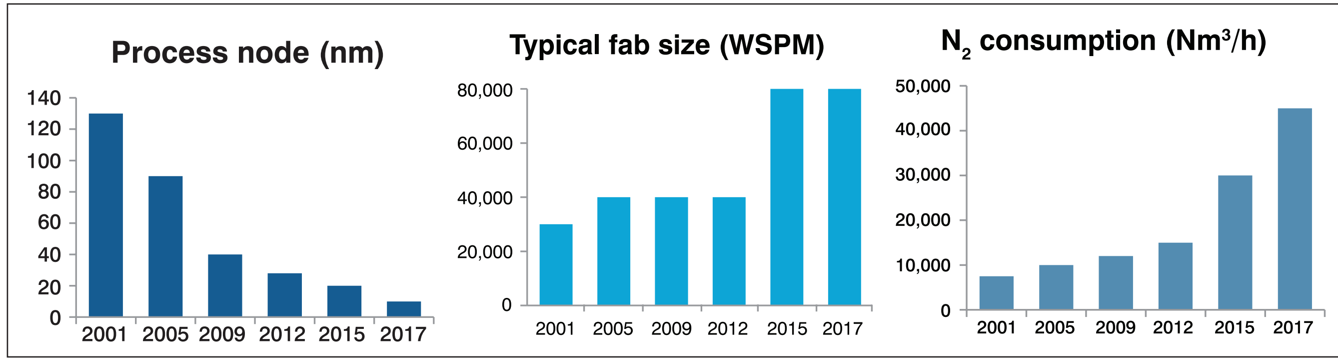
The highly competitive mobile devices market is forcing fabs to ramp to higher volumes faster than ever before. Additionally, development costs for new technology can exceed $2B (USD). In such an environment, economies of scale are essential for profitable operation.

In order to meet the demand and technological challenges, a larger volume and variety of gases is needed. These gases are used in multiple process steps such as etching/cleaning, deposition, doping, purging, and lithography/patterning in the manufacture of semiconductors.

Not only is the increased size of fabs contributing to the need for more gases, the move from single patterning to multi-patterning requires more gases for the production of each wafer.

As feature sizes are driven downward, new challenges emerge in maintaining the cost and performance gains. Until about 2006 at the 65 nm node, gains were obtained by shrinking physical devices using direct optical lithography. After that, more benefits were derived by introducing new materials into the process; for example, germanium in the transistor. By 20 nm, the minimal feature size became smaller than the wavelength of light and necessitated workarounds like multi-patterning to overcome physical limitations. All these factors have increased the consumption of gases per wafer.

Because of the need for low power and high performance, which 2D devices cannot handle, the industry is moving to 3D devices, which increases circuit density. This move to 3D FinFET and 3D NAND and the corresponding move to



increased transistor processing – epitaxy, etch, and ALD (atomic layer deposition) – drive the need for new and increased materials to construct more complex devices.

The gas most consumed in the production of electronics is nitrogen (N_2). Nitrogen is used for purging vacuum pumps, in abatement systems, and as a process gas. As process nodes have been driven down and the typical fab size has increased, nitrogen consumption has grown substantially. In large advanced fabs, there can be as much as 50,000 cubic meters per hour of nitrogen consumed, which compounds the need for cost-effective, low-energy, on-site nitrogen generators.

Another electronics manufacturing gas that is seeing an increase due to larger fabs and increased capacity is hydrogen. Hydrogen is utilized during epitaxial deposition of silicon (Si) and silicon germanium (SiGe), as well as for surface preparation. Significant volumes of hydrogen are also anticipated to be used in extreme ultra violet (EUV) in the future as 450mm wafers enter production streams. Hydrogen can be delivered economically as compressed gaseous hydrogen (CGH_2) or liquid hydrogen (LH_2) for smaller amounts and distances. However, due to the growing need for hydrogen, more fabs are now demanding on-site production through steam reforming or electrolysis. There is also an upswing in the need for rare gases such as neon, krypton, xenon, argon, and helium. This increased usage of gases that are not as readily available as nitrogen has driven sporadic temporary worldwide shortages, particularly helium and neon. Rare gases are also used for wafer cooling (helium), as source gases in lasers (neon), and as sputtering gases (argon and krypton).

So what are the critical challenges for fabs when the volume and type of gases multiplies due to added processes and more complex technology?

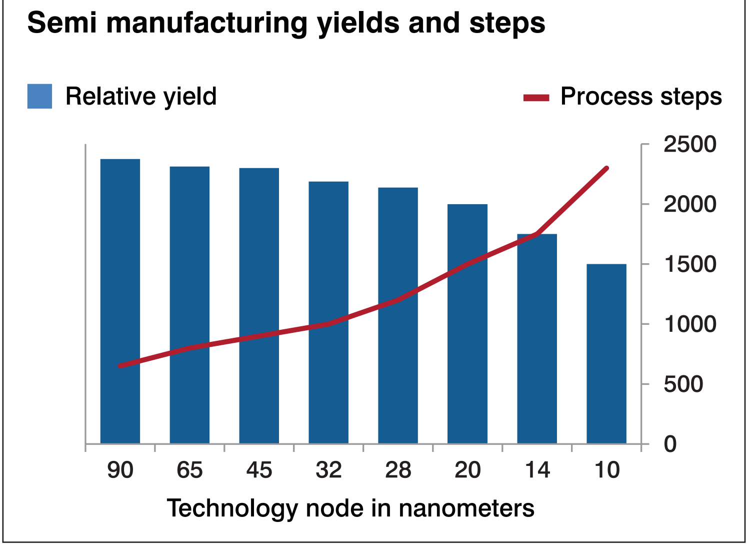
QUALITY - Changing needs due to complex technology

The first consideration for fabs is maintaining quality. Typically as the technology node gets smaller, the number of processes goes up and yield potentially goes down with each added process step. Manufacturers are diligently trying to overcome limits to stay on track with Moore's Law; doing so requires more stringent controls.

Critical process steps in high-volume semiconductor device manufacturing at aggressive feature sizes require stringent control of variability. For a silicon wafer with 100 or more advanced logic chips, each with up to 4 billion transistors and billions of connections, it is critical to remember:

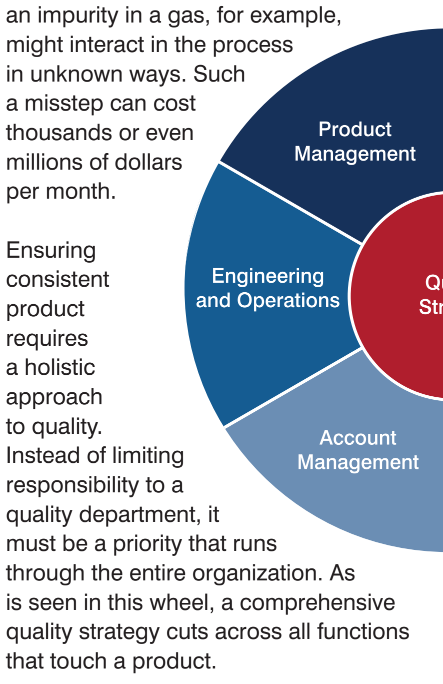
- Essentially all the transistors and connections have to work as intended on each chip.
- The process has to be repeatable from wafer to wafer while chip production proceeds at rates of up to 80,000 wafer starts or more per month through a fab.

Variation among transistors on a chip leads to poorer overall chip performance and must be minimized. Even trace contaminants – including those that are not specified on a standard Certificate of Analysis – can cause measurable shifts in semiconductor processes and affect chip performance in advanced devices. Given that process materials are a critical input in wafer processing, it is easy to see how the quality of electronic materials (EM) products becomes increasingly important for chip manufacturers at leading technology nodes.



Another important consideration is the challenge of the unknown: engineers don't know how a specific impurity might impact performance. This can lead to needing additional processes and controls, which can mean higher operational costs and more risk from higher investments. Any misstep along the way –

an impurity in a gas, for example, might interact in the process in unknown ways. Such a misstep can cost thousands or even millions of dollars per month.



Ensuring consistent product requires a holistic approach to quality. Instead of limiting responsibility to a quality department, it must be a priority that runs through the entire organization. As is seen in this wheel, a comprehensive quality strategy cuts across all functions that touch a product.

To meet the demands for rigorous quality control, organizations may need to hire materials scientists, chemists, and process engineers and change the culture of their organization so that every department has a strategy and plan that contributes to the overall quality vision.

Process stability across the supply chain is made possible through SPC (Statistical Process Control), SQC (Statistical Quality Control), MSA (Measurement System Analysis), and BCP (Business Continuity Planning) systems. Fingerprinting furnishes the means for rigorous measurement, reducing variability, and tightening controls. Gas purity, consistency, and reliability are then delivered as an integral part of the final product.

SUPPLY CHAIN – Drivers reflect complexity

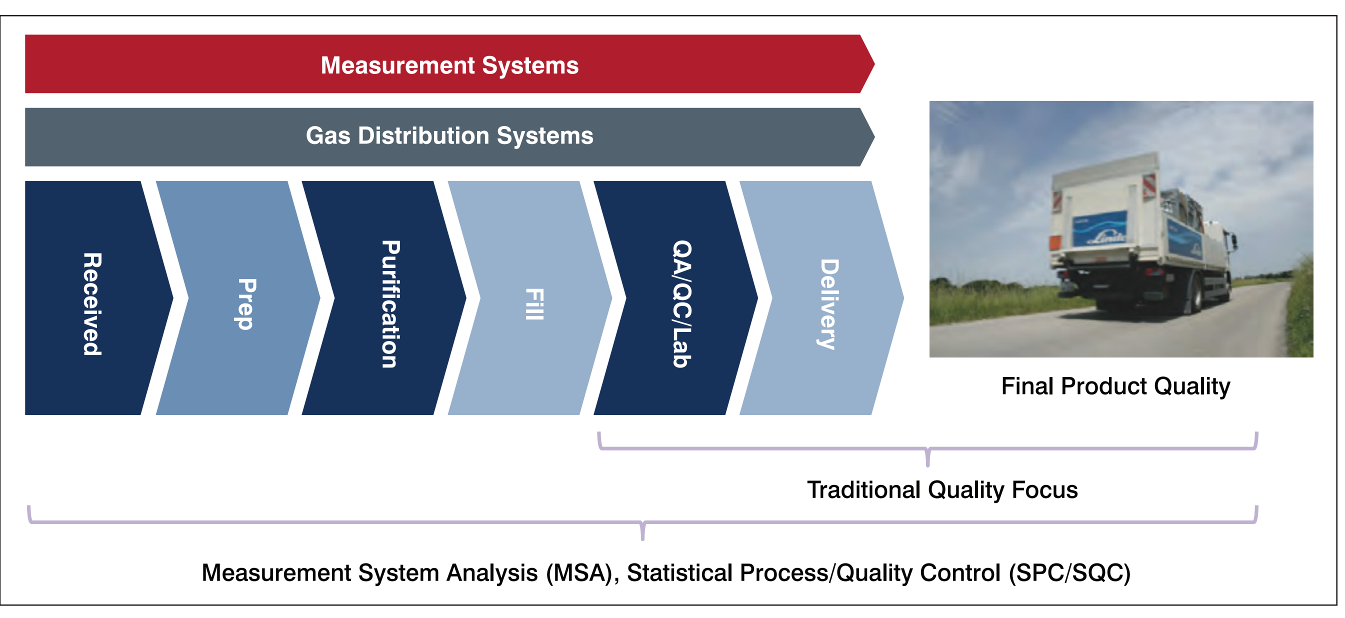
The increased demand and complexity of gases used in electronics manufacturing not only impacts quality, but also the supply chain. Many external factors can affect the supply chain including transportation or labor strikes and natural disasters. For example, after a magnitude 9.0 earthquake and subsequent tsunami hit Japan on March 11, 2011, all shipments coming in and out of Japan had to be checked for radiation.

A change in government regulations can also affect the supply chain, with an example being the 2008 Olympics. During the Beijing Summer Games, the Chinese government blocked hazardous materials from coming into multiple ports, including chemicals such as sulfuric acid, which is used in semiconductor manufacturing. Materials had to be trucked in, which required a lot of extra planning and two months extra time to deliver.

Limited raw material suppliers can impact availability for manufacturers. In order to secure supply, there is a move toward local and regional suppliers. Semiconductor manufacturers must partner with electronic materials suppliers and allow visibility into ramp demand of materials for new technologies and to do capacity planning so that together they can determine usage volumes for specialty gases.

To successfully maneuver all the complexities and potential pitfalls, it is crucial to cultivate an interlinked, comprehensive, customer-focused supply chain. Manufacturers can address these issues through Business Continuity Planning (BCP). They can start by assessing where and how to invest to diversify their supply chain on multiple continents. This includes doing procurement forecasting and planning with customers and suppliers to meet demand and identifying potential supply gaps by plotting product-source mapping.

It is essential to have at least two sources for raw materials and to have customers qualify both sources. Fabs should create raw materials, manufacturing, transportation, and labor shortage contingency plans and develop supply gap mitigation and implementation plans. Bringing materials closer to customers through localization and on-site plants cuts down on logistics complications and makes materials more readily available. It is essential to coach suppliers along



Water	Electricity	Natural Gas	Greenhouse Gases
10 cubic meters used per wafer at 14 nm node x 80,000 wafers per month x 12 months = **9,600,000 cubic meters** of water used per year (enough for 39,506 people in U.S.)	1220 kilowatt per hour used per wafer at 14 nm node x 80,000 wafers per month x 12 months = **1,152,000,000 kilowatt – hours** or 1,152,000 megawatt – hours electricity used per year (enough for 94,846 people) in U.S.)	61 cubic meters used per wafer at 14 nm node x 80,000 wafers per month x 12 months = **58,560,000 cubic meters** of natural gas used per year (enough for 26,899 people in U.S.)	8 greenhouse gases used, which if unabated, are the equivalent of 4.2 tons of CO_2 per wafer. After 90% abatement at 14 nm node x 80,000 wafers per month x 12 months = **400,000 tons CO_2** equivalents used per year

the whole chain on Statistical Quality Control (SQC), Statistical Process Control (SPC), and customer requirements to show them why and how things that they do can help customers avert disaster at multiple points in the supply chain.

SUSTAINABILITY – Reduce environmental impact

With complex supply chains, a scarcity of key materials, increasing environmental focus, and the need to reduce operating costs, the ability to ensure a secure and reliable supply of materials is intrinsic to staying competitive.

Fabs face several obstacles to being leaders in environmentally sustainable manufacturing, which is being mandated by an increasing environmental focus and concerns of customers as well as heightened governmental regulations. Semiconductor manufacturing is a highly complex energy and resource intensive process. Consequently, fabs are huge users of resources. Electronics manufacturing plants are not always located in the optimum position for materials deliveries, making it vital to think about how materials could potentially be recovered, purified, and re-used on-site, saving shipping costs, reducing logistical risks, and decreasing carbon footprints.

Materials such as helium and argon can be recovered on-site, purified, and returned for re-use in the manufacturing process. Materials such as sulfuric acid can be recovered on-site and be made available for use in other applications. And high-cost materials such as xenon can be recovered, shipped off-site, purified at an external facility, and then made available for reuse.

An industry success story illustrates how it is possible to eliminate tens of millions of tons of carbon dioxide (CO_2) emission equivalents per year through the use of fluorine (F_2), with zero GWP (global warming potential), in place of nitrogen trifluoride (NF_3), with a GWP of 17,200 and sulfur hexafluoride (SF_6) with a GWP of 22,800. This case involves a major memory fab, which uses on-site fluorine plants as a safer and more cost-effective alternative to cylinder fluorine for cleaning Chemical Vapor Deposition (CVD) chambers in its manufacturing process. It also uses fluorine to replace other fluorinated cleaning gases such as NF_3 following tests that demonstrated up to 40 percent reductions in cleaning time and a 35 percent decrease in the mass of gas used.

Conclusion

So what are the implications for manufacturers of the following four key factors in gas supply: Scale, Quality, Supply Chain, and Sustainability? They must proactively plan around both short and long-term needs. This requires longer term planning to include CAPEX investments and building on-site gas production and recovery when justified by size and growth expectations.

It is imperative that fabs do long-term planning in partnership with suppliers who commit to their needs – suppliers who value and implement process control and measurement and provide security and diversity of supply. It is only through this type of partnership that mutual needs can be truly understood and that the ever-evolving demands of consumers and the needs of manufacturers can be continually met.

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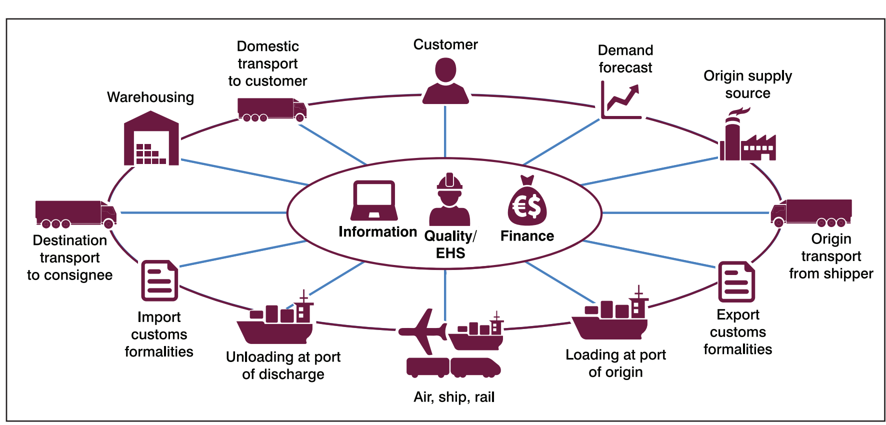

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Taking charge of change

Handling product and process change on an industrial scale is no simple subject. But there are solutions to manage change that semiconductor manufacturers have embraced as both effective and profitable. By Mark Andrews, technical contributor from Silicon Semiconductor.

CHANGE IS DISRUPTIVE. As a species, humans tend to oppose it since eons ago 'change' often meant danger. Even though we now live in a world free of saber toothed tigers, we are still beset with change that can be good, or bad. It's a touchy subject. Thankfully, humans have the ability to adapt, which is a key concept behind effective change management.

It's time to embrace change, manage it; make it work for us (for a change.) As every manufacturer knows, change is central to product lifecycles. Yet we often struggle with it. Manufacturing has become so fast-paced that some wonder whether they are managing change, or change is managing them.

Every manufacturer has to manage manufacturing process change in some form or fashion, whether a new product introduction or a continuous improvement; but not every manufacturer manages it effectively.

There is a lot to be gained from managing change beyond keeping one's sanity. The Change Management process in Systems Engineering is the process of requesting, determining attainability, planning, implementing and evaluating changes to a system. It has two main goals: supporting the processing of changes and enabling traceability of changes.

There are many components of managing change: ECR (Engineering Change Request), ECN (Engineering Change Notice), ECO (Engineering Change Order). Regardless of the term or the component, the goal is to manage and implement changes in a controlled fashion. Those who master changing products and processes as-needed / when needed will succeed. Those who stumble over change tend to fail.

Managing change is a core requirement of achieving a productive 'fast future' in which development times shrink, product lifecycles compress, manufacturing occurs globally and decentralized control, design and strategy become common corporate practices.

Central to winning in a Fast Future economy is realizing that managing change is not only doable, but can fit into a smoothly flowing factory floor, and can be highly profitable.

To see how vital dealing with change truly is for industry, consider the complexities of semiconductor products. Consumer devices today are created in shorter development cycles across different continents and distributed globally. The size of semiconductor markets keeps growing because they are in products that never had them previously while the population of people who can afford advanced products is also growing.

Manufactured products today are more likely to contain semiconductor components due to the versatility, control and functionality that they enable.

Consider major categories that did not have semiconductor components originally, but now rely upon them: light bulbs, automobiles, refrigerators, and telephones; hand tools with electric motors; not to mention the computers, smartphones and tablets that started life as semiconductor aggregations.

Products with logic/memory circuits are among the most complex. They must meet rising consumer expectations by being smaller, thinner and more capable; this elevates the need for integrated change management applications to the highest level.

Every single product that relies on semiconductors can have many variations driven by customer requirements such as geography, user interface, power types, privacy safeguards, RF links, materials composition and other differences including environmental and safety regulations as well as planned obsolescence. Research organizations like Gartner forecast that semiconductor sales will grow more than 5 percent in 2015.

Successful semiconductor manufacturers today have had to expand in order to sustain product development and withstand downward ASP pressure while meeting rising consumer expectations. Products that once were designed, manufactured and distributed from a single point are now multinational. Distribution can involve thousands of outlets; each point has the potential to impact a company's brand image thanks to millions of social media 'reviewers.'

More often than not, semiconductor manufacturers today rely on sophisticated manufacturing execution system (MES) applications to track and control every aspect of product

lifecycles. Particularly in the case of complex devices with multiple digital control, memory and RF interfaces, the manufacturing process involves hundreds if not thousands of steps, all orchestrated across distance and time. Changes occur by the hundreds each month; mistakes are costly. Big mistakes can be fatal.

While the pitfalls of manufacturing in a 'fast future' may seem daunting, the rewards can be equally amazing. Success means achieving superior quality while taking every practical step to improve manufacturing processes, embrace customer feedback and manage change.

Leading semiconductor manufacturers are making change work to their advantage by investing in unified MES applications that are capable of managing end-to-end processes including changing designs and other qualities. Those with multiple sites, complex products and global customers have led the charge to invest in modern MES technology. They are no longer hindered by islands of automation, legacy paper-based systems and disjointed operations; they can now innovate, adapt and succeed.

While every manufacturing process plays a role in delivering high quality / competitively priced finished goods, managing change is often one of the most difficult tasks to master. No matter the product, and no matter how automated and well-attuned the workplace might be, factories function best once stable processes and material flows are achieved. Factories love stability. Anything that disrupts stability effects productivity, yields and is a risk for creating waste, rework and shut-downs. But since change is inevitable, it's equally clear that enabling smooth and orderly change is most likely to return a factory to an optimal state.

Expert at helping manufacturers realize the benefits of MES and its attendant change management capabilities is the PLM Software Group of Siemens Corporation. The company's Camstar Product Management group focuses on assisting their industrial customers thrive while managing change.

Camstar Product Director Silvio Saouaf has seen almost every level of need and urgency as he has guided customers to choose change management applications and put them into practice. While no single customer story is exactly like another, semiconductor manufacturers typically appreciate

that they need a software system that can help their factories function more smoothly. But they are not always sure just how powerful a well-integrated system can be until they see it in operation.

"Anyone who has had a costly 'excursion' in their plant is aware of how expensive it can be in terms of lost productivity and actual cash loses," He explained. "In cases where outmoded or siloed systems are in use, one side of the factory literally can't tell what the other is doing; that's when mistakes can start piling-up and (customers) typically realize very fast why they need a system to manage change at every level."

Globalized semiconductor manufacturing has created great opportunities. But at the same time it has created more risk for the manufacturer.

"The global consumer market has created greater demand for products with more capabilities. Manufacturers are having to manage this with larger product portfolios and increasingly complex devices. It's a two headed dragon of opportunity and risk. If you're doing this without a change management system you are at risk of hurting your brand all the way down to liability for consumer safety in some cases."

Saouaf explained that while some manufacturers still try to manage change with a paper approach, most have found this too ineffective and resource intensive. Paper systems hitched to siloed inventory or product lifecycle applications can severely limit a company's ability to retrieve, track and manage data real-time.

The move towards integrated MES applications that work across all aspects of manufacturing has taken hold. But all applications are not created equal. He sees a number of manufacturers with an MES paired with product lifecycle management (PLM) based applications as well as enterprise resource planning (ERP) products that don't talk to each other, which creates bottlenecks.

The key to success is an integrated approach that also empowers the manufacturing team to deal with change. How manufacturers handle change is increasingly a make-or-break point for successful globalization, he said.

"A fact you have to remember about some applications is they started out as tools for accounting or 'just the engineers.' They weren't conceived as tools to be used by everyone that needs access," He said. "What amazes people when they see a truly integrated approach is how easy it can make the whole process."

"If everything you have is siloed, it gets more complex to manage change, especially when you involve more people and different languages," he said. "Success requires targeted collaboration, integration of the right facts and on the timeline the customer needs while allowing for localized inputs. An application like Camstar Change makes it easy for people to collaborate with the right individuals overseeing the process, all from one central authoring system. All parties have the correct input. And it is not just a document (they see,) they can look at the actual products that are going to change and how the changes will appear; there is no guesswork."

When considering applications that can increase productivity across multiple manufacturing, design and engineering teams in multiple locations, the ideal change management program should offer these capabilities:

Create and configure

- Plan changes by creating the change package at the authoring site
- Assign ownership, approvers and content editors as well as the target systems and sites
- Select a business process workflow from a configurable range of options

Add content

- Identify new products to manufacture, and/or products and processes that have changed
- Track modeling changes to determine which products and processes the

> "Every manufacturing plant encounters quality issues of varying size and complexity, but those using advanced MES with change management capabilities are able to track, isolate and rectify problems more quickly for a return to smooth operation"

change(s) affects
- Automatically organize dependencies and sequences

Approve changes
- Route the change package for review and approval, following the business process that the author models within the change management application
- Enable reviewers to assess the changes and their impact using the application's analysis tools
- Import approvals from the product lifecycle management (PLM) system

Deploy targets
- Perform one-click distribution to targeted sites and systems
- Easily deploy details of the changed process/procedure across one site or multiple global locations

Activate on each target
- Accept and activate changes according to a schedule that works for local environments
- Enable users to make changes to meet their local needs (within parameters that the author establishes.)

Globalization has accelerated the need for change management. As globalizing involves more widely-dispersed design, engineering and manufacturing locations, the need to effectively manage change is accelerating in-step. Semiconductor market growth is driven by expanding populations that can afford more advanced products.

Advanced devices today often adopt semiconductor based memory, logic and digitized control because these systems are more dependable, flexible and capable, which enables greater product diversity through software or firmware tweaks. Product lifecycles are also changing (usually shorter,) while design and manufacturing speeds-up to meet consumer expectations.

Any way that a manufacturer looks at the future, it's clear that 'fast' is a factor. The ability to quickly implement change and manage it will be decisive.

To stay ahead of consumer demands, manufacturers need complete control and visibility into the myriad of process steps each product requires. Achieving this requires integrated manufacturing execution systems (MES) applications that contain effective change management modules like the Camstar Change process offered by Siemens PLM. While it is possible to operate a manufacturing plant with siloed applications, an integrated approach not only saves time and increases productivity, it provides the level of traceability and accountability needed across large organizations.

Every manufacturing plant encounters quality issues of varying size and complexity, but those using advanced MES with change management capabilities are able to track, isolate and rectify problems more quickly for a return to smooth operation.

"The goal ultimately is a closed loop system with visibility up and down the line. It should incorporate all the available information to connect design and execution in a way that is not only functional but highly usable—it should deliver a great user experience. It should proactively prevent errors, yet be flexible enough to handle rework, scrap, warranty, recalls, and provide audit trails.

"For manufacturers that achieve an optimized level of change management, they can build any product in any plant throughout their system, at any time. They will lead their market and handling change will no longer be something to worry about, it will just be one more part of a well-managed product lifecycle," Saouaf said.

Footnote: Annie Mullen of Siemens PLM Software contributed to this article.

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THE MEMORY ROADMAP:
a paradigm shift from 2D to 3D

"There will never be enough memory": this idea has driven the continuous scaling of memory technologies. Today, DRAM and Flash, both charge-based memory concepts, represent the largest memory markets. For a long time, experts have predicted that emerging memories, such as STT-MRAM, resistive RAM and phase-change memory, all resistance based, would replace the common DRAM and Flash technologies in the Terabit era. According to Jan Van Houdt, Chief Scientist at imec and IEEE Fellow, we will first witness a paradigm shift from planar towards 3D technologies, rather than from charge-based to resistance-based memory.

IN TODAY'S ELECTRONIC SYSTEMS, a large part of the system area is consumed by memories. Jan Van Houdt: "Let's take a closer look at CPU (or central processing unit) centric systems, used in for example personal computer and server applications. Close to the CPU, on-chip, static random access memories (or SRAMs) are the dominant memories. These embedded SRAMs are volatile and excel in speed. But they consist of 6 transistors, and are therefore rather big and have a large cost per bit. Also on chip, less fast and somewhat denser, are higher cache memory levels, mostly made in SRAM or embedded DRAM technology. Off chip, farther away from the CPU, you find ROM (read only memory) or NOR Flash memories for code execution, DRAM chips for the working memory, and non-volatile Flash NAND memory chips for storage. In general, memories located farther away from the CPU are cheaper, slower, denser and less volatile."

The ever increasing performance of computation platforms and the consumer's hunger for storing and exchanging ever more data drive the need to keep on scaling memory technologies. For a long time, memory experts have been dreaming of one

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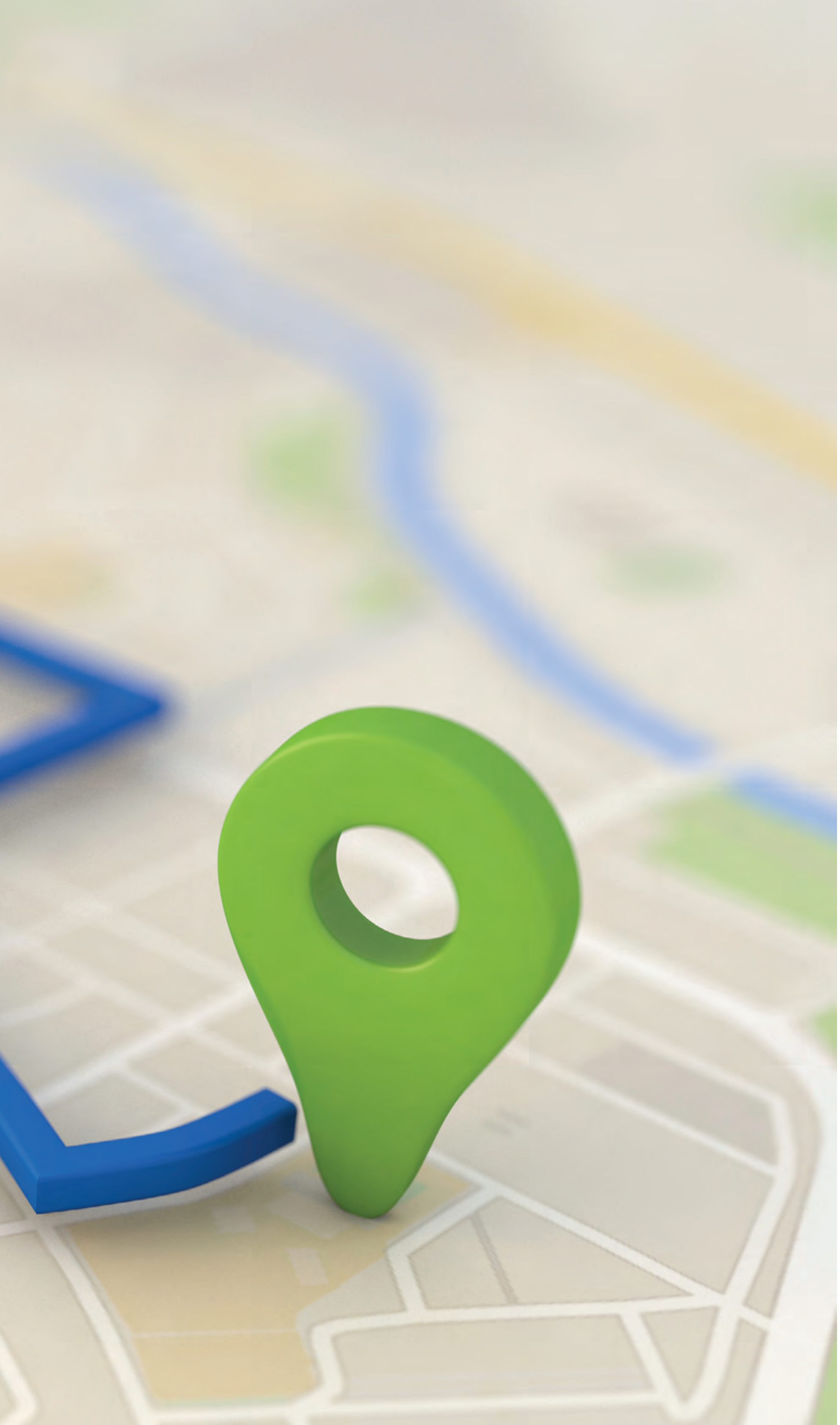


unified memory, a scalable memory concept that would replace all the different memories. Jan van Houdt: "This idea has meanwhile been abandoned. Electronic systems require ever more different memories with different sizes and specifications. For the terabit era, we expect that the memory hierarchy becomes even more complex. We will soon witness the introduction of two new memory classes: storage class memory (or SCM) and embedded non-volatile memory (or e-NVM). With SCM, we fill up the gap between DRAM and Flash. It will provide an intermediate step between high-density Flash and high-performance DRAM in terms of latency, speed and cost. SCM will mainly serve the server market: Google, Yahoo, Facebook... they will benefit from this new class of memories which do not necessarily require 10 years of retention. Another newcomer, embedded non-volatile memory, is today only present in some particular applications (microcontrollers and smart cards). Current non-volatile technologies like Flash are too complex to embed in high-end CMOS technology. Especially for mobile applications, there is growing interest in a new embedded non-volatile memory technology."

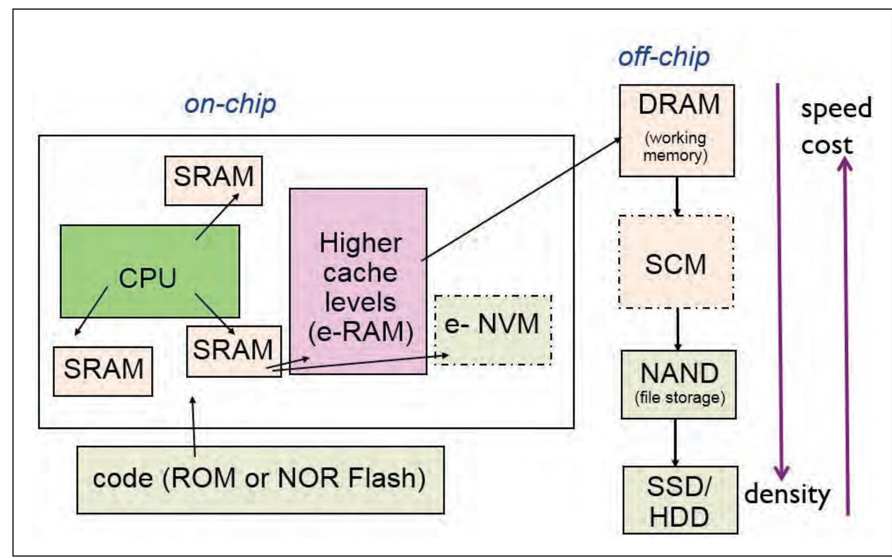
DRAM and Flash memories: scaling issues

Today, the memory market is dominated by DRAM and Flash memories. DRAM chips are now available up to 8GB densities in a 25nm technology node, while Flash has ended up at 16nm half pitch dimensions, yielding 128GB on a single chip with 2 or even 3 bits per cell. Both memories are charge based, and this generates some particular scaling issues.

Jan Van Houdt: "DRAM is structurally a very simple type of memory. It consists of one transistor and one capacitor that can be either charged or discharged. However, upon further scaling, this concept runs out of steam. One of the problems is related to periodic DRAM refreshment. Today, a DRAM memory is being refreshed about 16 times per second to deal with the slow discharge of the capacitor. When further scaled, the capacitor has to be refreshed even more frequently, hindering the performance of the memory. Scaling the capacitor not only increases the leakage, but also the aspect ratio, which has already increased to 35 for conventional double-sided crown capacitors. A new architecture, the one-pillar architecture, with new electrode materials and higher-k dielectrics, partly solves this problem. But even this pillar capacitor cannot be scaled down below 15nm." Nevertheless, DRAM scaling can continue, but not in the classical way. Jan Van Houdt: "An interesting way to scale on performance and power, is 3D stacking: stacking different DRAM dies and connecting them by using through-Si vias (TSVs).

This leads to the so-called hybrid memory cube, which also allows to take many logic functions off-(memory-) chip and optimize the chip system as a whole. A disadvantage of this solution is cost, since TSV technology is still a quite expensive technology."

With Flash, the problem is more complicated. Flash memory stores information in an array of memory cells, mostly made from floating-gate transistors. While in traditional devices, each cell stores one bit of information, more advanced concepts store 2 or even 3 bits per cell. Jan Van Houdt: "Today, a NAND Flash cell in a $4F^2$ cell layout provides the smallest dimension. But when we decrease the half pitch of the cell array, the threshold voltage shift associated with the tunneling of one electron towards the floating gate, dramatically increases towards several 100mV's. This limits programming accuracy dramatically at the 10nm technology node, and unless new smart ways around this 'single electron limit' are found, this could very well be the end of planar NAND technology. So, we are running out of electrons. The most attractive solution is to go 3D. Not by die stacking, as in DRAM, but by stacking vertical cells by using a charge trap Flash architecture. Following this 'bit cost scaling' (or BiCS) concept, the memory cell transistors are placed vertically on the chip in order to increase the density even further. This way, up to 32 cells have already been stacked in a functional device, and first products are on the market."



The classical (server-based) memory hierarchy.

What about the emerging memory technologies: STT-MRAM, PCM and RRAM?

In the past years, experts have predicted that new memory technologies, mainly resistance-based, would replace 'old' DRAM and Flash technologies in the years to come. At first, it was believed that phase change memory (or PCM) could replace NOR Flash, while resistive RAM (or RRAM) would replace NAND Flash. Spin-torque transfer memory was identified as the only technology that could potentially replace DRAM due to its high endurance.

Jan Van Houdt: "Recently, more and more experts believe that these new memory technologies may first end up in embedded applications and in storage class memory. Take STT-MRAM, for example. The core element of STT-MRAM is a magnetic tunnel junction in which a thin dielectric layer, usually 4 to 5 atomic mono-layers, is sandwiched between a magnetic fixed layer and a magnetic free layer. Writing of the memory cell is performed by switching the magnetization of this free magnetic layer. STT-MRAM is a very promising memory concept because of its non-volatility, high-speed, low-voltage switching (<1V) and almost unlimited read/write endurance. But there are some disadvantages. The memory is too large for Flash replacement, and cannot (yet) be used in a 3D configuration. Also, STT-MRAM is current driven, ending up with a high write power and large peripheral devices. The technology could potentially replace DRAM, but can at the moment not compete with the low cost of DRAM technology. Eventually, if (3D) DRAM has finally hit the wall, and STT-MRAM is able to shrink its size, this would become a possibility. On a shorter term, I expect STT-MRAM to replace embedded SRAM in higher caching levels (L3)."

Another resistance-based technology is PCM, which is based on the melting and (re-)crystallization of chalcogenide material. Jan Van Houdt: "PCM is a reasonably mature technology with a high endurance (on cell level), large programming window and non-

> "Recently, more and more experts believe that these new memory technologies may first end up in embedded applications and in storage class memory"

destructive read. The technology writes reasonably fast at low voltage. However, due to its large programming power and issues with material (in)stability, PCM is currently seen as a replacement for the declining market of NOR Flash technology."

And then there is RRAM, which relies on the formation of a conductive filament in an insulating layer. Jan Van Houdt: "Typically, an RRAM device consists of two electrodes that sandwich a thin dielectric layer. This layer serves as the ion transport and storage medium. The ionic movements and structural changes in this medium, caused by e.g. an electric field, cause a measureable change of the device resistance. RRAM comes in several flavors: oxide RAM (or OXRAM), conductive bridging RAM (or CBRAM) and vacancy modulated conductive oxide (or VMCO). In general, the concept is low cost, low voltage and can be realized with 'standard materials', like TaO_x. But although the resistive switching structures show excellent memory characteristics, implementation of high-density RRAM arrays lags behind, mainly due to sneak current issues.

To suppress the leakage paths, a non-linear selection device (or selector) is required to connect serially with each resistive switching element forming a memory cell. And that's one of the weaknesses of RRAM. In order to compete with Flash technology, I see the need for two major breakthroughs: RRAM needs to become more dense by directly going 'true' 3D, i.e., by placing cells vertically on a chip. In this configuration, there is however no space for the selector. Another breakthrough is therefore required in the development of a selector-less concept for 3D RRAM. But that's still in the future. As a first target, I see RRAM as a candidate memory technology for application in storage class memories and embedded non-volatile memories. The concept is especially interesting for Internet of Things and low-density applications."

Newcomers

Besides these charge- and resistance-based memory concepts, researchers explore other memory concepts to fill in the memory hierarchy. For example, there is the return of ferroelectrics: the FeFET. Jan Van Houdt: "FeFET is for sure not a newcomer. It has long been considered the ideal memory, but material issues, the breakdown of the interfacial layer and the bad retention characteristics have always been showstoppers. Recently however, a ferro-electric phase has been found in HfO_2, a well-known material, and this triggered new interest in this memory concept." Besides exploring new technologies, researchers also look at the system level. SRAM, for example.

Jan Van Houdt: "Memory makers do not consider this a true memory technology, since it is realized on chip in standard logic CMOS technology. But we do need a replacement for SRAM, since SRAM deteriorates with every new CMOS technology generation. And there are some interesting options that deserve further investigation. Ferro-electric tunnel junctions, for example, or spin-based domain wall switching. Spin-based concepts in general are very attractive, as they could possibly solve important issues with charge-based concepts (the decreasing number of electrons) or resistance-based concepts (which are current based)."

Conclusion: the paradigm shift

While emerging memories have been predicted to replace the common DRAM and Flash technologies in the Terabit era, the industry has clearly shifted towards a more conservative view. Jan Van Houdt: "This view focuses on the continuation of well-known concepts, even though pushing them to the required density levels is not straightforward either. The immaturity of the resistance-based concepts (mainly PCM, RRAM and STT-MRAM) has slowed down their introduction in the roadmap. We will first witness a paradigm shift from planar towards 3D technology rather than from charge-based to resistance-based memory. The resistance-based emerging memories will first show up in new application fields, like storage class memory and embedded non-volatile memory."

Jan Van Houdt received a PhD from the University of Leuven in 1994. During his PhD work, he invented the HIMOS™ Flash memory, which he transferred to several industrial production lines. In 1999 he became responsible for Flash memory at imec and as such was the driving force behind the expansion of imec's memory program. Today he is Chief Scientist of the Memory Department. He has published more than 250 papers in international journals and accumulated more than 200 conference contributions (incl. 35 invitations and 5 best paper awards). He has filed more than 50 patents and served on the program and organizing committees of 10 major semiconductor conferences. In 2014 he received the title of IEEE Fellow for his contributions to Flash memory devices.

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Beyond the curve to **foldable displays**

Lightweight, unbreakable, flexible and wearable; these are just a few of the development targets for contemporary consumer electronics. Over the past couple of years interest in flexible displays that meet these needs has increased significantly, with the market for this flexible display technology predicted to expand to more than $21billion by 2020[1]. Dr. Michael Cowin, Head of Strategic Marketing, SmartKem Ltd looks at the opportunities ahead.

FEW INDUSTRIES have the same rate of development as the electronics sector. Buoyed by consumer demand for fresh innovation and fierce industry competition, electronics development exists in a rapid cycle of continuous improvement. One of the most exciting and eagerly awaited outputs from this process is the development of bendable and flexible displays; a potentially transformative technology set to emerge over the next few years.

Curved displays are already available in the commercial space, with the more recent emergence of curved phones and television screens. Yet despite their novelty, the real 'wow' factor in the consumer experience has yet to be achieved. The value in the next generation of smart and wearable technology will come with the introduction of flexible and foldable devices such as smartphones, tablets and watches. However, this demands a new semiconductor platform with entirely new physical properties and form factor capability which in turn raises a unique set of challenges for traditional and new thin-film transistor (TFT) technologies to overcome.

Significant developments in electronic devices almost always require a corresponding advance in their functional components and materials. Leaps in processing power, for instance, have often occurred due to the emergence of increasingly smaller and denser transistors. In contrast, the rise of thin-film electronics has relied on the development of TFT technology with increasingly stable and uniform properties over wide areas.

These properties are in increasing demand; however the challenge now lies in ensuring the transistors also demonstrate true physical flexibility. This is set to become a key market driver, with organic semiconductors beginning to change the landscape of traditional TFT based platforms.

Organic semiconductors now deliver similar, and in most cases superior, properties to traditional inorganic devices, but with much improved physical flexibility.

Organic based TFTs (OTFTs) are already starting to penetrate the supply chain for the development of truly flexible Active Matrix Organic Light Emitting Diodes (AMOLED) displays and Electronic Paper Displays (EPD).

Indeed OTFT technology is now being seriously considered as a straight replacement in amorphous silicon (a-Si) lines for the manufacture of plastic, lightweight and ruggedised LCDs.

Figure 1: The evolution of flexible electronic devices has required a new approach to development, typified by the emergence of high performance organic semiconductors.

Furthermore the utility of organic semiconductors as a platform technology is set to play a pivotal role in how we see, touch and sense information in every aspect of our lives. This combined with the shift towards Big Data, The Cloud and the Internet of Things will drive flexible and adaptable technology fully into the mainstream in the form of a new generation of displays, touch screens and sensors.

Understanding organic semiconductors: Smart chemistry for smart electronics

Traditional inorganic TFT semiconductors are formed from amorphous or polycrystalline structures and as such are unable to meet the market demands of robust flexibility. In the case of Low Temperature Polycrystalline Silicon (LTPS), for example, the poly-crystalline network is partially responsible for the semiconducting properties but is also the root of the material's inflexibility. Organic semiconductors are fabricated from small organic molecular species, polymers or a combination of both which allows them to overcome this fundamental limitation through their intrinsically flexible nature; offering the potential of ultra-flexible displays that can be folded to a sub-millimetre bend radius with no change in TFT performance.

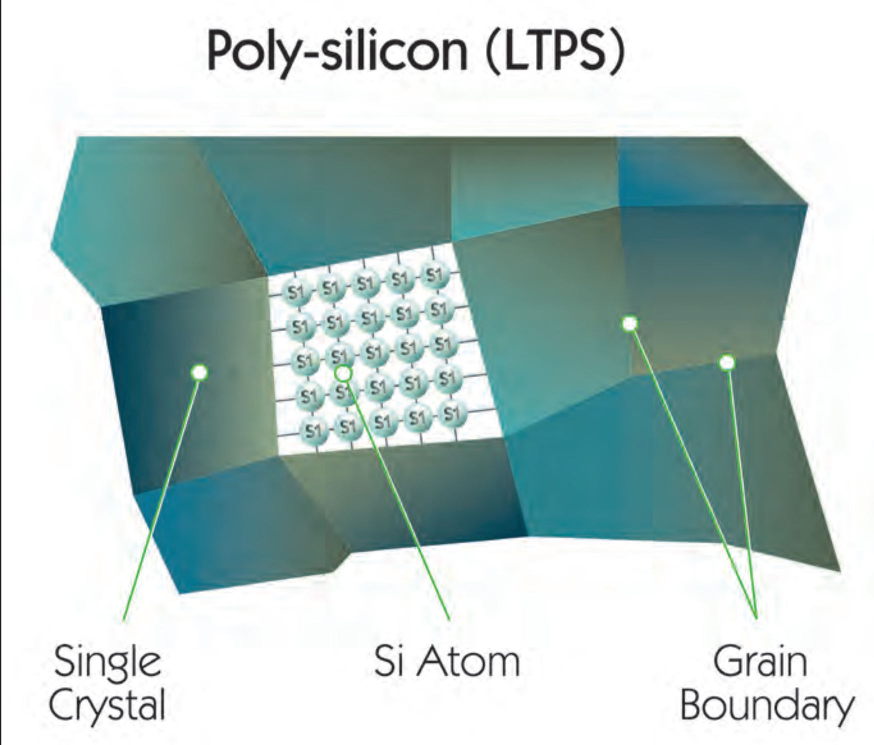

Image courtesy of AUO

This end product advantage is further complemented by a range of additional benefits such as a high mobility performance and a potential cost down proposition to manufacturers through ease of processing, higher yields and increased throughput achieved via low temperature processes such as Sheet-to-Sheet and eventual Roll-to-Roll (R2R) print techniques.

Organic semiconductor technology generally fits within two main material categories: polymeric and distinct molecular materials. A common feature of both is that they are types of conjugated systems, meaning they consist of alternating single and double bonds which lower the overall energy of the molecule and increase stability.
Efficient device operation can be ensured by matching the highest electron energy level of the organic semiconductor to the work function of a metal contact. For high performance TFTs, high charge carrier mobility is required which naturally favours crystalline small molecule semiconductors; molecules that are closely packed with regular arrangement in a crystal lattice increase good π-bonds and therefore efficient charge carrier mobility.

A new class of organic semiconductor materials eliminate such issues by designing into solution based semiconductor 'inks' the preferred features of chemically stable, high mobility, single-crystal organic semiconductors and combining them with amorphous semiconducting polymers or 'binders'. This material combination offers the electrical performance of single crystals but with the uniform processing characteristics required for high mobility.

As such the key benefits of organic semiconductors are realised with a technology platform that offers ease of production coupled with superior physical and electrical semiconductor performance in end-product form. Although organic semiconductors can be stable up to 300°C the ease by which these solution-based materials can be processed at low temperatures offers manufacturers a wide range of cost effective stack materials and substrates, and easier bond/de-bond and inter-

Characteristic	a-Si	LTPS	OTFT	Oxide
Flexibility & Fold Capability	✗	✗	✓✓	✗
Route to stretch-ability	✗	✗	✓✓	✗
Low Temperature Process	✗	✗	✓✓	✗
Print Compatibility	✗	✗	✓✓	✗
Mobility	✗	✓✓	✓	✓
Bias Stress Stability	✗	✓✓	✓✓	✗
Low Cost of Ownership	✓✓	✗	✓✓	✓
Established Supply Chain	✓✓	✓✓	✓	✓
Suitable for Wide Area	✓✓	✗	✓✓	✓
Reproducibility	✓✓	✓✓	✓	✗

Figure 2: The different TFT characteristics

layer alignment due to less expansion and contraction. This all adds up to significantly improving production yield (over high temperature processing) and thereby reducing production costs over any area of substrate.

One company leading the development of organic semiconductors is SmartKem with its product *tru*-FLEX™. While the electrical performance of *tru*-FLEX™ exceeds the need for applications such as AMOLED, LCD and EPD - more critically, the resulting TFTs are almost unbreakable, exhibiting flexibility down to a highly acute bend radius, thus eliminating the need for exotic and costly strain management layers. This offers original equipment manufacturers a high degree of confidence in product performance making the SmartKem *tru*-FLEX™ material a key component for highly rugged and reliable flexible display applications such as mobile and wearable devices.

Easing the printing processes

In addition to being the only truly flexible technology currently available, one of the major advantages of organic semiconductors comes from their ease of application. Solution based semiconductor inks can be applied to substrates through a range of additive processes and print production systems, including slot dye, spin coating and inkjet printing.

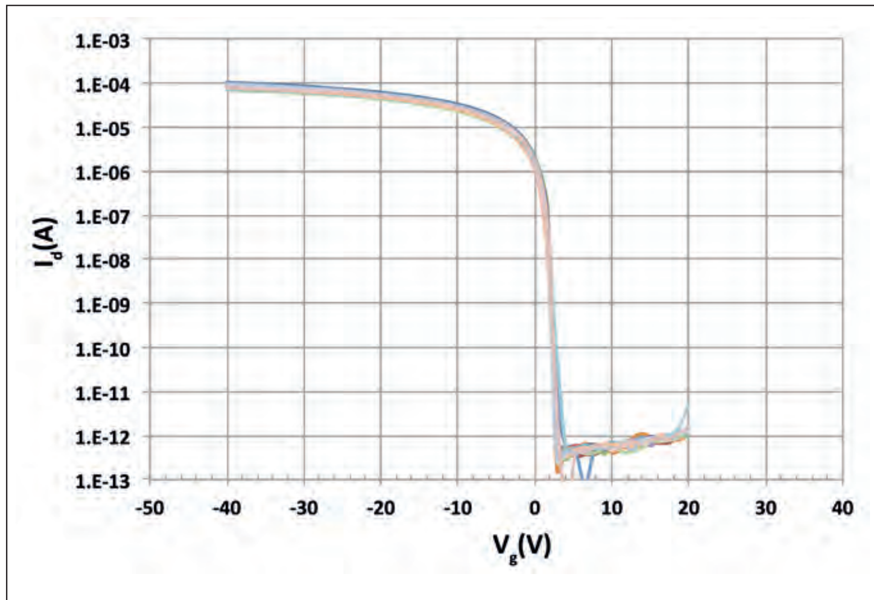

Figure 3: Typical linear transfer curves for SmartKem's tru-FLEX™ TFTs
x-axis : VG (V) y-axis : ID(A)

This application flexibility, along with the improvements in final product quality, process control and overall efficiency, make organic semiconductors an attractive prospect for manufacture. Organic semiconductor ink coatings are also compatible with R2R processing. Here, semiconductor materials are continuously or near continuously patterned onto a wide substrate area.

This high throughput process enables semiconductor fabrication and coating at a fraction of the time and cost of traditional manufacturing methods. Although still in its infancy, combining organic semiconductors with a scaled up R2R fabrication process is considered a realistic and incredibly lucrative prospect. For this reason many consider R2R processing the ultimate goal for electronics manufacture and organic semiconductors a critical component to achieving this.

The next generation of electronics

From displays and augmented touch screens to sensors, organic semiconductors are set to play a pivotal and diverse role in this new generation of electronics. Meeting the demands of this growing market requires developers of organic semiconductors to push boundaries in terms of the electrical performance and dynamic physical characteristics of these materials in TFT form. In response to this technological advancement the IEC standards for electronics are being re-written and re-defined to standardise every facet of this new industry.

Printable organic semiconductors have made the transition into pre-production and are enabling electronics manufacturers throughout the industry to make new and exciting form factor displays and products that will overhaul the current consumer world. And it's all a lot closer than you think.

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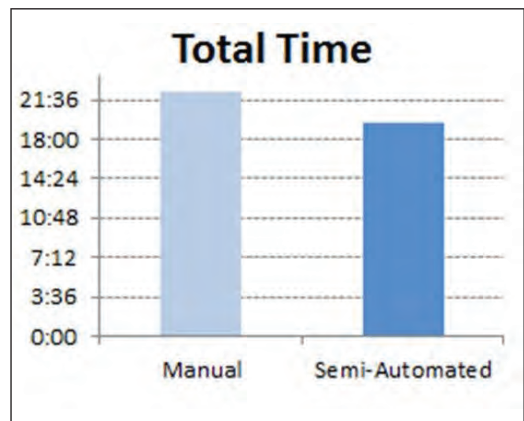
Maximizing productivity in the lab

Failure analysis labs typically involve lots of manual tasks performed by highly skilled operators. However, failure analysis labs are now adopting practices from the fab, such as increased automation, as the need for more and faster failure analysis feedback becomes critical to maximising yield. Todd Templeton from the FEI Company explains some of the practices and efficiencies that can be gained through automation in the modernised lab.

MOST PROCESSES found in today's advanced failure analysis (FA) labs rely heavily on skilled technicians performing a variety of tasks that require them to make hundreds, if not thousands, of small operations each day. These tasks might require operators to manually insert failed or defective components into electrical testers, grind down packaging or surface layers to expose specific circuitry, mark and navigate to suspect areas in a SEM or dual beam FIB-SEM, and set imaging or preparation conditions for SEM or TEM analysis. This sort of operation is very different from the process that occurs on the other side of the wall, in the fab. There, batches of wafers are processed according to specific recipes with very little human interaction. In most 300mm fabs, factory automation software directs the movement of FOUP (front opening unified pod) cassettes filled with wafers between process tools where recipes are automatically downloaded and run. Very few operators are required to run a fully automated, "lights out" fab. Efficiencies in operation are achieved largely because routine steps or processes have been automated and



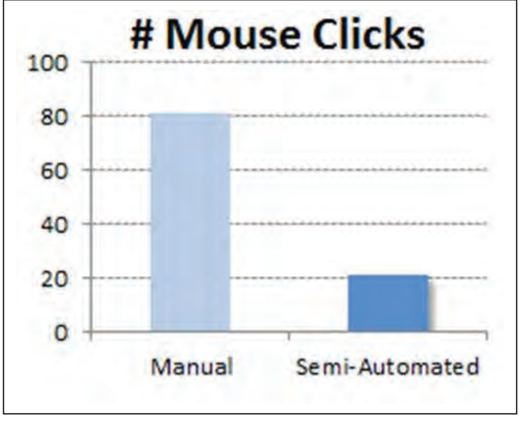


Figure 1. Throughput and mouse click comparison for making a thick lamella prepared for in-situ liftout.

the need for operator interaction minimized. This methodology is now making its way from the fab and into the FA lab as the need for more and faster failure analysis feedback becomes the bottleneck to yield ramp.

Transition from manual to automated

For many decades, the process of manufacturing semiconductor chips was managed through the use of a paper trail. Cassettes of individual wafers were batched together into lots and moved from process to process based on a printed set of instructions that accompanied the batch on the manufacturing floor. Later, as computational power increased, factory automation software was introduced into fabs to allow operators to move lots of wafers into a particular process step and determine the proper process conditions for the next manufacturing step. After manually selecting the correct conditions for the process step, the wafers were processed and then manually logged out and physically moved to the next manufacturing location.

As factory automation software became more sophisticated in the mid 1990's, operators on the factory floor were no longer required to manually enter in lot and process information. Recipes and lot tracking became more automated, reducing the number of mistakes and the amount of time wasted waiting for operators to be present. With the advent of overhead transport (OHT) systems

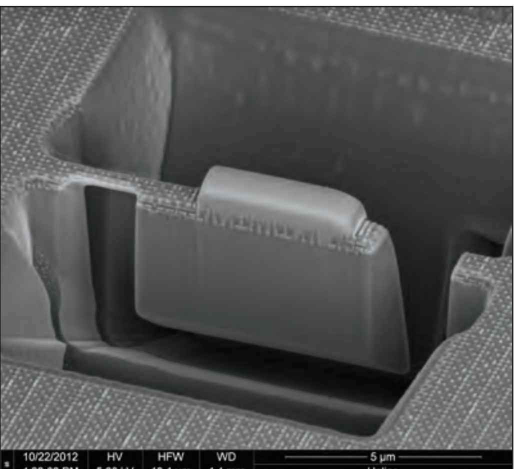


Figure 2. Thick lamella ready for ISLO.

central stockers were able to store, move, and retrieve 200mm standard mechanical interface (SMIF) and 300mm FOUP cassettes, eliminating the need for operators to interface with wafer lots and process equipment. Improved lot movement, reduced operator injuries, and fewer missed processing steps resulted from this enhanced automation.

Reducing operator strain and involvement in the more mundane aspects of failure analysis is a goal commonly vocalized by lab managers. Managers know that reserving their valuable human resources for the most critical process steps reduces operator fatigue and burnout. A method for creating recipes to automate basic, repetitive steps in the failure analysis process has been available for some time and is now showing benefits. For example, the first step in the preparation of a thin section for examination in a transmission electron microscope (TEM) is creating a thick lamella containing a specific feature or defect and preparing it to be lifted out of the bulk sample [1]. Once the operator has navigated to the location where the lamella is to be created, the next series of steps is generally the same for all samples created in that lab. Automating these steps, including automatically setting system operating parameters such as pattern sizes and locations for bulk silicon removal, FIB and SEM beam settings, and stage orientation, allows them to be executed without an operator in attendance.

Automation can significantly reduce process time and operator interaction with the tool. To illustrate this, we performed a test using an automated FIB-SEM (FEI Helios NanoLab 460F1 DualBeam with iFast automation software). The test evaluated the number of mouse clicks and time required to create a 150nm thick lamella ready for liftout, comparing a fully manual method a fully automated process. The results show that the automated recipe process was able to create the lamella 12% faster than the manual method and with nearly 75% fewer mouse clicks (Fig.1) In addition to offering ergonomic improvements to all users, the automated approach also allows novice operators to attain the quality and throughput

performance standards required in their labs more quickly. Once the thick lamella has been created, it must be extracted from the bulk sample and thinned to its final thickness – thin enough to transmit electrons and isolate the feature of interest – typically a few tens of nanometers. Extracting and manipulating a sample this size for thinning and transfer to the TEM is not trivial. One method, the in situ lift out (ISLO) process, proceeds by attaching the nearly free thick lamella (Fig. 2) to a nanomanipulator probe, cutting the lamella free, moving and attaching the lamella to a TEM grid, and finally cutting the attachment to the nanomanipulator probe. Once attached to the grid the lamella is thinned to final thickness with the FIB, and the grid, with the lamella attached, is transferred to the TEM. Because the typical dimensions for a thick lamella ready for ISLO are in the 0.5 – 2.0μm thick by 20μm wide range, the transfer process requires great precision.

The ISLO process was developed as a manual process and has been well documented [2-4]. Except for some very unique cases, nearly all TEM lamella that are extracted from bulk samples using ISLO follow an identical process, making this an ideal candidate for automation.

Challenges with automating the ISLO process include, but are not limited to: accurate movement of the nanomanipulator needle to prevent collisions, which may destroy the lamella or nanomanipulator needle; a predictable and repeatable needle shape; attaching the chunk to the TEM grid so proper final thinning and eventual zone axis alignment in the TEM can be realized; and finally, optimization of the speed and success rate at which this process can be performed. As a result of a comprehensive approach to solving these challenges a fully automated method for ISLO has been developed [5].

Increasing lab efficiency through automation

As a result of automating more and more of the process steps for creating TEM lamella, lab managers can increase the efficiency and productivity of their valuable human resources. In FA laboratories where no automation is employed, technicians must be at the dual beam preparation tool 100% of the time when creating TEM lamella. The process of selecting the target region of interest (ROI), placing the milling boxes and selecting the beam conditions to create a thick lamella, and then performing the ISLO process are all performed manually. Conversely, in labs which have adopted a more automated approach to creating lamella, technicians are able to oversee the operation multiple dual beam sample preparation tools at the same time.

An illustrative example comparing a fully manual FA lab with a more modern lab which has adopted automated system recipes for sample processing follows. In the fully manual lab, a technician can create a 100nm thick lamella and perform the ISLO process in roughly 29 minutes once the ROI has been identified. In the case where 8 lamellae from the same wafer are being prepared

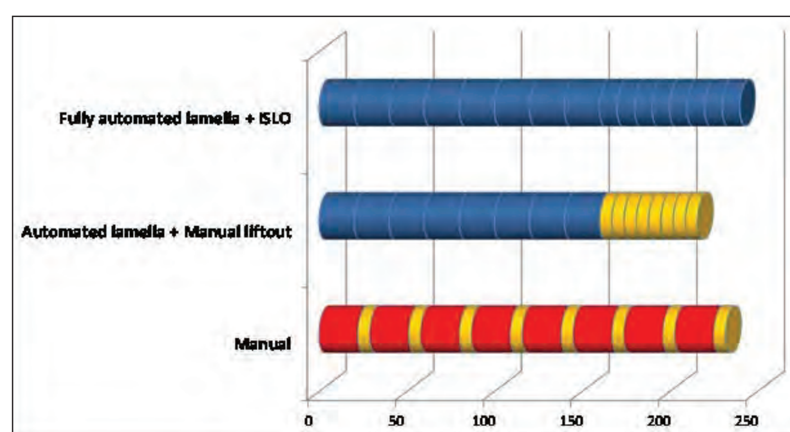
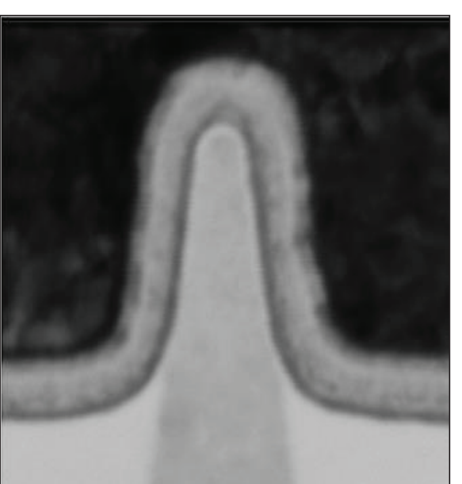
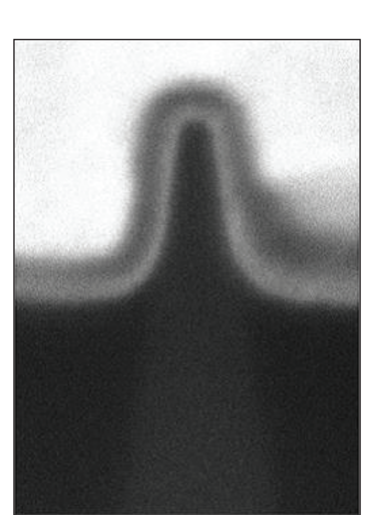


Figure 3. Comparison between manual and fully automated lamella creation and ISLO. Red represents the amount of time an operator is sitting at the instrument creating the lamella. Yellow represents the amount of time an operator is manually performing the ISLO process. Blue represents a fully automated process where there is no operator required at the instrument.





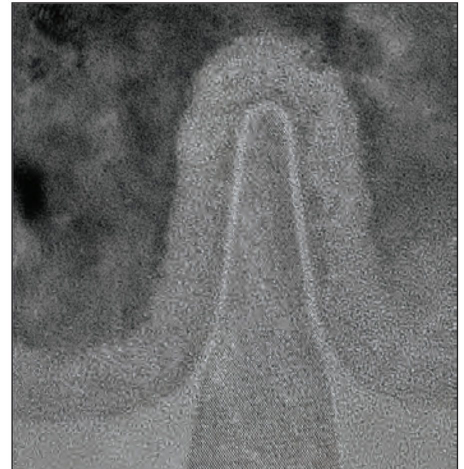


Figure 4. SEM cross-section image of a 22nm logic Fin-FET (top left), 30kV Bright Field STEM image (top right), and 200kV BF TEM image (bottom) using the in-situ liftout and transfer process.

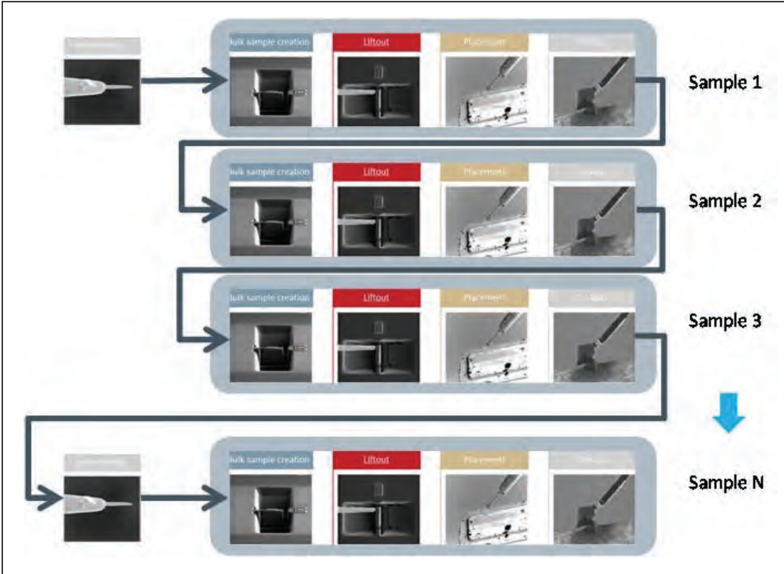


Figure 5. One possible sample process flow for lamella creation and ISLO using a fully automated recipe.

for transfer to TEM grids, the entire process can take up to 232 minutes (approximately 4 hours) assuming no breaks or interruptions. During this time, the technician is constantly interacting with the instrument. (Fig. 3)

In contrast, in high volume FA labs running fully automated recipes to create thick lamella for in-situ liftout, the time the operator is required to be in front of the instrument is greatly reduced. By using automated recipes to create the thick lamella, as previously shown in Fig. 1, the same dual beam system is able to run unattended for approximately 160 minutes.

During the nearly 3 hours that the DualBeam is running unattended, the technician can be working on an adjacent system to thin previously created lamella. In both cases, the end result of this process is a high quality, thinned lamella which will yield meaningful results in the TEM (Fig. 4)

With the addition of the capability to perform fully automated in situ lamella liftout and transfer, FA labs can gain further efficiencies by increasing the amount of time the DualBeam can run unattended. In this third scenario where even the liftout and transfer of the lamella is automated, after performing the initial setup to identify the region of interest and location on the TEM grid for the lamella, the DualBeam is able to run an entire 4 hours without operator intervention. In this case, a single technician would theoretically be able to operate two DualBeam systems, performing the final thinning on one instrument while another is automatically creating lamellae and transferring them to TEM grids.

Because these automated recipes can be configurable, one lab may choose to sequentially create all of the thick TEM lamellae and then perform the automated liftout afterwards, while another lab may choose to create and lift out each sample individually (Fig. 5). Similar to what happens with complex sample flows in the fab, labs are gaining the ability to configure and automate the process flow for each unique failure analysis sample, reducing the requirement for highly trained operators to be sitting at the tool. An additional benefit to increased automation is the ability to link data and process information at all stages of the FA process to each final image and report.

Conclusions

The development of automation software and integrated accessories for failure analysis equipment is now bringing more fab-like activities and processes into the FA lab. While highly trained technicians will always be an essential part of the FA lab, many of the tedious, repetitive tasks in the sample preparation process flow can now be handled automatically without the need for an operator at the tool. Standardizing and creating recipes for routine process steps which do not require the knowledge of trained technicians provides for a more efficient use of manpower. Labs moving to fully automated sample preparation recipes can significantly increase the number of high quality samples produced by each operator. Various automation components are now available to labs as they look to streamline the FA process to support the fab's ever increasing demand for more process data. As more and more automation moves into the FA lab one should not be surprised to see the proliferation of tools and blinking signal towers with only a few operators scattered throughout the lab.

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Acknowledgements

The authors would like to thank: Michael Schmidt, Rob Routh, JJ Blackwood, Ying Liu, Stacey Stone, Richard Young and Zdenek Kral for their suggestions and assistance in making the automated liftout process a reality.

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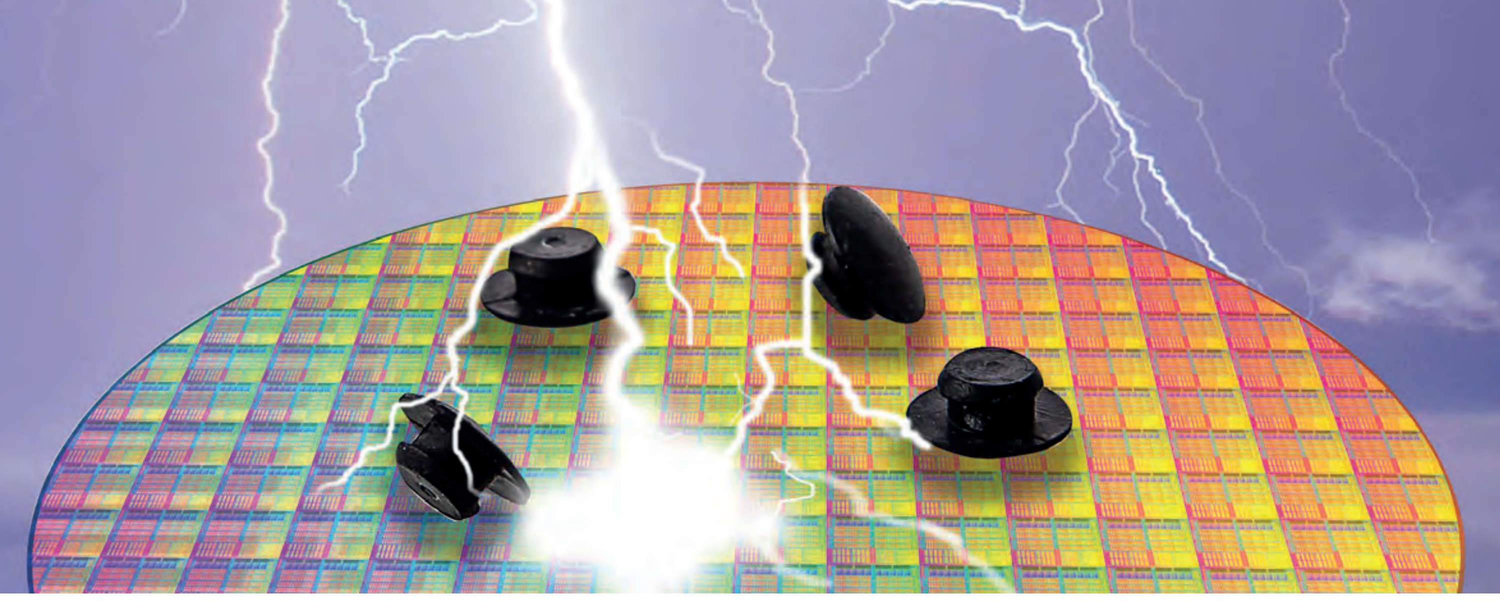

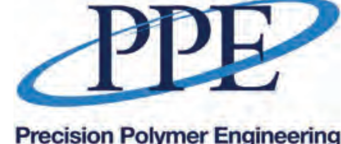

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How AMI tools image MEMS devices

The long-term functioning of a MEMS device depends on the integrity of the cavity; and the imaging and analysis of the seal protecting the cavity depends on acoustic micro imaging tools. Tom Adams, consultant, Sonoscan, Inc reports.

THE DEVICES known as MEMS (MicroElectroMechanical Systems) excel at collecting and reporting all sorts of data from all sorts of environments. MEMS devices collectively give us more data about the world we live in, and thus provide opportunities to live more advantageously in that world.

Blood pressure for example, was first measured a little over a hundred years ago, and since that time has been measured by fairly cumbersome mechanical equipment. Today a single MEMS device can be implanted that measures and reports blood pressure continuously. In a very different area, there's bad news for burglars: an extremely sensitive MEMS altitude/air pressure sensor can instantly report the slight but sudden change in air pressure caused by a window being opened three floors below.

Because they were made possible by the continued development of semiconductor manufacturing, MEMS devices share many features with semiconductor devices: they tend to be built in layers, they use many semiconductor materials, and they are inspected by some of the same tools, including Acoustic Micro Imaging (AMI) tools.

An AMI tool pulses ultrasound into a sample and receives the return echoes from material interfaces within the sample. A sample that consists of

a single material and that has no internal interfaces will therefore send back echoes from the top and bottom surfaces only - the top surface because it is the interface between the sample and the coupling fluid, and the bottom surface because it interfaces with what support the sample is resting on.

When a sample has (like a MEMS or semiconductor sample) multiple bonded layers, an echo will be returned from each interface between layers. If there is an anomaly in one of the layers, or between two layers, it is typically a gap-type defect such as a crack or delamination, void or non-bond.

Gaps typically return echoes of very high amplitude (more than 99.99% of the pulse), even if the gap is as thin as 100Å. In contrast, the interface between two well bonded materials will return only a fraction of the ultrasound, while the remainder proceeds deeper into the sample.

Gaps are thus easy to see when using an AMI tool, as are well-bonded interfaces. The echo also gives information about the depth of an interface, and about its polarity (whether in crossing an interface the pulse traveled from a material having higher acoustic impedance to material having lower acoustic impedance, or vice versa).

MEMS (Micro-ElectroMechanical Systems) devices are imaged by AMI tools at any of three stages: 1) while the devices are still in wafer form; 2) after dicing; 3) in their final packaged form. And some wafers, such as SOI, are imaged after bonding to eliminate poorly bonded pairs before etching. The frequencies of ultrasound used in of MEMS range from 50 MHz to 400 MHz.

Generally, lower frequencies penetrate better through materials, while higher frequencies give better spatial resolution in the acoustic image. Because they are thin and because the materials involved are highly transmissive of ultrasound, MEMS devices can be imaged at high frequencies for maximum image resolution.

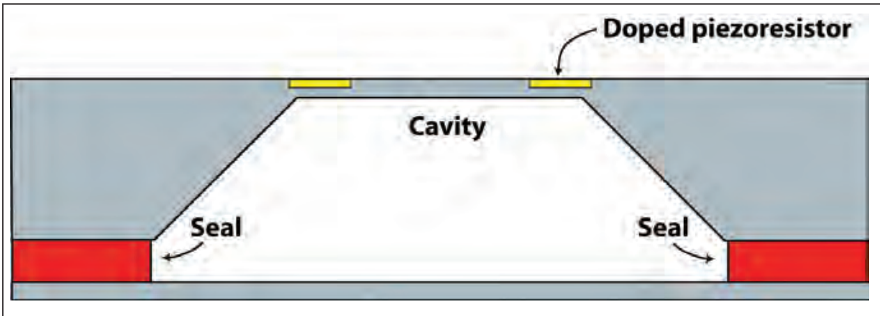

Figure 1. MEMS designs vary widely, but the seal protecting the cavity is the most frequent target of acoustic micro imaging tools.

But by far the most frequent purpose of acoustic imaging is to characterize the seal that surrounds the cavity and ensures the cavity's hermeticity. The cavity may contain a vacuum, air, or another gas. The seal may be made of glass, metal, epoxy or another material. The makers of the MEMS device want to ensure the successful functioning of the seal and of the device over the desired lifetime. Using SEMI standards, the permeability of the seal material to the external environment, and especially to humidity, can be quantified.

If the cavity contains a gas under pressure, the permeability of the seal material to the gas can also be quantified. In some MEMS pressure devices the cavity is divided into a sealed region and a region open to the outside environment. The Si membrane between the two regions deforms as the outside pressure changes, so the deformation rate, the seal quality and the permeability of the seal material all affect the functionality of the MEMS device.

What does a MEMS device look like to an acoustic micro imaging tool? Because the cavity contains gas or a vacuum, more than 99.99% of a pulse of ultrasound striking the silicon-to-cavity interface will be reflected and will create a bright white (highest amplitude) pixel in the acoustic image. All of the area of the cavity will thus be bright white, except where there may be solid features that extend from the ceiling to the floor of the cavity. These areas will be some shade of gray. Surrounding the cavity is the seal (Figure 1) that keeps the cavity intact. The seal has an interface to the silicon above and the silicon below. The cavity region will of course appear bright white, but what the operator of the acoustic micro imaging tool hopes to see around the cavity is a uniformly gray line meaning that the seal is without flaws. What he does not want to see are bright features within the seal; these would be delaminations, voids or non-bonds.

During the imaging process, the ultrasonic transducer scans the top surface of the MEMS wafer or individual device at a speed that can exceed 1 m/s. At this speed it sends several thousand pulses of ultrasound per second into the sample, and collects the return echoes from each one. Each echo becomes a pixel in the acoustic image.

Echoes from different depths within the wafer or device arrive at the transducer at different times. A time gate may be set to collect only echoes from the top to bottom of the seal.

An acoustic image of a pair of bonded wafers is shown in Figure 2. This is a fairly low resolution image of test wafers, where the purpose is to verify the reliability of the bonding process. In this case, when the two wafers were brought into contact to achieve fusion bonding, contact initiated at two locations rather than one. As the two wavefronts collided, they trapped air, resulting in the large and small bright white voids seen in the acoustic image. Regions where the two wafers are successfully bonded are black; there is no echo because there is no longer a material interface.

Figure 2. Acoustic image of two bonded MEMS wafers. White regions are voids between the wafers.

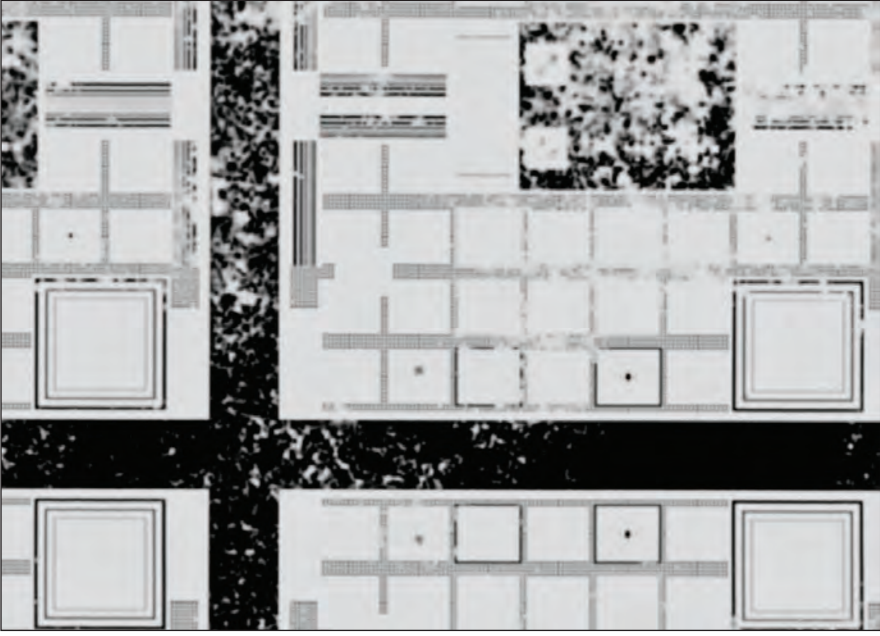

Figure 4. Large numbers of small defects (white) are present in the seal and other bonded regions of this MEMS wafer.

In development or production, higher ultrasonic resolution is used to inspect for individual voids such as those shown in the following images. Defects may be viewed by a technician who examines the acoustic image of the whole area of the wafer, or they may be found and reported by Digital Image Analysis (DIA) software.

Figure 3 is a small section of a high-resolution acoustic image showing rectangular cavities (bright areas) and the rectangular seals surrounding the cavities. Some of the seals are intact, but the circles identify locations where part of the seal is not attached to a wafer or is altogether missing. These circled defects will of course cause immediate failure of the MEMS device, but there are other, smaller anomalies that appear capable of causing eventual failure.

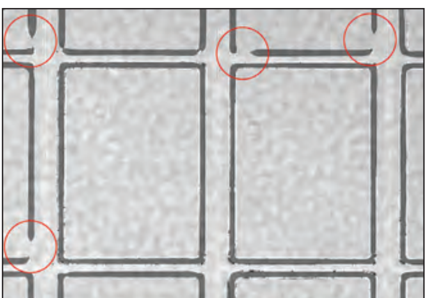

Figure 3. The cavities in this acoustic image of a MEMS wafer are bright rectangles; some of the seals are incomplete (red circles).

Figure 4 is the acoustic image of a small area of a MEMS wafer. The dark black lines are fairly wide seals along which the wafer will be cut for singulation. There are dark structures within the cavities that are bonded to one or both wafers.

But within the seal, as well as within the structures inside the cavity, are numerous small white areas which are defects. They may be areas of non-bonding on the top of the seal and other structures. Whatever their depth, some of defects on or in the seal are already large enough to compromise the hermeticity of the cavity.

The design and structure of MEMS devices vary greatly from one application to another, but the integrity of the seal around the cavity is always of critical importance. In some very recent MEMS designs, the seal may be as little as 6 microns wide, but the very high ultrasonic frequencies used to image MEMS devices, along with the high ultrasonic reflectivity of solid-to-gas anomalies, means that defects in the seal can still be imaged.

In some cases, the target of acoustic imaging may be something other than (or in addition to) the cavity seal. For example, it is important to know that the substrate wafer is free from tiny cracks that can occur during processing. The cracks are typically more or less vertical. The problem is that a nearly vertical, extremely thin crack does not reflect much ultrasound pulsed from above.

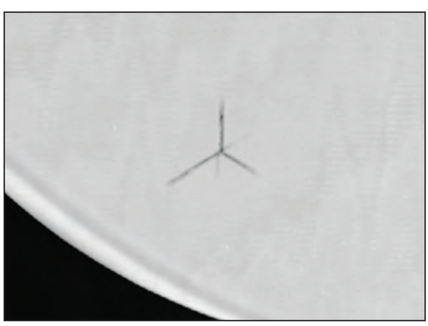

Figure 5. A crack such as this one in a single wafer may cause failure during later processes.

Figure 5 is the acoustic image of a single wafer in which a complex crack has formed. The risk is that such a crack will not survive subsequent processing, but will fail and likely destroy the wafer or wafer pair at a later stage.

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With the 7nm FinFET, parasitics come into play

With every new technology generation, an understanding of the interdependencies between design and technology becomes increasingly important. A shining example is the scaling of FinFET technology beyond 10nm. Marie Garcia Bardon, Researcher at imec, talks about the options and limitations of advanced FinFET scaling.

THE CONTINUOUS EVOLUTION of systems-on-chips for smart mobile applications and their accelerated time-to-market, put severe requirements on the logic roadmap. Marie Garcia Bardon: "With each new technology generation, we try to achieve area reduction, speed improvement, power reduction and cost reduction, all at the same time.

This has so far driven the technology scaling, at device level, from 28nm planar Si devices, towards 20nm planar and finally Si-based FinFETs at the 14/16nm and 10nm technology nodes. FinFETs have been introduced because they provide a better electrostatic control over the channel and maintain the sub-threshold swing closer to ideal.

For the 7nm technology node, new disruptive solutions are possible at device level to continue performance improvement: we might replace the Si channel material with non-Si high-mobility materials. Or we might move to gate-all-around structures, either in the form of horizontal or vertical nanowires, since they offer the ultimate electrostatic channel control. However, another component became increasingly important: parasitics capacitances and resistances."

Scaling the FinFET beyond 10nm: a parasitics-dominated era

From the 7nm node onwards, the impact of parasitics is becoming increasingly important. This means that unwanted capacitances and resistances increased due to tight dimensions and became non negligible at system level. And this substantially lowers the performance of the system in terms of speed and power. Marie Garcia Bardon: "We have to start considering parasitics that did not impact the systems performance before. At these small dimensions, we can no longer neglect the series resistances and parasitic capacitances in the back-end-of-line (e.g. parasitic capacitance between the interconnect layers) and in the front-end of line (e.g. fringe capacitances between gate and source/drain). The series resistance lowers the effective voltage on the transistor, while the parasitic capacitances eat part of the systems power and slow down its operation. If we want to meet the performance targets at the 7nm node, it will no longer be sufficient to optimize the transistor itself (channel material, gate all around etc). We have to introduce innovations that reduce these parasitic elements and their impact."

Evaluating various technology/design options

Marie Garcia Bardon has explored the design space that allows to meet the performance target. She and her team have discussed possible solutions and have identified the main performance limiters. Marie Garcia Bardon: "We can think of several innovations which allow a reduction of the device parasitics. For example, we can improve the spacer width and the dielectric constant, e.g. by using air gap spacers. Or we can lower the contact resistivity by using wrapped around contacts. We can also optimize the back-end-of-line width and pitch, and the fin height.

At design level, we can explore solutions such as fin depopulation, i.e., reducing the number of fins per device. And we will have to evaluate, through simulations and calculations, all these new

> "One of the main objectives of technology scaling has always been an improvement of the systems speed. But for future technologies, speed might not be the main driver anymore"

parameters at the same time, and see which options are the best to meet our targets. The results of these evaluations are benchmarks of the different options in terms of power and frequency, as well as target values for the different elements. For example, what would be the optimal series resistance for a FinFET with Si channel to still meet the targets? And what speed benefit do we expect from a wrapped around contact? For each option, we can evaluate how good the performance compares to the target speed. With these results, we help the technology researchers at imec and our partners to choose between the many options and give direction to the technology roadmap."

Dark silicon

One of the main objectives of technology scaling has always been an improvement of the systems speed. But for future technologies, speed might not be the main driver anymore. Marie Garcia Bardon: "With each new technology generation, we have been able to put more and more transistors on a chip. But the power reduction per transistor has not kept pace with this area scaling, due to the transistor leakage. This means that, with each new generation, there is a growing gap between how many transistors you can put on a chip vs. the percentage of transistors that can be powered with the same power budget.

This gap between area gains and power gains is referred to as 'dark silicon'. So, although we are still pushing area scaling, we might not be able to use the extra transistors on the chip for a certain power budget. And that's why we will also need solutions, at device level, to decrease the leakage."

A collaborative effort

Six years ago, Marie Garcia Bardon joined the imec INSITE team, where she started modeling and evaluating the different transistor generations. Imec's INSITE program allows both product designers and technology developers to make informed decisions, based on a wide range of scenarios concerning future technology developments. Marie Garcia Bardon: "Working in the imec INSITE team is like solving a puzzle: we have to put all the pieces together and evaluate how they perform together, starting from the technology aspects all the way towards system level. This means that we have to interact with various people at imec: experts in front-end-of-line, in litho, in back-end-of-line, etc. Even within our INSITE team, we work together with modeling specialists in diverse domains. And this is one of the things I really like about my job. Our research is actually a convergence of everything we do at imec within core CMOS. We explore and optimize many parameters at the same time, and cross the traditional design-technology boundary. We take into account system requirements, and evaluate how they impact technology. And vice versa, how technology solutions impact decisions at the design level. Therefore, all these insights are the results of a collaborative effort of many people involved."

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Marie Garcia Bardon, Researcher at imec, will give an invited talk at the 2015 International Conference on IC Design and Technology (ICICDT, http://www.icicdt.org/index.php) which will take place at imec, Leuven, Belgium, from June 1-3, 2015. A global forum for interaction and collaboration of IC design and technology for 'accelerating product time-to-market'.

More than Precision

Meeting the challenge of accurately assembling active optical cables

No one would dispute the fact that active optical cable (AOC) and Silicon Photonics technologies are getting tremendous attention due to the need of transferring more and more data at ever faster data rates. This is putting immense pressure on the assembly equipment suppliers to offer advanced tools and processes that push the envelope of ultra-precise die placement. For Dr. Johann Weinhändler of Amicra there is no end in sight.

AOC is one of the most efficient solutions currently available to meet the rapidly rising demand for bandwidth, performance, capacity and availability in large data centers, which need a flexible configuration of their server racks to keep pace with technology and data traffic conditions in the face of growing volumes of mobile and video content.

The development of active optical modules is attracting an immense development activity – regardless of their transmission capacities, which are on the verge of breaking the 400 Gbps barrier. By 2019, a mere four years from now, worldwide sales of $1.5 bn in AOC modules is predicted by a new market report issued by Communications Industry Researchers (CIR) based in Charlottesville, VA, USA. This exciting, and challenging, prospect mirrors the ongoing adoption of fiberoptic communication gear, replacing the heavy, slow and cumbersome copper assembly plants of old.

Progress in AOC has been fast and furious, challenging the vendors of manufacturing equipment for interconnect components as well. AOC modules operating at 40 Gbps are considered mainstream today. So, more and more vendors are looking to enter the high-performance segments providing up to 100 Gbps, if not aspiring right away up to 400 Gbps.

Main revenue generators, however, still are the 'workhorse' modules of the QSFP (Quad Small Form Factor Pluggable) and the copper-based CXP (InfiniBand) categories. By 2019, however, according to CIR these two will get the lion's share of annual sales generating $1.3 bn in revenue. They will carry the bulk of services in the Ethernet and IB protocol domains as required by most large data centers. The newer CFP (100 Form Factor Pluggable) and CDFP (400 Form Factor Pluggable) devices will reach just a fraction of that, amounting to less than $200m in sales.

A related market segment that is developing alongside the AOC modules is Silicon Photonics, which is promised a very bright future by French market researcher Yole Développement in their 'Silicon Photonics 2014' report. Although revenues are still slight ($25 m in 2013), its growth prospects reveal a CAGR of 38 percent to achieve a market volume of $700m by 2014.

Silicon Photonics, Yole states, will realize the advantages of low cost and high

systems integration that come with Si processing, with the added benefit of low power and low weight, plus higher functionality. Another benefit is increased reliability and availability in the face of the relatively short life span of typical rack servers.

Already on the market today are active optical cables from a number of mid-size vendors such as Luxtera, Mellanox and Avago, whereas the heavyweights like Intel, Cisco and IBM are just gearing up to enter the race on their terms. All this has instigated considerable action and investment on the side of equipment vendors to be able to provide adequate assembly and manufacturing tools for chip-to-chip and chip-to-wafer interconnect devices and processes.

Amicra is up to the challenge

Amicra Technologies, founded in 2001 and headquartered in Regensburg, Germany, is one of the worldwide leading providers of assembly tools for the manufacturing of AOC modules. The company is focusing its efforts and resources on extreme accurate placement and bonding techniques for VCSEL (vertical cavity surface emitter) chips and PIN (positive intrinsic negative) diodes. In its chosen field of precision placement processing Amicra offers high-accuracy (down to 0.5µm) micro-assembly cells, high-speed inking systems as well as laser and LED testing systems.

The company's key expertise is in the most exacting placement of VCSELs, pin and laser diodes as well as lenses inside AOC modules to ensure high data throughput rates (Figure 1). Amicra derives its expertise from its original founding mission: to provide first-rate equipment and processing specifically for fiberoptics applications. Targeted markets are the fiberoptic and MEMS manufacturing industries, as well as those making LEDs, optoelectronic and semiconductor devices, and propagating advanced concepts such as TSV, 3-D ICs, and high-fan-out board configurations.

Accordingly, Amicra's state-of-the-art AFCPlus and NovaPlus die and flip-chip bonding platforms are focused on VCSEL, PIN and lens attachment procedures, as well as laser diode attach on Si submounts via non-contact substrate heating. AFCPlus realizes a placement accuracy of up to +0.5µm at 3 Sigma – which is best in class - and a competitive total cycle time of less than 15 seconds.

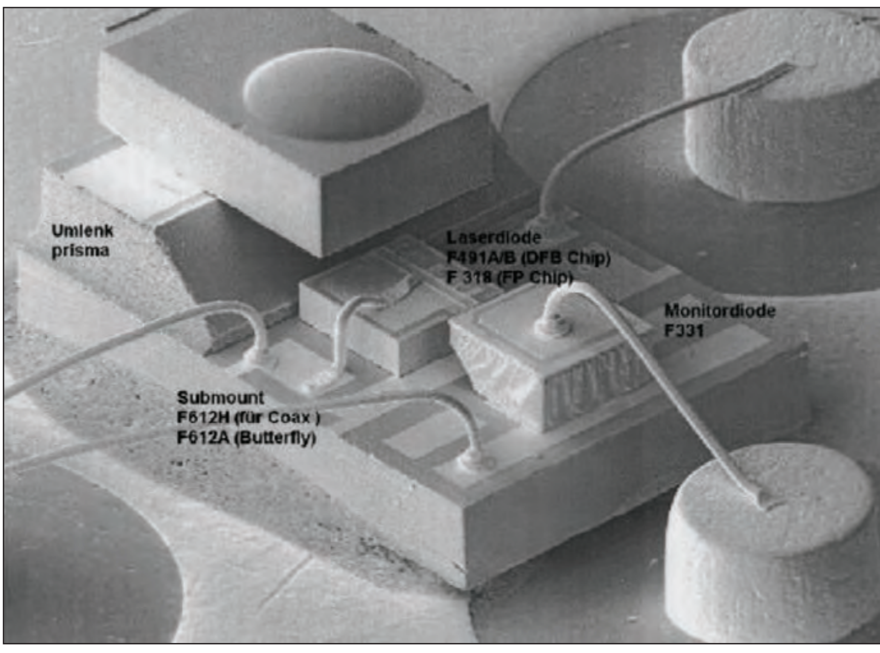


Figure 1: REM-image of a AOC module

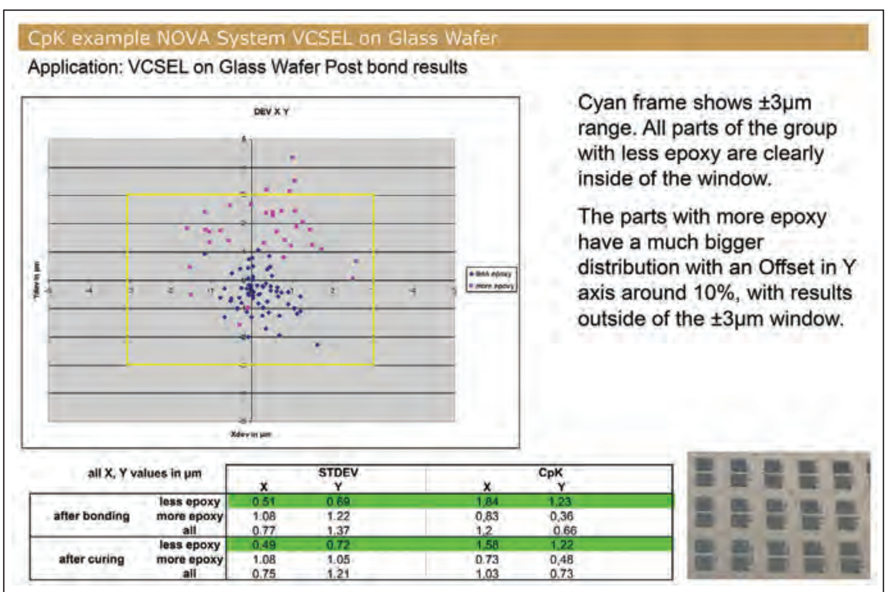
AFCPlus features a bond tool holder for eutectic bonding at temperatures up to 300 °C. Non-contact substrate heating with localized laser impact goes up to 450 °C. Another outstanding feature is active bond force control, which is adjustable between 10 grams and 2 kilograms. Epoxy stamping and volumetric dispensing are standard ingredients of the AFCPlus, as well as UV dispensing and UV curing at the bond location.

A different tack is pursued by Amicra's NovaPlus, a dual-bondhead die- and FC-attach machine. It was conceived for high-volume applications in the realm of opto, WLP, TSV and embedded chip (fan-out) placement tasks. Placement accuracy reaches up to +2.5µm at 3 Sigma. Another of the NovaPlus's advantages is its short cycle time of less than 3 seconds per bond. Accordingly, UPH values of up to 2500 (at +5µm) or up to 1200 (at +2.5µm) are achieved.

NovaPlus is based on a modular concept, including a fully integrated dispensing system that supports multiple dispenser types. A flip-chip option is also available. The machine supports 300mm wafers and rectangular substrates up to 600mm x 600mm in size.

The dynamic alignment capability offered on both machines is achieved by the concept of the camera measuring through the bond head and accurately detecting the positions of die and substrate in relation to each other. Feedback from the vision system during the measurement enables the calculation of the pertaining x-, y- and Θ vectors and die alignment by the appropriate shifts and turns until the final position and preset accuracy are reached. This corrective action is taking place during the entire bonding process. In the end, this method is faster and yields by a factor of 2x higher UPH values than the beam splitter alignment process.

Another concern with AOC is an acceptable Cpk value. Looking at die placement with a given Cpk value is an effective way to analyze the die



all X, Y values in µm		STDEV X	STDEV Y	CpK X	CpK Y
after bonding	less epoxy	0.51	0.69	1,84	1,23
	more epoxy	1.08	1.22	0,83	0,36
	all	0.77	1.37	1,2	0.66
after curing	less epoxy	0.49	0.72	1,58	1,22
	more epoxy	1.08	1.05	0.73	0,48
	all	0.75	1.21	1.03	0.73

Figure 2: Bonding of VCSEL on glass wafer with NovaPlus. Post-bonding CpK results. Cyan colored frame shows the +3μm range. All parts with less epoxy are inside the window.

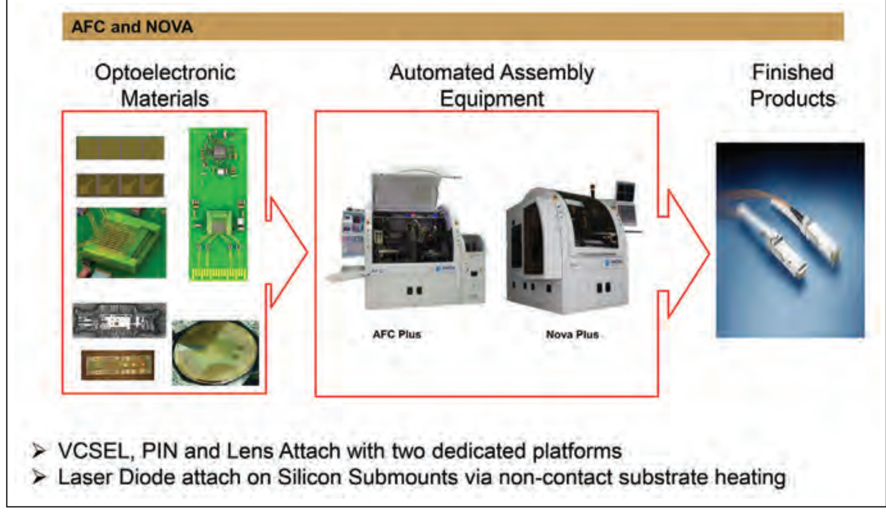


Figure 3: VCSEL placement of QSFP engine on PCB with AFCPlus or NovaPlus.

placement results. Cpk helps to predict with confidence the first-pass yield of the assembly process. Sufficient Cpk values are met by the AFCPlus and NovaPlus machines. An example is the precise placement of VCSELs on glass wafers shown in Figure 2.

Amicra's proprietary concept of dynamic component alignment ensures the most accurate placement at an efficient cycle time, and offers a resolution in the adjustment of components to be placed within <0.1μm. Amicra is leading the pack by being the sole vendor offering this type of dynamic alignment. It is achieved by keeping chips and substrates within the field of view of the camera during the entire placement process for corrective action. The principle pertains to die attach, flip-chip and lens attach.

QSFP assembly is a major application that is rapidly gaining in importance. Those modules require the exact positioning of the transceiver in relation to the optic cable to realize their superior port density as compared to SFP modules. An overview of AOC placement applications for the QSFP optical engine using either the AFCPlus or the NovaPlus is given in Figures 3 and 4, detailing the placement of one to twelve units per array. The principle here is to have the rotation of the Photodiode aligned relative to the rotation of the VCSEL. This yields full control of alignment and placement (all within the FOV of the camera). Typical post-bond measurements results are <120 CPH (+2μm @ 3 Sigma) on the AFCPlus, and 700 CPH (+3μm @ 3 Sigma) on the NovaPlus, using an epoxy process. Now to lens placement, using an UV epoxy. The major process steps as shown in Figure 5 are:

- Correlation of the lower side of the lens to its top side by means of the Amicra's Correlation Stage, and bonding relative to the VCSEL.
- Dispensing of UV epoxy,
- Placement and bonding of the lens via Amicra's dynamic alignment system,
- Post-bond measurement, done within the machine.

AFCPlus achieves a placement throughput of up to 189 lenses per hour at an accuracy of +1 - 2μm at 3 Sigma. NovaPlus moves this number up to 700 to 1200 lenses per hour at an accuracy of +2.5 - 5 μm at 3 Sigma. Slight variations can occur due to different material and process qualities.

Finally a brief look at the eutectic bonding process of laser diodes to wafers. A typical requirement in this regard, which is solved with the AFCPlus is the attachment of flipped, and non-flipped, laser diodes. AFCPlus performs this using an 80/20 AuSn soldering process with +3μm accuracy and contact-less heating from the bottom side and an optional heater from the top. Here, of course, the bonding is not carried out using an adhesive but deploying a contactless local laser heating procedure. Figure 6 shows some actual results of this process.

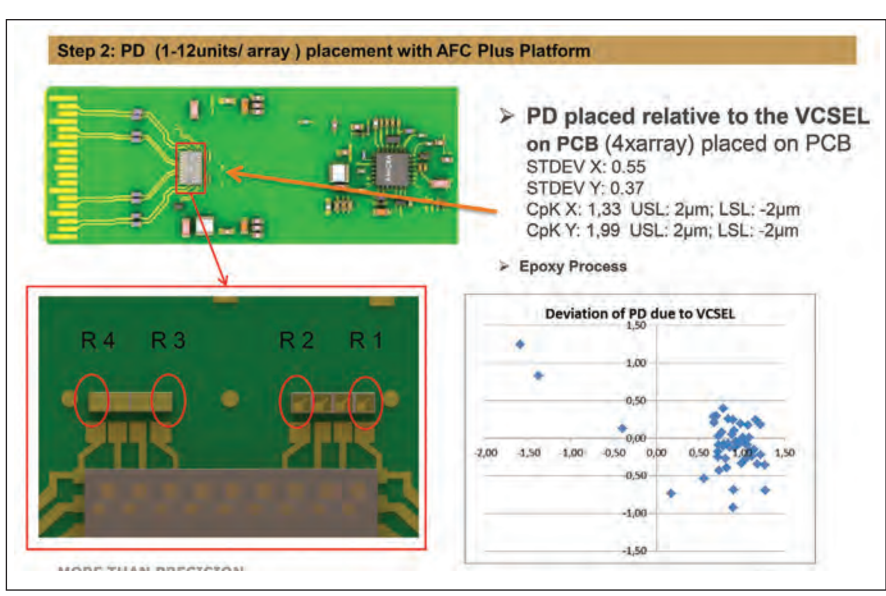


Figure 4: Photodiode placement with QSFP on AFCPlus.

Gearing up for silicon photonics

A very promising current Silicon Photonics application that is met by the capabilities of both the AFCPlus and the NovaPlus platforms is chip-to-wafer bonding of TOSAs (transmitter optical sub-assemblies), and ROSAs (receiver optical sub-assemblies). The use of these advanced assemblies will lower cost and boost performance, besides improving reliability in high-speed interconnect situations.

Silicon Photonics, discussed and hyped for a long time is slowly gaining traction – now that a major semiconductor manufacturer headquartered in California has committed to start producing Indium-Phosphide chips on Si, using Amicra's equipment. Other major IT gear vendors based in China, such as Huawei, are now hopping on the Si Photonics train as well.

By 2020, as market researcher CIR states in a newly released report, the market for chip-to-chip optical interconnect engines will reach $775m. On-chip optical interconnect, the next evolutionary step of future system configurations, will exceed $210m around 2025. It is envisioned that by then VCSELs will be replaced by silicon-based lasers or even quantum dot lasers integrated on-chip.

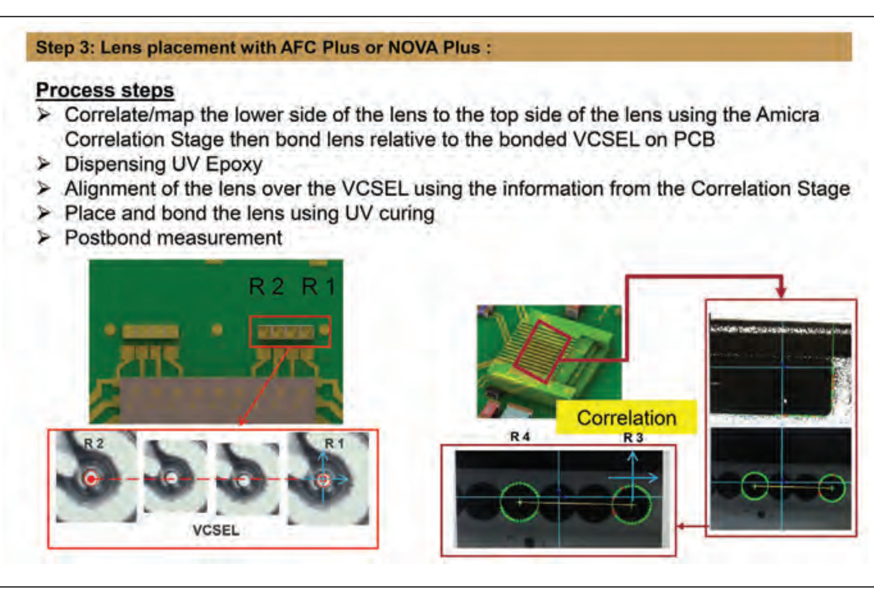


Figure 5: Lens placement process with QSFP on NovaPlus.

Conclusion

The exact rate at which the market is predicted to grow will always be argued and debated by marketing experts. But no one would question that AOC/silicon photonics production will continue to grow in the foreseeable future and that ultra-precise die placement is the key to success in this market.

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Creating and strengthening links between chipmakers and network builders

Killer consumables:

How clean are your seals?

In semiconductor manufacturing the threat of particle and especially metallic contamination to transistor integrity is a significant and potentially costly threat. This is mainly true for front end processing but, due to the high mobility of many of these contaminants, it remains a threat at all stages of the manufacturing process flow.

KNUT BEEKMANN, MARKET MANAGER FOR SEMICON, PRECISION POLYMER ENGINEERING (PPE)

WHEN WORKING at the nano-scale of chip production, even the lowest trace metal levels have the capacity to alter the electrical characteristics of the device and/or affect the reliability of the end product.

Background

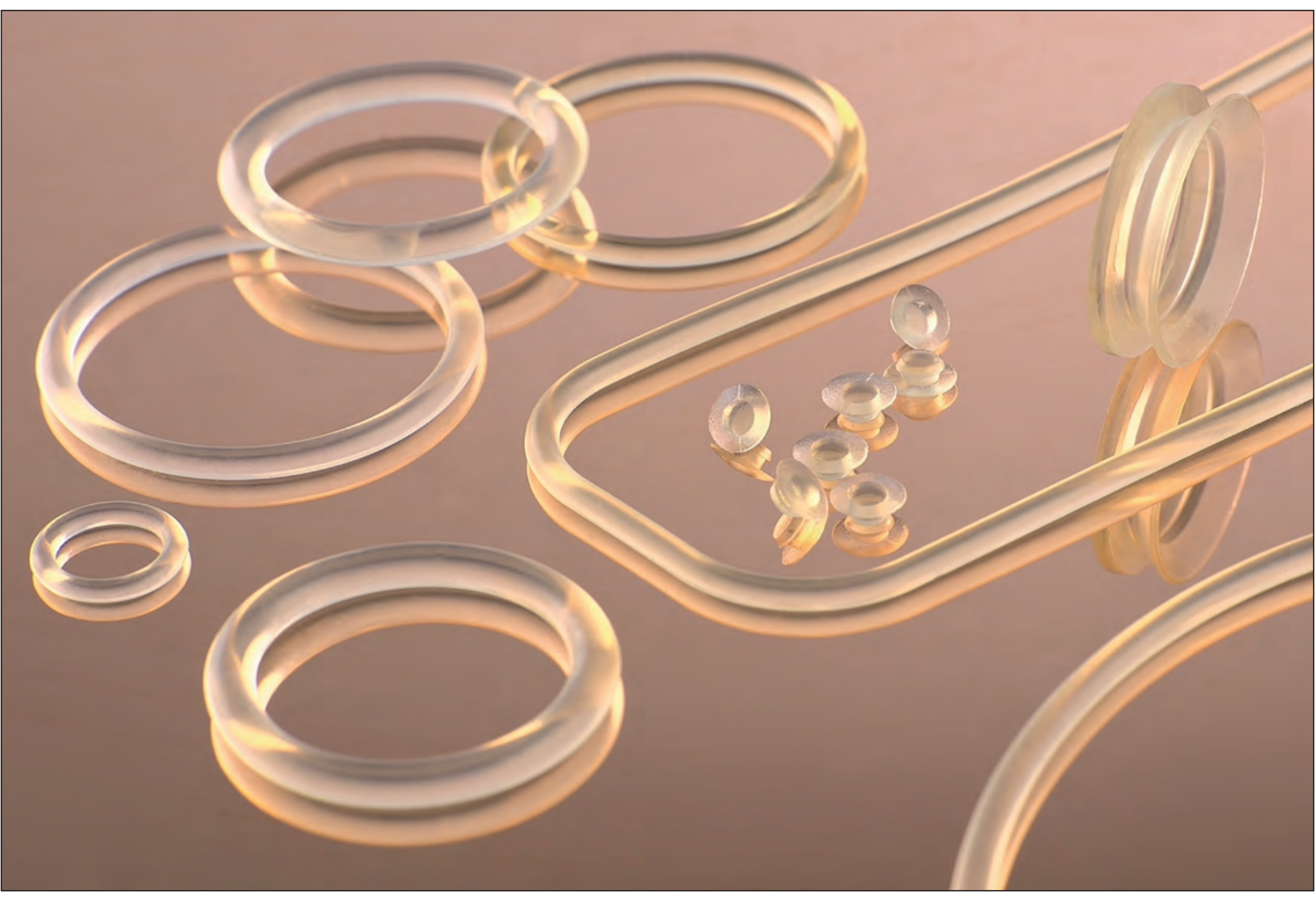
During routine operation, many components within the process tools and ancillary equipment will be subject to wear and abrasion, particularly those components within the process module that are directly exposed to harsh physical and chemical environments. The most critical locations are those where components are exposed to such environments and in proximity to the substrate being processed.

An equipment consumable item that can sometimes be overlooked is the elastomer seal or O-ring material. These seals have a certain lifetime proportional to the mechanical and chemical properties of the material and the physical constraints of the groove and location. Whilst an elastomer in a critical location may not actually determine the maintenance cycle of the process tool, byproducts and elastomer constituents will be released into the process environment during active operation. It's therefore clear that whatever is in the elastomer can contaminate the wafer and this applies equally to the trace metal content of the elastomer.

Trace metal contaminants fall broadly into two categories. Alkali metals which include elements such as sodium (Na), potassium (K) and lithium (Li) and heavy metals which include elements such as copper (Cu), iron (Fe), zinc (Zn), titanium (Ti) and chromium (Cr). The effects on the device of such contaminants vary depending on the type of the element. Sodium for example, can readily lose its outer electron to form an ion with charge +1. It can then readily diffuse through the oxide under the influence of an electric field even at room temperature, however; it cannot penetrate the silicon lattice which means that a charge can accumulate at the silicon/silicon dioxide interface. This in turn leads to unpredictable voltage threshold shifts and correspondingly random digital outputs from logic circuits.

Additional failure mechanisms include current leakage through the dielectric and reduced dielectric breakdown voltage, degradation of time dependent dielectric breakdown (TDDB), or complete breakdown of the gate[1].

Gettering layers are also no guarantee of eliminating the issue. PSG and BPSG layers are often used to getter sodium ions however; the presence of moisture either through integral process steps or atmospheric absorption can facilitate the release of trapped mobile ions in the getter[2]. Rather than accumulate at the semiconductor interface, heavy metals tend to diffuse through the semiconductor, where they effectively create energy states in the bandgap of the semiconductor causing changes in carrier lifetime or the diffusion length[3].



Consumer demands for faster, more powerful and portable technology with greater functionality is a key factor in driving the semiconductor manufacturing industry. Although the part of Moore's law that refers to shrinking technology remains largely intact, the pressure on cost reduction is rising throughout the whole value chain[4]. Reduced device dimensions and gate thickness leads to devices that become more sensitive to a number of factors including trace metal contamination.

It's clear that such contamination leads to unstable device performance, yield loss, device degradation with increased risk of reliability failures, potentially costing the fab in lost time, loss of revenue and wafer production capacity.

Purity in elastomers

When choosing elastomer materials for seals in process tools, manufacturers must decide on the appropriate material in accordance with the location in the tool and the chemistry involved. Critical locations where the elastomer is in contact with the chemistry or process media, where degradation takes place, and where the byproducts of this degradation can be transported to the wafer, require the highest quality seal material in order to avoid contaminating the device. The sealing product must precisely fit the characteristics of the operating equipment. Specialist sealing companies have significant experience and expertise in developing and customising elastomer seals and O-rings for use in semiconductor applications. There is often a large choice of products for any one particular application and "semiconductor compatibility" is often taken for granted especially in critical applications however; not all elastomer

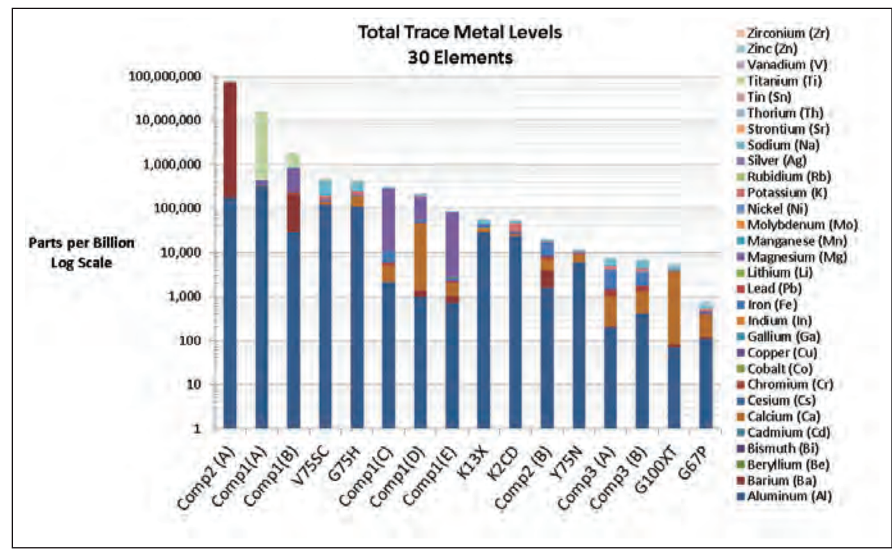


Figure 1. Comparative VPD ICPMS testing of elastomer materials

Figure 2. G67P trace metal content

Figure 3. G100XT trace metal content

materials are equal when it comes to the level of undesirable contaminants.

For many device applications, it is no longer adequate to measure contamination at the parts per million level. When analysing trace metal levels in elastomer materials, vapor phase decomposition (VPD) combined with inductively coupled plasma mass spectrometry (ICPMS) yields data down to parts per billion[5]. A number of different elastomer materials have been analysed by an independent test laboratory in order to quantitatively determine the amount of trace metal within each sample.

The materials analysed include the leading elastomer brands and the results are graphically represented in Figure 1. It should be particularly noted that In order to accommodate all the samples tested, a log scale was used. The results show that the elastomers that achieved the lowest trace metal content of all materials tested were entirely organic perfluoroelastomers or FFKMs with two Perlast® grades having the lowest levels and G67P in particular showing a factor 7 improvement over the next best grade. The cleanest fluoroelastomer or FKM material was found to be Nanofluor Y75N, again a fully organic highly fluorinated elastomer. Figures 2. and 3. above Illustrate the individual levels for several of the key contaminants that should be avoided for two of the cleanest materials tested.

Conclusion

During wafer processing, the inevitability of elastomer or seal wear in key tool locations during normal operation will expose the wafer to the degradation byproducts of the elastomer material, and therefore also the impurities contained within the elastomer. It becomes clear therefore, that the lifetime is not the only factor that should be considered when making elastomer choices for specific applications. FFKM elastomers are particularly suited to the most critical applications, and the harsh environments presented by higher temperatures, aggressive wet chemical and plasma processes. The more aggressive the environment and the more sensitive the device, the greater is the need to consider the degradation byproducts of the system components.

Use of high purity components becomes a preventative measure, guarding against costly transistor damage or increased risk of poor reliability. Contamination ultimately results in loss of yield, increased cost, or loss of reputation. Elastomer materials that contain only ultra-low levels of metallic contaminants are ideal for manufacturers of devices at advanced technology nodes and include all fabs wishing to minimise the risk of random changes to electrical characteristics and reliability failures.

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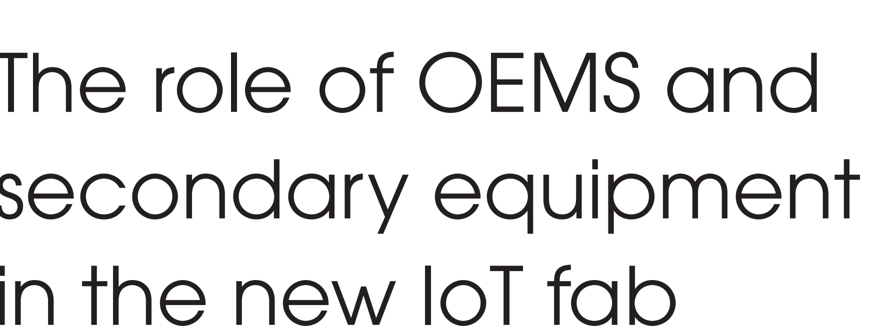


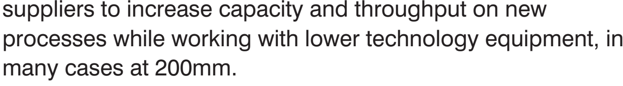
The role of OEMS and secondary equipment in the new IoT fab

To be competitive in the IoT market, cost is key and making the successful adaptation of secondary equipment is paramount. Tony McKie, CEO, memsstar tells Silicon Semiconductor why.

EVERYWHERE WE TURN, we see reference to the Internet of Things – or IoT – as the driver of future innovation, with the promise of making the world a better place. Perhaps more importantly, the IoT represents a significant market opportunity for a large portion of the electronics supply chain.

Gartner has defined the IoT as the network of physical objects that contain embedded technology to communicate and sense or interact with their internal states or the external environment. [1] Exploding at an exponential rate, the IoT is expected to grow at a CAGR of 31.72 percent by 2019 due to the vast number of integrated electronic devices that will be required in a huge range of products designed to inform, measure, control, record, and report.

This has resulted in a massive outflow of new systems and applications to be delivered faster, smaller and at very low cost. To meet these demands, there is pressure on industry

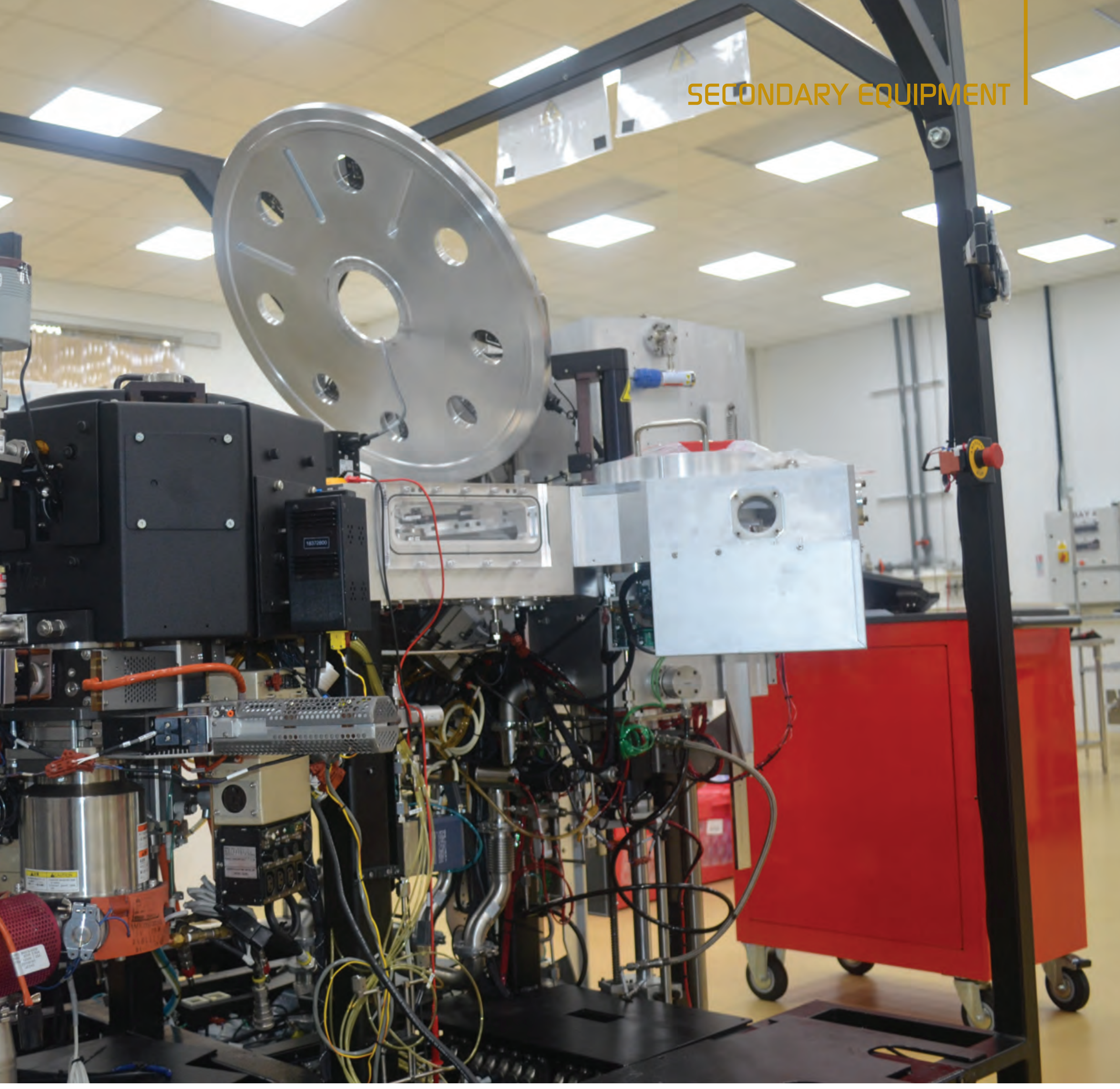


suppliers to increase capacity and throughput on new processes while working with lower technology equipment, in many cases at 200mm.

IoT driving growth

There is no market segment left untouched by the IoT; industrial, healthcare, automotive and consumer products are all embracing the opportunities it will afford. According to Yole Développement, the timeline for IoT applications is underway, with consumer and home automation applications already being implemented. By 2016, we can expect to see the IoT affecting retail and logistics. By 2018, it will be enabling health, life science, and industrial applications. By 2020, we can expect to see it implemented in transportation, security and public safety, and environmental applications. [2]

The semiconductor and related industries (e.g. MEMS, sensors, and compound semiconductors) provide the underpinnings



that enable the IoT. Predictions on the numbers of connected devices required for the IoT range from 25 to 35 billion. As such, the weight of its successful implementation falls squarely on the shoulders of industry suppliers to increase capacity and throughput on new processes.

Furthermore, the low cost and low-power requirements of these devices calls for legacy node silicon, rather than leading edge CMOS. Gartner research predicts we will need 100K wafers/month to meet these requirements, with supply coming from both 200mm and 300mm wafer fabs to reach this target.[3]

Impact on 200mm fabs

According to the SEMI 2015 Secondary Fab Equipment Report, 150mm and 200mm fab capacity represents approximately 40 percent of the total installed fab capacity. Additionally, 200mm fab capacity is on the rise, led by foundries that are increasing 200mm capacity by about 7 percent through to 2016, driven by new applications related to mobility, sensing and IoT. In 2014, 200mm fab investments by leading foundries and IDMs resulted in a 45 percent increase in spending for secondary 200mm equipment. [4]

In particular, the IoT provides a significant opportunity for second-tier manufacturers that have fully capitalized wafer fabs and are looking to add diversity to their product lines without investing in leading-edge silicon. Not all products will be manufactured in silicon, but increasingly also in alternative materials such as gallium arsenide that aren't suited to 300mm wafer sizes. Additionally, there is an increase in "More than Moore" class devices, as many of the IoT devices involve heterogeneously integrating analog chips, power management devices, image sensors, biomedical, MEMS and other technologies. Most of these are manufactured at 200mm, leaving 300mm wafer starts for leading edge CMOS and memory.

As such, 200mm fabs are experiencing a renaissance, particularly in Europe, where the offshore migration of leading-edge silicon manufacturing left behind legacy fabs searching for purpose. Many of these smaller companies have invested in technologies that aren't mainstream, but rather classified as more niche market. Although Europe has been doing this for a long time, these niche markets, such as MEMS, automotive, and medical devices, are now being captured under IoT.

SEMI market research shows that investment in "legacy" fabs is important in manufacturing semiconductor products, including the emerging Internet of Things (IoT) class of devices and sensors, and remains a sizeable portion of the industries manufacturing base:

- 150mm and 200mm fab capacity represent approximately 40 percent of the total installed fab capacity
- 200mm fab capacity is on the rise, led by foundries that are increasing 200mm capacity by about 7 percent through to 2016 compared to 2012 levels
- New applications related to mobility, sensing, and IoT are expected to provide opportunities for manufacturers with 200mm fabs [5]

Used, refurbished, remanufactured, certified and other classes of secondary equipment remain essential to the production strategies for these 200mm fabs. A recent survey by SEMI of top 200mm fab managers indicated that secondary equipment was the number one source for productivity improvements in the future. While the total secondary market is growing, the most popular tool sets are still in short supply. [6]

OEMs vs. Secondary equipment suppliers

One challenge of the anticipated IoT explosion and the impact it's having on 200mm fabs is how to cost effectively add capacity with tools that have 10-15 year old processing capabilities. Most OEMs have focused new process development on 300mm toolsets, looking to capture high-volume manufacturing at 300mm. While they still provide parts and service for 200mm tools in the field, very few are actually developing new processes on 200mm tools. This means that many fabs are turning to secondary equipment suppliers for the solution. For European-based companies in particular, establishing a partnership with a European-based secondary equipment supplier is particularly appealing.

Why is that? 10 years ago, as 300mm wafer shipments began to outpace 200mm platforms, the major OEMs enabled the transition with the availability of the comprehensive 300mm toolset and began a new 300mm technology race, meaning these tool suppliers limited their activities to service and spares for the now legacy 200mm toolsets.[7] Additionally, many of these OEMs shifted R&D efforts into developing 450mm toolsets, LED and solar panel manufacturing, rather than developing new 200mm processes for innovative legacy nodes. For IoT fabs, the question is not only can the industry withstand 200mm equipment at new prices, but also would the new tools provide new capabilities to accommodate the diversity of More-than-Moore class devices?

Customer requirements for secondary equipment are changing dramatically. It's no longer sufficient to simply deliver a used tool, or refurbish or make small modifications to older equipment for IoT device fabrication. Now, these tools have to be adapted to provide customized solutions for a wide variety of applications, as well as extending the life span and evolving the functionality of older equipment. This isn't without its challenges such as the availability of donor tools, where to source legacy components, the provision and knowledge transfer of

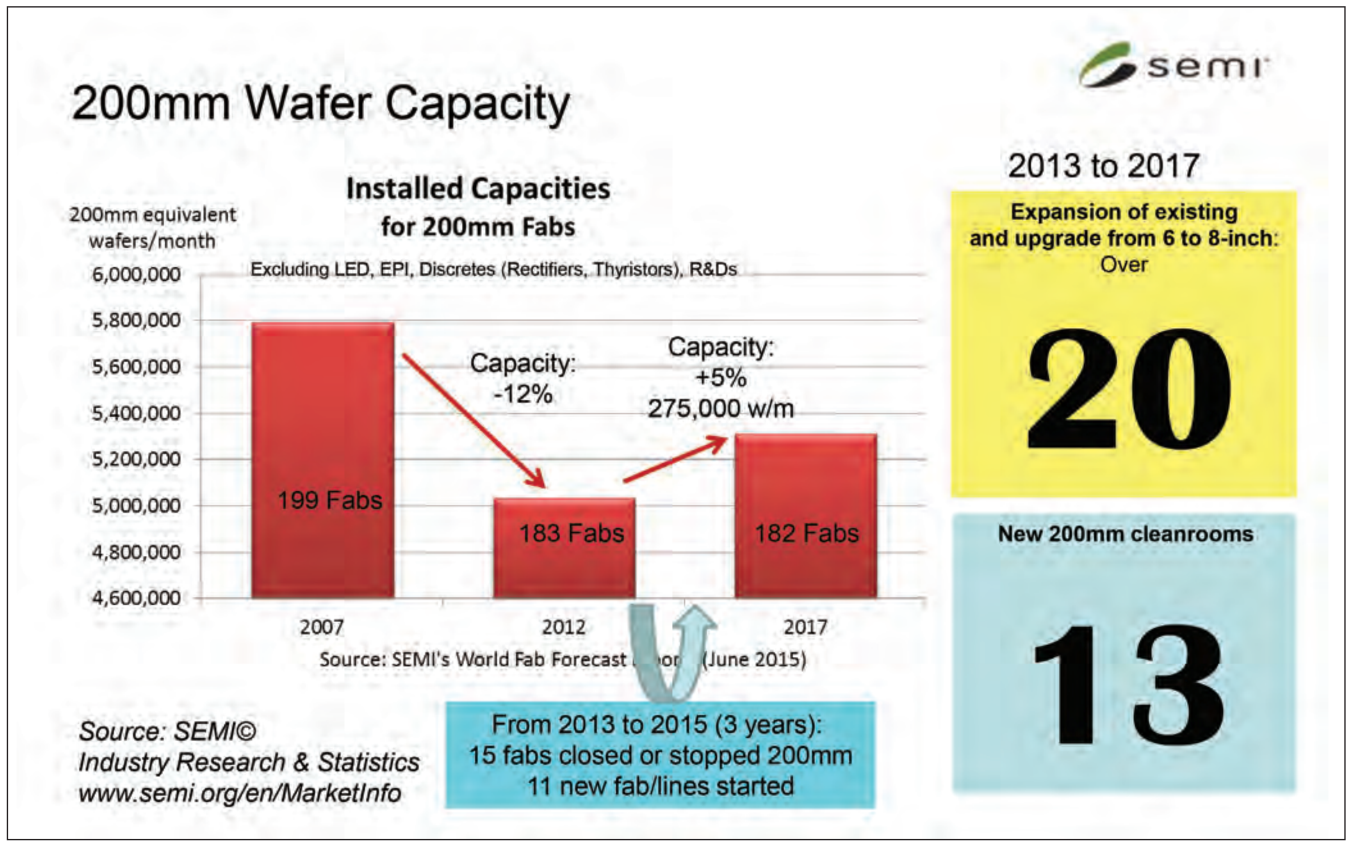


Image courtesy of SEMI

> While many OEMs have an interest in supplying toolsets to the IoT market and have remanufacturing capability, their legacy 200mm OEM tools were designed specifically for processing silicon. IoT devices call for processing on exotic materials such as compound semiconductors and glass for optical applications, which calls for re-engineering, particularly with regard to handling

engineering and process expertise in older technologies, and ensuring standards and quality to satisfy a demanding and extremely high volume industrial environment.

There are two viable options for sourcing semiconductor equipment: OEMs or secondary equipment suppliers. While many OEMs have an interest in supplying toolsets to the IoT market and have remanufacturing capability, their legacy 200mm OEM tools were designed specifically for processing silicon. IoT devices call for processing on exotic materials such as compound semiconductors and glass for optical applications, which calls for re-engineering, particularly with regard to handling. Additionally, the cost of procuring a tool with installation, full service support and training from an OEM, is typically much higher than securing the same from a company specializing in remanufacturing secondary equipment.

When sourcing secondary equipment for IoT fabs, it's important to look for the full solution. This goes well beyond just a piece of used equipment, and includes developing and implementing new process capabilities specific to IoT devices. A full service provider of secondary equipment not only refurbishes a tool, it remanufactures it to either original, or in many cases, new specifications, while providing full service support, installation, and training. The best-case scenario is for an IoT fab to engage in a long-term partnership with a secondary equipment manufacturer that understands the processes required for IoT device manufacturing, from developing the specialized tool processes, to adapting the tools themselves to handle new requirements or exotic materials. These companies can supply a full line, or fill in the gaps with tools that are engineered and customized to the fab's requirements and support technology transfer.

It's also important to consider tool knowledge. Many engineers and technicians working for secondary equipment suppliers have worked on four or five generations of these tools, since the time when they were state-of-the-art. They are able to transfer this knowledge and train customers on the tools.

Conclusion

To be competitive in the IoT market, cost is key and making the successful adaptation of secondary equipment is paramount. A supply chain that can quickly fulfill the need for re-purposed equipment, support, and services is critical. Choosing an equipment partner that can fulfill these needs will be vital for the success of the IoT fab.

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New paths to greener semiconductors

Manufacturers are working to reduce the environmental impacts of next-generation technologies by challenging common practices in today's semiconductor plants. Mike Czerniak, Environmental Solutions Business Development Manager, and David Hacker, Strategic Marketing Manager, at Edwards UK, Hartmut Schneider, Technology Manager Semiconductor, from M+W Group, Stuttgart, Germany discuss their solution.

THE SEMICONDUCTOR industry is constantly striving to reduce the environmental footprint of chip manufacture. This goal is especially true as manufacturers contemplate 450 mm wafer production. A key feature of the rationale for introducing 450 mm wafers will be scaling utility consumption at a slower rate than the surface area increases (i.e. 2.25x compared to current state-of-the-art 300 mm wafers), as reflected in the ITRS roadmap [1]. Scaling back utility consumption would have the complimentary benefits of reducing manufacturing cost and, at the same time, reducing CO2 footprint, which is becoming increasingly important as "green labelling" is more widely deployed. Yet several factors have conspired to actually increase energy-per-unit-area (kW/cm^2) in recent times. Energy saving during periods of wafer inactivity is one route towards off-setting this trend, but requires standardised signalling before it can achieve widespread adoption.

Another factor to be considered is the decreasing size of semiconductor devices themselves. As dimensions approach levels where atomic-scale factors come into play, some devices may require fine-tuning during manufacture. This will result in a need for a greater degree of data collection and analysis, and increased data connectivity within the fab environment to achieve the adaptive control required to maintain high process yields in a more flexible real-time environment. This is another area where standards and protocols are necessary for significant deployment of the latest prognostics and diagnostics. These concepts can be summarised as seen in Figure 1.

Right: Fig 1 Edwards phased development towards 450 mm

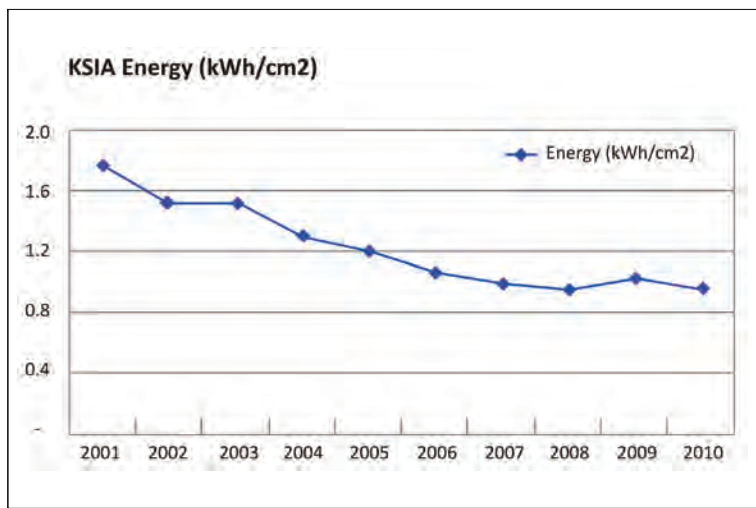


Fig.2 Energy use/wafer area in Korea [2]

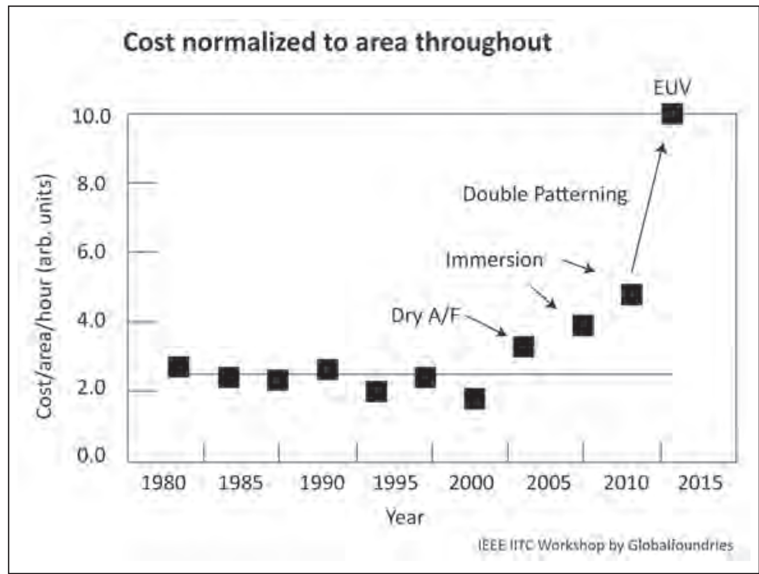


Fig.3 Cost/wafer area for 300 mm wafers [3]

Wafer size	Pitch	# Processing steps
200	0-1μm	~100
300	23nm	~1000
Future	Future	>1000

Fig.4 Table illustrating the impact of reduced feature size and increased wafer diameter on number of processing steps [4]

Drivers for utility consumption reduction

Since about 2005, the semiconductor industry has been steadily decreasing its kW/cm^2 footprint. But in recent times this trend has been in reverse, as shown in Figures 2 and 3.

In addition to the factors cited in Fig 2, the number of process steps required to manufacture leading-edge chips is trending upward, so even if an individual process step becomes more efficient, the net effect of more steps results in an overall increase. The table in Figure 4 illustrates this point:

Given the goal to support environmentally sound practices, the semiconductor industry is looking for ways to offset these trends and reduce utility consumption per unit area, which would also have the benefits of reducing overall cost while shrinking the carbon dioxide (CO2) footprint (6.89551 $\times$ 10^{-4} metric tons CO2/ kWh[5]). The latter is important to help reduce Green House Gas (GHG) emissions from the industry. Many manufacturers are already auditing emissions throughout the entire production process to enable using one of the many "Green Labels" currently available[6] a selection is illustrated in Figure 5.

Idle mode as a route to utility savings

Many automobiles save fuel (and CO2 emissions) by automatically switching off the engine whenever the vehicle is temporarily stationary, e.g. at red traffic lights; the engine automatically re-starts when the gas pedal is pressed.

This concept is the basis of an "Idle Mode" that can be replicated in a semiconductor fab by reducing the rotational speed of a vacuum pump and reducing the fuel or electrical power draw of a gas abatement system at times when the process tools are not actually running wafers, where a significant proportion of the fab's power is consumed, according to a 2012 ISMI energy study [7].

This study concluded that 300 mm Fab process equipment consumes 43 percent of the total power budget, and of that figure process pumps consume 41 percent and load-lock/transfer pumps consume a further 10 percent. Savings in these areas could substantially affect energy costs.

The issue of realising such savings in practice has been the lack of standardised signals to pumps, abatement systems and so forth to initiate and end periods of energy saving. Much equipment has had this capability for many years, so a SEMI task force was initiated to tackle the issue. It was agreed to split the work into two parts to simplify the task. Phase 1 would cover host to process tool communications,

Fig.5 A selection of International Green Labels

resulting in the publication of SEMI E167. Phase 2, covering tool to sub-fab equipment (e.g. pumps and abatement), is currently a work-in-progress. In both phases the process tool 'decides' when to initiate and end energy-saving idle modes because the tool knows when wafers are present and also when vacuum and/or abatement are required when wafers are not present, e.g. during maintenance activities.

Modelling 450 mm energy saving potential in EEM450PR consortium

Having established a potential pathway to idle mode energy savings for 450 mm wafer manufacture, the opportunity to model and test its potential impact on a 450 mm fab presented itself as part of the European EEM450PR project, part of Eniac [8].

In this consortium Edwards, M+W Group, Intel, IMEC, Artemis, Recif, Asys, Fraunhoffer, XYCarb and AIS Automation collaborated in Work Package 4.2, Factory Integration.

A Fab model was developed by M+W Group, based on 300 mm, 40k m^2, 120k WPM, 1400 tools (using IC Knowledge data regarding the toolset), 85 percent utilisation, and was populated with pumps and abatement systems appropriate to each

System	Actual Consumption with Green Mode		Saving	Baseline
Power	Actual Power Consumption	11,377 kW	17%	Aux Tools Total
			5%	Tools Total (BM)
PCW	Actual PCW Consumption	2,646 m³/h	17%	Aux Tools Total
			6%	Tools Total (BM)
Exhaust	Actual Exhaust Consumption	152,103 Nm³/h	0%	Aux Tools Total
			0%	Tools Total (BM)
N2	Actual N2 Consumption	7,862 Nm³/h	20%	Aux Tools Total
			11%	Tools Total (BM)
O2	Actual O2 Consumption	254 Nm³/h	23%	Aux Tools Total
			19%	Tools Total (BM)
NG	Actual NG Consumption	1,196 Nm³/h	23%	Aux Tools Total
			n.a.	Tools Total (BM)
UPW	Actual UPW Consumption	103 m³/h	23%	Aux Tools Total
			6%	Tools Total (BM)
WWT	Actual WW Consumption	106 m³/h	20%	Aux Tools Total
Source: M+W Group			6%	Tools Total (BM)

Figure 6 Potential utilities savings in a 300 mm fab using idle mode

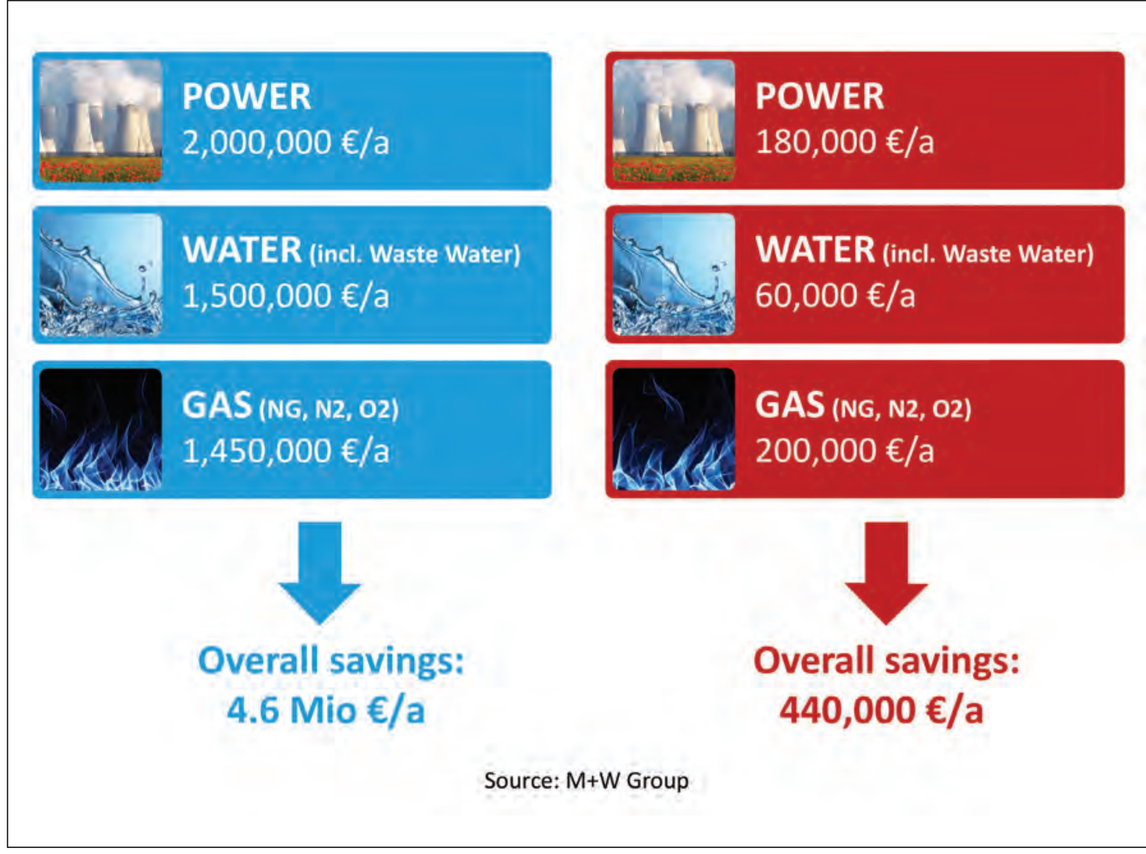


Figure 7 Potential utilities savings in R+D & HVM 450 mm fab scenarios

process application by Edwards, including their utility consumption. The potential savings are summarised in Figure 6. Using a similar methodology, 450 mm wafer fabs were populated and modelled for both High Volume Manufacturing (HVM) and R+D scenarios. The potential savings at 85 percent fab utilisation are summarised in Figure 7.

Testing the 450 mm energy saving model in EEM450PR consortium

Having constructed a 450 mm Idle Mode model, it was then tested in two scenarios, namely R+D and HVM. In the case of R+D, a pump and abatement system were connected to a CVD tool and utilities were monitored in process and idle modes initiated by an idle mode signal, as shown in Figure 8.

Fig 8 Idle mode savings at a 300 mm R+D fab
To check the HVM model, data from nine process tools including CVD and etch in a 300 mm fab was analysed over a one year period.

Potential savings were recorded if (a) neither vacuum nor abatement were required by the tool (e.g. for MFC calibration, etc.) and (b) the idle time was greater than 100 seconds (anything less than this can actually increase overall energy consumption due to the tools' operational practices and requirements.) Reviewing the data led participants to conclude that that an overall potential energy savings of ~17 percent could be achieved; representative graphs are shown in Figure 9.

Fig 9 Potential Idle modes in a 300 mm HVM fab
It is planned to cross-check these results with G450C on an actual 450 mm tool as a final model verification.

Fig 8 Idle mode savings at a 300mm R+D fab

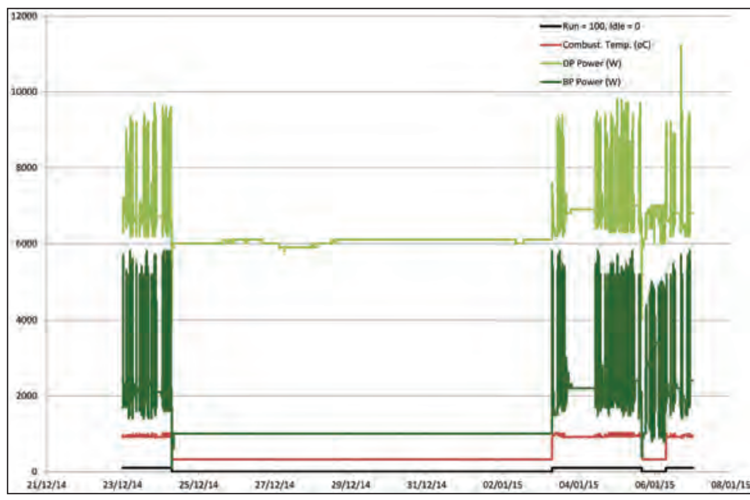
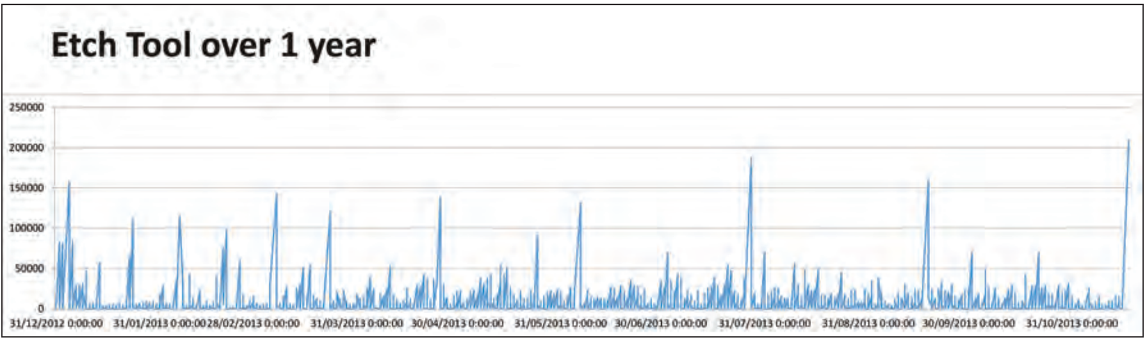
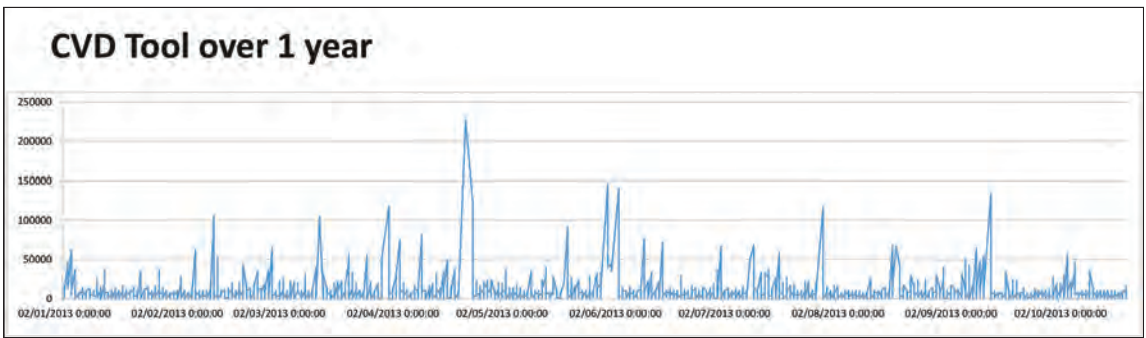


Fig 9 Potential Idle modes in a 300mm HVM fab





Summary and conclusion

By the time that 450 mm replaces current 300 mm wafers, HVM will need to adapt to meet the challenges these new technologies will introduce. A key element of this is increased data flow in general as individual processing steps need to be dynamically adapted so as to maintain consistent device performance as feature sizes continue to shrink towards the atomic scale.

Another aspect of future fabs will be the need to decrease utility consumption in order to: offset any increase in the number of processing steps, the introduction of new energy-hungry steps, and any increases in process gas flows associated with larger wafer diameters.

The most promising route to achieving such savings is to implement Idle Mode savings strategies. The potential to positively impact at 450 mm has been modelled and the model tested at 300 mm R+D and HVM.

Fundamental to the deployment of Idle Mode savings processes is the provision of suitable standardised signalling, between the HOST/MES system and the processing tool (SEMI E167[9]), and subsequently between the process tool and sub-fab equipment, such as pumps and gas abatement, which is currently a work-in-progress.

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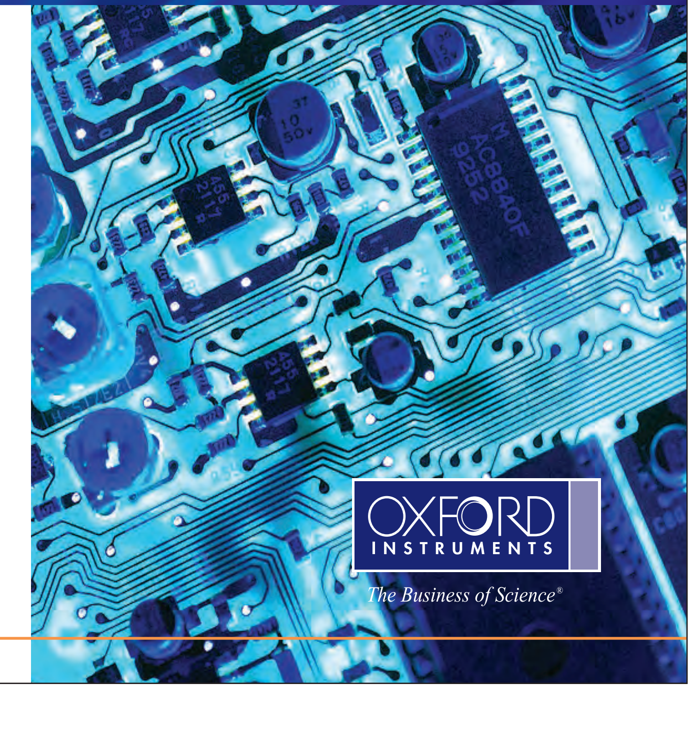

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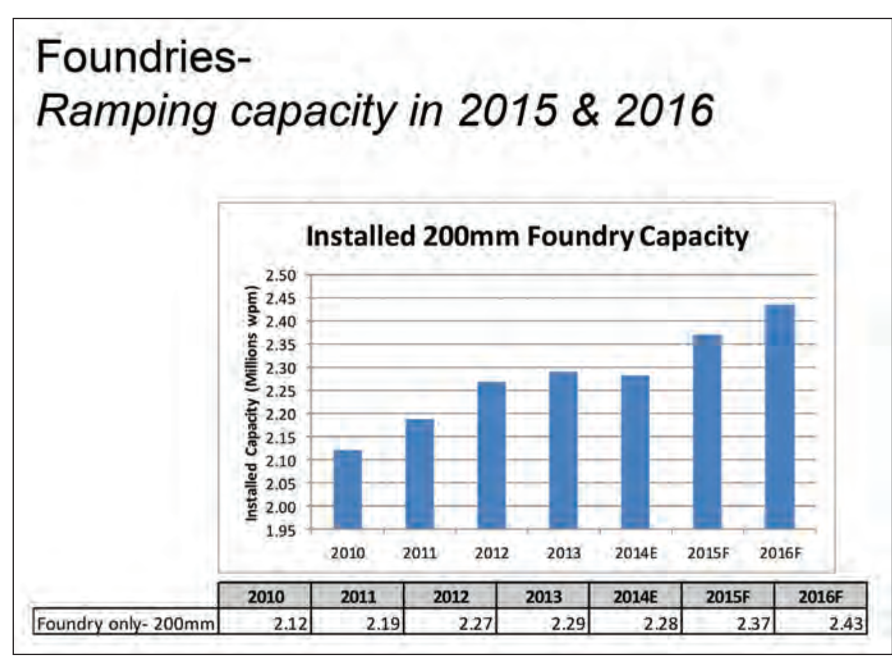
Sourcing refurbished semiconductor equipment

Erik Hanson, Refurbished Products Manager, Cascade Microtech, Inc tells Silicon Semiconductor why going straight to the OEM for refurbished equipment reduces both the risk and cost.

WHILE ADVANCED node device manufacturing has transitioned to 300 mm equipment and the industry anticipates the transition – someday – to 450 mm, a quiet renaissance is taking place in the 200 mm equipment market. The Trillion Sensors initiative and the Internet of Things (IoT) are breathing new life into 200 mm fabs, especially in analog chips, power management devices, image sensors, and new emerging applications in biomedical, MEMS, and other areas. As many of these devices (destined for consumer markets) are based on mature technologies, there are significant advantages to outfitting 200 mm fabs with certified used test and measurement equipment that has been either refurbished or remanufactured, rather than purchasing new 200 mm equipment.

There are three main options for purchasing refurbished equipment:
1. Open market
2. Third-party vendor
3. Original equipment manufacturer (OEM)

Each option has its advantages and disadvantages. In this article, we will look at the market for refurbished semiconductor equipment, examining the three procurement options. Finally, through a brief case study, the best approach will be presented.



	2010	2011	2012	2013	2014E	2015F	2016F
Foundry only- 200mm	2.12	2.19	2.27	2.29	2.28	2.37	2.43

Figure 1. Chart from SEMI Secondary Equipment Market and Trends, February 2015
200 mm fab capacity is on the rise, led by foundries that are increasing 200 mm capacity by about 7 percent through to 2016, compared with 2012 levels. This is driven by new applications related to mobility, sensing, and IoT.

200 mm semiconductor fabrication capacity is on the rise

In January 2015, SEMI published its latest Secondary Fab Equipment Report to determine the market size and identify key trends and issues impacting this important industry segment. [FIG.1]

According to the report, 150 mm and 200 mm fab capacities represent approximately 40 percent of the total installed fab capacity in the world. Additionally, 200 mm fab capacity is on the rise, led by foundries that are increasing 200 mm capacity by about 7 percent through to 2016 compared with 2012 levels. This is driven by new applications related to mobility, sensing, and IoT. For 2014, 200 mm fab investments by leading foundries and independent device manufacturers (IDM) resulted in a 45 percent increase in spending for secondary 200 mm equipment.

While SEMI did not include test equipment and assembly and packaging equipment in this report, it's safe to assume that the ratio of used test equipment versus total used equipment sales is the same as the ratio of new test equipment versus new equipment sales. This gives us an indication of the volume of devices that are being fabricated at 200 mm, which will ultimately require 200

mm test equipment to characterize these devices quickly, at low cost, with minimal setup, and in parallel.

Despite the growing demand for capacity at 200 mm, the global economic climate and new production strategies have led to the consolidation of many semiconductor manufacturing companies, as well as the closing of many 200 mm fabs. This has contributed to an estimated 6,000 used tools now on the global market in various states of repair. Many of the tools on the market are incomplete, harvested for spare parts, and/or improperly maintained.

The majority of used equipment today is between 7-13 years old. Much of it has not been properly decommissioned and decontaminated, presenting further legal, environmental, and health risks for purchasers, shipping companies, installation and operations personnel. Clearly, the risk accompanying used equipment has increased exponentially. It is more critical than ever that purchasing agents apply their full due diligence to mitigate that risk.

Figure 2. Of the three procurement options for refurbished equipment, original equipment manufacturers are the logical choice to reduce risk and improve overall cost of ownership.

Why buy refurbished?

A number of factors come in to play when deciding where to spend equipment dollars. To remain competitive among the low-cost producers, legacy fab managers need to balance tight process and time-to-market budgets. In fact, according to a SEMI survey of top 200 mm fab managers, secondary equipment will be the number one source for future productivity improvements.

As major OEMs have shifted efforts to 300 mm and in some cases 450 mm, they have mothballed 200 mm tooling. Used 200 mm equipment that has been refurbished or remanufactured to meet new device requirements can be a very desirable way to upgrade legacy fabs while remaining competitive in the market.

Sourcing options and scenarios

Buying test equipment on the secondary market can be compared with purchasing a used car. It all comes down to buyer expectations and their willingness to take risks. Options range from eBay or other online resellers, used car dealers, or through a certified pre-owned program at new car dealership. This logic can be applied to the secondary equipment market as follows. [FIG.2]

The open market option

Purchasing used equipment on the open market through an online broker or an auction website is like buying a used car online. Generally, the ones who benefit the most from this option are mechanically inclined, and can handle the inevitable repairs. Many are engineers with years of experience using these systems. They are comfortable taking the risk on an "as-is" system. In these cases, the purchase is based purely on price, which is typically the lowest initial purchase price available. The only other clear advantage of purchasing used equipment through the open market is the equipment's availability for immediate pick up. However, it may be sitting in the previous owner's lab, or a reseller's warehouse.

The disadvantages far outweigh the advantages. There is no guarantee of the tool's functionality, or whether it will be suited to the customer's application. As-is means there are no software updates, and in all likelihood, electronics hardware is outdated. The customer has to arrange pick-up logistics including installation, and assume additional costs including packaging, freight, and import/export logistics and fees. The most a customer can hope for in the way of a warranty is a 14-day money-back guarantee. Essentially, the customer is on his/her own. They may rely on the OEM service provider to get a system up and running, and to obtain spare parts and service. This is, of course, not included in the purchase price. All things considered, it adds considerably to the total cost of ownership.

Third-party vendors

Slightly less risky than purchasing used test equipment on the open market is to purchase it through a third-party vendor. This can be compared with purchasing a used car from a used car dealership. Third-party equipment vendors frequently contract with former field service engineers of the OEMs whose tools they sell. These engineers install the equipment, put it through diagnostics, and make sure it's operational.

One advantage third-party vendors have is the ability to reconfigure an existing tool because they often purchase equipment in lots that include several stations complete with assembly parts and accessories. This allows them to swap out accessories sold with a probe station to cater toward a DC application or an RF application based on the customer's requirements. These third-party companies advertise they can guarantee some level of performance, but they typically don't employ

Figure 3. A refurbished Cascade Microtech SUMMIT™ semi-automated probe station with an eVue™ Digital Imaging System is a reliable, robust solution for today's 200 mm test and measurement requirements.

professionally certified installation and service experts. While they may have a certain level of experience working on tools, it is not necessarily with equipment from the specific OEM in question. With regard to warranty for purchase, the longest standard third-party warranty on the market is 90 days, and additional warranties for service and parts need to be considered as part of the tool's overall costs.

Online purchasing won't save you money

Take for example this actual situation of a purchase made from an online marketplace for a used wafer probe station originally manufactured by Cascade Microtech, a supplier of wafer probe equipment to the semiconductor test market.

The tool was sold by an online merchant for $25,000. The customer, a high-end semiconductor device designer and manufacturer, was looking for a tool for their Failure Analysis group. The tool was non-functional when it arrived at the customer site, so the customer spent an additional $2,500 with a third-party service provider to get the system up and running. Unable to successfully get the system running properly, they contacted the OEM – Cascade Microtech – who provided updated control hardware and software, as well as other components to replace those that were not well maintained by the previous equipment owner. After paying an additional $15,000 for necessary parts and service, the system was restored to full functionality. At the end of the day, the total out-of-pocket cost for the tool was $42,500.

Had the customer gone directly to the OEM (Cascade Microtech), the required replacement parts would be included as part of the standard certified refurbishment process. The price for a similarly equipped certified used system purchased directly from Cascade Microtech would have been approximately $32,000, and would include the company's standard warranty. The customer actually spent $10,500 more than if they had gone directly to the OEM, and could have avoided the headaches incurred. Additionally, the customer lost opportunities, time, and revenue while the tool was not operational.

The OEM advantage

Many semiconductor OEMs sell used systems that are fully factory refurbished. Parts that wear out are replaced, and the latest compatible control electronics and software are added. Each piece of equipment is fully tested and must pass the same functional specifications it did when it originally shipped as new. Professional packaging, transportation, and installation ensure equipment functionality at the customer site, not just the manufacturing facility. The tool comes with a standard warranty similar to the warranty provided with new equipment. The systems are certified-used and eligible for service contracts, and are serviceable by the OEM's field service engineers. [FIG.3]

The OEM will either use the same sales channel and sales process as with its new equipment, or it will have a separate selling organization for used equipment. Used equipment in stock is sold on a first-come, first-served basis, and is delivered in about half the time of new equipment. In many cases, the OEM is actively seeking used equipment and can pay cash or provide credit for returned equipment toward future products or services.

Go to the source

It's clear from this brief example that going straight to the OEM for refurbished equipment reduces both the risk and cost in comparison with the open market or third-party vendors. While the initial purchase price may be slightly higher than other options, the quality and support are superior, and overall cost of ownership is far less.

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Silicon tech

evolves to 450 mm

Manufacturers are pooling resources to double global IC capacity. Will achieving the next milestone in silicon evolution give members a competitive edge? Silicon Semiconductor's Mark Andrews spoke to Todd Fosler F450C new program manager.

WE HAVE all heard industry tales with a familiar backstory: entrepreneurs in Country X conceive a great new technology. Through tenacity and sleepless nights, these struggling geniuses create revolutionary new products. After a massively-successful IPO the founders buy super cars and retire to Tahiti.

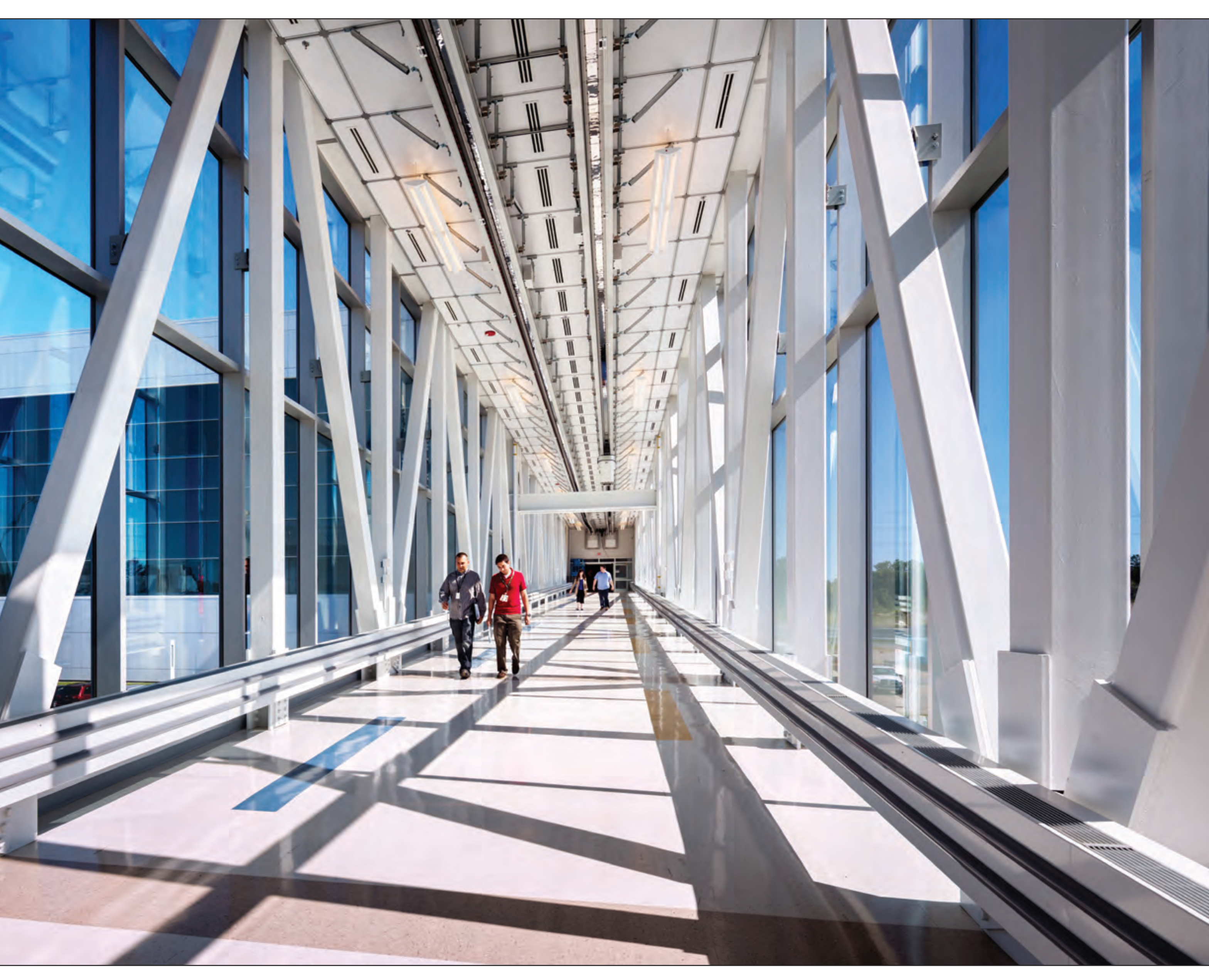
While dreams of miraculous success may draw some to the industry, most Silicon Superstars won their fortunes by designing and selling innovative products that met needs/solved problems. For every celebrity CEO on a stage, there are armies of scientists, engineers and manufacturers backing them up.

Consider the 300 mm silicon wafer, now the largest substrate in high-volume manufacturing (HVM). Fabs didn't jump to 300 mm wafers overnight, nor have they abandoned 200 mm, which is surging for MEMS and other applications suited to their size. Work continues on both wafer types to improve yields and performance. Technologies evolve over time. Each cutting-edge breakthrough arrived after many steps.

Costly investments are made and risks are taken to achieve new semiconductor milestones. While the business of technology rewards innovation, it can just as easily crush a company. This adage holds true: risk nothing/win nothing.

Manufacturers saw 450 mm wafers as challenging from the outset. Today's successful 300 mm technology was created through 'institutional entrepreneurship'—companies worked solo or in limited partnerships to innovate. Pieces of the puzzle fit together and are still evolving. While foundational work that achieved 300 mm success might see repurposing in 450 mm, many separate issues need to be resolved, so manufacturers saw that a new risk-reducing approach was needed.

A consortium of companies dedicated to facilitating 450 mm fabrication formed in 2011 with the backing of New York Governor Andrew Cuomo who offered seed money and a home at the Colleges of Nanoscale Science and Engineering (CNSE) housed at the State University of New York (SUNY) Polytechnic Institute campus in Albany. The Global 450mm Consortium (G450C) was created first. It focuses on the tooling and



process challenges of manufacturing with 450 mm wafers. It was followed in 2013 by the Facilities 450 Consortium (F450C), which was chartered to overcome the infrastructure-related hurdles of 450 mm fabrication.

Silicon Semiconductor's Mark Andrews recently spoke to Todd Fosler who joined the F450C earlier in 2015 as its new program manager. Fosler brings 20 years of semiconductor manufacturing experience to the partnership. While with Intel, he managed and developed implementation of new manufacturing capabilities that enabled the transition to 300 mm wafers for functions including sort, assembly and test. He had previously focused on fab design, construction and conversion methods in various engineering and leadership posts. He specializes in how to integrate the demands of new tools and process technologies into a facility design that is optimized for sustainability and affordability.

Fosler considers the F450C a first-of-its-kind partnership that is leading the global effort to design and build next generation 450 mm facilities. He said that 12 companies serving various functions and processes in semiconductor manufacturing comprise the consortium's roster: Air Liquide, Busch Vacuum Pumps and Systems, CH2M, CS Clean Systems, Ceres Technologies, Edwards, Haws Corporation, Mega Fluid Systems, M+W Group, Ovivo, Pfeiffer Vacuum and Swagelok.

Q Transitioning from one wafer size to another has in the past been an evolutionary process. How does the F450C see itself enabling the move? The consortia are housed on a SUNY campus; does the State of New York hope new 450 mm fabs will be built there?

A F450C was formed to enable the world's leading semiconductor facility companies to collaborate and develop the 450 mm high-volume facility construction standards. This is so that when the industry is ready to pull the trigger on the 450 mm transition, the time to get the first production wafers out is not gated by facility construction standards or uncertainty about fab infrastructure solutions.

SULY Poly CNSE have been a great home for both consortia.

> "Anytime you are working with the leading edge of technology, there is a lot of experimentation with successes and failures, but we learn from the failures and move forward"

The promotion of STEM education locally has made it a perfect home that aligns with the general push to make upstate NY a high-tech hub. While I can't speak for NYS, I do think they are making it an attractive location for companies to create new employment opportunities as these fabs are constructed and ramped into production.

Q Public/private partnerships are not new. How does the consortium's partnership with the State of New York differ from others?

A This collaboration is unique because the industry understands that 450 mm facility challenges require collaboration across the entire value chain. Working alongside each other at the CNSE, G450C and F450C can more effectively explore options and align on facility standards with industry partners. Without this collaboration, our goals of developing viable 450 mm standards and technology solutions would not be possible.

Anytime you are working with the leading edge of technology, there is a lot of experimentation with successes and failures, but we learn from the failures and move forward. The companies in this consortium, along with SULY Poly CNSE, are working together to find the best way to move forward and develop the technology the semiconductor manufacturers need to enable the 450 mm transition.

Q It seems almost any technology conference focused on the needs of silicon semiconductor manufacturing has tracks about challenges tied to the move from 300 to 450. What areas are the F450C focused upon?

A Our members' priorities for facilities-related projects are: utility right-sizing, standardize tool install procedures and minimizing the number of points-of-connection; improve AMC detection/response, helium recovery/recycling and green-mode systems usage. Equally important to the work we do in 450 mm technology is the work of the Global 450 Consortium (G450C). G450C members consist of Intel, TSMC, Samsung, IBM and GLOBALFOUNDRIES.

Q The equipment being installed in the new SULY Poly CNSE fab, is it 300 mm-based with adaptations for 450 mm, or is new equipment created specifically for 450 mm?

A Within the consortium, we encourage our members and the sub groups to concentrate on technologies that are scalable between wafer sizes so that fabs can benefit today regardless of which wafer size they produce. However, our main objectives and timelines deal with 450 mm tools, as evidenced by milestones like Nikon's lithography tool being delivered to the Albany Campus (http://bit.ly/1CKkTA3), which joined existing 450 mm infrastructure. According to CNSE, the investment in tools on the campus has surpassed the $700 million mark (http://bit.ly/1L0de8Z).

Q Can you give us a better indication of what members are focusing on right now?

A Recently, F450C hosted an interactive panel featuring five representatives from F450C and G450C. The discussion centred on two main recurring themes: access to manufacturing information; and manufacturing sustainability and resource conservation. The event reflected the spirit of collaboration essential in this transition and in developing technology that can scale between wafer sizes, a current focus of F450C's members. Full footage of the panel can be found here: http://www.f450c.org/f450c-hosts-panel-semicon-west-2015/

Q Are there advantages to making the move to 450 mm wafers that the consortium feels don't get enough discussion and should be more widely considered by the industry as a whole?

A Yes. This will certainly be the most efficient wafer-size transition when it does reach that point. Until then, members of the consortium are not waiting for 450 mm to drive the need for more efficient systems and tools. The recent R&D efforts signal the movement toward technologies that can be used in existing production lines, but that can also be scaled-up for the first 450 mm fabs. Speaking to efficiency and the aforementioned resource management, the work being done at SULY Poly CNSE highlights some of the most technologically advanced methods of conservation and monitoring. Consortium members Haws

Corporation and Ovivo focus their efforts on water consumption and waste stream management, knowing how important those will be in relation to a larger wafer size. Additionally, our members are directly addressing power management issues that fabs face today, but that will also be useful as we ramp to high-volume manufacturing in 450 mm in the future, specifically our vacuum manufacturers. Abatement systems will continue to be extremely important regardless of wafer size. Joe Guerin

of CS CLEAN SYSTEMS often speaks of the need to strike a balance for each process technology and wafer size, and emphasized that during our panel.

Q I heard one technologist say that no one wants to be the last person to build a totally new 300 mm plant, yet no one wants to be the very first to build a 450 mm plant. Do we need 450 mm technology right now?

A Part of F450C's mission is to reduce the cost risk for the first 450 mm fab to be built. We are aiming to make this the most efficient transition in industry history. This hasn't always been the case. In earlier transitions, one company carried most of the risk by building the first new wafer size fab and working out the technology startup issues alone. Through collaboration, we are taking the burden off one player
as the entire industry comes together to anticipate, plan and support the transition.

Q It is interesting to see the semiconductor industry take this approach. Historically, companies have wanted to pioneer new technology to be first to market – Is being first too risky in 450 mm?

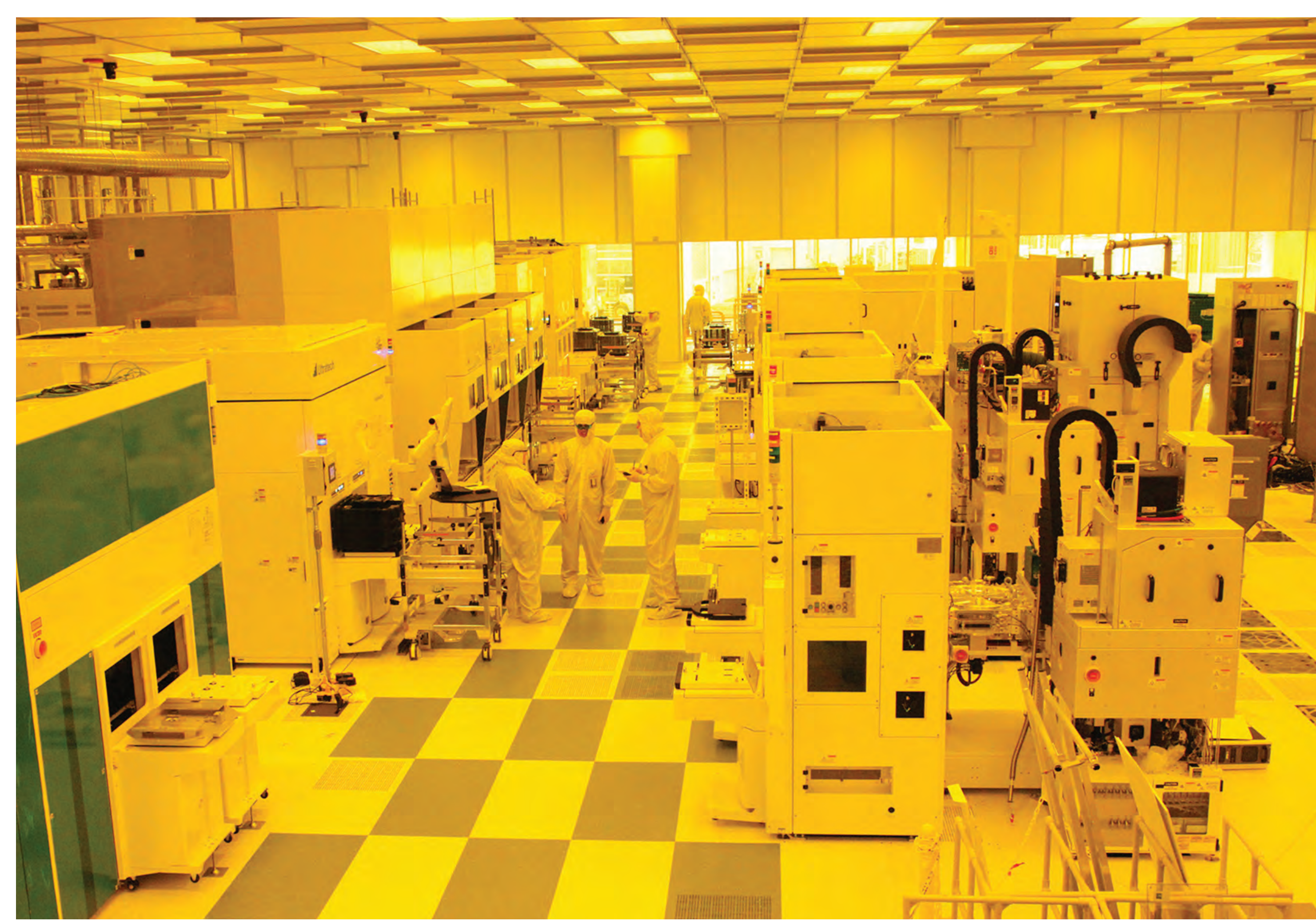
A Cooperation between different companies and suppliers will reduce risks of major manufacturers when the first 450 mm fabs are built. It's a business decision to join the F450C or G450C (depending on the company's function) and less risk typically garners more participation from the industry.

Q Consolidation remains an industry reality. At the same time some medium-sized fabs are becoming 'Mega Fabs'—all are still using 300 mm. Does consolidation paired with fab expansion underscore the need for 450 mm?

A A company's market forecast and need for cost-effective manufacturing capacity expansion will drive the decision on when to build a 450 mm fab to meet market demand. 300 mm fabs continue to be built around the world, and many of them are 450 mm capable, so the industry is indicating it's prepared to convert when the supply chain is ready to deliver.

Q Can you summarize the general feeling of the consortium's members with regard to 450 mm and the technical achievements we've seen so far?

A The consortium is working collaboratively, and the developments we have already achieved in power management, wafer handling, waste containment, green mode and many



(From our SEMICON West Panel - (from Right to left) moderated by F450C Program Manager Todd Fosler, and consisted of five panelists: David Skilbred, Director of Program Coordination/Management, G450C.

more are not just for 450 mm, but will be applied in existing 300 mm fabs and other size fabs as well.

Overall, the companies involved with both consortiums see the value in investing in R&D for this technology, much of which can be applicable to today's technology. Our members are working to enable the transition to the 450 mm wafer, in line with G450C members so that the transition is as smooth as possible for the entire industry.

Q Please explain what the consortium feels should be known about itself, its charter or operation. How do the G450C and F450C groups work together?

A The structure of the F450C and G450C creates an environment where we are working on early facilities technologies that will enable the introduction of 450 mm into HVM. We have an increased focus on facility and process sustainability and affordability and we have an opportunity through our collaboration at CNSE to advance the combined learnings of the consortia's membership into the 450 mm transition.

In my first couple of months as program manager I have witnessed the collaborative atmosphere of G450C, F450C and SULY Poly CNSE. To this point, there hasn't been a ton of surprises but there has been a staggering amount of information shared between each of the players that help in setting industry standards. Our members mostly work in subgroups that focus on a particular part of the 450 mm wafer manufacturing process. The research that is developed as part of the subgroups is then shared amongst the rest of the consortium members and, if relevant, with the G450C and SULY Poly CNSE.

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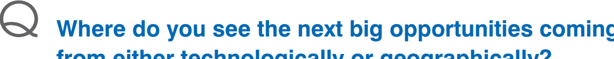
Siemens helps manufacturers boost agility

Silicon Semiconductor spoke to the team at Siemens to find out what was achieved in 2015 and what the future holds.

Q What have been the highlights of 2015?

A Camstar was acquired by Siemens in late 2014 and integrated into the Siemens family of software products in 2015. Siemens Manufacturing Operations Management (MOM) software portfolio enables manufacturers to implement their strategy for the complete digitalization of manufacturing operations. Enabling optimization of production processes within the Digital Enterprise, Manufacturing Operations Management software products focus on improving efficiency, flexibility and time-to-market.

Camstar also continued to expand the capabilities of its Semiconductor Suite manufacturing execution system (MES) – supporting the full manufacturing process from substrate, fabrication, probe, assembly and test – to increase customer value while reducing deployment time. Camstar Change, Siemens' Manufacturing Process Change Management solution, was also expanded to provide additional capabilities requested by customers.



Q Where do you see the next big opportunities coming from either technologically or geographically?

A The manufacturing landscape is expanding and growing and there will be great opportunities for vendors that can provide a comprehensive solution that helps global manufacturers manage all aspects of their global supply chain, from raw material sourcing to manufacturing to finished good delivery and use by customers. The top opportunity for Semiconductors goes beyond having the best plants. Semiconductor leaders need to build a strong global manufacturing networks that can learn and adapt to the needs of the supply chain and the customers' demand for new, innovative products. The agile network needs very strong information flow between MES and other enterprise applications such as ERP, supply chain and product lifecycle management systems.

Enterprise Manufacturing Execution (MES) is critical because of its ability to quickly and easily set up multiple plants and relationships between them and its ability to make changes rapidly and consistently across plants. A true enterprise MES will help pinpoint how to optimize the global operations network. The global manufacturing network brings additional needs to manage rapid and frequent change. Manufacturers are faced with an increasing level of product and process changes to meet the demands of the ever-changing markets they serve.

Q Are you working on anything "new" for 2016?

A Siemens continues to deliver new out-of-the box capabilities for our customers based on industry best practices for all of our product lines – using industry-leading technologies.

We are expanding our portfolio of Enterprise-class capabilities to support our global manufacturers by enabling them improve speed, agility, transparency and interoperability. Siemens is dedicated to continuously enhancing the capabilities of the Camstar Semiconductor Suite (MES) to meet the need of manufacturers with front-end as well as back-end operations.

Q What, if any, major changes do you see for the supply chain in the next five years?

A Semiconductor manufacturers rely heavily on speed of innovation and have many more people in design, supply chain, and related functions. They also have complex products with customization and variations that are manufactured across complex supply chain networks. The resulting variety of products leads to high product mix in plants, variability across the network, and larger challenges analyzing what works and does not.

This is why so many manufacturers are talking about creating agile global networks. Their operations span the globe, and they know they can do better in leveraging those production and supply chain assets. Creating an adaptive global network in which they optimize operations for high performance for customers' and their own success is high on their strategic goals.

Q What part will your company play in these changes?

A Siemens plays a significant role in helping semiconductor manufacturers manage their global supply chains. Siemens offers a portfolio of robust, industry-proven products that provide a holistic approach to optimizing the entire value chain. Siemens also plays a major role in helping manufacturers digitalize their business so they can effectively deliver highly innovative products using highly innovative processes.

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Bulk chemical supply vendor forecasts 2016 growth

Silicon Semiconductor spoke recently with Ametek, a leading US supplier of tubing and pipe used for bulk chemical distribution (BCD). Ametek sees growth prospects in 2016 driven by product innovation and increasing demands for manufacturing chemical purity.

Q What have been the highlights of 2015 for your company?

A Ametek is a major supplier of tubing and pipe for bulk chemical distribution (BCD) in most of the top semiconductor fabs in the US. Our products also have a significant presence in Asian markets. Because we are a preferred supplier of heat exchangers to most of the UHP acid manufacturers in the US and several in Japan we were optimally positioned to support a significant extension of heat exchanger service life through process and design improvements.

We continue to produce the highest quality and highest purity tubing, pipe and heat exchangers available for the semiconductor market. Additional 2015 successes included the launch of the FLUOR-X UHP (ultra-high purity) tubing and pipe product line.

Q Where do you see the next big opportunities coming from either technologically or geographically?

A We see a need for higher temperature and pressure PFA tubing and pipe as well as double containment pipe/tubing for bulk distribution inside semiconductor fabs. We look to growth in Korea and India for both industrial and UHP products. The market is also seeing increased purity expectations for electronic acids - parts per quadrillion (ppq), and for the UHP tubing and UHP heat exchangers to meet that requirement. Tool manufacturers need increasingly smaller footprints and we expect an increase in UHP requirements in cooling chemicals for wet processing and drain coolers.

Q Are you working on anything "new" for 2016?

A The industry thrives on innovation, so we have a variety of new products in development. These include higher temperature and pressure tubing/pipe: color-coded dual containment tubing; UHP tubing and UHP heat exchangers capable of meeting parts per quadrillion chemical quality; higher BTU per footprint and higher purity levels of wet bench/drain cooler UHP heat exchangers constructed of Fluoropolymer materials.

Q What, if any, major changes do you see for the supply chain in the next five years?

A The market could see some mergers of current Fluoropolymer suppliers and/or some contraction in suppliers. But at the same time we also sense some new/current resin suppliers expanding outside the US in such areas as India and China

Q What part will your company play in these changes?

A We plan to continue strengthening our relationships with the three major Fluoropolymer resin suppliers and closely monitor the volatility in the resin market and continue to expand our presence in Asia.

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A closer look at silicon's big future

Inspection and metrology leader KLA-Tencor delivers a wide range of integrated solutions for enhancing productivity in nano-scale IC manufacturing. According to Senior Vice President David Fisher, silicon's evolving needs will continue to drive growth in 2016 and beyond.

KLA-Tencor and Lam Research Corporation announced their intent to merge on October 21st. Like other headline-making mergers, the pending KLA / Lam marriage follows a familiar pattern: like-minded companies with complementary capabilities join forces to offer integrated solutions for essential industry needs. KLA-Tencor brings metrology and inspection leadership; Lam delivers deposition, etch and clean expertise. Silicon Semiconductor's Mark Andrews spoke with David Fisher, KLA-Tencor's Senior Vice President of Corporate Strategy, Marketing and Acquisitions to gain his perspective on the technologies he sees as critical to optimizing performance and quality in next-generation electronic devices. Today's leading foundries and device manufacturers depend upon highly refined 300mm technologies for high volume production of memory and logic circuits. But 300mm is just one part of a larger universe..

New and revived technologies utilize 200mm (and smaller) wafers even as the industry refines 300mm processes and also prepares for a 450mm future. KLA-Tencor sees great opportunity up and down the wafer spectrum because quality, efficiency and profitability always top the list of customer must-haves.

Q **IoT –** While new M2M devices are not yet widely seen in today's marketplace, this is a burgeoning field with the potential to radically grow the number of intelligent devices in consumers' lives. What do you see as a compelling argument for the growth of this industry and how does KLA-Tencor enable next-generation technology like IoT?

A KLA-Tencor shares the view that the continual drive to lower the cost of power chips with embedded communications is enabling significant growth potential in IoT. Early adoption, perhaps because of the current price point, appears to be focused at Automotive and Industrial, but we expect proliferation as chip costs come down and functionality goes up. Perhaps the most exciting aspect to IoT is the network, communications and algorithmic processing that will be required to harness the value of the data being captured by the end devices. Clearly, this expansion of communications infrastructure is happening today on a smaller scale in automotive at the local system level, but it is anticipated it will migrate to the global distributed level over time.

This growth in low cost/high function devices is creating a resurgence in inspection and metrology investments at mature fabs, and we expect there is potential for new fab investments and major expansions on >90nm design rules. These fabs have increasingly advanced requirements for a broad range of defect detection and metrology measurements. Although the economics are different than leading edge fabs, they still have similar yield and time to market constraints in order to meet their profit objectives. Those constraints are driving customers to seek out inspection and metrology tools, which used to be leading edge, but are now more affordable as they are older models. For example, the leading edge 8920 inspection tool is often the ideal broad range sensitivity and low cost of ownership (COO) system for IoT segments, delivering features like defect binning and tool-to-tool matching and leveraging our experience from the leading edge fabs.

Q **Optics Inspection –** How does optical inspection play a role in developing next-generation devices? What are the major trends and challenges for this field in the next year?

A For over more than a decade, the end to optical inspection has been predicted as geometries shrink and resolution capability comes into question at each node. In spite of those predictions, however, optical still continues to be the workhorse inspection tool in both the mask shop and the fab, as it offers throughput and hence COO that e-beam has been unable to approach. As a result, KLA-Tencor continues to invest in and

offer new optical systems that offer large advances in sensitivity over previous models. One difference at current nodes is that the defect landscape is not just limited to size (ever shrinking), but also where they occur (surface vs. buried). Additionally, metrology challenges around CD and overlay control have increased significantly with multi patterning. Also, there is demand for full wafer coverage at a good COO. To meet these challenges, KLA-Tencor is launching optical inspection tools at an unprecedented pace. We have extensions to the core optical 29xx Series, and have announced a "Generation 5" broadband plasma system that we are bringing to market in 2016, as well as new offerings for mask inspection, package inspection, CD, overlay and films metrology—all based on photon (optical) systems.

Q **Reticle Inspection –** As performance goals continue to move device geometries to smaller sizes, how does this challenge reticle inspection techniques? How do more efficient and accurate approaches benefit the customer and ultimately, end users?

A As argon fluoride (ArF) immersion lithography continues to be pushed into more aggressive nodes, customers are developing more aggressive reticle enhancement techniques such as inverse lithography optical proximity correction (OPC) techniques, and different masking technologies such as chrome-less phase lithography. Even in regions where the masking techniques were previously straightforward, customers can now add features such as ortho edge fragmentation to ensure they have a common process window. As a key supplier of inspection equipment for reticle inspection, KLA-Tencor works closely with our industry partners to align on the challenges and requirements for reticle inspection. As such, we developed the Teron 640 with our latest Dual Imaging mode inspection technique which utilizes the combination of high sensitivity, high resolution inspection followed with aerial imaging and innovative physics based defect dispositioning. These techniques maximize usable sensitivity on mask (including finding new sources of defects in high MEEF regions) while reducing the burden for offline disposition.

KLA-Tencor is also in the process of releasing a Reticle Decision Center which will add further operational efficiency to mask manufacturing operations, offering inline concurrent automated defect classification for the Teron platform and other options to analyze defects offline from other systems in the mask house. These new technologies will enable mask shops to handle the latest generation masking technologies and improve operational efficiency.

Inverse lithography – As device geometries continue to shrink, the number of process steps increase to maintain quality and high yields. These factors increase costs and affect production timetables. Can you explain the key advantages of inverse lithography in silicon device manufacturing and what tools customers need to maximize performance and reduce time to market?

A With EUV delays, ArF immersion lithography is being pushed further into technology nodes beyond its resolution limits, and as such it is constantly working at the edge of its operating window. Depth of focus budgets continue to shrink as the scanners operate at the limits of Low K1 lithography. One of the OPC techniques available to lithographers is Inverse Lithography Techniques (ILT), which provides more process latitude and helps achieve a common process window for the different regions of the exposure field. The challenge is that optimizing a full device/exposure field for ILT can take days to optimize even on the largest OPC computing clusters due to the complex calculations and modeling factors.

Furthermore, the write times for a mask using current technologies would go from 8-10 hours to multiple days. For layers where a common process window cannot be achieved, layers may need to be further split from two patterning layers with etch steps to three patterning steps and three etch steps (3P3E), further impacting device cycle times and device economics.

As an alternative to full field, ILT may be used in the most critical regions of the exposure field. In doing so, there needs to be accurate models for OPC verification and potentially mask verification tools to ensure that a common process window can be achieved with the proposed differing OPC solutions within the field. To further optimize the use of ILT, the race is on to develop multi-beam technology for mask writing to enable the ideal freeform shapes coming from the OPC models in a more manageable cycle time.

5D Patterning Control Solution – Quality control is becoming an especially crucial consideration for manufacturers including defect detection and being able to feed data forward/backwards to improve future wafer lots as well as correct deficiencies of lots in process. How does KLA-Tencor's approach deliver superior results and otherwise positively affect manufacturing?

A At KLA-Tencor, we see the challenge of quality control (QC) to require a two-step solution. The first step is to try and deliver the most capable point products for each application, such as macro inspection or film thickness measurement. The second step is to then harness the data from those point QC products alongside with information from the tools doing the processing to try and create higher order QC in the fab.

KLA-Tencor's 5D solution is our product offering which is the second step in the solution. 5D seeks to provide the best on-product-overlay (OPO), CD uniformity (CDU), and ultimately edge placement error (EPE) by providing lithography control and reducing variability in all areas of the fab. The 5D product is not limited to data streams from KLA-Tencor's products, but is an open architecture that can take data from QC products by other suppliers and can create correctibles for process equipment such as lithography, etch and deposition tools.

For example, by combining WaferSight PWG patterned wafer geometry systems with Archer overlay metrology systems and 5D Analyzer data analysis and patterning control, KLA-Tencor's stress induced overlay solution has demonstrated reduced OPO and lithography COO.

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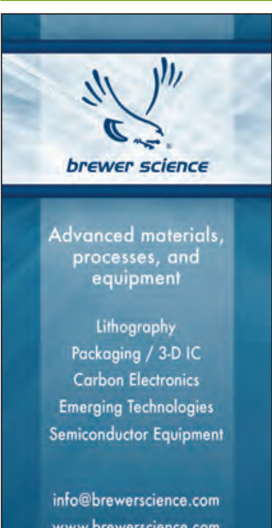

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