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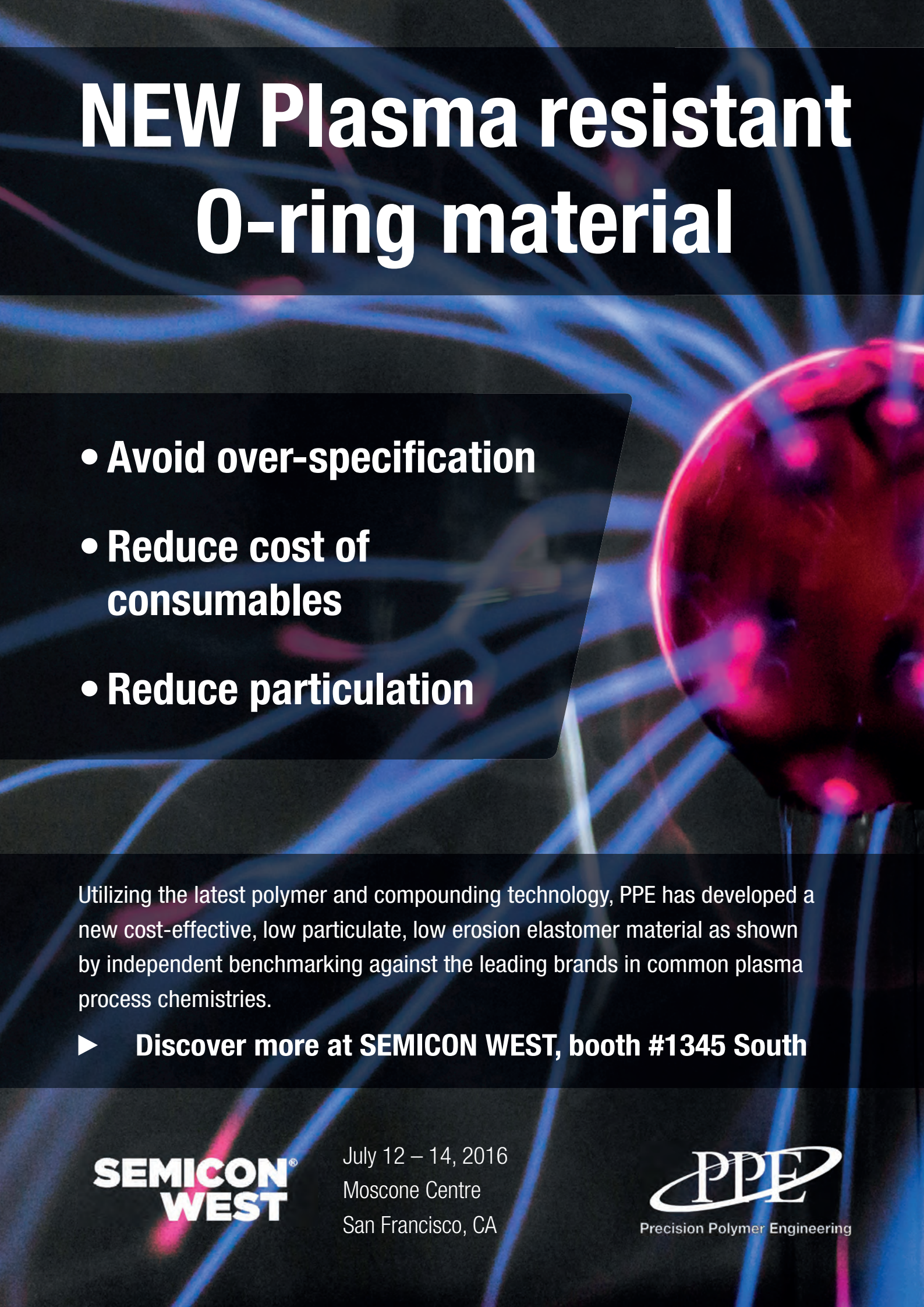

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PPE
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editor'sview

by Jackie Cannon, Editor

The never ending story

INDUSTRIAL SEMICONDUCTOR revenues rose slightly in 2015 despite weakness in the overall semiconductor industry and, in particular, economic headwinds in China, which is a major global consumer of industrial chips. Year-over-year global industrial semiconductor revenue rose less than 1 percent in 2015 to reach $41.9 billion. This slight revenue increase in 2015 follows solid growth of 11.5 percent in 2014 and 9.8 percent in 2013, according to IHS Inc.,

When industry starts speaking of slight revenue increases we are entering a phase of caution and low risk moves. For manufacturers the means that the stakes are getting higher and it is harder to make an educated guess about whether a new idea might be truly beneficial, or, so complex that any benefit it delivers is too costly in terms of time, materials, hard cash or all three.

Recently the features I have reviewed have reflected the cautious mood with the focus on yield, managing uptime and safeguarding the bottom line. As we approach SEMICON West the mood is sober and it will be interesting to see if this is reflected on the hall floors.

However the silicon semiconductor industry is both enduring and contradictory. While it is consolidating it is simultaneously expanding. For every growth spurt in the industry – be it from chasing a market or a market segment, to innovations that have become commoditised – the number of semiconductor companies grow. Then when markets change, some companies suffer revenue hits others plateau and shareholders force a sale. This ebb and flow is a tale as old as time.

The million dollar question is what comes next? There will inevitably be new markets and devices that will drive a new growth spurt. The IoT is the dark horse, but I doubt the only one.

See you in San Francisco.

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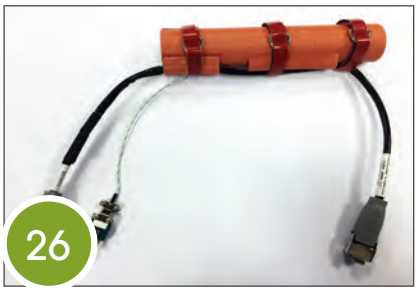


Imec and Holst present multi-standard low-power wide-area radio chip

NANOELECTRONICS research centres imec and Holst Centre (set up by imec and TNO), presented a low-power wide-area (LPWA) multi-standard radio chip at imec's annual technology forum in Brussels (ITF Brussels 2016). The new radio chip can operate with a lower level of power consumption than any other radio chip technology released to date for long range connectivity in sensor networks. The sub-GHz radio chip's technology can serve a multitude of protocols including IEEE 802.15.4g/k, W-MBUS, KNX-RF, as well as the popular LoRa and SIGFOX networks, and future cellular IoT for applications such as smart metering, smart home, smart city and critical infrastructure monitoring.

The radio chip operates in industrial, scientific, medical (ISM) and short-range devices (SRD) bands, covering a frequency range from 780 MHz to 930 MHz. The robust, low-power design combines a large link budget, with state-of-the-art interference rejection and lowest bill of materials by minimizing external components as compared to of-the-shelf available chips. The radio is implemented as a complete System-on-Chip (SoC) including the RF front end, power management, an ARM processor, 160 kBytes of SRAM and peripherals like SPI, I2C and UART. It features a targeted sensitivity of -120dBm at 0.1 percent BER (1kbps) and ultra-low power consumption of 8mW (Rx) and 113mW (Tx) for 13.5dBm output power. The receiver supports a wide gain range to handle input signals from -120dBm to -15dBm, corresponding to a large dynamic range of 105dB. The PA features automatic ramp-up and ramp-down for ARIB spectral mask compliancy.

Furthermore, the output power is controllable from <-40dBm up to 15dBm. "With the foreseen release of the NB-IoT protocol in June 2016 by the 3GPP, it is clear that protocols such as NB-IoT, SigFox and LoRA are here to stay for the coming years," stated Kathleen Philips, program director perceptive systems at imec/Holst Centre. "Our novel sub-GHz radio chip can serve multiple of these protocols and is an ideal solution for long-range wireless connectivity for IoT applications."

Imec's Industrial Affiliation program on the Intuitive Internet-of-Things (IoT) focuses on developing the building blocks for the future. The program explores an intuitive IoT, with sensor systems that can detect and assist with the needs and wants of people in an unobtrusive way, and can take into account their varied perspectives and surrounding environment.

Along with low-power radio chips, imec also develops ultra-small, low-cost, intelligent, and ultra–low power sensors and heterogeneous sensor networks. Interested companies are invited to partner with imec on its varied research initiatives. Companies can also connect with imec to request access to imec's technological advances to further develop their projects through licensing programs with imec.

Tessera goes legal with Broadcom for patent infringement

TESSERA TECHNOLOGIES has announced that it and certain of its subsidiaries filed legal proceedings for patent infringement in both domestic and international jurisdictions against Broadcom and, in some cases, against certain of Broadcom's customers and distributors.

The proceedings are in the United States International Trade Commission, the U.S. District Court for the District of Delaware, and courts in Germany and the Netherlands, alleging infringement of a total of eight patents.

Tessera first reached out to Broadcom several years ago to explore technical collaboration on semiconductor technology development, and subsequently to discuss licensing Tessera's intellectual property. Following a series of in-depth licensing discussions, the parties were unable to reach a licensing arrangement.

"Today's actions were not taken lightly and are made only after years of effort to reach a fair and equitable resolution without litigation," said Tom Lacey, CEO of Tessera. "At this point, we believe that litigation is necessary to defend our intellectual property rights. As we have said in connection with other legal matters, we remain willing to negotiate a resolution that fairly compensates Tessera and its shareholders for our valuable

intellectual property. However, we are also fully prepared to proceed through the entirety of the legal process, and we remain very confident in our ability to achieve a positive outcome."

Broadcom is not an existing Tessera customer, and as such the proceedings announced today do not impact Tessera's second quarter revenue or earnings per share guidance or 2016 full-year revenue guidance. The Company expects 2016 litigation expense will remain within its current target operating model based on anticipated case activity for the remainder of the year.

Imec expands silicon platform for quantum computing applications

AT THE QUANTUM EUROPE CONFERENCE, Belgian's nanoelectroninc research centre imec announced that it is ramping-up its R&D activities focused on quantum computing.

Imec will implement qubits and supporting nanoelectronic functionality for quantum computing, leveraging its advanced silicon platform that was established within the framework of its industrial affiliation program with additional support from the EU through e.g. ECSEL projects SENATE and TAKE-5.

Widely seen as a possible solution to complex computing problems which are intractable on classical computers, quantum computing uses quantum physics to create and manipulate quantum states within electronic devices (qubits) to enhance the performance over that of existing, 'classical' approaches.

Of the many device proposals for qubit implementation, the ones compatible with existing silicon technology will provide the most viable solution for interfacing with the outside world.

The goal of imec's initiative is to establish a bridge between the most advanced transistor technology and emerging quantum technology options, representing a natural extension of imec's silicon platform. This will ensure routes to demonstrate the quantum computing functionality compatible with industries' platform technologies.

Assuming a key position in the quantum technologies ecosystem, imec will support the transition of new quantum technologies, from the physics lab to technology feed into the supply chain. Imec's platform will help translate laboratory demonstrators into commercial products. It will be open for universities, SMEs and industrial partners of imec's quantum technologies programs.

"The coming decades will be characterized by a wave of quantum technology based applications, ranging from communication, simulation and sensing, to computation. However, to enable this, the industry will need technical support to adopt and to integrate these new technologies into products and services", stated Jo De Boeck, CTO at imec. "Imec's industry relevant silicon platform for the advanced technology nodes, is currently used to screen technology options for the 5 nm nodes and beyond.
The same platform is hence the ideal basis to start implementing quantum devices as quantum effects are becoming the starting point of developing a quantum platform."

Fairchild launches new discrete and bare Die IGBTs

FAIRCHILD supplier of high-performance semiconductor solutions, is expanding its growing portfolio of automotive-grade semiconductor solutions for hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV) and electric vehicles (EV) with its new discrete and bare die IGBTs and diodes. These IGBTs and diodes are ideal for traction inverters, a core component of all HEVs, PHEVs and EVs that convert the batteries' electricity from direct current into the three-phase alternating current required by the vehicles' drive motors.

All of these new discrete and bare die IGBTs and diodes use advanced third generation Field Stop Trench IGBT technology and a soft fast recovery diode qualified to automotive-grade standards and have additional features and options. The combination of these technologies, features and options enables Fairchild to provide products with a very tight parametric distribution for both discrete and bare die solutions.

"Our new discrete and bare die IGBTs and diodes are compelling options for automakers and their suppliers that require performance, reliability and flexibility to build the traction inverters best suited to their specific requirements," said Sergio Fissore, Vice President and General Manager of the Automotive Business Unit at Fairchild. Fairchild's new FGY160T65SPD_F085 and FGY120T65SPD_F085 discrete IGBTs are suited to traction inverters and other HEV/PHEV/EV powertrain components that require high power density and high reliability.

"An additional enhancement to their robustness is extra screening at final testing that addresses the specific needs of traction inverters applications and is applied to 100 percent finished goods," explained Fabio Necco, Director of the H/EV product line at Fairchild. "Along with a best-in-class 650 V breakdown voltage, which is 50 V higher than existing solutions, this extra step provides further protection against electrical overstress."

Complementing their performance and reliability is the flexibility these discrete IGBTs give designers to customize their products. Designers can simply add IGBTs in parallel to achieve the required system power rating, while also improving the overall efficiency of their traction inverter or other powertrain component designs.

Fairchild is also announcing availability of its PCGA200T65NF8, PCRKA20065F8, PCGA300T65DF8, and PCRKA30065F8 bare die IGBTs and diodes for automakers and automotive parts suppliers building their own power modules for high-performance traction inverters and other motor-driving components.

The bare die IGBTs are also available with integrated monolithic current sense and temperature sense to provide additional levels of protection. The bare die IGBTs can be customized to meet special requirements. Options include changing the gate pad size and location to accommodate different diameters of aluminium wire, resizing the die, and customizing the breakdown voltage and other electrical parameters. A solderable top metal version is also available and is designed for advanced wire bondless assembly technologies such as soldering technologies as sintering.

Fairchild is also expanding its portfolio with a new automotive-grade module currently in development, which integrates IGBTs, freewheeling diodes and gate drivers in one electrically-isolated package. It is ideal for auxiliary motor control applications such as oil pumps and A/C compressors and it is the smallest solution in the market, simplifying the power stage design, assembly and improving the EMI performance. The power module is sampling now and will be available in production quantity in June.

Synopsys launches pre-wafer simulation solution

SYNOPSYS has announced a pre-wafer simulation solution to help semiconductor manufacturers reduce process node development time. The new solution provides a comprehensive process, transistor and circuit simulation flow that enables technology development and design teams to evaluate various transistor and process options using a design technology co-optimization methodology that starts in the pre-wafer research phase. The generation of SPICE models, design rules and parasitics from TCAD and lithography simulations allow the creation of early process design kits to evaluate the performance, power, area and cost of a new process node.

"To meet the performance, power, area and cost targets of the 10-nm process node and beyond, semiconductor manufacturers need to evaluate a larger number of process options, device architectures and materials, and account for design criteria in selecting the best options," said Dr. Anda Mocuta, Director of Technology Solutions and Enablement at imec. "The new simulation solution from Synopsys enables seamless links in the DTCO chain and helps speed up the down-selection of technology options," added Dr. Mocuta.

Rudolph adds high-speed 3D metrology to the NSX Series

RUDOLPH TECHNOLOGIES has announced the availability of new, high-speed 3D metrology on its flagship NSX Series, a highly-flexible inspection and measurement platform for process development and control of die-level interconnects.

Already in use by multiple customers worldwide, the NSX Series with high-speed 3D metrology is capable of both high-volume production monitoring and advanced process development.

"The new capability provides a 200-400 percent throughput improvement over our previous Wafer Scanner bump metrology system, and when paired with our Discover Software, provides a complete coplanarity solution for our customers," said Scott Balak, Rudolph's director, inspection product management. "With the increasing number of new packaging technologies being developed by foundries, outsourced assembly and test (OSAT) manufacturers, and integrated device manufacturers (IDMs), the flexibility and reliability of this new capability on the trusted NSX Series platform is especially valuable to customers seeking to move rapidly from pilot lines to production."

Data is collected in seconds from millions of bumps and then analyzed by Rudolph's Discover Software analysis database. Engineers gain unique insight into critical metrology applications, from both an individual bump point of view or holistically as a wafer, as part of a simultaneous product and process control solution.

"Manufacturers are looking for a more comprehensive and flexible process control solution that provides, not only inspection or bump data, but also usable analytical information about their processes," said Mike Goodrich, vice president and general manager of Rudolph's Process Control Group. "Our powerful Discover analysis software provides insight into the process that is otherwise unavailable to process control tool owners.

The high-speed 3D bump metrology capability incorporates a three segment optical range, giving our customers the flexibility to control both smaller micro bumps and larger traditional solder bumps with a single inspection and metrology platform. When combined with Rudolph's advanced automation capability, customers can measure thin and warped wafers without the extra expense of frame and tape mounting."

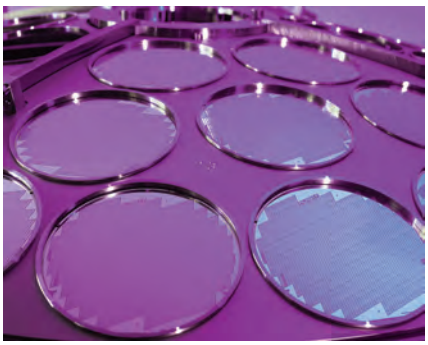
Goodrich concluded, "We understand the importance of 3DIC and next-generation packaging processes and we have aggressively pursued development of this comprehensive 3D coplanarity solution to meet our customers' needs for a cost efficient, multi-functional process control tool."

Fujitsu boosts efficiency of manufacturing with collaboration with Intel

FUJITSU LIMITED has announced that it has with Intel Corporation carried out a field trial to visualize manufacturing processes at Shimane Fujitsu Limited, which primarily manufactures notebook PCs. The field trial linked the FUJITSU Cloud Service IoT Platform with the Intel IoT Gateway. As a result of this trial, the companies were able to rationalize functionality testing and repair processes on Shimane Fujitsu's manufacturing line, and in line with this, cut additional shipping costs that resulted from delays by 30 percent. The trial was a part of the IoT collaboration with Intel, launched in May 2015.

Going forward, Fujitsu will further strengthen its collaboration with Intel in the IoT field, creating new solutions and making them available to customers.

EV Group receives multiple orders for fusion bonder



EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets has announced that it has received multiple orders for its GEMINI FB XT automated fusion wafer bonders from multiple leading device manufacturers.

The GEMINI FB XT offers industry leading wafer-to-wafer alignment accuracy, customizable pre- and post-processing configurations with faster handling and improved process flows that increase throughput by up to 50 percent compared to the previous-generation platform, as well as integrated metrology to maximize yields and productivity in high-volume manufacturing (HVM).

These latest orders for the GEMINI FB XT system will support several leading-edge HVM applications, including 3D stacked image sensors, memory stacking, and die partitioning for next-generation 3D system-on-chip (SoC) devices.

Vertical stacking of devices has become an increasingly viable approach to driving continuous improvements in device density and performance without the need for increasingly costly and complex lithography processing.

Wafer-to-wafer bonding is an essential process step to enable 3D stacked devices. However, tight alignment and overlay accuracy between the wafers is required to achieve good electrical contact between the interconnected devices on the bonded wafers, as well as to minimize the interconnect area at the bond interface so that more space can be made available on the wafer for producing devices.

Leveraging EVG's XT Frame platform and an equipment front-end module (EFEM), the GEMINI FB XT automated production fusion bonding system is optimized for ultra-high throughput and productivity. It incorporates EVG's proprietary SmartView NT face-to-face aligner to achieve wafer-to-wafer overlay alignment accuracy below 200 nm (3 sigma), which leads the industry in performance and is essential to enabling 3D integration.

In addition, the system can accommodate up to six pre-and post-processing modules for surface preparation, conditioning and metrology steps such as wafer cleaning, plasma activation, alignment verification, debonding (allowing pre-bonded wafers to be separated automatically and re-processed if necessary) and thermo-compression bonding. This enables the GEMINI FB XT to support fully automated and integrated wafer loading, alignment, bonding and unloading of bonded wafers in HVM environments.

AMICRA to deliver bonder to Asia

AMICRA MICROTECHNOLOGIES, a German-based vendor of advanced back-end processing equipment for advanced packaging applications, has received a significant order for its NOVA FanOut Large-Panel Die/Flip-Chip Bonder from a large Asian subcontractor located in Taiwan. The AMICRA NOVA FanOut, to be delivered in July 2016, will be part of a large panel pilot manufacturing line.

AMICRA's top-class NOVA FanOut Die/Flip Chip Bonder is laid out for a number of advanced applications such as WLP, MCP, SiP, PoP, eWLB and embedded-die placement tasks. It supports an extremely large 600 mm x 550 mm bonding area and offers a placement accuracy of +3.0 μm at 3 Sigma.

The NOVA FanOut is based on AMICRA's proven dual-head NOVA Plus Die-attach and Flip-chip Placement system introduced in 2010. NOVA FanOut enables its users continuous high-speed processing at a very low cycle time of <3 sec. Auto-loading is provided for wafers up to 300 mm diameter and up to 450 mm substrate wafers, as well as the 550 mm x 600 mm substrate working area.

Among the special features of the NOVA FanOut are its software options to optimize the placement accuracy according to the user's front-end equipment. Its unique dynamic alignment system ensures repeatable placement accuracy while automatically compensating for environmental changes during operation. Additionally, the NOVA FanOut supports heated options for advanced fan-out processes.

Another advanced AMICRA product is the ultra-high-precision AFC Plus Bonding System, which realizes a placement accuracy of +0.5 μm at 3 Sigma for die and flip-chip attach. At a cycle time of <30 sec, it is well suited for processing micro-optic and micro-mechanic components, with eutectic bonding via diode laser or heating plate. AMICRA also offers the fully automated, high-speed wafer inking system AIS, and the semi-automatic wafer inking system SIS. In 2015, AMICRA introduced its fully automated, high-speed precision dispensing system HDS, offered in a quad- or dual-headed configuration to support underfill, glob-top, general dispensing applications and more.

Commenting on this latest purchase order for the NOVA FanOut Large-Panel Bonding System, Johann Weinhaendler, Managing Director of AMICRA Microtechnologies GmbH, stated: "With its large substrate area to accommodate a 550 mm x 600 mm panel in an inline conveyor system and its best placement accuracy of 3 μm, the NOVA FanOut provides an optimum die-bonding solution for the fan-out process. This will substantially solidify our innovative position and commitment to the fan-out market."

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Okmetic introduce enhanced SOI wafer

OKMETIC has introduced an enhanced SOI wafer (E-SOI) into its SOI product family (Silicon-On-Insulator).

The company believes that because of its new level of layer thickness uniformity and unprecedented properties E-SOI is an ideal platform for applications such as HV BCD devices, silicon photonics and high-precision silicon-based MEMS sensors.

"The device layer thickness of E-SOI is freely adjustable between 1.0 μm and >100 μm and the thickness tolerance independent of target thickness is as low as +/-0.1 μm. With the wide selection of silicon starting materials from Okmetic's in -house crystal growth, and similar flexibility in wafer customization as Okmetic BSOI wafers, the E-SOI technology provides an ideal wafer solution to both semiconductor and sensor applications", describes Senior Development Manager, Technology Jari Mäkinen, who was the leader of the development project.

Okmetic's SOI (Silicon-On-Insulator) wafers are manufactured by bonding technology. Two silicon wafers are bonded together, having an insulating oxide between. In a typical application sensing elements and possible IC devices are built on the active layer. Buried oxide is an effective etch-stop, and can also act as a sacrificial layer. Handle wafer is supporting the structure but it can also be utilized in sealing the structure or as part of the sensing element. In addition to E-SOI, Okmetic's SOI family includes Bonded SOI (BSOI) and Cavity SOI (C-SOI) wafers.

"Okmetic's strategic focus is on high-performance wafers for the manufacture of sensors, discrete semiconductors and analog circuits. E-SOI complements Okmetic's wide product selection perfectly and provides our customers an ideal platform for the manufacture of high-end devices", concludes Anna-Riikka Vuorikari -Antikainen, Okmetic's Senior Vice President, Customers and Markets.

ClassOne completes new funding round

CLASSONE TECHNOLOGY, manufacturer of electroplating systems for MEMS, sensors, LEDs, opto-electronics, and RF substrates, has announced the completion of a major new round of funding from Salem Investment Partners of Winston-Salem, North Carolina.

"It's evident that 2016 will be another significant growth year for ClassOne Technology," said Byron Exarcos, CEO of ClassOne. "With this new funding we will fill order backlogs and address a forecast that is strong and rapidly increasing. This surge in business is coming from the many emerging markets that build products on 200 mm and smaller substrates. These users are looking for advanced plating performance at an affordable price - and that's precisely what Solstice systems are designed for. As a result, more and more of these companies are ordering our tools. And that now includes many of the top-tier manufacturers from around the world. We're delighted to see the exceptional and sustained growth that ClassOne Technology is achieving across the US, Europe and Asia," said Meredith Jolly, vice president at Salem Investment Partners.. "It's even more remarkable given that the company just introduced the Solstice system two years ago. It's great to be on a winning team and to be able to contribute to their success."

ClassOne's Solstice electroplating line is designed specifically for ≤200mm wafer processing, Solstice tools are available in three different models and can electroplate a range of metals and alloys, either on transparent or opaque substrates. The company also just announced their Plating-Plus capability which allows Solstice to perform additional processing - such as Metal Lift-Off, Resist Strip and UBM Etch - along with plating on one tool.

SUSS MicroTec launches operator-assisted surface laser imagers

SUSS MicroTec, a global supplier of equipment and process solutions for the semiconductor industry, has launched the LI Series - a new surface laser Imaging platform as pre- announced on May 4, 2016.

The technology of the LI for laser surface processing ranges from sub micrometric pattering of resist coated substrates to micro- ablation, photo-chemistry treatment as well as metrology.

The patterns, defined by a CAD process, are transferred by accurately moving the targeted substrates underneath a focused and scanning laser beam. In addition, the Laser Imager configuration is highly customizable, to best fit the specific requirements of each user.

The technology supports substrate sizes from small pieces up to 300 mm, and it reaches a resolution down to 0.8 μm. Multi-layer alignment is possible via both top and bottom side alignment optical systems.

Beside the 405 nm GaN laser for standard thin resist lithography processes, a second laser source can also be added to additionally address diverse processes such as, among other, thick resists like SU8, and infrared sensitive materials.

The company claims the core advantage of the laser imager is its flexibility, making it suitable for the various requirements of academic and industrial R&D facilities.

The main applications include a wide variety of nano- and 3D structuring for high resolution wafer lithography, micro-optical components, sensors, microfluidic devices, and photo mask manufacturing.

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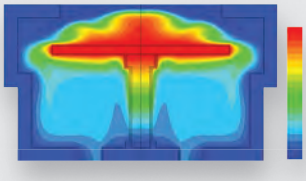

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Silicon chip with integrated laser: Light from a nanowire

Physicists at the Technical University of Munich (TUM) have developed a nanolaser, a thousand times thinner than a human hair. Thanks to an ingenious process, the nanowire lasers grow right on a silicon chip, making it possible to produce high-performance photonic components cost-effectively. This will pave the way for fast and efficient data processing with light in the future.

EVER SMALLER, ever faster, ever cheaper – since the start of the computer age the performance of processors has doubled on average every 18 months. 50 years ago already, Intel co-founder Gordon E. Moore prognosticated this astonishing growth in performance. And Moore's law seems to hold true to this day.

But the miniaturization of electronics is now reaching its physical limits. "Today already, transistors are merely a few nanometers in size. Further reductions are horrendously expensive," says Professor Jonathan Finley, Director of the Walter Schottky Institute at TUM. "Improving performance is achievable only by replacing electrons with photons, i.e. particles of light."

Photonics – the silver bullet of miniaturization

Data transmission and processing with light has the potential of breaking the barriers of current electronics. In fact, the first silicon-based photonics chips already exist. However, the sources of light for the transmission of data must be attached to the silicon in complicated and elaborate manufacturing processes. Researchers around the world are thus searching for alternative approaches.

Only once the wires protrude beyond the mirror surface they may grow laterally – until the semiconductor is thick enough to allow photons to jet back and forth to allow stimulated emission and lasing

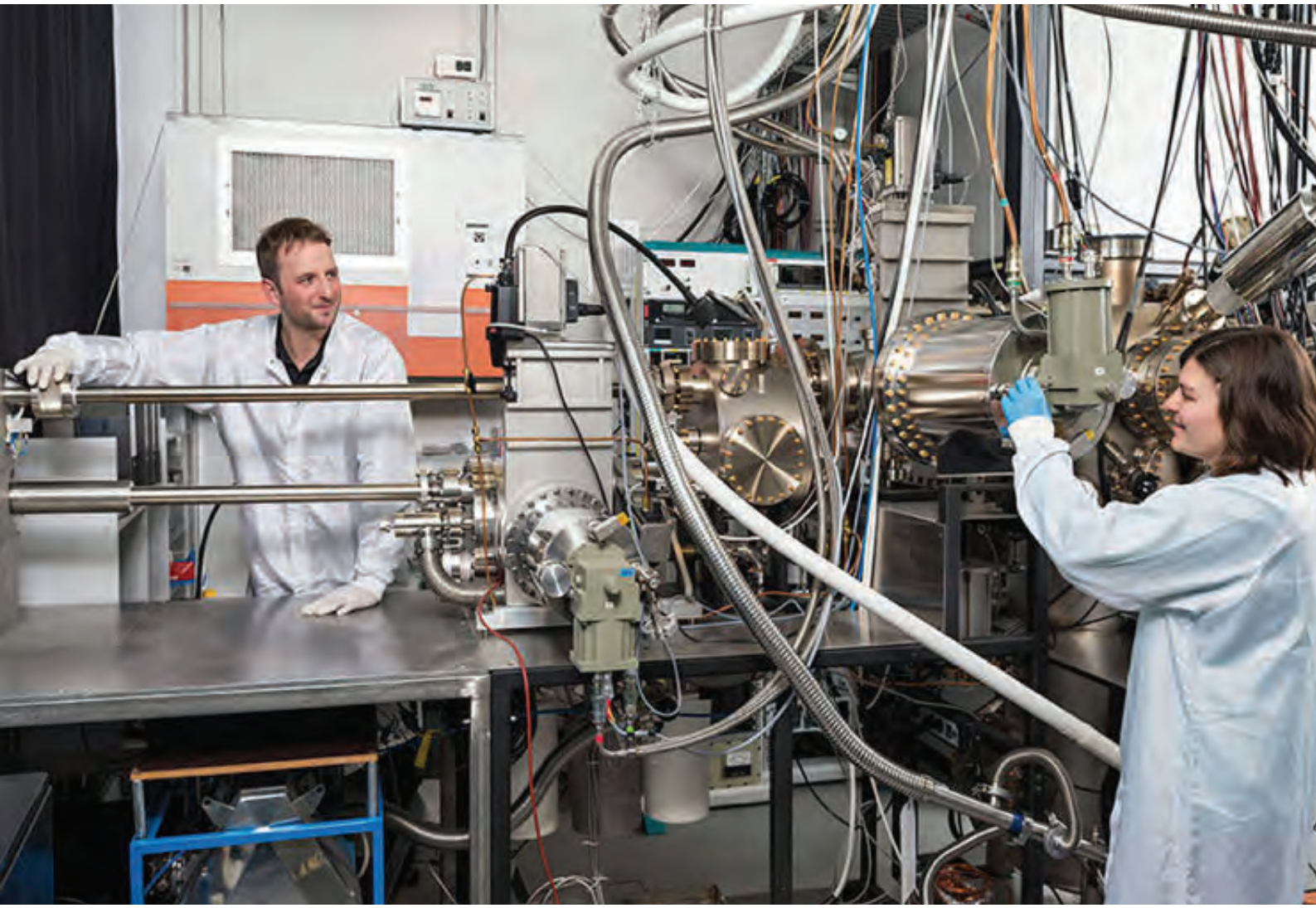
Scientists at the TU Munich have now succeeded in this endeavor: Dr. Gregor Koblmüller at the Department of Semiconductor Quantum-Nanosystems has, in collaboration with Jonathan Finley, developed a process to deposit nanolasers directly onto silicon chips. A patent for the technology is pending. Growing a III-V semiconductor onto silicon requires tenacious experimentation. "The two materials have different lattice parameters and different coefficients of thermal expansion. This leads to strain," explains Koblmüller. "For example, conventional planar growth of gallium arsenide onto a silicon surface results therefore in a large number of defects."

The TUM team solved this problem in an ingenious way: By depositing nanowires that are freestanding on silicon their footprints are merely a few square nanometers. The scientists could thus preclude the emerging of defects in the GaAs material.

Atom by atom to a nanowire

But how do you turn a nanowire into a vertical-cavity laser? To generate coherent light, photons must be reflected at the top and bottom ends of the wire, thereby amplifying the light until it reaches the desired threshold for lasing.

To fulfil these conditions, the researchers had to develop a simple, yet sophisticated solution: "The interface between gallium arsenide and silicon does not reflect light sufficiently. We thus built in an additional mirror – a 200 nanometer thick silicon oxide layer that we evaporated onto the silicon," explains Benedikt Mayer, doctoral candidate in the team led by Koblmüller and Finley. "Tiny holes can then be etched into the mirror layer. Using epitaxy, the semiconductor



Benedikt Mayer and Lisa Janker at the epitaxy facility at the Walter Schottky Institute, TU Munich – Photo: Uli Benz / TUM

nanowires can then be grown atom for atom out of these holes."

Only once the wires protrude beyond the mirror surface they may grow laterally – until the semiconductor is thick enough to allow photons to jet back and forth to allow stimulated emission and lasing. "This process is very elegant because it allows us to position the nanowire lasers directly also onto waveguides in the silicon chip," says Koblmüller.

Basic research on the path to applications

Currently, the new gallium arsenide nanowire lasers produce infrared light at a predefined wavelength and under pulsed excitation. "In the future we want to modify the emission wavelength and other laser parameters to better control temperature stability and light propagation under continuous excitation within the silicon chips," adds Finley. The team has just published its first successes in this direction. And they have set their sights firmly on their next goal: "We want to create an electric interface so that we can operate the nanowires under electrical injection instead of relying on external lasers," explains Koblmüller.

"The work is an important prerequisite for the development of high-performance optical components in future computers," sums up Finley. "We were able to demonstrate that manufacturing silicon chips with integrated nanowire lasers is possible."

The research was funded by the German Research Foundation (DFG) through the TUM Institute for Advanced Study, the Excellence Cluster Nanosystems Initiative Munich (NIM) and the International Graduate School of Science and Engineering (IGSSE) of the TUM, as well as by IBM through an international postgraduate program.

Quantum dot solids: this generation's silicon wafer?

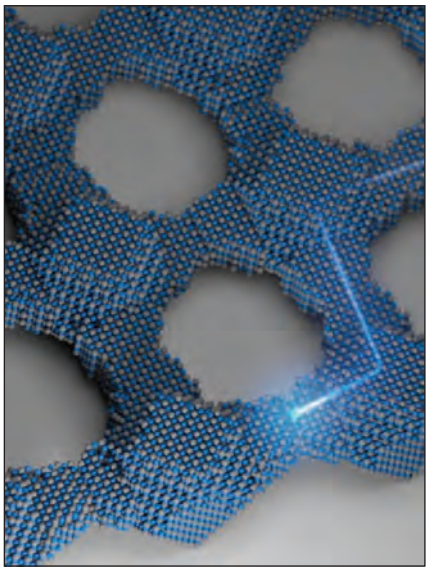
Connecting the dots: Playing 'LEGO' at the atomic scale to build atomically coherent quantum dot solids.

JUST AS the single-crystal silicon wafer forever changed the nature of communication 60 years ago, a group of Cornell researchers is hoping its work with quantum dot solids – crystals made out of crystals – can help usher in a new era in electronics.

The team, led by Tobias Hanrath, associate professor in the Robert Frederick Smith School of Chemical and Biomolecular Engineering, and graduate student Kevin Whitham, has fashioned two-dimensional superstructures out of single-crystal building blocks. Through a pair of chemical processes, the lead-selenium nanocrystals are synthesized into larger crystals, then fused together to form atomically coherent square superlattices.

The difference between these and previous crystalline structures is the atomic coherence of each 5-nanometer crystal (a nanometer is one-billionth of a meter). They're not connected by a substance between each crystal – they're connected to each other. The electrical properties of these superstructures potentially are superior to existing semiconductor nanocrystals, with anticipated applications in energy absorption and light emission.
"As far as level of perfection, in terms of making the building blocks and connecting them into these superstructures, that is probably as far as you can push it," Hanrath said, referring to the atomic-scale precision of the process.

The Hanrath group's paper, "Charge transport and localization in atomically coherent quantum dot solids," is published in this month's issue of Nature Materials.



Credit: Kevin Whitham, Cornell University.

This latest work has grown out of previous published research by the Hanrath group, including a 2013 paper published in Nano Letters that reported a new approach to connecting quantum dots through controlled displacement of a connector molecule, called a ligand. That paper referred to "connecting the dots" – i.e. electronically coupling each quantum dot – as being one of the most persistent hurdles to be overcome. That barrier seems to have been cleared with this new research. The strong coupling of the nanocrystals leads to formation of energy bands that can be manipulated based on the crystals' makeup, and could be the first step toward discovering and developing other artificial materials with controllable electronic structure.

Still, Whitham said, more work must be done to bring the group's work from the lab to society. The structure of the Hanrath group's superlattice, while superior to ligand-connected nanocrystal solids, still has multiple sources of disorder due to the fact that all nanocrystals are not identical. This creates defects, which limit electron wave function.

"I see this paper as sort of a challenge for other researchers to take this to another level," Whitham said. "This is as far as we know how to push it now, but if someone were to come up with some technology, some chemistry, to provide another leap forward, this is sort of challenging other people to say, 'How can we do this better?'"

Hanrath said the discovery can be viewed in one of two ways, depending on whether you see the glass as half empty or half full.

"It's the equivalent of saying, 'Now we've made a really large single-crystal wafer of silicon, and you can do good things with it,'" he said, referencing the game-changing communications discovery of the 1950s. "That's the good part, but the potentially bad part of it is, we now have a better understanding that if you wanted to improve on our results, those challenges are going to be really, really difficult."

This work made use of the Cornell Centre for Materials Research, which is supported by the National Science Foundation through its Materials Research Science and Engineering Centre program. X-ray scattering was conducted at the Cornell High Energy Synchrotron Source, which is supported by the NSF and the National Institutes of Health.

Researchers engineer a first in flexible electronics

New thin-film transistor could pave the way for pliable devices.

AN ENGINEERING RESEARCH TEAM at the University of Alberta has invented a new transistor that could revolutionize thin-film electronic devices.

Their findings, published in the leading science journal Nature Communications, could open the door to the development of flexible electronic devices with wide-ranging applications, from display technology to medical imaging and renewable energy production.

The team was exploring new uses for thin film transistors (TFT), which are most commonly found in low-power, low-frequency devices like the display screen you're reading from now. Efforts by researchers and the consumer electronics industry to improve the performance of the transistors have been slowed by the challenges of developing new materials or slowly improving existing ones for use in traditional thin film transistor architecture, known technically as the metal oxide semiconductor field effect transistor (MOSFET).

But the U of A electrical engineering team found an ingenious workaround on the problem. Instead of developing new materials, the researchers improved performance by designing a new transistor architecture that takes advantage of a bipolar action.

In other words, instead of using one type of charge carrier, as most thin film transistors do, it uses electrons and the absence of electrons (referred to as "holes") to contribute to electrical output. Their first breakthrough was forming an "inversion" hole layer in a "wide-bandgap" semiconductor, which has been a great challenge in the solid-state electronics field.

Once this was achieved, "we were able to construct a unique combination of semiconductor and insulating layers that allowed us to inject 'holes' at the MOS interface," said Gem Shoute, a PhD student in the Department of Electrical and Computer Engineering who is lead author on the article.

Adding holes at the interface increased the chances of an electron "tunnelling" across a dielectric barrier. Through this phenomenon, a type of quantum tunnelling, "we were finally able to achieve a transistor that behaves like a bipolar transistor."

"It's actually the best-performing [TFT] device of its kind—ever," said materials engineering professor Ken Cadien, a co-author on the paper. "This kind of device is normally limited by the non-crystalline nature of the material that they are made of."

The dimensions of the device itself can be scaled with ease to improve performance and keep up with the need for miniaturization—an advantage that modern TFTs lack. The transistor also has power-handling capabilities at least 10 times greater than commercially produced thin film transistors.

Electrical engineering professor Doug Barlage, who is Shoute's PhD supervisor and one of the paper's lead authors, says his group was determined to try new approaches and break new ground. He says the team members knew they could produce a high-power thin film transistor—it was just a matter of finding out how.

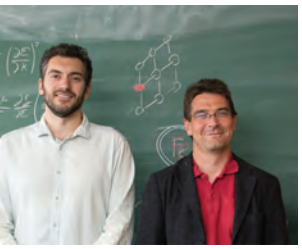
"Our goal was to make a thin film transistor with the highest power handling and switching speed possible. Not many people want to look into that, but the raw properties of the film indicated dramatic performance increase was within reach," he said. "The high quality sub-30-nanometre [a human hair is 50,000 nanometres wide] layers of materials produced by Professor Cadien's group enabled us to successfully try these difficult concepts."

In the end, the team took advantage of the very phenomena other researchers considered roadblocks. "Usually tunnelling current is considered a bad thing in MOSFETs and it contributes to unnecessary loss of power, which manifests as heat," explained Shoute. "What we've done is build a transistor that considers tunnelling current a benefit."

The team has filed a provisional patent on the transistor. Shoute says the next step is to put the transistor to work "in a fully flexible medium and apply these devices to areas like biomedical imaging, or renewable energy."

Gigantic ultrafast spin currents

SCIENTISTS from TU Wien (Vienna) are proposing a new method for creating extremely strong spin currents. They are essential for spintronics, a technology that could replace today's electronics.



Marco Battiato (l) and Karsten Held (r)

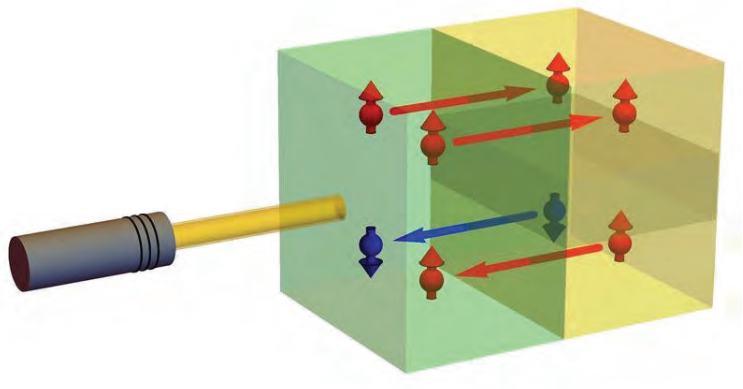
IN OUR COMPUTER CHIPS, information is transported in form of electrical charge. Electrons or other charge carriers have to be moved from one place to another. For years scientists have been working on elements that take advantage of the electrons angular momentum (their spin) rather than their electrical charge. This new approach, called "spintronics" has major advantages compared to common electronics. It can operate with much less energy.

However, it is difficult to create such a spin current, which is required in spintronics. In the journal "Physical Review Letters", physicists from TU Wien (Vienna) have now proposed a new method to produce gigantic spin currents in a very small period of time. The secret is using ultra short laser pulses.

Magnets and semiconductors

For every electron, two different spin-states are possible; they are called "spin up" and "spin down". The electron spin is responsible for ferromagnetism: when many electron spins in a metal are aligned, they can collectively create a magnetic field. Therefore, using ferromagnets to create spin flux seems like a straightforward idea. "There have been attempts to send an electric current through a combination of magnets and semiconductors", says Marco Battiato (TU Wien). "The idea is to create a flux of electrons with uniform spin, which can then be used for spintronic circuits. But the efficiency of this method is very limited."

Marco Battiato and Karsten Held found another way. In computer simulations, they analysed the behaviour of electrons in a thin layer of nickel when it is attached to silicon and hit with ultra-short laser pulses. "Such a laser pulse has an overwhelming effect on the electrons in nickel", says Karsten Held. They are swept away and accelerated towards the silicon.



A laser pulse hits nickel (green). Spin-up-electrons (red) change into silicon (yellow). Electrons with both spin-orientations change back from silicon into nickel.

An electric field builds up at the interface between nickel and silicon, which stops the current. Electrons still keep on migrating between the nickel layer and silicon, but the motion in both directions cancel each other, there is no net charge transfer.

Spin up and spin down

But even when no electric charge is transported, it is still possible to transport spin. "In the nickel layer, there are both spin-up electrons as well as spin-down electrons", says Karsten Held. "But the metal atoms influence both kinds of electrons in different ways. The spin-up electrons can move rather freely. The spin-down electrons however have a much higher probability of being scattered at the nickel atoms."

When the electrons are scattered, they change their direction and lose energy. Therefore, the majority of the electrons which do make it all the way to the nickel-silicon interface are spin-up electrons. Electrons which move in the opposite direction have equal probabilities of being in the spin-up or spin-down state.
This spin-selective effect leads to a dominance of spin-up electrons in the silicon. This means that a spin current has been injected into the silicon without creating a charge current. "Our calculations show that this spin-polarization is extremely strong – much stronger than we could create with other methods", says Marco Battiato. "And this spin flux can be created in femtoseconds." Time is of the essence: today's computer processors operate with gigahertz frequencies. Billions of operations per second are possible. Even higher frequencies in the terahertz range can only be reached with extremely fast elements.

So far, the method has only been tested in computer simulations. But Battiato and Held are already working with experimentalists who want to measure this laser-triggered spin flux. "Spintronics has the potential to become a key technology of the next few decades", says Battiato. "With our spin injection method there is now finally a way to create ultrafast, extremely strong spin currents."

Connecting the photonic integrated circuits community

PIC Magazine

B2B specialist publisher and event organiser Angel Business Communications, publisher of Compound Semiconductor Magazine and organiser of CS International and PIC International conferences has announced the launch of Photonic Integrated Circuits (PIC) Magazine, a new quarterly digital magazine which aims to provide timely, comprehensive coverage of every important sector within the photonic integrated circuits industry.

PIC Magazine will provide comprehensive coverage of all aspects of this industry, and each issue will carry features and research from the full spectrum of the integrated photonics community. So whether you focus on system integration, developing and manufacturing components, financing this sector, or providing the materials and equipment needed to support this industry, PIC Magazine will be your essential magazine.

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On-Site Generated Fluorine:

High-speed chamber cleaning with zero global warming potential

On-site generated fluorine enables faster chamber cleaning and eliminates the need for the largest use of restricted greenhouse gases in semiconductor manufacturing processes.

Dr. Paul Stockman, Head of Market Development at Linde Electronics, explains the chemical properties underlying the benefits.

IN PART 1 OF THIS ARTICLE [1], we described the safe and reliable on-demand production of fluorine as demonstrated by Linde's on-site fluorine generators, with an installed base of more than 30 systems over the last 20 years and more than 15 years serving electronics manufacturers. With production capacities of one to hundreds of tons per year, these systems first displaced cylinder sources of F_2 and ClF_3 used for chamber cleaning of semiconductor processes, and have subsequently become the preferred bulk supply of chamber cleaning agents for large LCD and thin-film photovoltaic manufacturing. In Part II, we discuss the fundamental chemical properties of fluorine that allow it to deliver significant process and cost of ownership benefits, while at the same time eliminating the need for the majority of greenhouse gas (GHG) usage in high-tech manufacturing.

Chamber cleaning requirement

Chemical vapor deposition (CVD) processes used in high-tech thin film manufacturing require periodic cleaning to remove particles and films from the

surfaces of the vacuum chamber and process equipment. The frequency of the cleaning can be as short as once per deposition cycle, or may range up to once per several days, depending upon the thickness of the film deposited and the sensitivity of the devices being made. Without cleaning, these films and particles lead to defects that render semiconductor chips inoperable, displays with dark pixels, and solar modules with degraded efficiencies.

Most high throughput CVD processes employ automated, on-line cleaning with gas-phase chemicals as a time-saving alternative to off-line manual and wet processes. These gases must not only react with compounds in the deleterious films and particles, but also must be non-reactive towards the chamber materials of construction. In order to maximize the availability of the costly CVD equipment, chamber cleaning processes must be quick. And increasingly, device manufacturers are looking for processes that have low environmental impact and long-term sustainability. Most importantly, the cleaning processes must be very low cost per process cycle: it's cleaning, after all.

F-gases and activation

Fluorine-containing gases, or F-gases, meet all of the technical and cost requirements for chamber cleaning agents. The gases are activated to release the fluorine atoms as neutral radicals, which subsequently react with residual thin-films to form a gas-phase waste stream and are removed through the vacuum exhaust system of the chamber. While very reactive towards the thin-film compounds, fluorine radicals are inert towards most of the metals and ceramics used in CVD equipment, provided that moisture and oxygen are excluded.

Historically, the electronics industry has used fluorocarbons (C_xF_y): sulfur hexafluoride (SF_6), and nitrogen trifluoride (NF_3) as feedstocks to supply the fluorine radicals. These gases are easy to compress and transport in cylinders, and the cost to supply has been reduced through higher-volume manufacturing and packaging. However, these gases have certain process inefficiencies inherent to the high bond strengths and side reactions associated with the carbon / sulfur / nitrogen carrier atoms. These gases have also been the target of environmental scrutiny and regulation because they are all very strong greenhouse gases with global warming potentials thousands of times that of CO_2. As a cost-effective alternative, fluorine (F_2) has zero global warming potential (GWP) and none of the process inefficiencies of the earlier chamber cleaning agents.

Three methods can be used to activate the F-gases to release fluorine radicals [Figure 1]. In low-pressure CVD (LPCVD) process equipment operated at very high temperature, greater than 700°C, the thermal

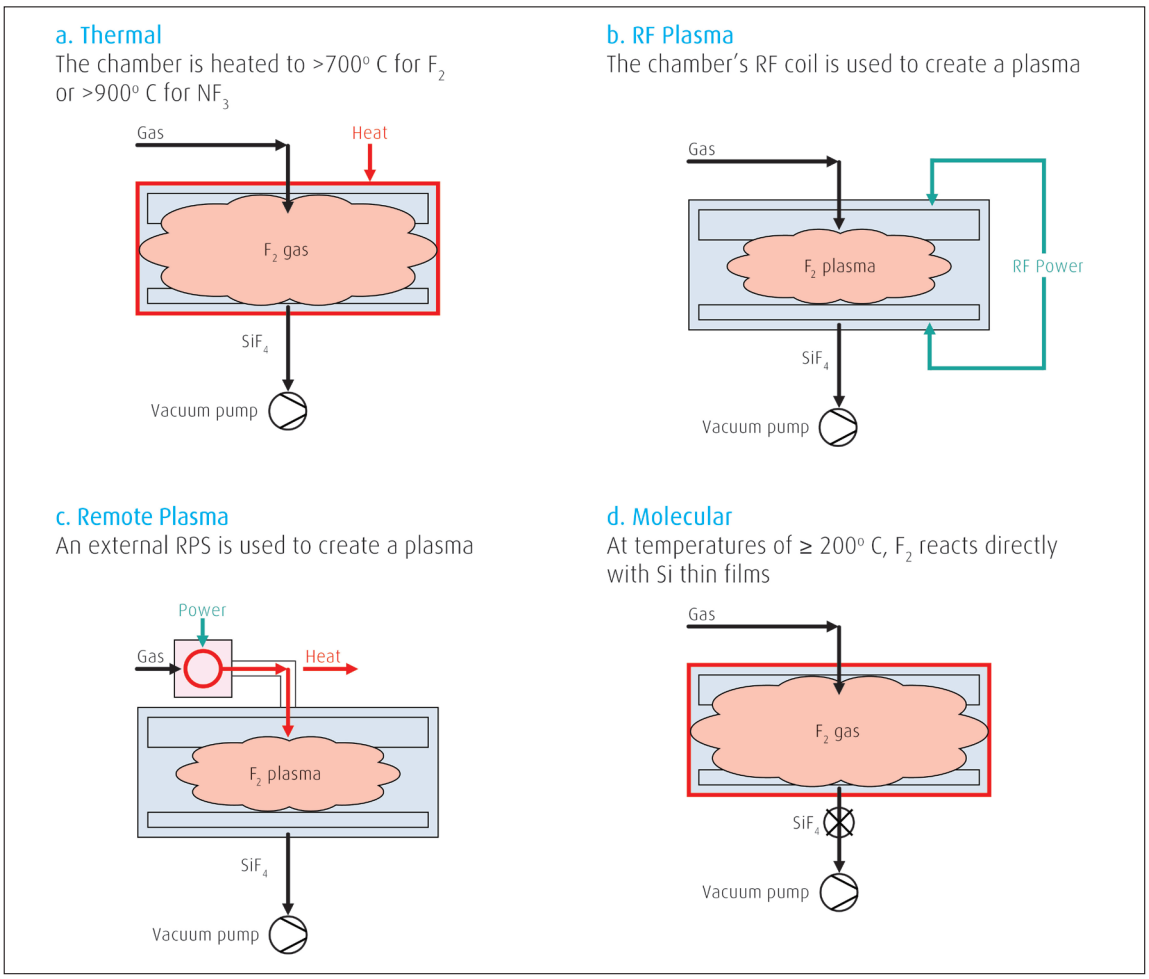

Figure 1: Activation methods for CVD chamber cleaning

> In order to maximize the availability of the costly CVD equipment, chamber cleaning processes must be quick. And increasingly, device manufacturers are looking for processes that have low environmental impact and long-term sustainability. Most importantly, the cleaning processes must be very low cost per process cycle: it's cleaning, after all.

energy from the chamber walls is sufficient to break the molecular bonds and release fluorine radicals. In plasma-enhanced CVD (PECVD) equipment, process temperatures are much lower, and too much time would be spent to heat and then cool the chamber for cleaning. Instead, the internal RF coil used to activate the plasma of the thin film reactants is also used to activate the F-gas cleaning agent. The cleaning rate is limited by the amount of energy that can be supplied by the RF power source.

With the advent of larger, more expensive 300 mm PECVD equipment, external remote plasma sources (RPS) were introduced in order to increase the energy available for cleaning gas activation, thereby decreasing the cleaning time. Most current generation PECVD tools use this method to increase the tool availability. Importantly, argon is not required to support the plasma in the RF or RPS methods. Finally, a fourth method using a low temperature direct reaction between molecular F_2 and the silicon thin film has been demonstrated as a very fast alternative method for this application. [2]

Thermodynamics and kinetics: Theory

Both the thermodynamics – or chemical energy – and kinetics – or chemical pathways – of cleaning gas activation need to be considered to understand and exploit the significant process advantages available when using F_2 vs. other F-gas alternatives. After a short look at this fundamental science, we will present process data from a variety of tools and applications that demonstrate these advantages.

As the most electronegative atom in the periodic table, fluorine forms strong bonds with most other atoms, including some stable compounds with rare gases. It is not surprising then that C_xF_y, SF_6, and NF_3 all have very high bond energies – the amount of energy required to release fluorine radicals. In contrast, fluorine forms a very weak bond with itself, and therefore F_2 requires very little energy for activation. Table 1 shows the energy required to remove individual fluorine radicals from a given F-gas and summarizes the average energy of activation. In the subsequent examples, we will see how this translates into much higher cleaning rates achievable with F_2.

Once the fluorine radicals are created through activation, chemical simplicity maximizes the amount of fluorine radicals that are available for cleaning from F_2. There is only one chemical

$$F_2 \text{ --> } F\cdot + F\cdot \qquad (1)$$

pathway (1) that can be followed, and recombination in the gas-phase to reform F_2 is kinetically forbidden. Therefore, almost all of the fluorine radicals created from F_2 go on to react with the thin films and particles targeted for cleaning. With the addition of different atoms, there is more than one available pathway during activation. For example, with NF_3 and RF activation, at low

$$NF_3 \text{ --> } \cdot NF_2 + F\cdot \qquad (2)$$

$$\cdot NF_2 \text{ --> } :NF + F\cdot \qquad (3a)$$

$$\cdot NF_2 + \cdot NF_2 \text{ --> } N_2F_4 \qquad (3b)$$

	F_2	NF_3	SF_6
Bond energies	F---F 159 kJ/mol	F_2N---F 248 kJ/mol	F_5S---F 387 kJ/mol
		FN---F 278 kJ/mol	F_4S---F 229 kJ/mol
		N---F 316 kJ/mol	
Activation energy for each F atom produced	F from F_2 80 kJ/mol	F from NF_3 281 kJ/mol	F from SF_6 308 kJ/mol

Table 1: Bond strengths and activation energy of CVD chamber cleaning gases

pressures, the desired pathway (3a) dominates. However, as the flow of NF_3 and the RF power increase, recombination of the intermediates (3b) competes, with a result that only approximately 50 percent of the fluorine atoms become effective cleaning radicals [3].

With SF_6, the effect is even more pronounced, and oxygen is added to prevent the deposition of sulfur during the cleaning.

$$SF_6 + {}^1/_2\, O_2 \rightarrow SOF_4 + 2\, F\cdot \qquad (4)$$

The effective net reaction (4) means that only 33 percent of fluorine atoms are actually used.

Thermodynamics and kinetics: Results

Now we take a look at the process effects of the thermodynamics and kinetics on commercial PECVD tools for Gen 5 LCD processes from AKT/AMAT, Oerlikon, and Ulvac. In each case, a silicon thin film has been deposited on the chamber walls at an operating temperature of 200°C.

The cleaning gas flow has been normalized to atomic F· in units of standard liter per minute (slm). The endpoint for the cleaning was determined by OEM recommended methods. The cleaning rates have been normalized to the OEM recommended method, which is set at 1.

In Figure 2 [2] and Figure 3, RF activation of F_2 vs. SF_6 and NF_3 is compared, and the RF power used is noted in the figures. The results confirm the kinetics limitation on efficiency: 33 percent for SF_6 and 50 percent for NF_3 vs. F_2. Furthermore, for the same cleaning rates, F_2 consumes one-third of the electrical power for activation.

And finally, for the same equipment set, F_2 can achieve a much faster cleaning rate: 5x vs. SF_6 and 3x vs. NF_3. This is due ultimately to the limitations of the power required for activation. Similar results have been published by others on 300 mm semiconductor tools [4].

Results in Figure 4 from a similar experiment using a tool with an RPS [5] demonstrate the improved utilization of NF_3 with this method of activation. Because the RPS completely decomposes the cleaning gas, all the fluorine is converted to fluorine radicals and the cleaning rates are the same for F_2 and NF_3 for the same amount of atomic F· flow.

However, because the F_2 bonds are so much weaker than those from NF_3, the RPS can convert much more F_2 into F· radicals and the achievable cleaning rate for F_2 is 3x to 4x that of NF_3. And for the same cleaning rate, F_2 cleaning requires 50 percent of the RPS electrical power required for NF_3. Finally, because there is no carrier atom in F_2, 20 percent less mass is used to achieve the same clean vs. NF_3.

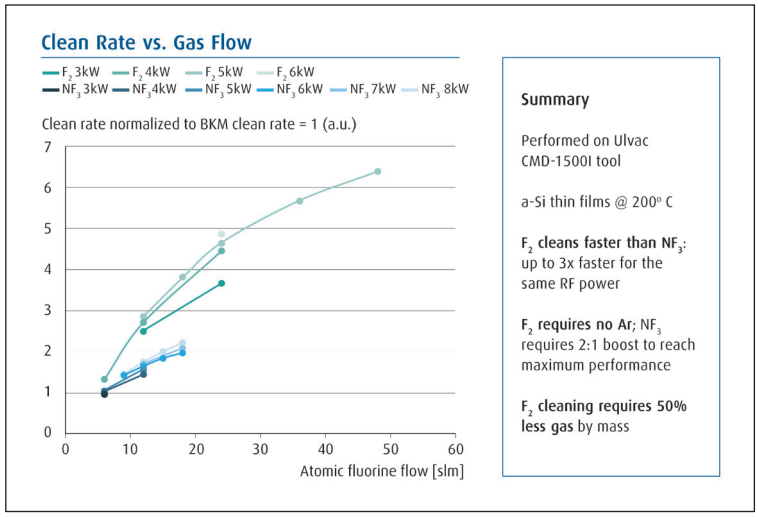

Figure 2: RF Plasma cleaning on an Ulvac tool: F_2 vs. NF_3

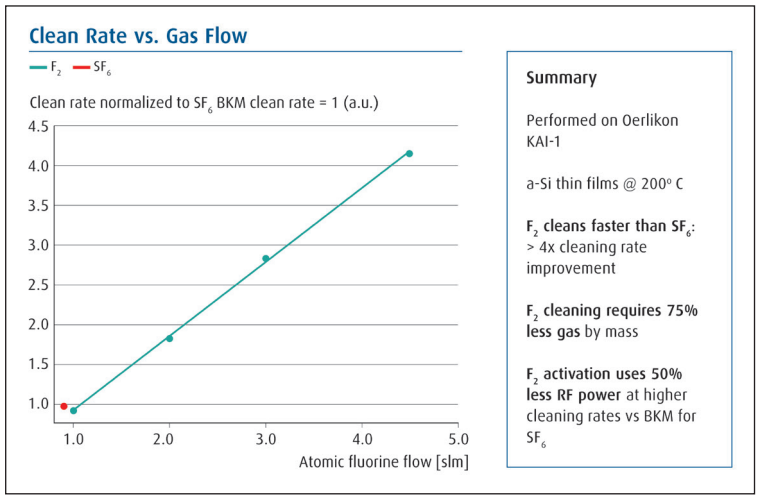

Figure 3: RF plasma cleaning on an Oerlikon tool: F_2 vs. SF_6

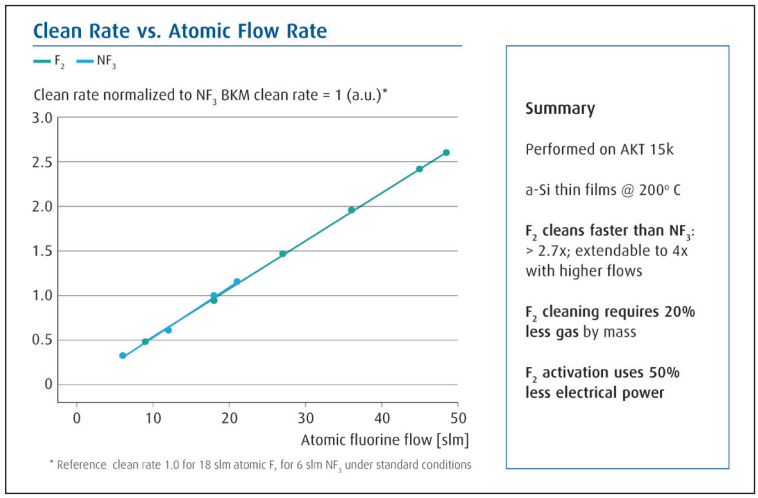

Figure 4: RF plasma cleaning on an AKT tool: F_2 vs. NF_3

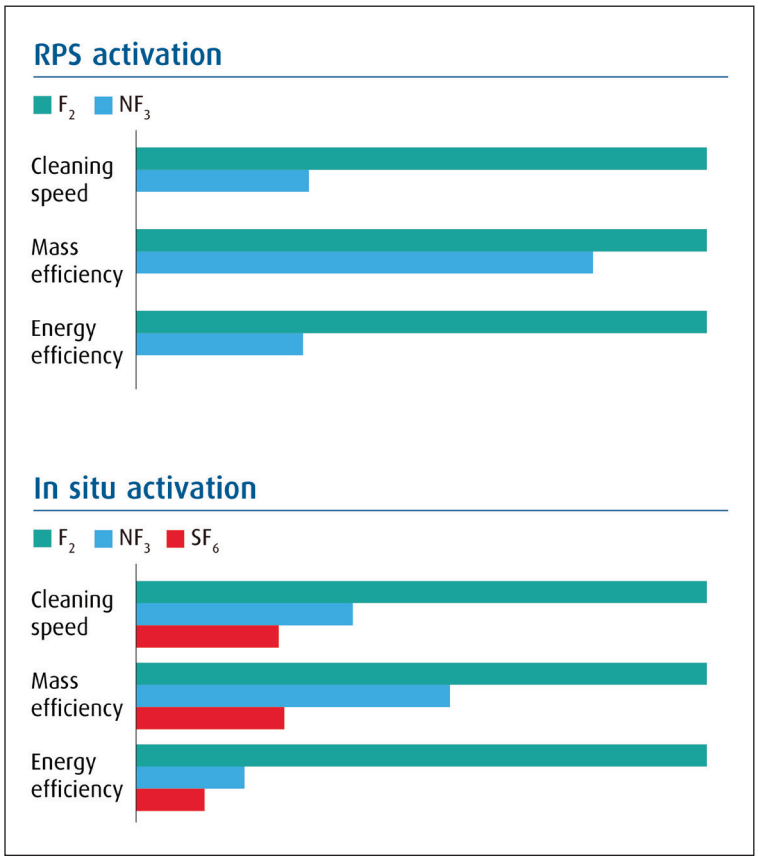

Figure 5: Summary of PECVD chamber cleaning performances

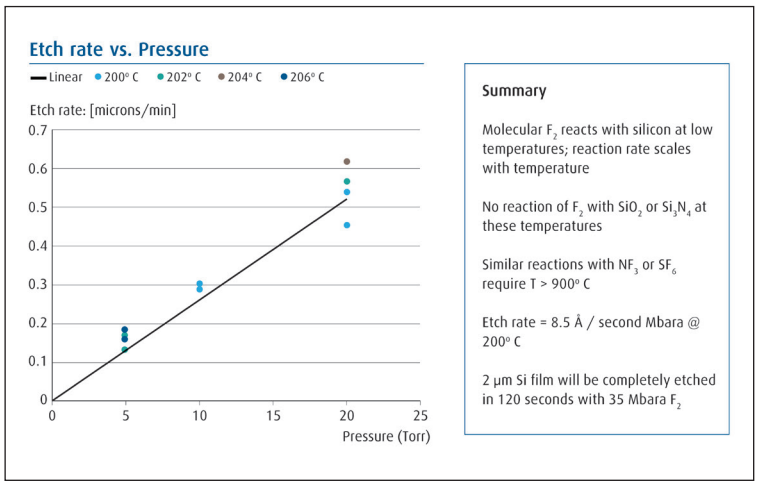

Figure 6: Molecular cleaning with F_2

Figure 5 summarizes the F_2 process benefits vs. SF_6 and NF_3 for speed, mass efficiency, and energy efficiency demonstrated for chamber cleaning. Faster cleaning, less gas used, and lower energy consumption are achieved across all of the tested PECVD tools. While the other chamber cleaning methods discussed above rely on first converting F-gases to F radicals, there exists an alternate cleaning method unique to F_2 for silicon films. The responsible kinetic mechanism is a direct reaction between F_2 and the silicon surface [6]. As seen in Figure 6, the cleaning rate is directly related to the amount and pressure of F_2 available. This method has been further demonstrated to be achievable under zero flow conditions, indicating a very fast and cost-effective clean [3].

On-site fluorine: The zero global warming potential choice

Beyond the significant process benefits demonstrated by using F_2 as a chamber cleaning agent, growing adoption of F_2 also alleviates serious problems associated with the use of GHGs like C_xF_y, SF_6, and NF_3. Unlike GHGs, F_2 does not absorb UV radiation and convert it to heat energy, and therefore it does not have any global warming potential (GWP) or contribute to global warming. Table 2 (see page 27) illustrates the very large GWPs associated with other chamber cleaning gases.

In 1990, C_xF_y and SF_6 gases were recognized for their potential to damage the environment and were included in the Kyoto Protocol for the reduction of GHGs. Large-scale adoption of NF_3 for chamber cleaning began just after this time. Scripps Institute scientists, tasked by the US government since the 1970s to collect atmospheric samples for monitoring of ozone-destroying compounds, analyzed their repository and found that NF_3 has been growing at a semi-exponential and unabated rate since industrial use began in the 1990s [7]. They showed that more than 10 percent of NF_3 produced ultimately escapes into the atmosphere. Recently, several national and local environmental authorities have moved to monitor the use of NF_3. The US Environmental Protection Agency has included NF_3 and other GHGs commonly used in the electronics industry as part of its reporting rule. Manufacturers are required to report not only the amount of individual GHGs used, but also to measure the gases at key steps in their processes.

While not yet regulated by means of a carbon equivalent tax, the cost of compliance is estimated at over $1 million (USD) for larger fabrication facilities [8]. Because cleaning gases constitute approximately two-thirds of the GHGs used in a typical semiconductor fab, converting PECVD chamber cleaning to fluorine will allow some mid-tier manufacturers to decrease their total GHG usage below the reporting threshold, while the largest manufacturers will be able to significantly reduce their compliance burden.

Clean Gas	Atmospheric Lifetime	Global Warming Potential
CF_4	50,000 years	6,500 GWP_{100}
C_2F_6	10,000 years	9,200 GWP_{100}
C_3F_8	2,600 years	7,000 GWP_{100}
SF_6	3,200 years	23,900 GWP_{100}
NF_3	740 years	17,200 GWP_{100}
F_2	0 years	0 GWP_{100}

Table 2: Global warming potentials of CVD chamber cleaning gases

Summary

Manufacturers in the semiconductor, display, and photovoltaic industries have safely and reliably chosen on-site F_2 for their CVD chamber cleaning requirements. Initially adopted for its cost and process enhancement benefits, F_2 is now proving to be an easy choice for manufacturers who also want an environmentally sustainable alternative.

For the past 20 years, Linde has been the leader in providing on-site fluorine generation for the electronics industry and other markets. With over 30 installations, Linde continues to support its customers' choice for faster, more efficient cleaning processes with zero global warming potential. Linde partners with manufacturers and OEMs for the extension of these benefits to additional applications.

DR. PAUL STOCKMAN joined Linde in 1996. He currently is Head of Market Development, Linde Electronics, where he guides Linde's strategy to anticipate the needs of its customers in the semiconductor, display, solar and LED markets. During his career with Linde, Dr. Stockman has held roles in electronic materials product, purification and analytical development; equipment development; as well as Technology and Commercialisation Manager for Linde's on-site fluorine equipment. Dr. Stockman has been granted 5 U.S. patents and holds a Ph.D. in Chemical Physics from the California Institute of Technology.

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Visit: **www.linde.com/electronics** for more information

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Ensuring safety and uptime by managing condensable gases

The need to safely exhaust CVD reaction by-products is increasing as complex device structures gain prominence in microelectronic manufacturing. Edwards Vacuum has applied novel solutions to increase safety, reduce downtime and control costs.

BY CHRIS O'ROURKE, APPLICATION MANAGER, EDWARDS VACUUM

THE RANGE OF CVD process precursor materials and associated reaction by-products susceptible to condensation in dry-pump foreline and exhaust systems continues to grow as the scope of new materials incorporated into emerging device structures expands. To a limited extent, the tendency for materials to condense in pipe-work can be reduced by diluting the exhaust with inert gas, a technique also widely used to control flammability in process exhausts. However, in the face of ever-increasing flow rates of flammable precursor gases in a number of CVD processes, dilution flow rates are increasing at a correspondingly high rate. As a result there is a strong motivation to reduce dilution rates to lower cost and improve abatement efficiency.

An alternative and more cost-effective strategy is needed to control condensation of liquids and solids in the process exhaust stream. Clearly, the major perceived risk associated with condensation is blockage of the exhaust pipe and a consequent process interruption caused by excessive dry-pump exhaust pressure or breach of seal integrity due to high pipe internal pressure. However, there are also other serious hazards that may result from condensed materials in exhaust pipes. For example, if partly reacted silicon compounds condense in exhaust pipes during a deposition process, and are subsequently exposed to fluorine during the following chamber-cleaning process, an exhaust fire is likely to occur, resulting in a serious risk to equipment and personnel. Similarly, condensed materials which incorporate fluorine may release HF vapour when the exhaust system is dismantled for cleaning and the condensate exposed to atmospheric water vapour.

To counter the condensation threat and improve system safety and productivity, thermal management systems are widely employed to control operating temperatures of forelines and exhaust pipes. These systems typically comprise electrical heater mats in close contact with the foreline or exhaust pipe wall, enclosed by high-efficiency thermal insulation material. However, these systems are really only fully effective if they are carefully installed on the pipes to avoid cold spots, and their operation controlled in real time to ensure correct pipe operating temperature at all times. Furthermore, when designing pipe thermal management systems, care has to be taken that introduction of diluting gases into the exhaust system, or introduction of reactive gases such as oxygen or natural gas into the point-of-use abatement system,

Process type	Exhaust challenge
Low-K CVD	Complete abatement of complex and condensable low-k precursors
SACVD	Safe and effective abatement of high flows of TEOS, mixing with F_2
LPCVD Nitride	Safe handling of high flows of easily condensable materials
LPCVD Poly	High silane flow, associated solid reaction products (powder)
Epitaxy	Condensation of reactive (explosive) polysiloxane reaction products
Metal Etch	Control of condensable and corrosive gases and liquids
W-CVD	Control of H_2 flammability, control of solid reaction products (powder)
HDPCVD	Abatement of high F_2 flows
PECVD Nitride	Condensation of ammonium hexafluorosilicate
Poly Etch	Abatement of PFC gases and control of corrosive gas condensation
Implant	Safe removal of highly toxic hydrides at sub-atmospheric pressure

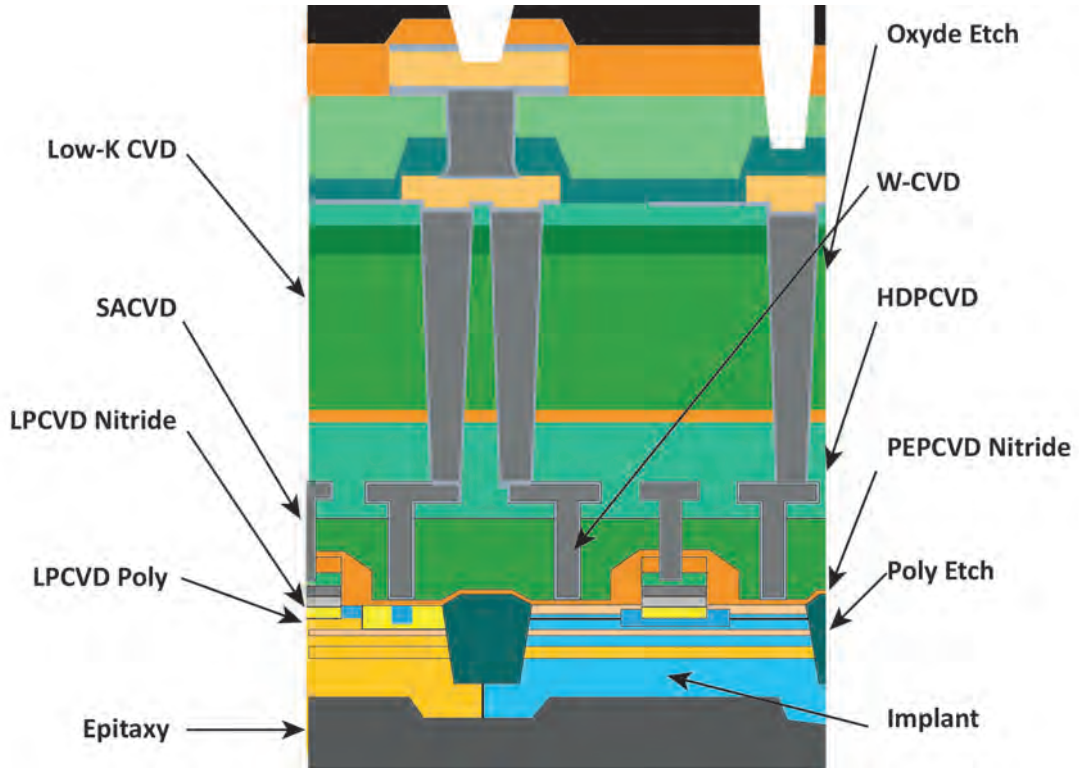


Figure 1: Many semiconductor manufacturing processes have the potential to cause condensation of liquids or solids in the exhaust gas stream, resulting in equipment down-time and lost production.

does not promote local exhaust gas cooling and condensation. This specific consideration requires that the temperature of injected gases and all other factors that can affect the exhaust gas temperature are controlled as part of a total process solution.

Typical applications of exhaust pipe temperature management systems

Many semiconductor manufacturing processes and their related exhaust management challenges are known to have potential to cause condensation of liquids or solids in exhaust gas pipes (see Figure 1).

There are many common examples of exhaust pipe blockage by condensable materials. For example, ammonium chloride (NH_4Cl) is formed in LPCVD nitride processes and condenses readily in exhaust pipes to form solids which can block the exhaust pipe and stop the process. This is particularly bad news if the process tool is a batch-type system (vertical furnace) – in this case an entire batch of wafers is put at risk.

Similarly, ammonium hexafluorosilicate ($(NH_4)_2SiF_6$), very fine white powder, can form during a silicon nitride PECVD process when ammonia comes into contact with fluorine-containing species generated during a chamber cleaning step from nitrogen trifluoride gas (NF_3). The resulting powder can very quickly block down-stream pipework, associated vacuum pumps and point-of-use abatement systems, causing equipment downtime and presenting a health and safety hazard for operating and service personnel (see Figure 2).

In principal, the solution is straightforward: maintaining exhaust/abatement system components above a critical temperature to prevent condensation, as shown in Fig. 3 below.

However, in practice there is a great deal of complexity and know-how involved in designing, installing and operating an effective exhaust temperature management system. It has now become vital that the installer has a detailed understanding of the process, its reaction products and their impact on the reliability and robustness of the sub-fab equipment. Furthermore, in addition to the more familiar condensation-prone process exhausts, epitaxy processes and emerging ALD processes now pose serious exhaust management issues as they migrate into high volume manufacturing.

Epi process exhausts have become notorious for their tendency to accumulate condensed highly reactive polysiloxane materials. These pose a particular hazard for service personnel since they have a tendency to react violently or even explosively when mechanically disturbed or exposed to air, and unfortunately, some emerging ALD processes have shown similar tendencies. The result is to put pressure on sub-fab equipment manufacturers to develop suitable best-known methods (BKMs) for setting up their products, including vacuum pumps, point-of-use abatement systems and the associated forelines and exhaust pipes, to provide safe and reliable operation. The requirement to continuously develop an understanding of emerging new processes now extends to designers of pipeline temperature management systems so that they are able to develop product solutions that deliver consistent, uniform and reliable pipeline temperature control.

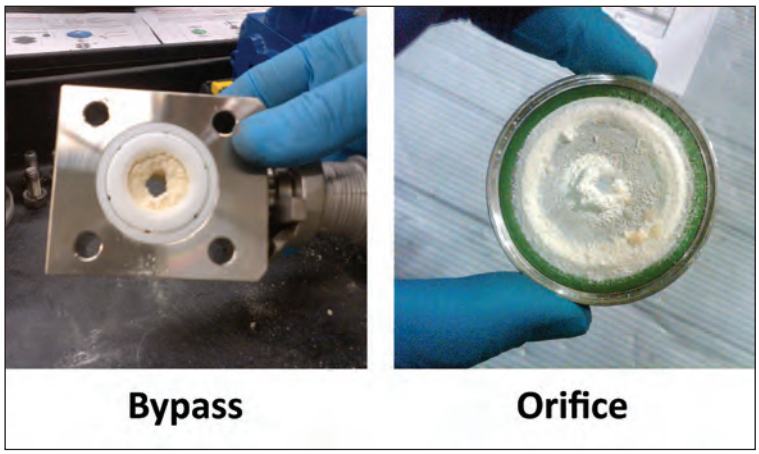


Figure 2: Ammonium hexafluorosilicate ($(NH_4)_2SiF_6$) build-up in downstream pipework and associated equipment can result in pipe blockage and lost production time

Legacy thermal management systems

Vacuum pumps and point-of-use abatement systems intended for use in high-volume manufacturing fabs are typically designed to conform to specific process BKMs, ensuring that the gases are maintained at an appropriate temperature throughout each piece of equipment. This might be achieved by incorporating heated elements at each vulnerable point, such as the flow control orifice shown in Figure 3. Equally important, and in some ways more challenging, is controlling temperature throughout the forelines, which connect the process equipment to the pump, and the pump exhaust lines, which connect the pump to the point-of-use abatement system. These pipe systems are invariably configured on a case-by-case basis to fit the location of the equipment or the available space and therefore require equally flexible and configurable pipeline heating solutions.

Early generations of pipeline temperature control systems aimed for flexibility by simply wrapping the pipes with an electrically powered heating element (such as a tape-heater) and enclosing it with an insulating material such as fiberglass. They usually included a simple local control mechanism typically comprising a temperature-sensitive switch to interrupt electrical power to the heater element above a certain

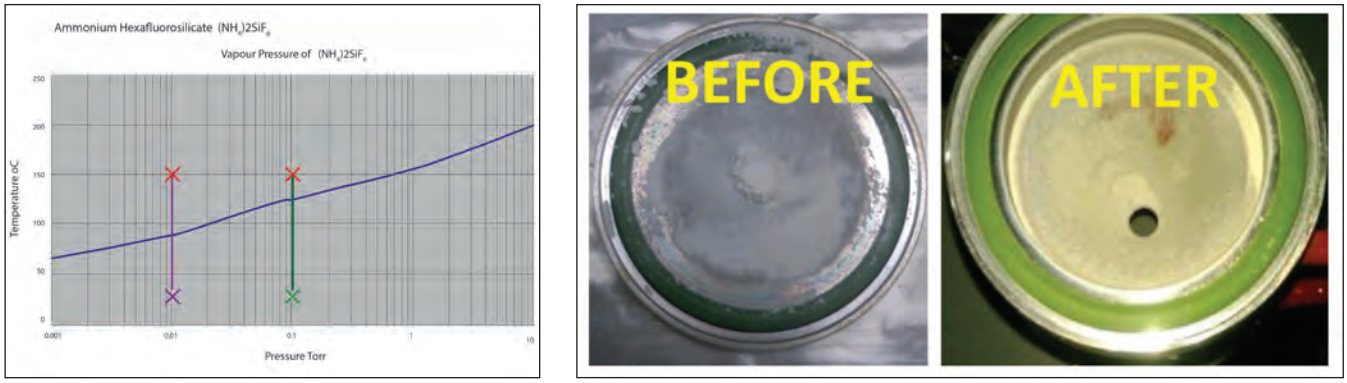


Figure 3: As the phase diagram on the left shows, maintaining the temperature of the gas above a critical temperature / pressure will prevent condensation of ammonium hexafluorosilicate. The before and after photos show a blocked orifice plate on the left and a completely clear heated conical orifice on the right.

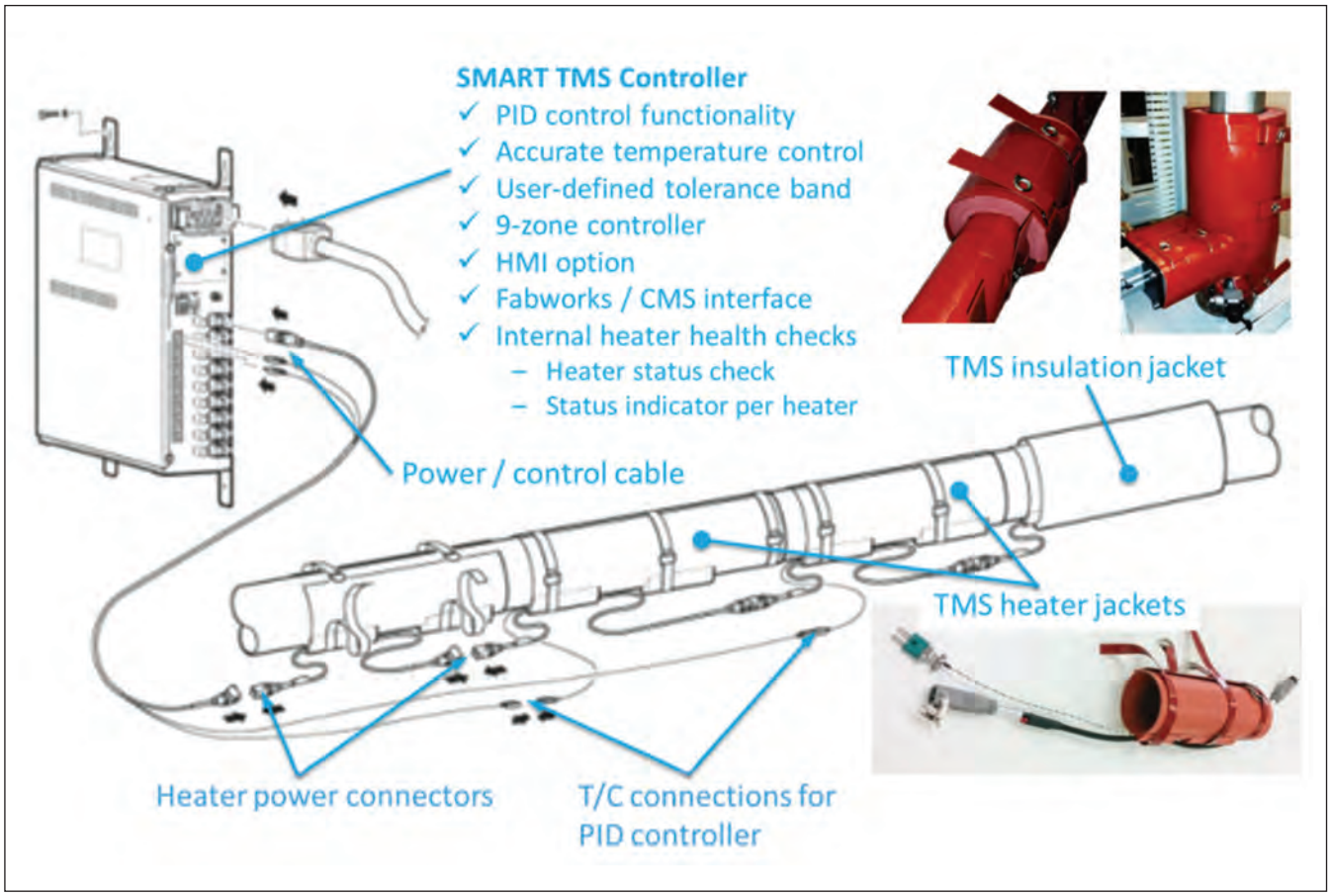


Figure 4: A state-or-the-art intelligent temperature management system can manage multiple heaters from a single remote location, providing visual indictor lights for each. Insulation is precisely sized and designed to allow consistent, one-handed installation on hard-to-access pipe runs to ensure temperature uniformity.

temperature set-point (typically 180°C). A safety fuse set at a higher temperature than the set-point was incorporated to prevent damage to the system in the event of a thermal switch problem. A monitor light was occasionally included to provide visual indication if temperatures fell below an acceptable level. The power supplied to the system was set to a constant level intended to maintain the temperature somewhere just below the switch set point.

However, in practice several problems were encountered with this simple control technique that seriously impacted its reliability. Firstly, on start-up from cold, the temperature could over-shoot the switch set-point causing the fuse to blow, with consequent system downtime for fuse replacement. Secondly, if the heating element temperature approached and remained close to the set-point, the switch would cycle rapidly, gradually changing its operating characteristics and ultimately resulting in complete failure of the switch.

Finally, the monitor lights proved to be unreliable over time and depending on the configuration of the pipe heating system, were not always readily observable by the operator.

Whilst legacy pipe heating systems suffered a number of intrinsic component reliability issues, a far larger problem centered on the configuration and installation of the system.

It is relatively easy to wrap a straight pipe run with a temperature control element and heat it effectively. However, pipe bends, mitred joints and elbows present a more difficult temperature management challenge, as do gate valves, purge ports, bellows, flanges, test ports, support brackets and all the essential components of a process exhaust system. In practice a section of uncontrolled pipe as short as 5 cm can cause a cold spot that results in unacceptable condensation of solids in the exhaust pipe, leading to unplanned system downtime whilst the blockage is cleared. A further challenge to control of exhaust gas temperature is presented by the introduction of purge gas used to reduce the concentration of flammable gas to a safe level. If the temperature of the injected gas is not controlled at its point of introduction, it can cause a reduction in temperature of the process exhaust gas flow resulting in local condensation despite the installation of a temperature management system on the rest of the exhaust system.

The evolution of intelligent thermal management systems

These problems have been comprehensively addressed in the most recent generation of intelligent thermal management systems. A typical state-of-the-art intelligent pipeline temperature management system is shown in Figure 4. Advances in the technology can be conveniently categorised in five general areas.

Development of comprehensive process BKMs

The onus is now on the supplier of the pipeline temperature management system to ensure that its product provides a level of performance suitable for the target process that ensures maximum personnel safety and process reliability.

Functionality

Temperature can be controlled precisely at any set-point between ambient and some maximum, typically 180°C. "Fail On" technology ensures maximum protection from condensation in the case of a component failure; an intelligent controller enables configurable alarms and temperature to be set through a single remote interface.

The temperature management control system can also be integrated with sub-fab equipment and fab monitoring and control software to provide alerts, health checks, temperature readouts and data analysis. Although materials of construction are selected to permit onsite modification to accommodate changes in pipe configuration with minimal dust and particulate creation, availability of a wide selection of heater and insulation jacket sizes can reduce the need for onsite modifications.

Simplicity

Components are designed for easy installation in tight or confined spaces to improve the consistency and reliability of pipe temperature management installations and to save time and effort on difficult-to-reach pipe runs. Reliable electrical connectors are easy to access and manipulate. Each component incorporates an automatic internal health check capability, including a local indicator light to assist during installation and troubleshooting.

Reliability

Solid state relays rated for long life (over 50 million cycles) have replaced mechanical thermal switches as the primary temperature control mechanism. A selection of shaped heating and insulation components ensures complete coverage of elbows, joints and other challenging features and provides a uniform temperature throughout the exhaust system. Materials of construction are designed for repeated use with improved longevity, enabling their re-use when process tools are upgraded, moved or replaced. Appropriate materials flammability ratings provide assurance against component fires in case of accidents (such as a fire caused by ignition of flammable gas mixtures in the exhaust pipe).

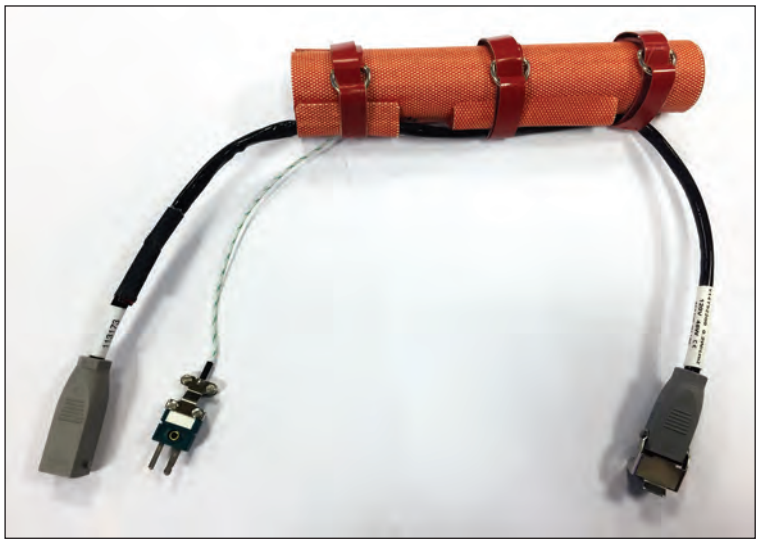
> "New intelligent thermal management systems address many of the shortcomings of previous generations. They can reduce equipment downtime and minimise health and safety risks to operating and service personnel"

Efficiency

Efficient insulation and configurable operating temperatures provide better thermal control, improved temperature uniformity throughout the exhaust system, and reduced energy consumption.

Conclusion

Temperature management of forelines and exhaust pipes is critical to prevent condensation of hazardous process materials and byproducts throughout the vacuum and abatement sub-system. New intelligent thermal management systems address many of the shortcomings of previous generations. They can reduce equipment downtime and minimise health and safety risks to operating and service personnel. These systems also provide flexibility, ease of installation, consistency of operation, improved energy efficiency and increased functionality with programmable remote controllers that interface readily with sub-fab equipment, process tools and fab control software.



Acoustic screening
reveals component defects

Plastic encapsulated microcircuits (PEMs) are mainstays of consumer, defence and commercial electronic products. Tom Adams, consultant at Sonoscan, explains how to safeguard your bottom line with optimized acoustic screening.

IMAGINE a typical plastic-encapsulated microcircuit (PEM) component. Inside this particular PEM lies an area of electronic mold compound that is separated from the die paddle by a gap. This very thin gap may be called a delamination, suggesting that the two materials were once bonded but later separated; or it may be a 'non-bond,' suggesting that the two materials were never bonded. One side of the gap borders the die attach, but the gap does not extend under the die.

Regardless of its specific defect, this PEM poses a risk to any system in which it is installed. If the die must dissipate significant amounts of heat, the chief risk is that the gap will expand laterally under the die as a result of thermal cycling. There it will reflect heat being dissipated from the die back into the die. In time it may cause the die to overheat and fail electrically.

Figure 1: Automated acoustic micro imaging tools (here the Sonoscan DH2400) use carefully defined standards to make good accept/reject decisions on large numbers of components.

If the PEM is to be used in a low- or medium-priced consumer product, such failure may not be of critical concern. But if the PEM is to be used in a higher-level product (automotive, medical, military, aerospace, and some commercial products), such an internal gap-type defect is of considerable concern and should be found before the PEM is mounted on a board. The PEM itself may be inexpensive, but if it is going into a critical application it should be screened acoustically for internal structural defects before use. Undiscovered defects can cost the manufacturer time, money and even its priceless brand reputation.

The most effective non-destructive means of finding gap-type defects is an acoustic micro imaging tool such as a Sonoscan C-SAM system. Laboratory, semi-automated and automated versions (Figure 1) all use a scanning transducer that pulses very high frequency or ultra-high frequency (ultrasound) into the PEM or other sample thousands of times per second. A pulse that encounters a gap-type defect is virtually 100 percent reflected by interface between the solid material and the air in the gap, even if the gap is as thin as 10 nm.

There are two widely used modes of acoustic imaging for screening PEMs:

- **Reflection mode imaging.** A pulse striking a well-bonded interface is partly reflected to the transducer and partly transmitted across the interface. A "white" pixel in the acoustic image is made by a pulse striking a gap-type interface; a "gray" pixel is made by a pulse striking a well-bonded interface between solids. Pixel colors are

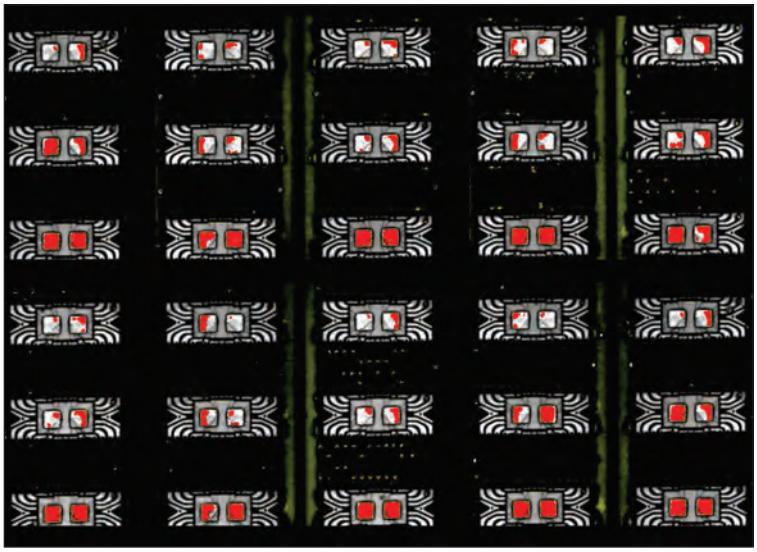


Figure 2: Acoustic image of JEDEC-style tray holding small PEMs. The numerous red features are disbonds of the mold compound from the die face - a defect very likely to break a wire bond.

sometimes altered for viewing.

- **Thru-SCAN imaging.** The echoes are pulsed into the sample, but the reflections are ignored by the transducer. Pulses that exit the bottom of the sample are recorded by a separate sensor. In a THRU-Scan acoustic image, exiting pulses are typically gray, while locations where the pulse was blocked by a gap above are black because no ultrasound was detected.

Either reflection-mode or Thru-SCAN can be used in screening parts. Where it is useful to see a defect in detail and to know the approximate depth of a defect or feature, reflection mode is employed. If the goal is simply to identify a defect at any depth, Thru-SCAN is used.

Reflection mode was used in Figure 2, which shows a portion of a JEDEC-style tray of small PEMs. In these images, red indicates internal gap-type defects. Here the defects are delaminations between the die face and the mold compound. These are particularly risky defects because they can shear off wire bonds on the chip. In this image there are probably no acceptable components.

Whichever imaging mode is used, the acoustic data and images will identify the gap-type defects in all of the components in the lot, whether the lot consists of a handful of components or tens of thousands. Imaging can also reveal some non-gap defects, such as a die that is tilted or rotated from its intended position.

Clear definitions of acceptable and non-acceptable structural anomalies should be made before screening is performed in order to determine which components to scrap and which to use in production. The overall goal is to achieve the highest product reliability without scrapping components with internal defects that are probably harmless. It is easy enough to look at an acoustic image and examine a bright white feature that indicates a gap on the die paddle or in the die attach. But how do you accurately evaluate the risk this gap presents? The results of acoustic imaging are easier to interpret if they can be compared to an existing standard.

Several industry standards are available that can be used for comparison. One is Application of Scanning Acoustic Microscopy to Plastic Encapsulated Devices, Basic Specification No. 25200 of the ESCC (European Space Components Coordination). This standard provides guidelines for determining reject of components having defects of specific sizes. For voids in the die attach material of plastic packages, this standard would reject a component where more than 50 percent of the die attach area is occupied by voids. It would also reject components where a single void occupies 15 percent or more of the die attach area, or a void in a corner than occupies 10 percent or more of the die attach area. Finally, it would reject any plastic encapsulated component where 70 percent or more of any one quadrant is occupied by voids. These are straightforward values that are measured and reported automatically by C-SAM tools.

But for a specific lot of a plastic encapsulated components, these guidelines may not be a perfect match. There are simply too many attributes that can vary from one component type to another. IPC/JEDEC J-STD-020 E, Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices, lists more than 20 critical attributes. If even one of these attributes is changed in the redesign of a component, the component may need to be requalified for moisture sensitivity. The critical attributes include items such as die thickness, die passivation, wafer fabrication process, die attach process, and lead frame finish.

J-STD-20 is an industry standard, but was not designed for predicting overall reliability. It measures the ability of a given lot of plastic encapsulated parts to survive exposure to atmospheric humidity during assembly. A component's moisture sensitivity level is related to overall reliability, but generally does not accurately predict that reliability. It is not uncommon for engineers arranging for the acoustic inspection of one or more lots of components at one of Sonoscan's applications laboratories to mention that they would like to use J-STD-20. It may be an appropriate choice, or lab personnel may suggest a standard more directly related to reliability. If the customer is concerned about die attach defects, a good choice may be MIL-STD-883 Method 2030, Ultrasonic Inspection of Die Attach, or PEM-INST-001: Instructions for Plastic Encapsulated Microcircuit

> “Since each component has its own profile of attributes, finding an industry standard that is, without modification, a satisfactory match for a given component can be difficult”

(PEM) Selection, Screening, and Qualification. The customer's goal typically is to screen out those components whose internal structural defects are very likely to cause defects - multiple long delaminations on the top side of many of the lead fingers, for example, or voids that occupy 70 percent of the die attach. The more critical the application, the less risky will be the defects that can be accepted. Since each component has its own profile of attributes, finding an industry standard that is, without modification, a satisfactory match for a given component can be difficult. Often a standard needs to be altered to fit well with a particular component; even J-STD-20 is used, with appropriate modifications. The odds of successful acoustic screening can be improved if the customer acquires more information about the component to be screened and its application.

Customers can acquire this information by performing some form of life test on the component in question. Depending on the particular hazards the component will face in service, the user might employ thermal stress testing, mechanical shock testing, radiation testing, or another test type. Putting the results of testing together with an industry standard should bring the user closer to achieving optimal results from acoustic screening. Life testing might reveal, for example, that thermal stress causes small delaminations between the die attach and the die, but that additional thermal stress does not greatly enlarge these delaminations.

Figure 3 is the acoustic image of a PEM before and after 1000 cycles of thermal testing. Before testing, there were delaminations on several of the lead fingers where the wires are bonded. After 1000 cycles, these delaminations have hardly changed, but the mold compound is now delaminated from essentially all of the area around the die. The testing has identified two anomalies that should be sought during acoustic screening.

Additional insight is available from Sonoscan's test lab personnel, who have imaged thousands of different plastic encapsulated microcircuits, and who can help with modification of standards. The lab references about a dozen military and industrial standards for screening PEMs, but these are often just starting points. Many companies that use the lab have developed and maintain their own standards. Standards can be modified in any way that will benefit a particular application. If, for example, there is a hot spot on the die, instructions can be written to reject a component having any heat-blocking anomaly at the same x-y coordinates.

Occasionally an acoustic imaging mode other than reflection or THRU-Scan modes is used for specific purposes. If a component is likely to have structural defects at multiple depths (a TO-220, for example), an imaging mode can be used that scans multiple depths. There is no reduction in scan speed, and each depth produces its own acoustic images.

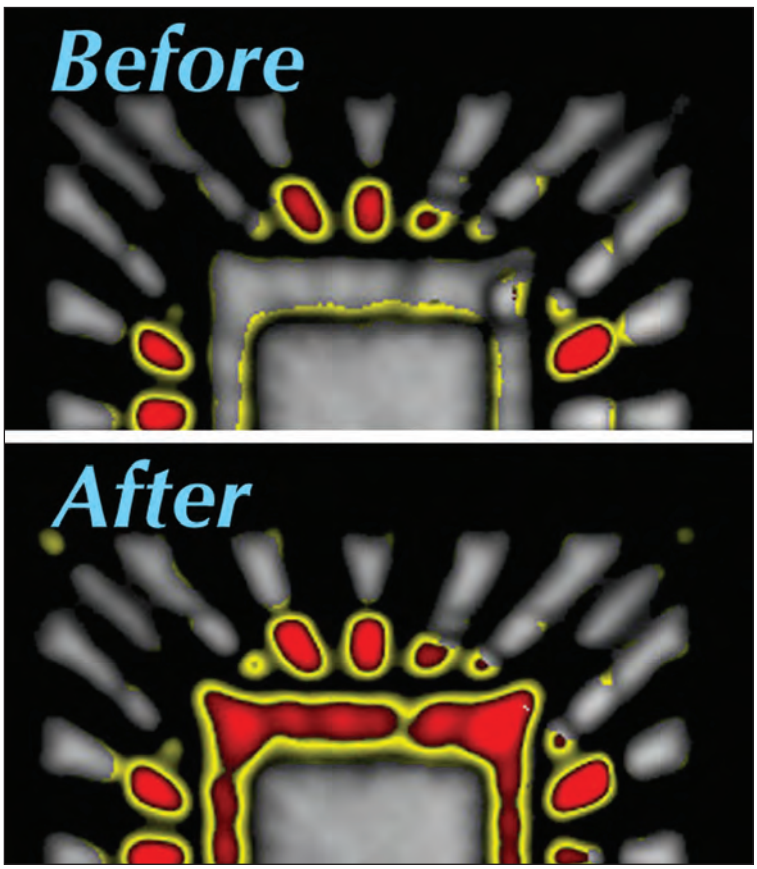


Figure 3: A PEM imaged acoustically before and after 1,000 thermal stress cycles, which had little impact on existing voids but which the die paddle to delaminate from the mold compound.

New probe manufacturing technology addresses semiconductor test challenges

EFC unlocks a new level of miniaturisation and performance in probes. Hafeez Najumudeen, Product Marketing Manager, Omron Electronic Components Europe, tells Silicon Semiconductor how.

SEMICONDUCTOR probe pins are approaching a crunch point. Silicon geometries are getting ever finer, and packaging density has been increasing for SMT ICs, LCDs, fine-pitch glass substrates, and other electronic components. Such high-density devices require inspection in many areas, so multiple probe pins must be placed with a very small spacing between each. The package unit pitch for recent devices is only 0.4 to 0.5 mm. In a few years, it is expected to be 0.3 mm or less. Yet the probes used to connect to and test these devices are manufactured with the same stamping and pressing techniques as they have been for many years.

A new electroforming (EFC) technology is emerging which overcomes many of the limitations of stamping and pressing. EFC enables the creation of probe pins that are not only much smaller, but also lower resistance and higher performance. EFC probe pins can not only support much narrower pitches, but also offer benefits for testing at high frequencies, very low voltages and high currents. This paper describes electroforming (EFC) technology and looks at the contribution that it can make to semiconductor manufacturing and testing.

What is electroforming?

Electroforming is a metal forming process that builds ultra-thin metal components through the electroplating process (Figure 1). The components are produced by

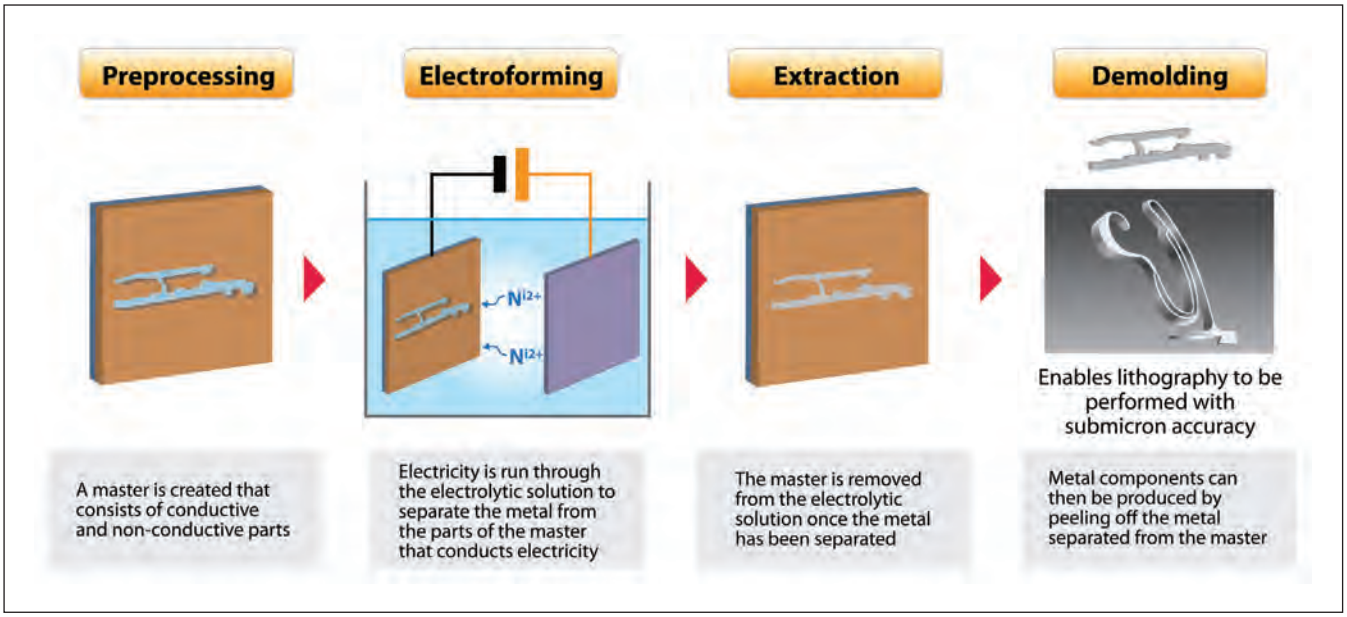


Figure 1: The EFC manufacturing process.

developing a layer of metal onto a base form (master). Once the plated layer has been built up to the desired thickness, the newly formed part is stripped off the master substrate.

Microfabrication technology allows for considerable component design flexibility and is also used to meet more exacting needs for shapes and sizes, since it enables the transfer of a pattern with submicron-scale (0.0001 mm) surface roughness accuracy. Unlike conventional electroplating, electroforming builds thicker, stronger metal layers which become the actual contact structure it also enables high-precision production of extremely small, thin and fine patterned parts.

Benefits of EFC

Omron has introduced electroforming technology into the fabrication of the semiconductor probe pins, which were previously formed with presswork. This enabled forming narrow parts with a high aspect ratio (ratio of thickness and width). Plates with a width one-third of their thickness have been produced. With traditional pressed contacts it is difficult to allow the plate width to be less than the plate thickness.

With electroforming, it is also possible to bend contacts much further. Traditionally, a plate can be bent to a radius of up to twice the plate thickness by dynamic mechanical tooling. Electroforming has achieved a 0.04 mm bend radius by transferring a pattern with static chemical processing. This allows for much more freedom in creating round shapes, opening new possibilities in component design. EFC has also allowed micro slits of 35 microns and holes of 50 microns to be created. These were not possible with traditional presswork.

EFC is an entirely new style of pin that combines four components (upper and lower plungers, spring and conductive path) into one. They have a flat structure which enables placement of pins at any angle, thus making it easier to reduce pitch compared to a conventional cylindrical probe pin. The versatility of electroforming technology enables a single component to incorporate a spring section to provide contact force and durability, and a barrel section that turns on power when it fits the plunger, separate from each other. No electricity flows through the miniaturised spring section, thus solving such problems as excessive temperature rise, the spring section's disconnection, and unstable resistance.

Since there is no need for costly investment in press dies and other equipment, as well as the time-consuming die-making process for prototyping and mass production of probe pins, specific demands for customised non-standard specifications can be satisfied speedily.

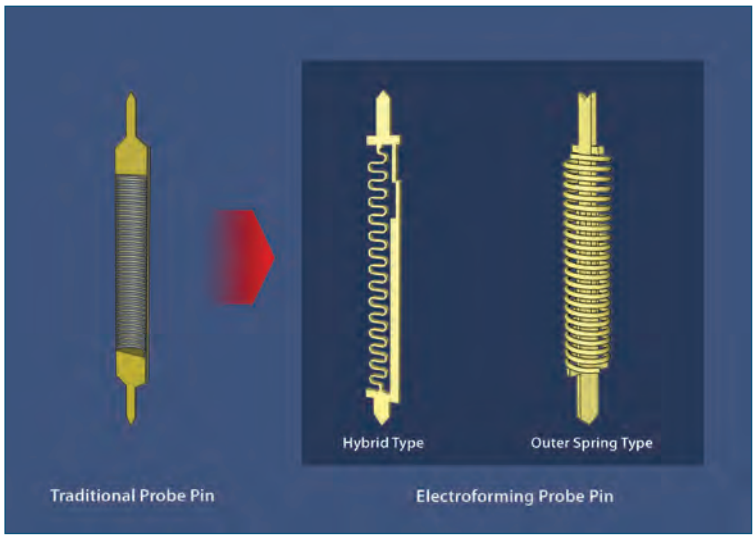


Figure 2: EFC is being used to advance the manufacture of semiconductor probe pins.

Omron has produced flat probes of 60 microns thickness (Figure 2), and sockets of 150 micron pitch can be assembled. EFC probes can also be very robust. The larger 0.6 mm diameter outer spring type can handle up to 2A. To assemble these tiny contacts, a special air tweezer tool has been created.

Addressing the issues

One of the most fundamental benefits of electroforming is that harder materials can be used – leading to greater resilience. In order to reduce the damage to components when attempting to miniaturise them through press work, softer copper alloys with lower strength have been used, leading

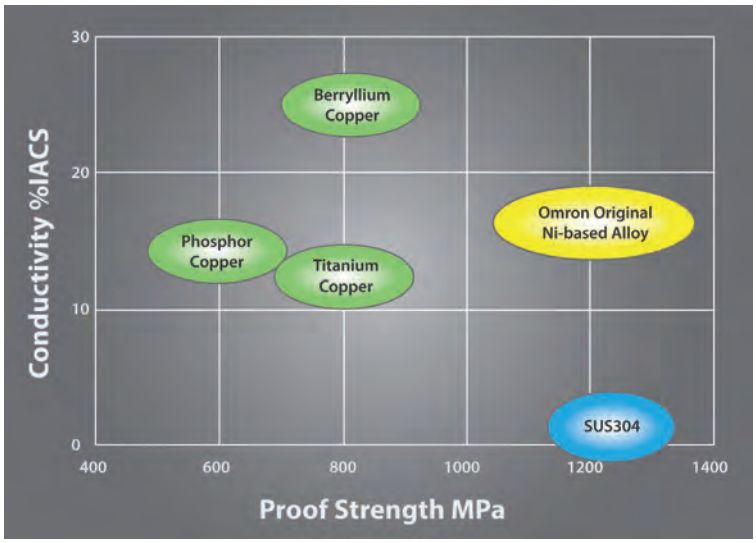


Figure 3: harder nickel alloys can be used to manufacture probe pins improving performance.

> advance semiconductor test engineers have been waiting for. Semiconductors are not only getting more compact, but higher frequency, higher power and lower voltage devices are emerging too. The improved performance of EFC supports offers benefits for all of these devices and enables the manufacture of more durable probes

to greater deformation under pressure during tests. Electroforming allows complex shapes to be manufactured in harder, nickel alloys reducing deformation under pressure as well as the risk of breakage.

Another issue is contact failure due to contamination on the pad of the device under test (DUT). Since electroforming allows complex shapes to be manufactured, a number of solutions are available here. For example a 'wiping' structure can be created at the end of the probe pin to remove contamination. Alternatively, probe pins with multiple plungers can be designed which maintain reliable contact even if one plunger is blocked by contamination.

A further issue is the inductance of the pins that can have a negative effect on rise time. The improved characteristics of electroformed materials and their greater hardness means that the length of the coil spring can be reduced to reduce inductance. If required, a plate spring can be created to ensure minimal inductance. The smoothness of electroformed contacts is an advantage when testing very high frequency semiconductors of 100GHz or above. High frequency currents tend to travel on the surface of the conductor (skin effect) and roughness of the surface extends the current path and hence the losses.

With EFC technology, burs on cut edges and warping (undercutting) that are unavoidable with presswork do not occur. A roughness average (Ra) of less than 0.1 micron can be achieved with EFC, compared to typically 2 microns with pressed contacts.

The future

Years of development and real world applications have demonstrated that EFC is the advance semiconductor test engineers have been waiting for. Semiconductors are not only getting more compact, but higher frequency, higher power and lower voltage devices are emerging too. The improved performance of EFC offers benefits for all of these types of devices and enables the manufacture of more durable probes simultaneously.

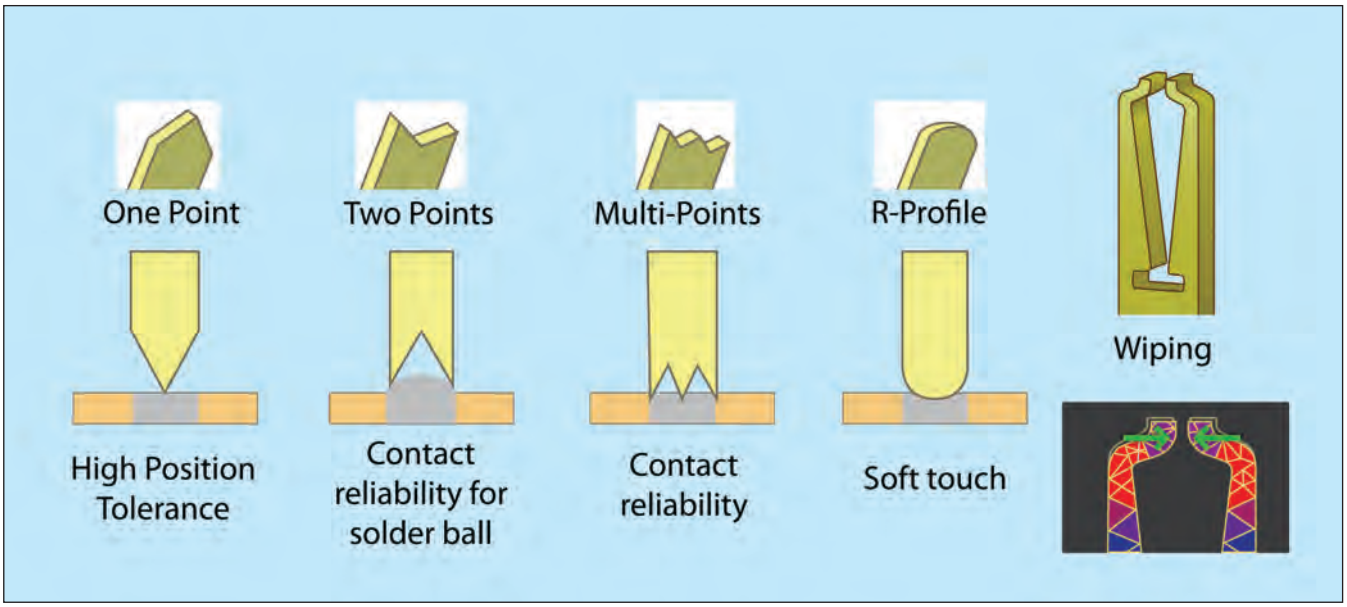


Figure 4: EFC enables the creation of a wide range of end profiles according to customer requirements.

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Improve deposition and process control with minimal metrology overhead

Run-to-Run control can significantly improve process performance, but often at considerable time and cost. Taking a higher level view that applies novel methodologies can increase performance and savings with minimal metrology burdens says Joerg Reichelt, Yulei Sun – Rudolph Technologies, Inc. Tilo Bormann, Andreas Gondorf – Vishay Siliconix Itzehoe GmbH.

SEMICONDUCTOR manufacturing is arguably the most sophisticated and unforgiving volume production technology ever developed [1]. It consists of a complex series of hundreds of unit process steps. The technology continues to evolve; it becomes more complex as device sizes and associated manufacturing tolerances shrink, which is aggravated by increasing layer and mask quantities as well as introducing new materials and process steps when manufacturers seek to accommodate a greater mix of products at higher volumes and efficiencies. R2R process control is a strategy that seeks to optimize process performance by tuning the operating parameters for the next cycle based upon previous cycle result measurements.

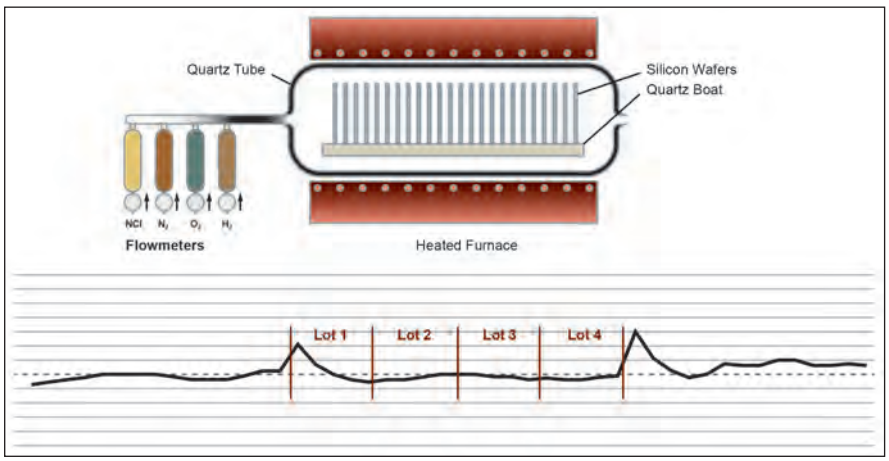

Figure 1 Wafer-to-wafer thickness variation is a relatively well-behaved function of position within the furnace carrier that can be approximated by a piecewise linear function.

Traditionally, R2R controllers for semiconductor manufacturing are process-centric[2], meaning the R2R controllers are designed to solve the local control problems at a single step in the manufacturing process without aiming at the bigger picture of a series of steps.
For example, in a furnace deposition and CMP process flow, the majority of the post-CMP wafer-to-wafer thickness variation usually comes from variation in the pre-CMP thickness of wafers as they complete the deposition process in the furnace. The deposition process is complex, with many parameters available to adjust performance that also need to be controlled. A process-centric design philosophy will implement a multi-input-multi-output (MIMO) furnace controller [3] to minimize the wafer-to-wafer thickness variation locally before it can propagate downstream to the CMP process. An additional CMP control strategy would be designed to compensate for the post-CMP wafer thickness variation introduced by the CMP tool drift.

The complexity of the deposition process makes R2R control difficult. Adjusting the operating parameters requires the execution of complex experiments that consume significant time and resources. In addition, deposition furnaces are different from most other types of process equipment in that they are designed to process multiple lots of wafers loaded into a single carrier in each run. In contrast, the CMP process operates on one wafer at a time. The performance of a CMP tool on a given product wafer usually drifts relatively

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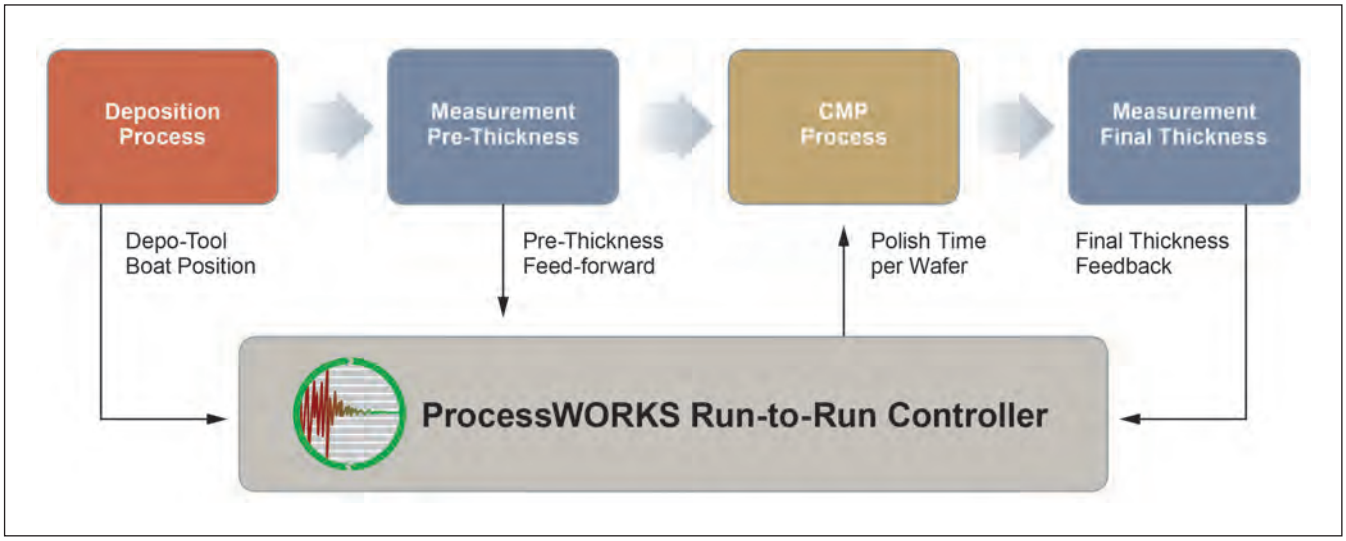

Figure 2 The multistep R2R controller uses inputs fed forward and backward from sampled pre- and post-CMP measurements to calculate polish times for each wafer.

slowly over time, so control strategies typically operate at the lot level, adjusting polishing time for a subsequent lot based upon measured thickness of the previous lot. Lot level R2R control is a well-developed and widely accepted practice for CMP. It is possible to adjust polishing times for each individual wafer, but this requires thickness measurements of each wafer after deposition. The measurement overhead for such wafer-level control introduces prohibitive time and cost overhead.

Multistep R2R control

To address the issue of thickness variability without introducing unacceptable metrology overhead we have developed a multistep R2R control strategy using Rudolph Technologies' ProcessWORKS software. Essentially, this approach postpones compensation for post furnace wafer-to-wafer thickness variation until the CMP step, providing control for both steps. The strategy is based on our observation that most wafer-to-wafer, post-furnace thickness variation is a relatively well-behaved function of the wafer's location in the furnace carrier that can be approximated by a piecewise linear function (Figure 1). Thus it is possible to interpolate the likely thickness of each wafer based on sampled measurements of a few wafers in each lot, yielding a significant reduction in the overall metrology burden when compared to a conventional wafer-level control strategy. In this case we sampled 5 wafers in locations spread evenly through each lot. Likely thicknesses for unmeasured wafers were interpolated based on these sample measurements; CMP polishing times for each wafer were calculated based on the measured and interpolated thickness values. Post-CMP measurements of the thickness of the same 5 wafers were used to monitor and control CMP performance at the lot level. All calculations were handled automatically by the ProcessWORKS software.

Results

Implementation of the multistep R2R controller using ProcessWORKS is relatively straightforward; no programing is required. The operator defines the equation to calculate the output parameter, in this case polishing time, and configures the system interface with metrology and process equipment and factory control software. In our case, integration took three weeks and the controller was deployed in the factory five weeks after an initial requirements gathering meeting.

Figure 3 compares SPC charts before and one month after the controller was brought into production, showing a 72 percent improvement in Cpk for post

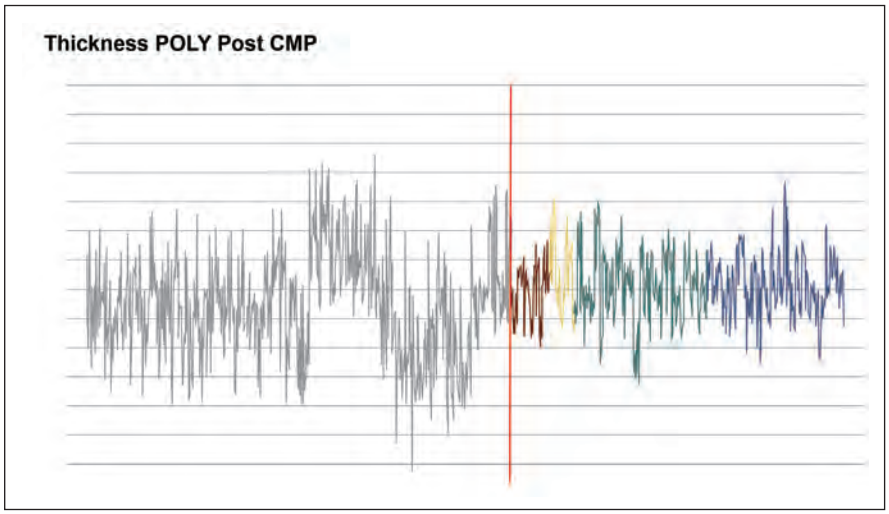

Figure 3 Post CMP wafer thickness measurements are illustrated before and one month after the multistep R2R controller was brought into production. These results demonstrate a 72 percent improvement in Cpk. The colors on the right side of the plot represent different CMP tools.

CMP wafer thickness and the elimination of all out-of-limit excursions. The colors on the right side of the plot, after controller implementation, represent different CMP tools and make apparent the consistency of the improvements across all tools. After implementation of the controller, observations that the post-CMP thickness was also dependent on which furnace was used to process the wafer at the deposition step led to additional modifications in the R2R controller to include a correction for the furnace in polishing time calculations, yielding an additional 39 percent improvement in Cpk.

Figure 4 shows a box plot comparing pre- and post-controller thickness variation and again demonstrates the significant improvements.

Figure 5 shows the impact of the reduction in thickness variation on the performance of the downstream etch process.

In addition to process performance gains, the multistep R2R controller saved an hour per day by eliminating the need for a daily tool monitoring run, reduced operator/engineering time for manual adjustments and extended preventive maintenance cycles.

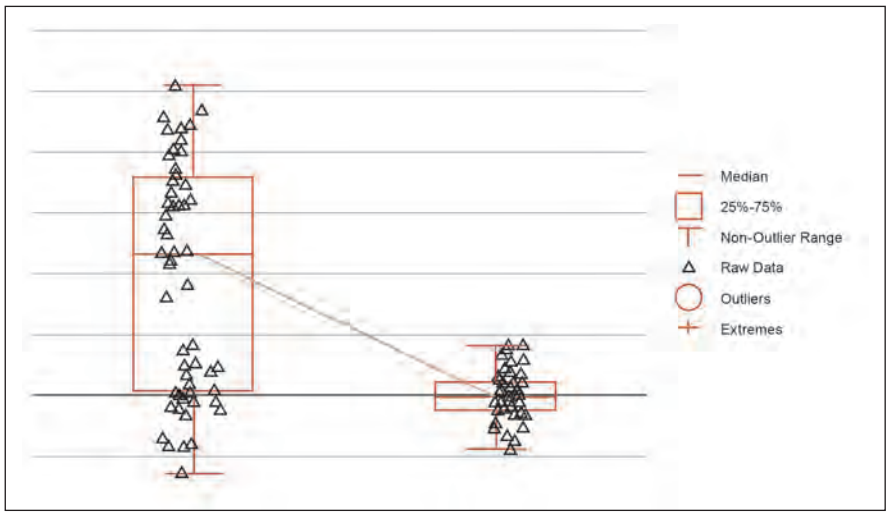

Figure 4 A box plot of pre- and post-controller wafer thickness variation.

Conclusion

We have described the use of a multistep R2R process control strategy to reduce post CMP wafer-to-wafer thickness variability. It has successfully reduced the combined variability of the deposition and CMP processes without adding an unacceptable metrology burden. We were able to integrate the controller with the Vishay factory systems in three weeks, which allowed us to deploy the CMP controller within five weeks of the initial requirement gathering meeting. Since the deployment of this wafer-level CMP controller in production, the Cpk of the CMP process has increased by 72 percent with zero spec limit violations. The post-CMP wafer-to-wafer thickness variation has been reduced by 70 percent. We subsequently discovered that the post-CMP thickness is also dependent on which furnace was used to process the wafer at the deposition step and additional modifications to the R2R controller now use different values for different furnaces when calculating the polish times, improving Cpk by another 39 percent. Additional benefits of the controller included the elimination of nonproductive daily tool monitoring runs, reduction of engineering/operator time for manual adjustments and the extension of preventive maintenance cycles.

Rudolph Technologies and Vishay. Figures can be downloaded at:

https://rudolphtechnologies.sharefile.com/d-s469e110d6184e288

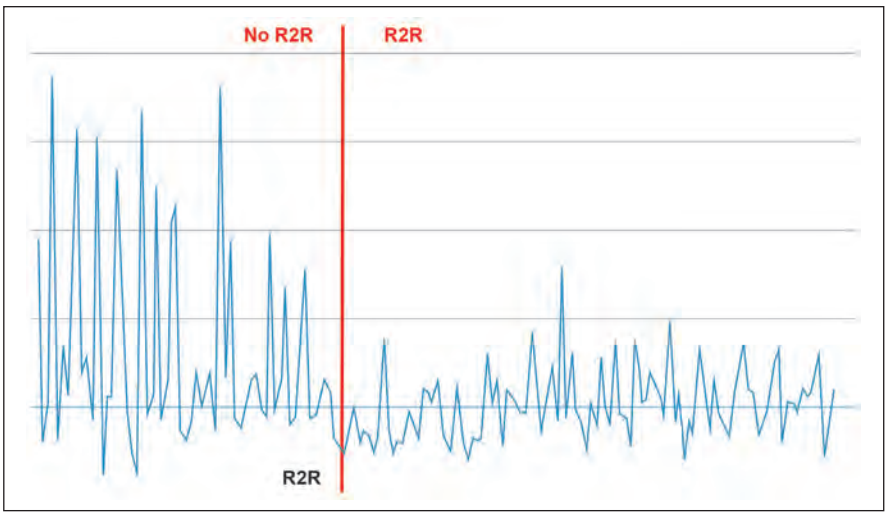

Figure 5 Improvements in wafer-to-wafer thickness control significantly increased the performance of the downstream etch process.

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A closer look at silicon's big future

Inspection and metrology leader KLA-Tencor delivers a wide range of integrated solutions for enhancing productivity in nano-scale IC manufacturing. According to Senior Vice President David Fisher, silicon's evolving needs will continue to drive growth in 2016 and beyond.

KLA-Tencor and Lam Research Corporation announced their intent to merge on October 21st. Like other headline-making mergers, the pending KLA / Lam marriage follows a familiar pattern: like-minded companies with complementary capabilities join forces to offer integrated solutions for essential industry needs. KLA-Tencor brings metrology and inspection leadership; Lam delivers deposition, etch and clean expertise. Silicon Semiconductor's Mark Andrews spoke with David Fisher, KLA-Tencor's Senior Vice President of Corporate Strategy, Marketing and Acquisitions to gain his perspective on the technologies he sees as critical to optimizing performance and quality in next-generation electronic devices.

Today's leading foundries and device manufacturers depend upon highly refined 300mm technologies for high volume production of memory and logic circuits. But 300mm is just one part of a larger universe. New and revived technologies utilize 200mm (and smaller) wafers even as the industry refines 300mm processes and also prepares for a 450mm future.

KLA-Tencor sees great opportunity up and down the wafer spectrum because quality, efficiency and profitability always top the list of customer must-haves.

Q **IoT –** While new M2M devices are not yet widely seen in today's marketplace, this is a burgeoning field with the potential to radically grow the number of intelligent devices in consumers' lives. What do you see as a compelling argument for the growth of this industry and how does KLA-Tencor enable next-generation technology like IoT?

A KLA-Tencor shares the view that the continual drive to lower the cost of power chips with embedded communications is enabling significant growth potential in IoT. Early adoption, perhaps because of the current price point, appears to be focused at Automotive and Industrial, but we expect proliferation as chip costs come down and functionality goes up.

Perhaps the most exciting aspect to IoT is the network, communications and algorithmic processing that will be required to harness the value of the data being captured by the end devices. Clearly, this expansion of communications infrastructure is happening today on a smaller scale in automotive at the local system level, but it is anticipated it will migrate to the global distributed level over time. This growth in low cost/high function devices is creating a resurgence in inspection and metrology investments at mature fabs, and we expect there is potential for new fab investments and major expansions on >90nm design rules.

These fabs have increasingly advanced requirements for a broad range of defect detection and metrology measurements. Although the economics are different than leading edge fabs, they still have similar yield and time to market constraints in order to meet their profit objectives. Those constraints are driving customers to seek out inspection and metrology tools, which used to be leading edge, but are now more affordable as they are older models.

For example, the leading edge 8920 inspection tool is often the ideal broad range sensitivity and low cost of ownership (COO) system for IoT segments, delivering features like defect binning and tool-to-tool matching and leveraging our experience from the leading edge fabs.

Optics Inspection – How does optical inspection play a role in developing next-generation devices? What are the major trends and challenges for this field in the next year?

A For over more than a decade, the end to optical inspection has been predicted as geometries shrink and resolution capability comes into question at each node. In spite of those predictions, however, optical still continues to be the workhorse inspection tool in both the mask shop and the fab, as it offers throughput and hence COO that e-beam has been unable to approach. As a result, KLA-Tencor continues to invest in and offer new optical systems that offer large advances in sensitivity over previous models.

One difference at current nodes is that the defect landscape is not just limited to size (ever shrinking), but also where they occur (surface vs. buried). Additionally, metrology challenges around CD and overlay control have increased significantly with multi patterning. Also, there is demand for full wafer coverage at a good COO. To meet these challenges, KLA-Tencor is launching optical inspection tools at an unprecedented pace. We have extensions to the core optical 29xx Series, and have announced a "Generation 5" broadband plasma system that we are bringing to market in 2016, as well as new offerings for mask inspection, package inspection, CD, overlay and films metrology—all based on photon (optical) systems.

Reticle Inspection – As performance goals continue to move device geometries to smaller sizes, how does this challenge reticle inspection techniques? How do more efficient and accurate approaches benefit the customer and ultimately, end users?

A As argon fluoride (ArF) immersion lithography continues to be pushed into more aggressive nodes, customers are developing more aggressive reticle enhancement techniques such as inverse lithography optical proximity correction (OPC) techniques, and different masking technologies such as chrome-less phase lithography. Even in regions where the masking techniques were previously straightforward, customers can now add features such as ortho edge fragmentation to ensure they have a common process window. As a key supplier of inspection equipment for reticle inspection, KLA-Tencor works closely with our industry partners to align on the challenges and requirements for reticle inspection. As such, we developed the Teron 640 with our latest Dual Imaging mode inspection technique which utilizes the combination of high sensitivity, high resolution inspection followed with aerial imaging and innovative physics based defect dispositioning. These techniques maximize usable sensitivity on mask (including finding new sources of defects in high MEEF regions) while reducing the burden for offline disposition.

KLA-Tencor is also in the process of releasing a Reticle Decision Center which will add further operational efficiency to mask manufacturing operations, offering inline concurrent automated defect classification for the Teron platform and other options to analyze defects offline from other systems in the mask house. These new technologies will enable mask shops to handle the latest generation masking technologies and improve operational efficiency.

Inverse lithography – As device geometries continue to shrink, the number of process steps increase to maintain quality and high yields. These factors increase costs and affect production timetables. Can you explain the key advantages of inverse lithography in silicon device manufacturing and what tools customers need to maximize performance and reduce time to market?

“One of the OPC techniques available to lithographers is Inverse Lithography Techniques (ILT), which provides more process latitude and helps achieve a common process window for the different regions of the exposure field. The challenge is that optimizing a full device/exposure field for ILT can take days to optimize even on the largest OPC computing clusters due to the complex calculations and modeling factors”

A With EUV delays, ArF immersion lithography is being pushed further into technology nodes beyond its resolution limits, and as such it is constantly working at the edge of its operating window. Depth of focus budgets continue to shrink as the scanners operate at the limits of Low K1 lithography. One of the OPC techniques available to lithographers is Inverse Lithography Techniques (ILT), which provides more process latitude and helps achieve a common process window for the different regions of the exposure field. The challenge is that optimizing a full device/exposure field for ILT can take days to optimize even on the largest OPC computing clusters due to the complex calculations and modeling factors. Furthermore, the write times for a mask using current technologies would go from 8-10 hours to multiple days. For layers where a common process window cannot be achieved, layers may need to be further split from two patterning layers with etch steps to three patterning steps and three etch steps (3P3E), further impacting device cycle times and device economics.

As an alternative to full field, ILT may be used in the most critical regions of the exposure field. In doing so, there needs to be accurate models for OPC verification and potentially mask verification tools to ensure that a common process window can be achieved with the proposed differing OPC solutions within the field. To further optimize the use of ILT, the race is on to develop multi-beam technology for mask writing to enable the ideal freeform shapes coming from the OPC models in a more manageable cycle time.

KLA-Tencor’s latest mask inspection tools offer the capability to inspect complex ILT masks.

Q **5D Patterning Control Solution –** Quality control is becoming an especially crucial consideration for manufacturers including defect detection and being able to feed data forward/backwards to improve future wafer lots as well as correct deficiencies of lots in process. How does KLA-Tencor’s approach deliver superior results and otherwise positively affect manufacturing?

A At KLA-Tencor, we see the challenge of quality control (QC) to require a two-step solution. The first step is to try and deliver the most capable point products for each application, such as macro inspection or film thickness measurement. The second step is to then harness the data from those point QC products alongside with information from the tools doing the processing to try and create higher order QC in the fab.

KLA-Tencor’s 5D solution is our product offering which is the second step in the solution. 5D seeks to provide the best on-product-overlay (OPO), CD uniformity (CDU), and ultimately edge placement error (EPE) by providing lithography control and reducing variability in all areas of the fab. The 5D product is not limited to data streams from KLA-Tencor’s products, but is an open architecture that can take data from QC products by other suppliers and can create correctibles for process equipment such as lithography, etch and deposition tools. For example, by combining WaferSight PWG patterned wafer geometry systems with Archer overlay metrology systems and 5D Analyzer data analysis and patterning control, KLA-Tencor’s stress induced overlay solution has demonstrated reduced OPO and lithography COO.

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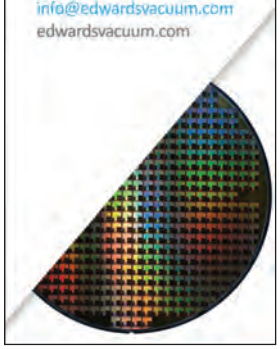

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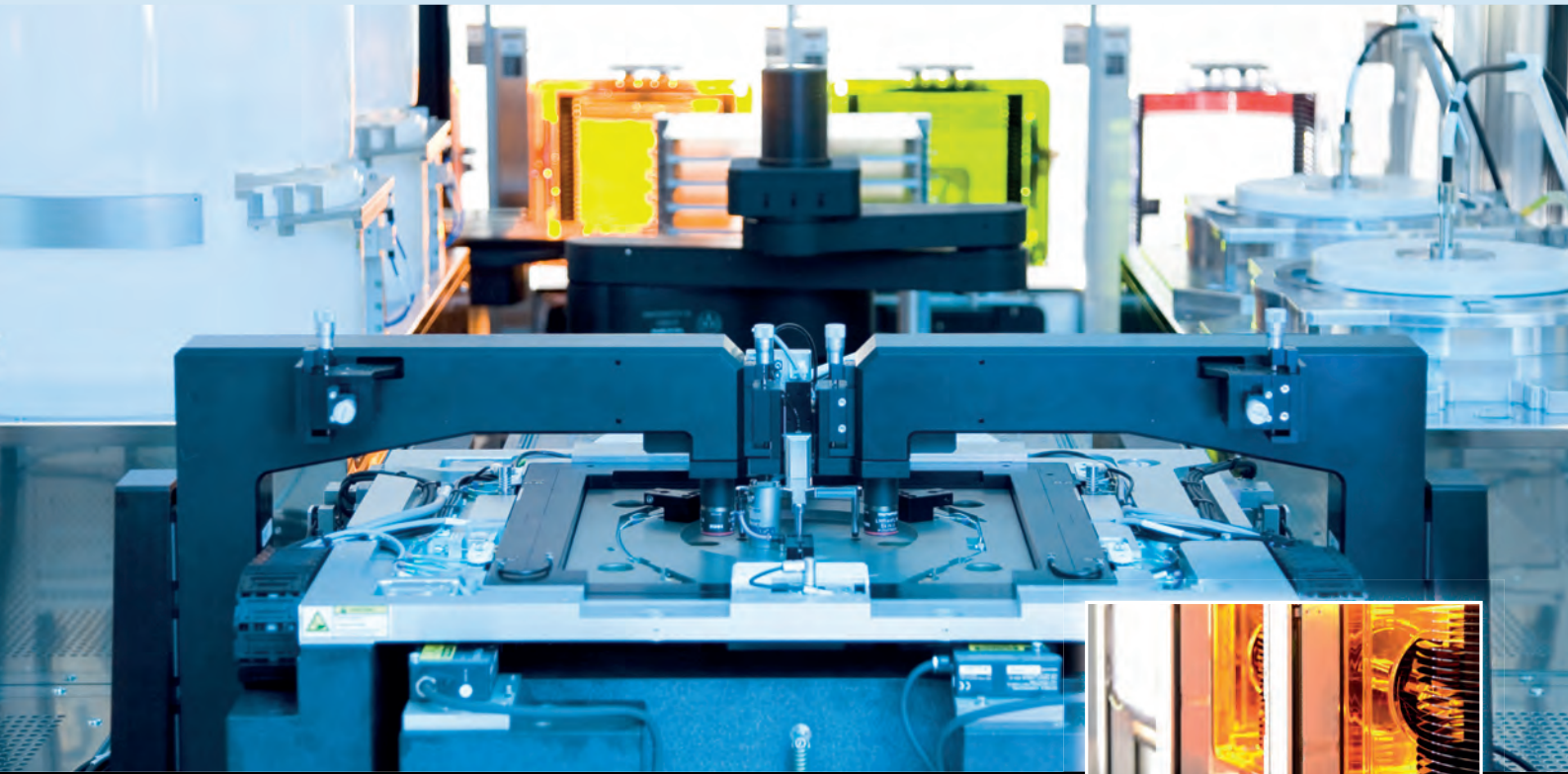

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