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executiveview

by Mark Andrews, Technical Editor

Looking for growth in 2016

THE MID-2016 NUMBERS are here and growth seems to be on holiday. The industry is hopeful that emerging technologies will revive momentum. But should it instead consider a more sweeping paradigm shift?

In March the world's largest fab, Taiwan Semiconductor Manufacturing Company (TSMC), reported slumping sales. The leading downward indicator was undeniable, again pointing to the risk of vertical market overdependence.

"…smartphone growth this year is mostly from the medium and the low end," said TSMC Co-CEO Mark Liu to investors in a conference call. "We see the over-$500 phone reducing, but the $400 phone is increasing quickly." Liu forecast 'negative growth' in PCs and tablets, with overall world semiconductor markets growing about one percent in 2016.

In mid-May International Data Corporation (IDC) joined Gartner Inc., IHS Inc., and IC Insights Inc. in forecasting that the 2016 market could decline by two percent or more. On the dissenting side was the World Semiconductor Trade Statistics (WSTS) group that forecast 'slightly positive' sales in 2016 and moderate growth in 2017.

Analysts and industry watchers continue to cite the struggling world economy as reason behind gloomy outlooks. While many believe growth will hinge on emerging applications it may be time to rethink the paradigm. Robust growth in semiconductors has long been tied to waves of successful consumer products driving demand. PC sales held the number-one spot for nearly 30 years; smartphones created their own wave. What growth driver comes next is the billion-pound question. Internet of things (IoT), wearable and flexible electronics might become future standard bearers, but no technology has yet emerged to deliver the growth that PCs and smartphones did previously.

How about programmable hardware? That's the solution advocated by the Global Semiconductor Alliance. The idea is not new. In fact, many hold that the industry owes its early success to the days when chips by Intel, Motorola and Western Design helped drive start-ups like Apple, Osborne and Sinclair. Some succeeded. Some failed. Some were acquired. Yet semiconductors started a long expansionist trend in the 1970s because of programmable microprocessors. Even though today's best devices are faster and smaller by orders of magnitude, they mostly follow a manufacturers primary design. Along with open-source hardware, open instruction set architectures could encourage innovation. While chip vendors now spend literally millions of dollars for proprietary instruction sets, the Berkeley RISC-V is freely available under license.

Growth in 2016 and beyond will likely come from many directions. To be certain, macro-economic conditions have to be conducive before consumers will pony up for new mobiles, IoT-enabled smart homes or wearable technology.

Until then we will keep watching the market. It took 'unconventional wisdom' to birth the industry; revitalization will also likely come from unexpected directions.

Publishing Editor Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Technical Contributor Mark Andrews
Senior Sales Executive Robin Halder robin.halder@angelbc.com +44 (0)2476 718979
Sales Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
USA Representatives Tom Brun Brun Media E: tbrun@brunmedia.com +001 724 539-2404
Janice Jenkins E: jjenkins@brunmedia.com +001 724-929-3550
Amy Rogers arogers@brunmedia.com +001 678-714-6775
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214
Circulation Director Jan Smoothy jan.smoothy@angelbc.com +44 (0)1923 690200

Chief Operating Officer Stephen Whitehurst stephen.whitehurst@angelbc.com +44 (0)2476 718970
Directors Bill Dunlop Uprichard – CEO, Stephen Whitehurst – COO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal, Jason Holloway.

Published by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. T: +44 (0)1923 690200 F: +44 (0)1923 690201 E: ask@angelbc.com

Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 F: +44 (0)2476 718 971 E: info@angelbc.com

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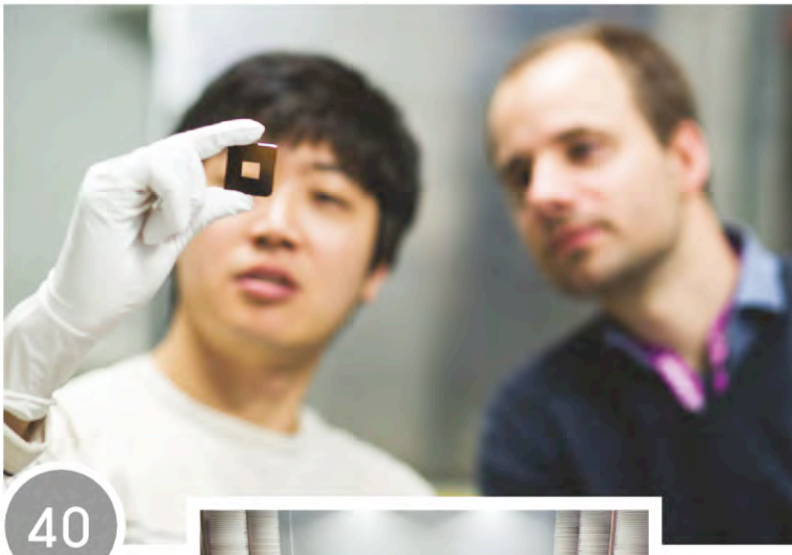

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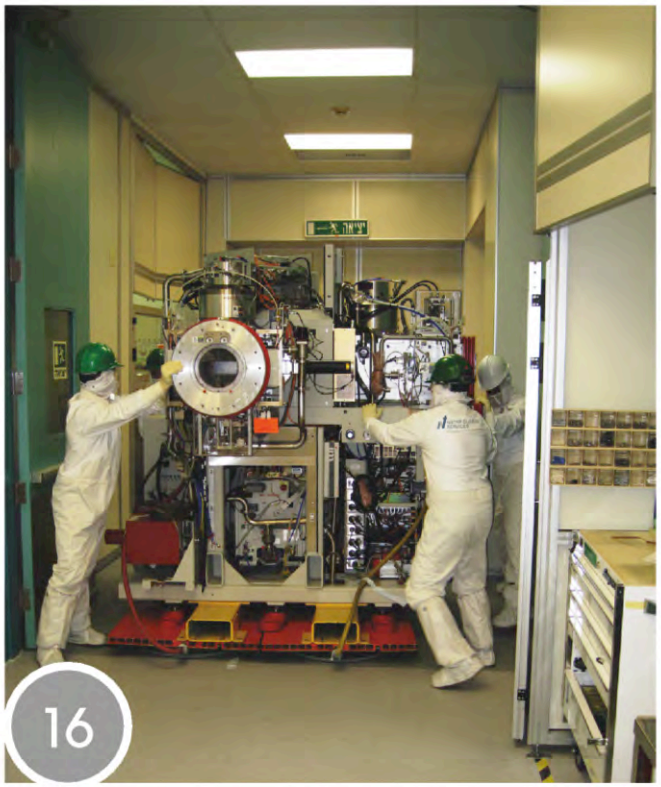

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GLOBAL FOUNDRIES PLAN 300 MM FAB IN CHINA

GLOBAL FOUNDRIES have signed a memorandum of understanding to drive its next phase of growth in China. Through a joint venture with the government of Chongqing, the company plans to expand its global manufacturing footprint by establishing a 300 mm fab in China. Global Foundries is also investing in expanding design support capabilities to better serve customers across the country.

"China is the fastest growing semiconductor market, with more than half of the world's semiconductor consumption and a growing ecosystem of fabless companies competing on a global scale," said Global Foundries CEO Sanjay Jha. "We are pleased to partner with the Chongqing leadership to expand our investment in support of our growing Chinese customer base."

The initial plan of the project includes upgrading an existing semiconductor fab to accommodate the manufacturing of 300mm wafers using Global Foundries' production-proven technologies from its Singapore site. The proposed joint venture will provide immediate access to a state-of-the-art facility, accelerating time-to-market with production planned for 2017.

"In recent years, Chongqing has followed the cluster model to vigorously develop the electronic information industry, becoming one of China's most important locations for intelligent end products manufacturing," said Huang Qifan, Mayor of Chongqing.

"During the period of China's thirteenth five-year plan, Chongqing will continue to develop the intelligent IC and other strategic emerging industries, and promote sustained and healthy economic development in the region. Global Foundries is a world-famous IC manufacturing company, and we welcome them to participate through cooperation to achieve mutual benefit and win-win. Cooperation between the two parties will help to enhance the production of intelligent IC technology in Chongqing, further improving the electronic information supply chain in Chongqing and the rest of China."

Global Foundries continues to strengthen its sales, support, and design services offerings in China, doubling over the past year with plans for continued growth. The company's current presence is anchored by world-class design centres in Beijing and Shanghai, which have extensive expertise in custom designs supporting a robust ASIC platform, coupled with foundry design capabilities for a variety of technology nodes.

These capabilities are complemented by key regional partners in its design and IP ecosystem.

NANOFOCUS INTRODUCES NEW INSPECTION SYSTEM

NANOFOCUS AG, developer and manufacturer of optical 3D surface measuring technology, has introduced a new measuring system μsprint hp-opc 3000 for the optical inspection of probe cards within the framework of the IS-Test Workshop in Munich.

μsprint hp-opc 3000 enables an innovative and future-oriented process step in wafer production. The process is specially designed for the requirements of wafer test locations with a variety of different probe cards as well as large-volume throughput. A pilot system is already installed at a renowned manufacturer of semiconductor elements.

Probe cards are special test devices that are used for standard function tests of wafers at the end of the so-called front-end process. This means, they are used after the functional structures of the electronic elements on a wafer are fully manufactured. The μsprint hp-opc 3000 system is responsible for ensuring that the wafers are in sound condition after testing, for reducing yield losses as well as for minimizing the time and number of complex maintenance cycles the probe cards are subjected to regularly. As wafers already completed the most important part of value creation with the manufacturing of the functional structures, damage during testing represents a significant economic loss. Furthermore, faulty probe cards can cause damage during wafer testing. Although such faulty probe cards can lead to a correct result of the functional test, they can cause unnoticed damage to a wafer rendering it unusable.

On the one hand, such incidents represent an economic loss due to recall actions, on the other hand, a minimized quality perception of the delivered products by the customer. Beyond that, using the μsprint hp-opc 3000 can shorten and/or specify repair cycles more clearly. This provides an important contribution to the reduction in operative costs when using probe cards.

μsprint hp-opc 3000 is a process-capable capacity tool. It can be integrated into process control systems via a SECS/GEM communication interface. The tool complies with all necessary and common standards required at front-end wafer test locations.

Meyer Burger awarded CHF 10 million contract for its diamond wire saws

MEYER BURGER has been awarded important contract for over CHF 10 million for its newest generation DW288 Series 3 diamond wire saws.

The newly launched DW288 Series 3 diamond wire cutting technology from Meyer Burger has been selected for the manufacture of high performance mono-crystalline silicon solar wafers by existing photovoltaic customer in Asia.

The customer plans to expand its production volume of mono-crystalline wafers to support the increasing demand for its high quality solar wafers. The contract value is over CHF 10 million. Delivery and commissioning of the systems is scheduled for the second half of 2016.

The DW288 Series 3 is the newest generation of Meyer Burger's successful diamond wire cutting technology which was introduced to the market at the beginning of 2016.

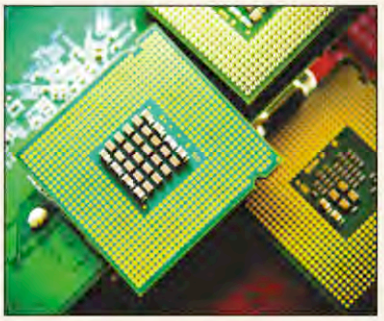
Since its launch, Meyer Burger has provided the photovoltaic market with a total of over 2.0 gigawatts of cutting capacity reflecting substantial orders for the DW288 Series 3.

With its newest generation of its environmentally friendly, water-based diamond wire cutting technology, Meyer Burger continues to significantly reduce manufacturing costs for solar wafers while gaining a significant share of the growing mono-crystalline silicon market.

Chip market to shrink in 2016?

THE GLOBAL SEMICONDUCTOR market will fall by 2.4 percent in 2016 to $327 billion before turning to modest growth in the following years, according to the European Semiconductor Industry Association referring to figures from the World Semiconductor Trade Statistics (WSTS) organization.

WSTS has overturned its previous prediction of growth in 2016 (see Analog, US to lead chip market growth) and delayed the prospect of growth. It now reckons that global market will grow in 2017 and 2018 led by the Asia-Pacific region and by optoelectronic, sensor and analog ICs.



For 2016, growth in optoelectronics (1.8 percent), sensors (7.6 percent), and analog (1.0 percent) is expected to be offset by declines in memory (-10.2 percent) and logic (-2.5 percent).

By geography, for 2016, declines are expected across all regions with the largest decline in Americas. This all-round declining prediction comes despite year-on-year growth shown by the Japanese marker in the first four months of 2016.

WSTS has come out as the most bearish of forecasters but close to IDC that recently forecast 2016 market contraction at 2.3 percent with the global market shrinking to $324 billion (see IDC joins forecasters predicting chip market fall). Two other market research firms, Gartner and TrendForce, have previously predicted a contraction of 0.6 percent.

SPTS RECEIVES REPEAT ORDER FROM HUATIAN TECHNOLOGY

SPTS TECHNOLOGIES, an Orbotech company and a supplier of advanced wafer processing solutions for the global semiconductor and related industries, has received a repeat order from Huatian Technology (Kunshan) Electronics Co., Ltd for its Sigma fxP physical vapor deposition (PVD) systems.

Huatian Technology, a subsidiary of the Chinese IC test and packaging services company, TianShui Huatian Technology Co., Ltd (TSHT), will deploy the additional Sigma fxP PVD systems to expand its existing capacity of 300mm packaging lines for under bump metallization (UBM) and CMOS image sensor (CIS) packaging services.

According to SEMI's February 2016 report, China is the largest regional market for packaging equipment with 30 percent of global demand, and has grown at a CAGR of 19 percent over the past 10 years.

In 2014, the Chinese government published the National Integrated Circuit Industry Development Promotion Summary, also known as the national "guideline." One objective of the guideline is for China packaging technology to achieve world-class levels by 2020.

"China aims to be self-sustaining in ICs, with a goal of becoming 70 percent self-sufficient by 2025. As a result, significant investments are being made throughout the domestic supply chain," stated Kevin Crofton, President of SPTS Technologies and Corporate Vice President at Orbotech. "With the purchase of these additional Sigma fxP PVD systems, Huatian is well positioned to meet the growing demand for wafer level packaging services from its global and domestic customers."

Mr Aimo. Xiao, CEO of Huatian Technology (Kunshan) Electronics Co., Ltd stated, "To implement our growth plan, it is important to partner with suppliers such as Orbotech's SPTS, which share our philosophy of technology innovation and success through the highest quality customer support. The Sigma fxP PVD system delivers first-class results at a low cost of ownership, which helps us remain cost competitive and grow our business. We look forward to working more closely with Orbotech-SPTS as we continue to build our 300mm packaging capabilities for the next phase of our growth."

David Butler, Vice President of Product Management and Marketing at SPTS, will be giving an invited talk on PVD technologies on April 21st at the 2016 Symposium on Advanced Packaging and System Integration in Wuxi, China. This premier conference is hosted by Yole Développement and NCAP China, the National Centre for Advanced Packaging.

The SPTS 300 mm PVD system for bumping applications comprises wafer degas, pre-clean and PVD modules for depositing UBM/RDL seed layers in advanced packaging schemes.

Cost of ownership savings can exceed 30 percent through a unique approach to wafer degassing, a high rate pre-clean and long life targets and chamber furniture. The same PVD modules can also be used to deposit Ti-Cu seed or Thick Al alloy redistribution layers (RDL) in CIS wafer level packaging.

Boston Semi Equipment secures additional investment

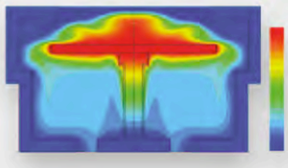
BOSTON SEMI EQUIPMENT, LLC (BSE), the semiconductor equipment company redefining the price-performance model for semiconductor test automation equipment, announced today that its senior investment partner has committed to a new round of capital funding. This additional investment is a vote of confidence in the company's new strategic direction and the market potential for BSE's product development activities.

BSE, founded in 2010 as a secondary equipment provider to the semiconductor industry, has been transitioning its business to become an original equipment manufacturer (OEM) of automation equipment for the handling and testing of semiconductor devices. BSE now develops and markets its own test handlers, wafer probers and custom designed automation equipment for the semiconductor market. "This additional investment is being used to complete new products and fund engineering projects to expand BSE's product offerings for our customers," commented Colin Scholefield, Executive Vice President, Boston Semi Equipment.

"Increasing the number of BSE-developed automation products for today's semiconductor test floor will enable our customers to come to one source for more of their test automation needs."

BSE also provides semiconductor manufacturers, OSATs and fabless companies with the legacy automatic test equipment they continue to use on their test floors every day. BSE's worldwide team of product specialists helps customers maximize the productivity of all BSE products.

Optimize the Thermal Performance of your Process Equipment.



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Diamonds could enables advances in nanotechnology

Nanomaterials have the potential to improve many next-generation technologies. They promise to speed up computer chips, increase the resolution of medical imaging devices and make electronics more energy efficient. But imbuing nanomaterials with the right properties can be time consuming and costly.

A new, quick and inexpensive method for constructing diamond-based hybrid nanomaterials could soon launch the field forward.

University of Maryland researchers developed a method to build diamond-based hybrid nanoparticles in large quantities from the ground up, thereby circumventing many of the problems with current methods. The technique is described in the June issue of the journal Nature Communications.

The process begins with tiny, nanoscale diamonds that contain a specific type of impurity: a single nitrogen atom where a carbon atom should be, with an empty space right next to it, resulting from a second missing carbon atom. This "nitrogen vacancy" impurity gives each diamond special optical and electromagnetic properties.

By attaching other materials to the diamond grains, such as metal particles or semiconducting materials known as "quantum dots," the researchers can create a variety of customizable hybrid nanoparticles, including nanoscale semiconductors and magnets with precisely tailored properties.

"If you pair one of these diamonds with silver or gold nanoparticles, the metal can enhance the nanodiamond's optical properties. If you couple the nanodiamond to a semiconducting quantum dot, the hybrid particle can transfer energy more efficiently," said Min Ouyang, an associate professor of physics at UMD and senior author on the study.

Evidence also suggests that a single nitrogen vacancy exhibits quantum physical properties and could behave as a quantum bit, or qubit, at room temperature, according to Ouyang. Qubits are the functional units of as-yet-elusive quantum computing technology, which may one day revolutionize the way humans store and process information. Nearly all qubits studied to date require ultra-cold temperatures to function properly.

A qubit that works at room temperature would represent a significant step forward, facilitating the integration of quantum circuits into industrial, commercial and consumer-level electronics. The new diamond-hybrid nanomaterials described in Nature Communications hold significant promise for enhancing the performance of nitrogen vacancies when used as qubits, Ouyang noted.

While such applications hold promise for the future, Ouyang and colleagues' main breakthrough is their method for constructing the hybrid nanoparticles. Although other researchers have paired nanodiamonds with complementary nanoparticles, such efforts relied on relatively imprecise methods, such as manually installing the diamonds and particles next to each other onto a larger surface one by one. These methods are costly, time consuming and introduce a host of complications, the researchers say.

"Our key innovation is that we can now reliably and efficiently produce these freestanding hybrid particles in large numbers," explained Ouyang, who also has appointments in the UMD Centre for Nanophysics and Advanced Materials and the Maryland NanoCentre, with an affiliate professorship in the UMD Department of Materials Science and Engineering.

The method developed by Ouyang and his colleagues, UMD physics research associate Jianxiao Gong and physics graduate student Nathaniel Steinsultz, also enables precise control of the particles' properties, such as the composition and total number of non-diamond particles. The hybrid nanoparticles could speed the design of room-temperature qubits for quantum computers, brighter dyes for biomedical

imaging, and highly sensitive magnetic and temperature sensors, to name a few examples.

"Hybrid materials often have unique properties that arise from interactions between the different components of the hybrid. This is particularly true in nanostructured materials where strong quantum mechanical interactions can occur," said Matthew Doty, an associate professor of materials science and engineering at the University of Delaware who was not involved with the study. "The UMD team's new method creates a unique opportunity for bulk production of tailored hybrid materials. I expect that this advance will enable a number of new approaches for sensing and diagnostic technologies."

The special properties of the nanodiamonds are determined by their nitrogen-vacancies, which cause defects in the diamond's crystal structure. Pure diamonds consist of an orderly lattice of carbon atoms and are completely transparent. However, pure diamonds are quite rare in natural diamond deposits; most have defects resulting from non-carbon impurities such as nitrogen, boron and phosphorus. Such defects create the subtle and desirable color variations seen in gemstone diamonds.

The nanoscale diamonds used in the study were created artificially, and have at least one nitrogen vacancy. This impurity results in an altered bond structure in the otherwise orderly carbon lattice. The altered bond is the source of the optical, electromagnetic and quantum physical properties that make the diamonds useful when paired with other nanomaterials.

Although the current study describes diamonds with nitrogen substitutions, Ouyang points out that the technique can be extended to other diamond impurities as well, each of which could open up new possibilities.

"A major strength of our technique is that it is broadly useful and can be applied to a variety of diamond types and paired with a variety of other nanomaterials," Ouyang explained. "It can also be scaled up fairly easily. We are interested in studying the basic physics further, but also moving toward specific applications. The potential for room-temperature quantum entanglement is particularly exciting and important."

Answers for Today's Packaging Needs

Creating smaller packaged IC devices with more input and output connections led to the creation of wafer-level packaging (WLP). Yield Engineering Systems details the benefits of vacuum cure processing for fan out wafer-level packaging.

CONSUMERS DEMAND for increased mobility and high functionality with ease of use is driving the need for 3D integration. Sophisticated packaging techniques are required to achieve platforms with reduced footprint and high performance.

This increased demand for 3D integrated devices requires more complex and sophisticated packaging techniques and processes. To save money and achieve higher yields requires equipment that combines quality, functionality, flexibility, and control for the process engineers. Yield Engineering Systems' (YES) PB Series automated and manual vacuum cure ovens are specifically designed to address the concerns of process engineers who are now faced with new challenges. One key challenge is the need to use new dielectric materials and create new processes to achieve the desired results.

The Use of Dielectric Materials – Wafer-level packaging (WLP)

Before the year 2000, polyimide and related materials were most often used as a stress buffer layer. Needing only the following, these layers were not critical and the cure process could be done in various methods.

- High temperature stability for multiple process and reflow
- Low outgassing
- Good adhesion to dies
- High elongation for die stresses

Today's material demands must support multilayer RDL and WLP packaging requirements. Some of these demands are:

Image 1: The YES VertaCure is equipped with pre-heated and filtered N_2 purge in horizontal laminar flow.

- High temperature stability for multiple processes and reflow
- Fast curing for multiple layers to keep up with throughput
- Low temperature curing for sensitive devices
- Chemical resistance to development solvents
- High elongation for die stresses
- Water-based development for less environmental impact
- Good adhesion to previous layer(s)

The objectives of a proper cure process are to:

- Complete the imidization process
- Optimize film adhesion performance
- Remove all residual solvents and extraneous gases
- Remove photosensitive components
- Create highly cured dielectrics for good adhesion
- Enable faster and lower temperature cures of PI and PBO
- Lower shrinkage - Lower stress
- Increase elongated toughness and resistance to crack propagation
- Decrease shrinkage, tension and brittleness

To convert the polyimide precursors to a stable film, proper temperature with extended bake (for polyimides) is required for complete imidization; it also drives off the N-methylpyrrolidone (NMP) casting solvents and orients the polymer chains for optimal electrical and mechanical properties.

Desired process conditions for properly cured materials

Controlled temperature ramp rates (heating and cooling) need to be characterized for the desired material. The imidization rate of the precursors needs to be controlled to take into account differences in the thermal expansion coefficient between the film and the underlying substrate. If the imidization rate is not controlled properly, there can be localized mechanical stress variations across the wafer. In addition, if the casting solvents evolve non-uniformly across the wafer, film thickness that is not uniform can occur due to uneven imidization. Mechanical stress variations can be observed as wrinkled film or as distorted metal lines in the structures under the film layer. The film can also delaminate because adhesion performance has not been optimized. Mechanical stress variations can affect yield and reliability. It is critical that controlled temperature ramp rates are used to provide a larger process window for proper curing.

Non-uniform heating can cause a skin to form on the surface of the polyimide film during the curing process. This skin can prevent the efficient evolution of the casting solvents and other volatile gases. If a cured film still has residual solvents or other volatile gases, then localized areas of the film can rupture in a phenomenon known as 'popcorning.' These ruptures occur in subsequent process steps in tools that have either a high vacuum or a high temperature environment. This rupturing is due to the sudden release of gas bubbles/solvents trapped in polyimide film that has not been properly cured. In addition, a 'solvent-free' film will minimize the queue time needed to allow for outgassing when the next process step is a high vacuum process, such as metallization.

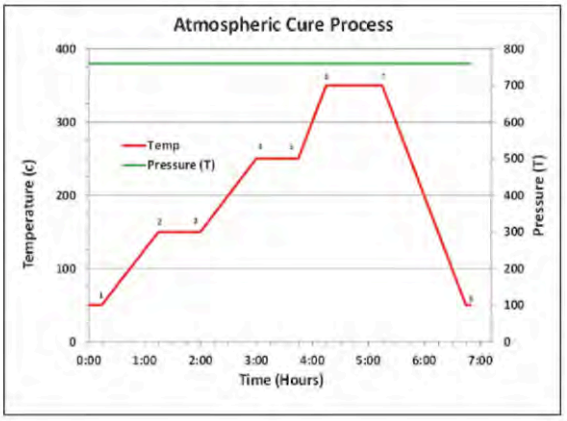

Figure 1: Atmospheric cure process graph. **Nodes 1-6** - Vapor diffusion across flow boundary layer limits solvent evaporation rates; low temp, dwell steps required for evaporation. As solvents evolve, imidization of polyimide precursors occur, affected by temp. ramp rates. Atmosphere is ~23% O; high-flow N_2 is required to reduce O. **Nodes 6-7** - Process held at temp. needed for complete imidization of polyimide film. High flow of N_2 may still be required. **Nodes 7-8** - Process temp. is ramped down; curing process complete.

Environment oxygen level needs to be <10 ppm. The presence of oxygen in the process chamber inhibits the proper crosslinking of the polyimide precursors to polyimide thin film. The result is incomplete imidization which leads to a brittle film and variable stress in the polyimide film on the substrate. Also, ambient oxygen darkens the film. Film transparency is critical when multiple layers are used during subsequent processing. For multi-layer processes, alignment marks for a process sequence can be obscured by layers of low transparency polyimide films. In summary, pure nitrogen (ambient) is required to reduce the level of oxygen in the process chamber.

Background O_2 level control is essential. Air cooling outside the door opening that enables the door and sealing O-ring temperatures to be maintained below 200°C while the oven operates is required for optimal performance. Process temperatures up to 550°C can occur, which makes meeting this requirement difficult. Superior O_2 leakage control through the door is maintained by employing double door gasket techniques. Low pressure nitrogen is flowed between

Image 2: YES-PB12-2P-CP manual vacuum cure oven

The Preferred Method!

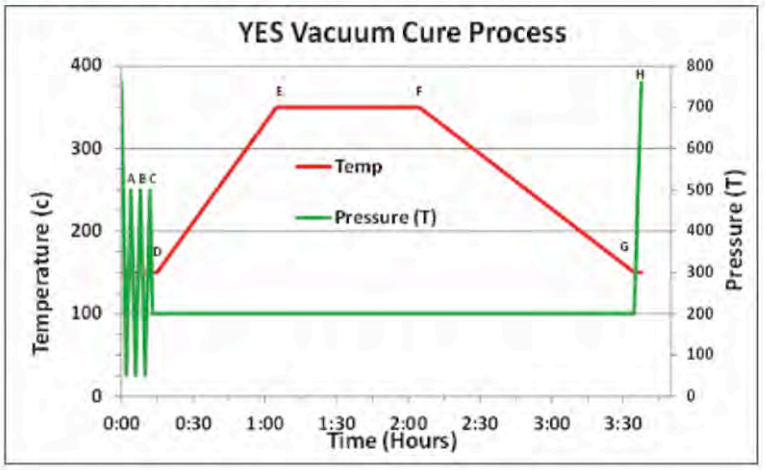

Figure 2: Yield Engineering Systems' vacuum cure process graph using a YES-PB12-2P-CP.
Points A-D - 3 short vacuum/hot N_2 purge cycles reduce O level quickly. Boiling point of NMP casting solvents at 50 Torr is 135°C, so first vacuum pull of purge cycle sets polymer to improve thickness uniformity.
Points D-E - A laminar flow of hot N_2 purge balanced against a vacuum gives a 200 Torr pressure level to continuously remove oxygen. At reduced pressure, NMP solvent is efficiently removed without skin forming; this enables a controlled ramp to imidization temp.
Points E-F – Temp. held as required for full imidization of polyimide film.
Points F-H – Temp. is ramped down; chamber is vented; curing process complete.

the two gaskets. If the inner seal should fail, the seal will 'leak' nitrogen inside the oven, not atmosphere, thus maintaining low oxygen levels.
Proprietary three cycle pre-process pump/purge O_2 level reduction aids the cure process. The chamber is pumped down to 50 Torr followed by a 600 Torr hot nitrogen purge back-fill producing a factor of 50/600 times background O_2 reduction during each cycle. This results in less than 10 ppm O_2 during ramp to process.

Management of cure oven conditions is essential. Maintaining critical O_2 levels, cure temperature, and pressure control for polymer cure ensures success. The polymer curing process is quite complicated and demanding in nature. Temperature uniformity is essential to avoid cracks in the polyimide layer and color variations. There are three major inhibitors affecting the curing of polyimide films: Oxygen, moisture and solvents.

- Oxygen inside the polymer can only be removed by inducing a pressure differential such as by an external vacuum.
- Water boils at 39°C at 50 Torr, a significant drop from the 100°C in atmosphere, making it easier to remove water at reduced pressure.
- NMP solvent boils at 205°C in atmosphere. Some polymers start imidization around 205°C, hence it is difficult to avoid the formation of a skin on the top of the polymer before all the solvent is removed in an atmospheric pressure bake. At a reduced pressure, in the 50 Torr range, NMP boils at 120°C. Therefore, all the solvents can be safely removed before imidization initializes. If the polymer surface is imidized before all the inhibitors are removed, it may result in wrinkles, cracks, discoloration and outgassing during any subsequent process steps. (See figure 1 + 2)

Observations of polyimide film cured under vacuum:

1. Process time for ramping the temperature to cure temperature is reduced. The reduced pressure enables the efficient evolving of NMP solvents, thereby eliminating the need for temperature dwell steps.
2. No wrinkles in the film. Imidization rates can be better controlled when casting solvents are efficiently evolving from the film. As a result, the controlled temperature ramp rates can be adjusted to provide a larger process window for the proper curing of a polyimide film.
3. No 'popcorning.' At this reduced pressure the NMP solvent is efficiently removed without any skin being formed on the polymer. There are no bubbles of solvents; no extraneous gases trapped in the polyimide film. A very low solvent load in the film should help with productivity due to reduced queue time needed for outgassing
4. The amount of nitrogen needed to decrease oxygen levels is reduced. Three short vacuum/hot N_2 purge cycles reduce the oxygen level quickly because oxygen is removed faster in a vacuum.
5. Film is transparent. A steady laminar flow of hot N_2 purge balanced against a vacuum gives a 200 Torr pressure level that continuously removes oxygen, keeping levels <10 ppm.
6. For improved wafer cleanliness, the laminar flow of the pre-heated N_2 is preferred over recirculating the N_2 flow from a standard atmospheric bake oven.

Conclusion

Materials have expanded to meet the diversity of processes now common in semiconductor manufacturing.
These dielectric materials consist of:

- Polyimides
- PBO (Polybenzoxazoles)
- BCB (Benzocyclobutene – Cyclotene)
- Epoxy 'hybrids'

Uses depend upon the number of layers, low-k dielectric layers, and type of device as well as device properties, type of application, throughput, wafer size, technology node, environmental considerations and more.

Process control of the imidization rate of the material is a crucial factor in the proper curing of a film. This control is enhanced when casting solvents can be efficiently evolved from the film. Reduced ambient pressure enables the efficient evolving of solvents, without the use of temperature dwell steps. As a result, temperature ramp rates can now be optimized to provide a larger process window for the proper curing.

As planarization continues, dielectric materials and process are critical. Material properties affect package reliability. New requirements continue to change. New chemistries, new processes…Ever changing for a better tomorrow.

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PRODUCTIVELY MANAGING EQUIPMENT RELOCATIONS

Manufacturing consolidations have led to industry-wide change. When fabs open or close, relocating valuable process tools is a key consideration. As specialist NSTAR explains, making a move productive and efficient takes a trusted partner.

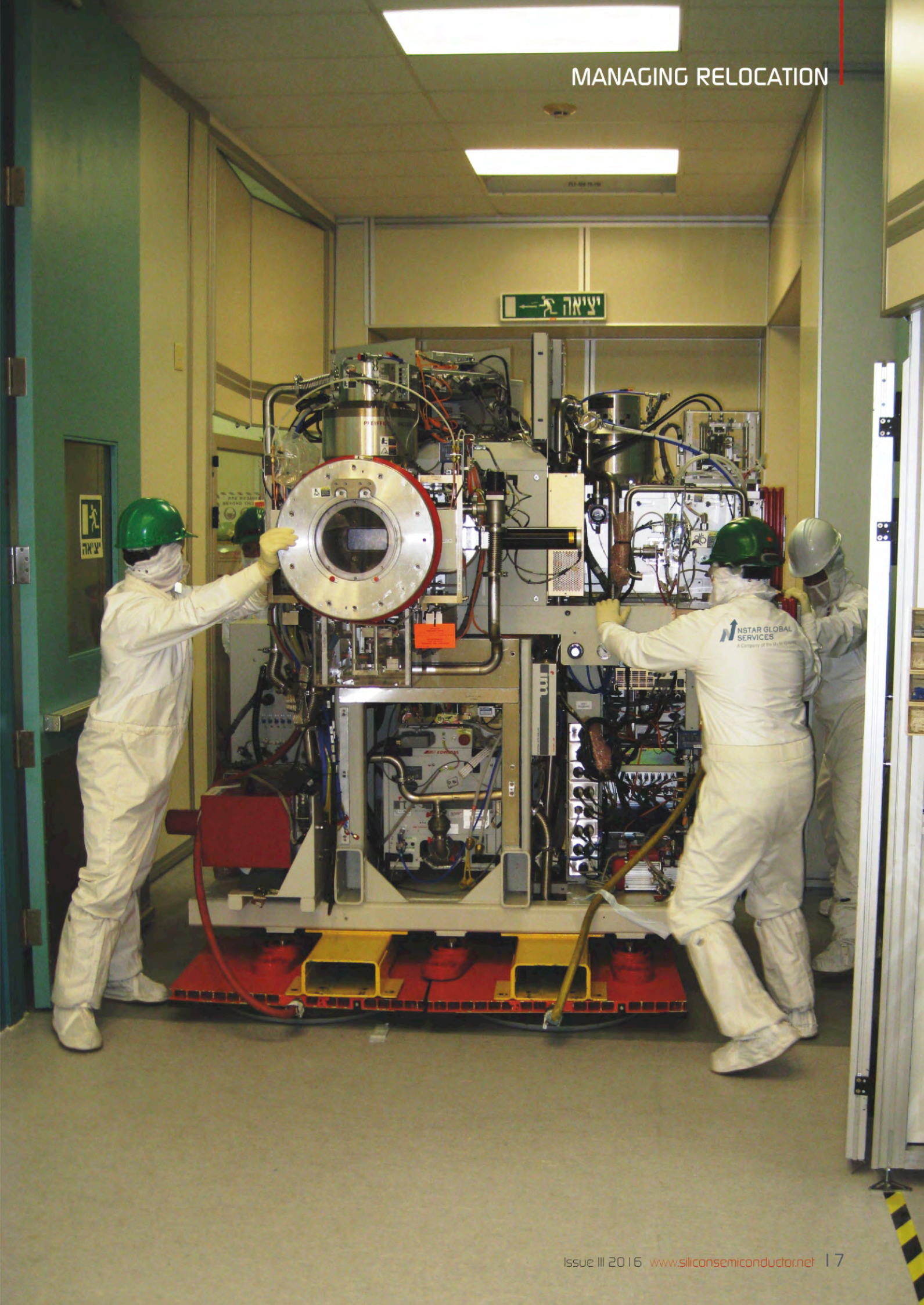
OVER THE PAST FEW YEARS, the secondary market for 200mm semiconductor manufacturing equipment has been on a roller coaster ride. First the market declined, causing as many as two hundred 200mm fabs to close, resulting in an estimated 6,000 used semiconductor tools coming onto the market. This was followed by a resurgence in added capacity driven by new applications related to mobility, sensing and the Internet of Things (IoT) as well as refurbishment of 200mm fabs to leverage legacy node silicon and alternative materials process tools to build devices that do not require the capacity of 300mm wafers. Industry consolidation has further added to the number of high quality process tools moving across regions and to different countries.

Many plant owners are outfitting 200mm and other fabs with refurbished tool sets purchased on the secondary market. Considering that a large number of these tools are located at manufacturing facilities scattered across the globe, removing process equipment from a particular factory—either to relocate the asset, resell it, or scrap the tool—can be a monumental logistical nightmare if not handled correctly. This article discusses the complexity of semiconductor equipment relocation, using two case studies to illustrate best practices.

Decontaminating, decommissioning and relocating complex process tools is a highly specialized business that requires very specific skills, and considerable expertise. There are two paramount concerns: to protect the value of the asset, and, to ensure that the decommissioning and relocation is conducted safely. A third element—time—also drives some moves when relocating assets to another facility is done because the receiving fab operator needs the tool to be brought up to full capacity as rapidly as possible.

Semiconductor chips are built in fabs and foundries that use extremely sophisticated equipment requiring a variety of toxic gases, chemicals and high electrical power. The decommissioning and relocation process is built around safety as the primary concern. The process for de-installation starts with 'fingerprinting' the tool so that its as-is condition is documented, recording the system functionality, the last qualification records and creating a ghost image of the tool software. Then, the system is decontaminated: chemical and physical hazards are removed, and any process gases or liquids are flushed/purged. The system is next disconnected from all utilities, all lines are capped or plugged, and any loose parts are individually labelled, wrapped and packed into shippable containers along with necessary documentation. Finally, the process tool itself is rigged, packed and crated for transport, and the site is remediated for any environmental impacts resulting from prior manufacturing operations.

At every step along the way, the de-installation process is documented; following proper safety protocols is critical. (For example, in some cases, the use of hazardous material suits and self-contained breathing apparatus are required.) The key to successful equipment relocation is meticulous planning, rigorous project management and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adherence to best known methods (BKM), all with a strong overlay of 'safety first.' Depending on the project size, teams should include a project manager, a safety manager and enough engineers/technicians to execute the project, along with any specialized equipment for loading, delivery and on-site setup if the tool is moving to a new operational location. The complexity of the project is also determined by whether the tool or tools are in a working fab—if manufacturing operations are ongoing, the decommissioning and relocation project must be designed to not impact ongoing production.

Case studies

One recent case involved decontaminating, decommissioning, disassembling, moving out/crating, shipping, uncrating and installing over 70 semiconductor process tools, and ancillary and support equipment within live production environments across the globe at different integrated device manufacturer (IDM) locations. The IDM contracted M+W Group as the general contractor and NSTAR Global Services as the project management team to handle the relocation. It began with the de-install process in Israel and concluded with installation in Singapore.

The relocation team provided technical resources who liaised with the client's tool owners to provide a concise snapshot of the tools' fingerprint prior to decommissioning (which included functionality audits, making ghost images of hard drives, and last qualification records). Following the steps previously outlined, and using BKMs, the tools were disassembled and loose parts were individually labelled, wrapped and packed into shippable containers. Each tool travelled with a complete parts inventory assembled prior to crating, with all pertinent shipping documents provided.

At the time de-installation was taking place in Israel, the team was simultaneously preparing the receiving site facility in Singapore to reduce tool downtime, enable full integration and ensure a smooth transition of the production process. The same engineers and technicians who handled the de-installation performed the reinstallation to ensure continuity of tool knowledge. Most importantly, the entire project was achieved with zero safety incidents.

A second relocation case study involved moving tools from a deactivated facility, with tools destined for installation in multiple locations for reinstallation. One hundred semiconductor process/metrology tools required decontaminating, decommissioning and rigging-out from a facility in Taiwan that had closed and was no longer in production. This situation creates an entirely different set of challenges and site restrictions. The tool inventory had been sold to various companies and brokers with the understanding that a single general contractor (GC) would control the overall site management. The GC mandated that all documentation and discussions be conducted in Taiwanese. To facilitate these conditions, the company assigned a bilingual Asia project manager who assembled a team of Taiwanese resources comprising a safety officer, lead engineers, engineers and technicians. All team members were involved in daily meetings with the safety officer during the ongoing tool removal, and site walks were conducted three times a day. Throughout the project, safety protocols were strongly emphasized. Even under drastically different conditions, the project was successfully completed without incident.

Conclusion

As illustrated in this article, managing the logistics of semiconductor equipment relocation is an extremely complex process, with many and varied challenges that differ from one situation to another—all depending on tool locations, conditions at both originating and receiving sites, government restrictions, etc. Relocating semiconductor equipment requires a specialized skill set, and should not be undertaken in an ad hoc manner. Rather, for optimal outcome in semiconductor, flat-panel display and solar manufacturing industries it is best to contract with a company specializing in equipment decommissioning, decontamination and relocation services such as NSTAR Global Services (M+W Group).

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Wafer defects can't hide from Park Systems

Atomic Force Microscopy (AFM) leader Park Systems has simplified 300mm silicon wafer defect review by automating the process of obtaining high-resolution 3D images, making it faster and simpler than ever before.

SEMICONDUCTOR MANUFACTURERS have options for defect review once inspection tools have identified potential flaws on bare silicon wafers. While conventional AFM provides data-rich 3D images, the process is slow compared to 2D, SEM-based techniques. A new AFM process developed by Park Systems changes that equation like none other.

Park Systems (Suwon, Korea and Santa Clara, California, USA) is one of the leading pioneers of atomic force microscopy (AFM) for semiconductor manufacturers and researchers. The company's founder (Sang-Il Park, PhD) led early efforts to commercialize the technology after being an integral part of AFM's development team at Stanford University in the 1980s.

Park Systems made the extreme, high-resolution 3D imagery of AFM commercially practical, going on to develop products and software for surface roughness measurement in hard disk media that became an industry standard (the Park HDM series product family). Park's AFMs are also 'non-contact' review tools, which eliminates the possibility of tool tips accidentally touching surfaces and possibly damaging wafers under review.

While quality, data-rich images have been a hallmark of Park's AFMs from the beginning, this extreme quality came at the price of speed and simplicity. The company subsequently automated AFM scanning for disk media and has now brought a similar approach to reviewing defects of interest (DOI) on silicon wafers up to 300mm. Its hardware and software also support extreme ultraviolet (EUV) reticle photo masks, a critical step in creating future 450mm silicon wafers.

Finding silicon wafer DOIs is challenging. All bare silicon wafers have a unique crystalline structure that is prone to small defects (Figure 1)that may be one nanometer or smaller. Manufacturers determine threshold sizes of interest along with shape and

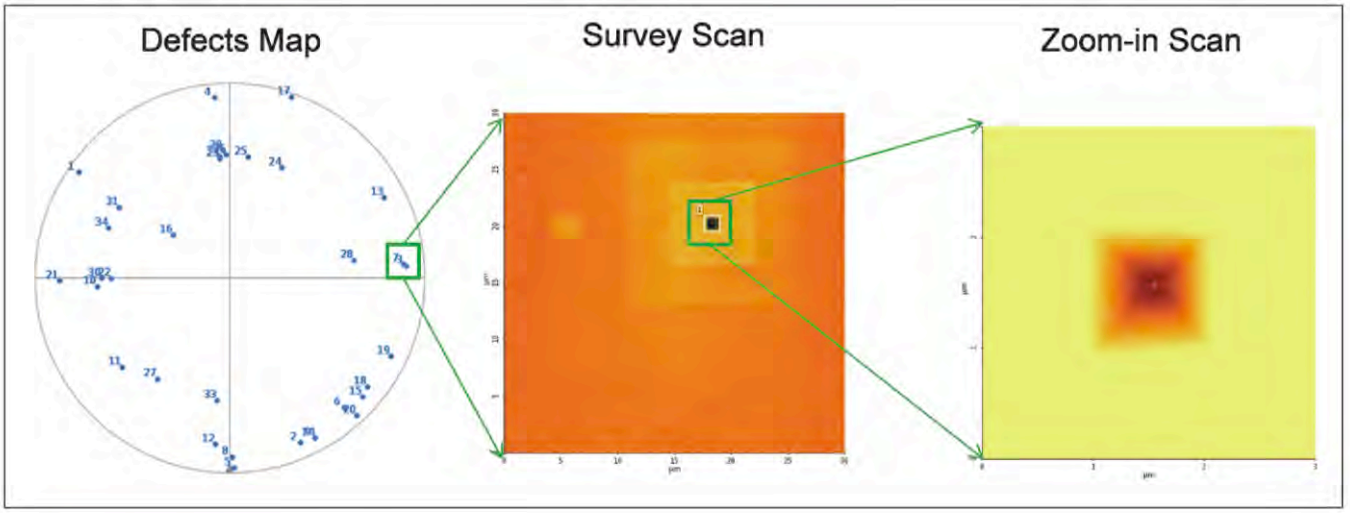

Figure 1: After coordinate mapping, ADR AFM will automatically perform a survey scan, zoom-in, processing, analysis and classification of each defect.

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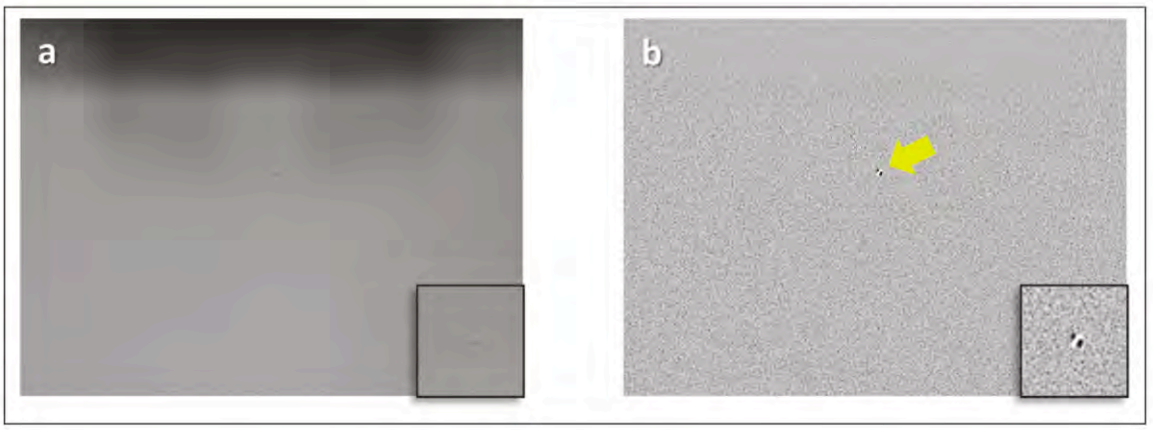


Figure 2: Images collected via (a) standard vs. (b) enhanced vision of a bare silicon wafer with one small defect. The insets show magnified views. The small defect is easily observable in enhanced vision.

depth characteristics that need attention. But while thresholds vary by manufacturer, it is clear that shrinking device geometries will impact whether defects once considered too tiny for concern could present problems for next-generation devices. There are a variety of laser light scattering techniques and process tools for inspecting wafers quickly, scanning hundreds or even thousands per hour. But inspection is just the beginning. A follow-up review by scanning electron microscope (SEM) or AFM takes inspection coordinates and zeros in on each location to image the defects. While SEM review is relatively quick, it cannot reveal much detail beyond a 2D image: a defect's 'X' and 'Y' dimensions. AFM goes much farther, creating X, Y and Z 3D images along with detailed topographic maps that further help identify and characterize an imaged DOI. AFM reveals defect details that SEM can routinely miss.

Park's AFM defect review is highly accurate, which is a key ingredient for success in an industry that measures in microns and nanometers. The accuracy of their AFMs is so great that the company holds a roughly 90 percent share of the market for hard disk drive defect review systems.

"Whether the defect is on a silicon wafer or the surface of hard drive media, the key is how accurately the review device locates it and delivers the information needed for proper defect classification. SEM may give

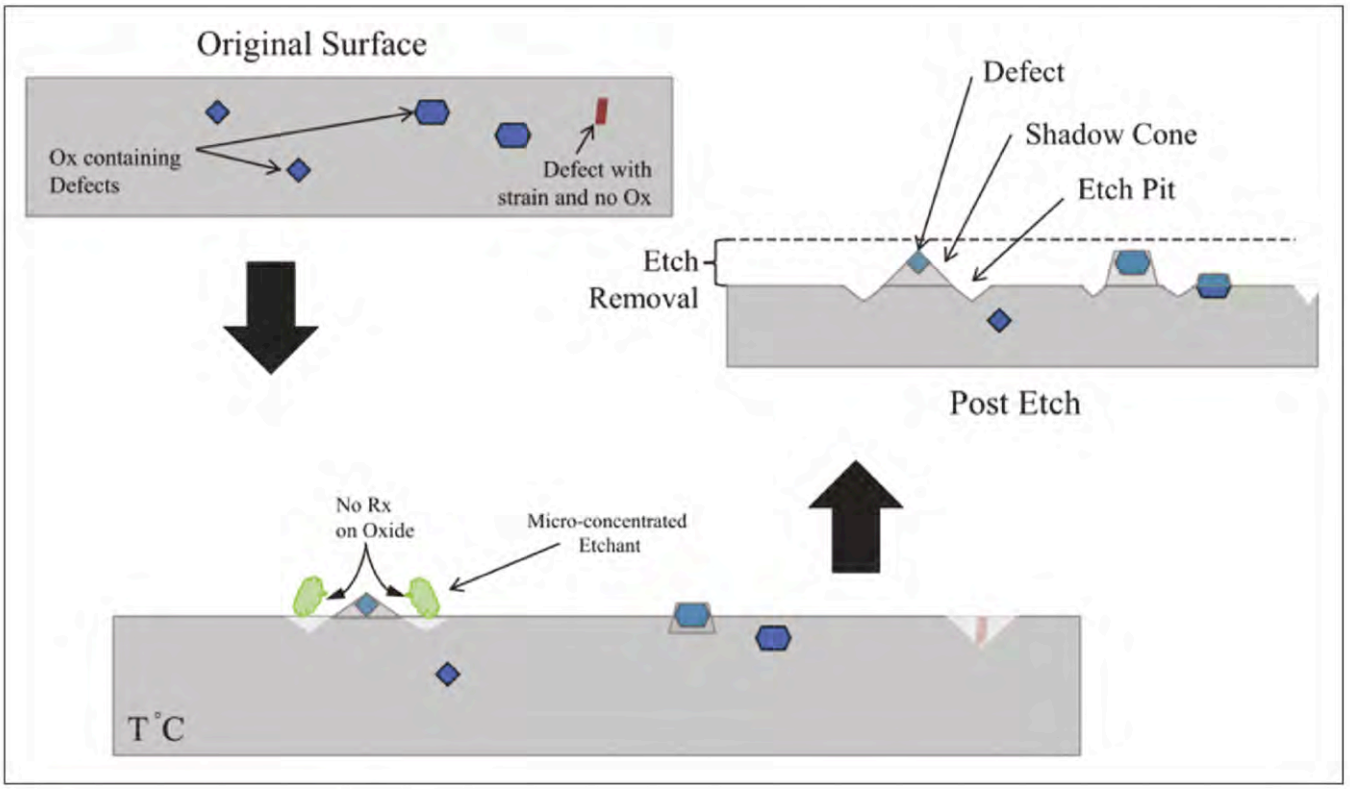


Figure 3: Schematic of the process used to decorate crystal imperfections for defect inspection.

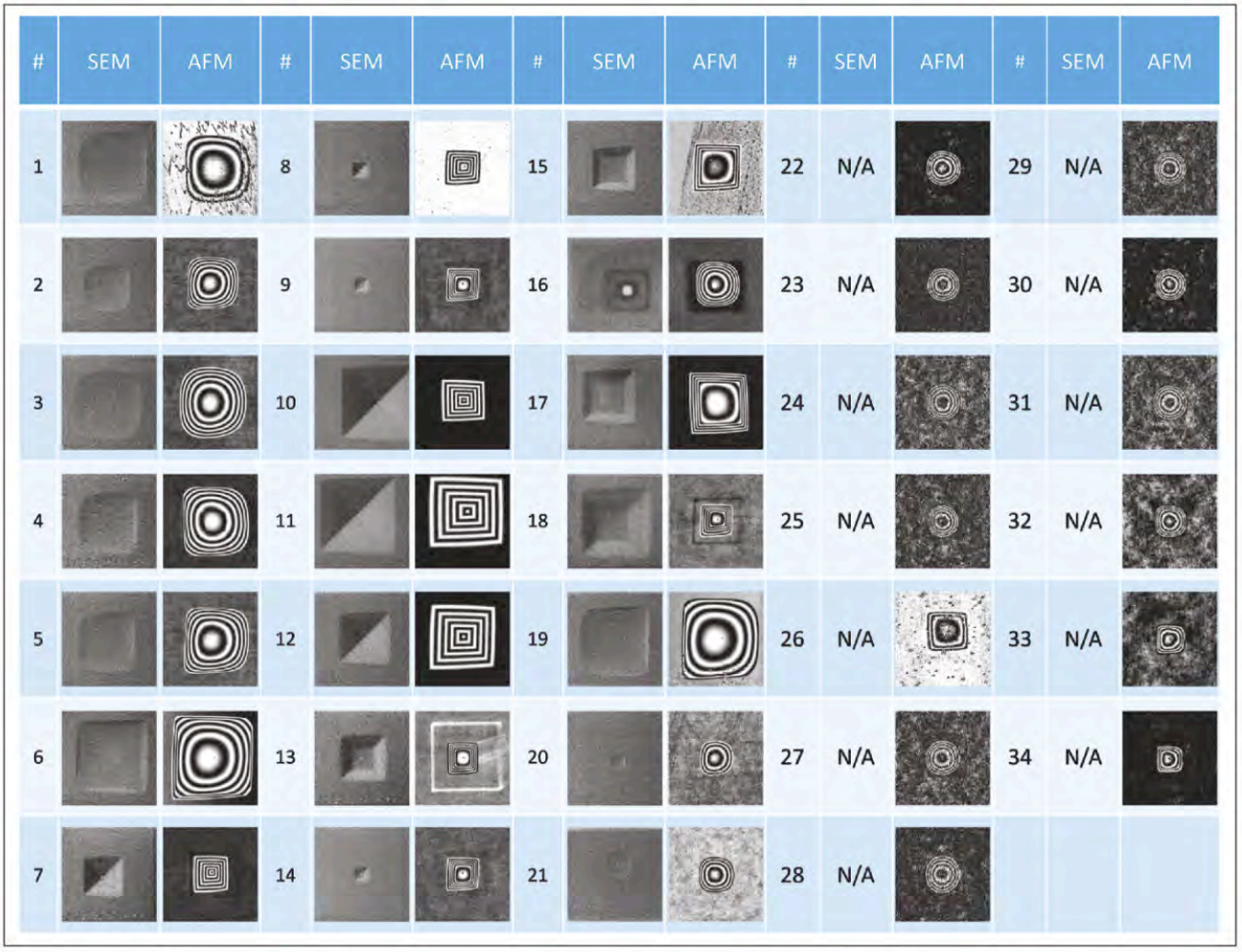


Figure 4: Defect review results with ADR AFM vs. SEM are shown. ADR AFM was able to locate and image all defects; SEM did not find defects 22 to 34. AFM and SEM images are rotated 180 degrees with respect to each other.

a quick image, but it lacks the information that can be provided by AFM (see figure 4).

"As a reference tool, AFM is the 'go-to' technology. Other AFMs can be a challenge to operate, so Park Systems addresses the problem with ADR: automatic defect review. We automated defect review and simplified it, so any technician can start the review process, and then simply walk away to do other tasks while the ADR AFM is operating," said Ardavan Zandiatashbar, PhD, Park's senior applications scientist.

While different manufacturers have varying approaches to how they handle silicon wafer defects, all likely agree that better data about a particular defect determines whether it is serious enough to affect lithographic processing, or whether defects are so great in number and size that a wafer should be rejected outright.

"We started with hard drive media defect review. Manufacturers needed to know the source of defects for failure analysis purposes. While SEM can give a quick image, its image can't easily tell you if a defect is a pit or a bump or how tall or how deep it is. This is where AFM comes in; it helps you to identify and classify defects accurately and completely. We do what others cannot do," Zandiatashbar said.

Wafer defects in Park's study typically fall into eight basic categories—additional categories in different wafer surface reviews are possible. Some defects can't be classified at the inspection stage and may not fit into a typical category even after AFM review. But through AFM, the manufacturer will definitely know a defect's size and depth; they can apply their own standards to determine what actions should be taken.

"Many manufacturers want to use AFM routinely, but locating the defects and linking the AFM to inspection tools were critical issues previously. Results from conventional AFMs depend on the skill of the operator. We eliminated those issues by automating the process. Now, instead of reviewing just a few defects per day through laborious efforts and changing

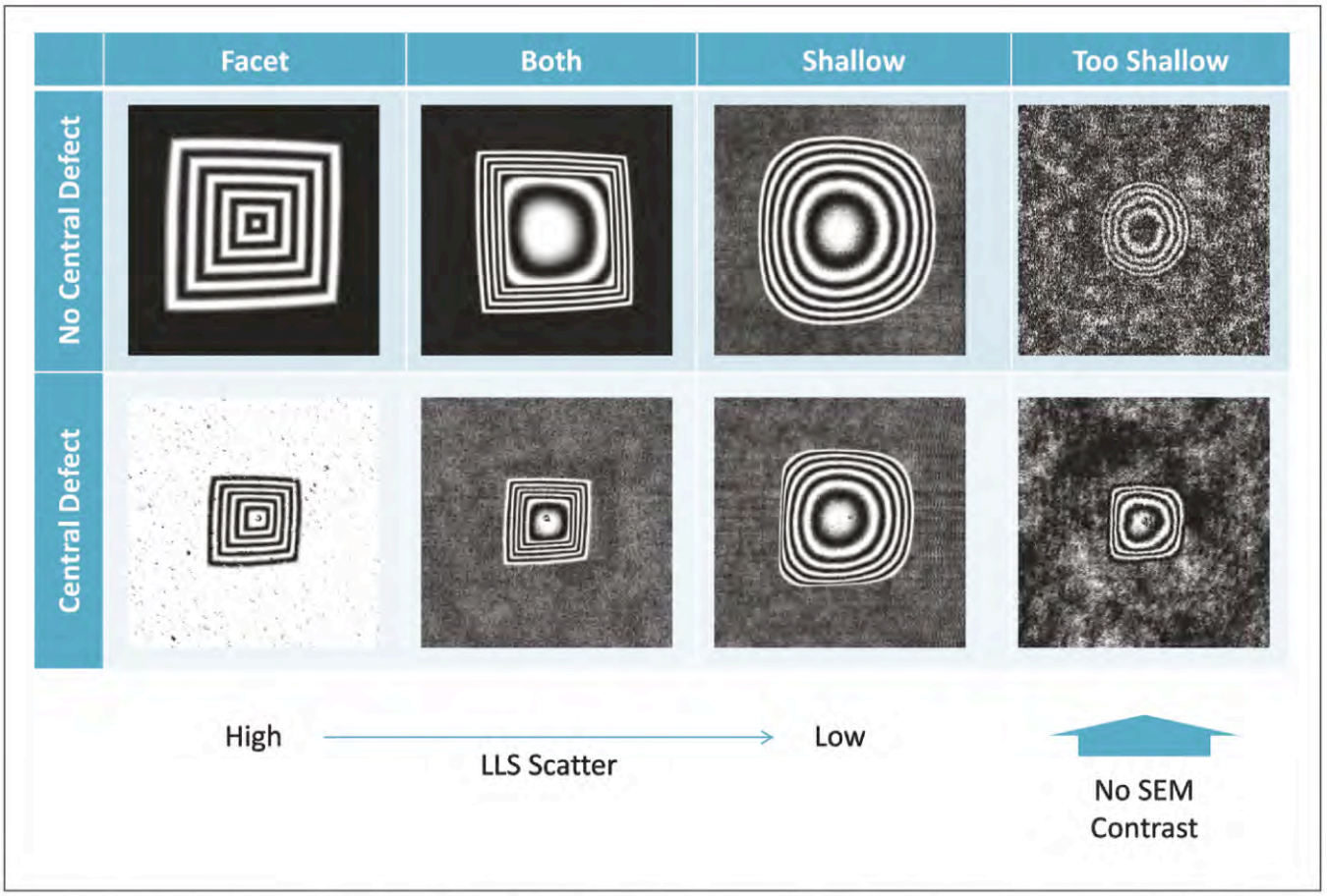


Figure 5: Defect classification based on the AFM data.

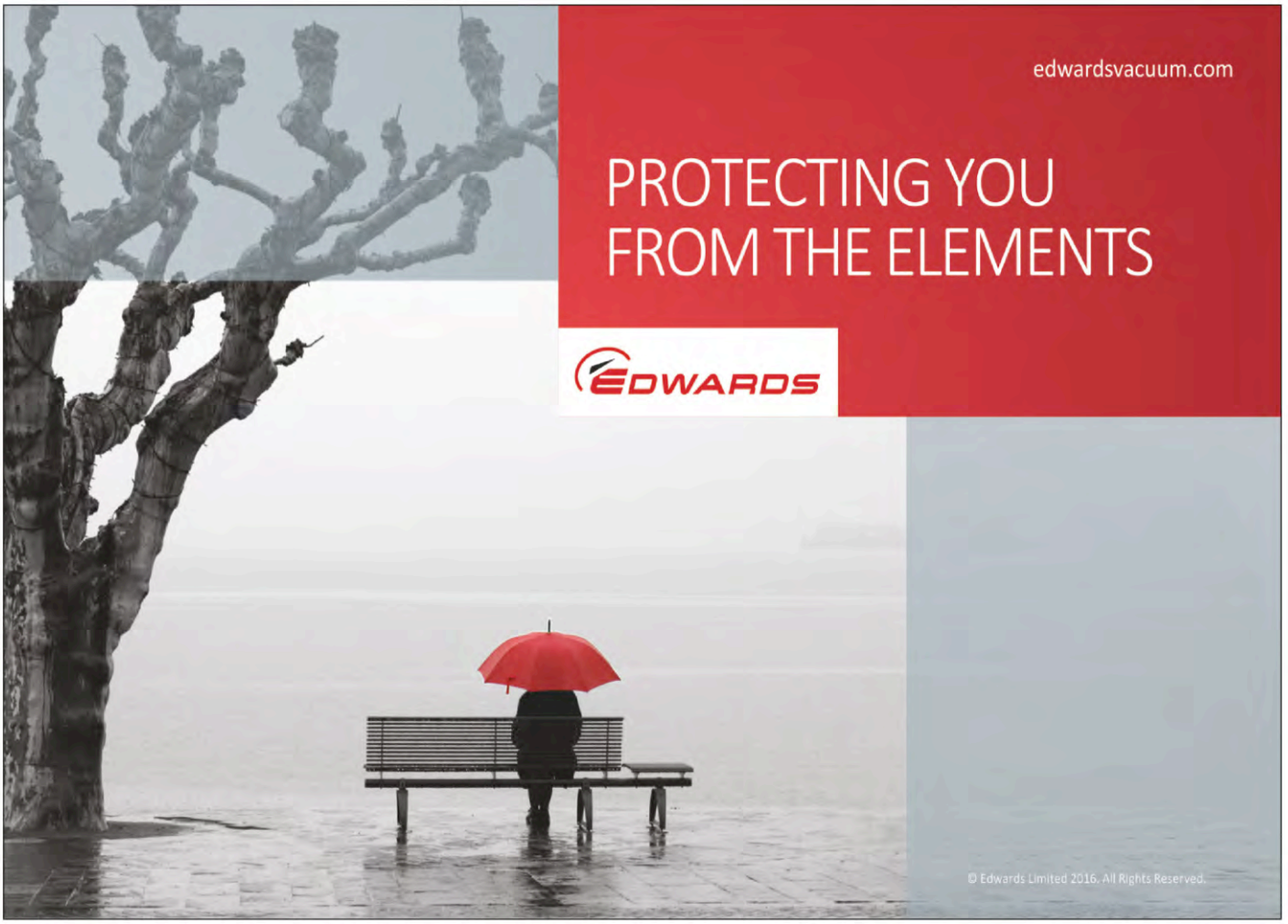
numerous tool tips, Park's ADR AFM can image and fully characterize between four and 10 defects per hour. A technician can start ADR and let it run 24/7. Manual AFM review proceeds only as quickly as a skilled operator can function," he added. "Park's ADR AFM is a turn-key solution."

In addition to automating the review process, Park's non-contact approach to AFM does not alter the wafer's surface in any way, meaning every wafer reviewed can go onto further processing as needed. SEM-based review processes have another issue beyond quality of data. Their electron beams also have the potential to 'burn' scan areas (see figure 6). This effect is typically more critical for photo-resist layers, but any disruption of a wafer's surface area can affect yield or other important factors.

The differences in results obtained using Park Systems ADR AFM compared to SEM-based results are dramatic. In a test conducted by Park, a wafer containing surface defects was reviewed using both SEM and AFM-based techniques. The ADR AFM utilized was from Park's NX-WAFER family of products. 34 defects identified at the inspection stage were candidates for review. The first 21 defects were imaged by SEM, which delivered aerial, 2D views without sufficient information about the depth or out-of-plane dimensions. The remaining 13 defects were not found by SEM despite identification during a laser light scattering (LLS) inspection (see figure 4).

Park's ADR AFM was able to find all 34 defects. The SEM had found defects down to a certain size threshold; those imaged by ADR AFM were typically

The differences in results obtained using Park Systems ADR AFM compared to SEM-based results are dramatic. In a test conducted by Park, a wafer containing surface defects was reviewed using both SEM and AFM-based techniques. The ADR AFM utilized was from Park's NX-WAFER family of products. 34 defects identified at the inspection stage were candidates for review.



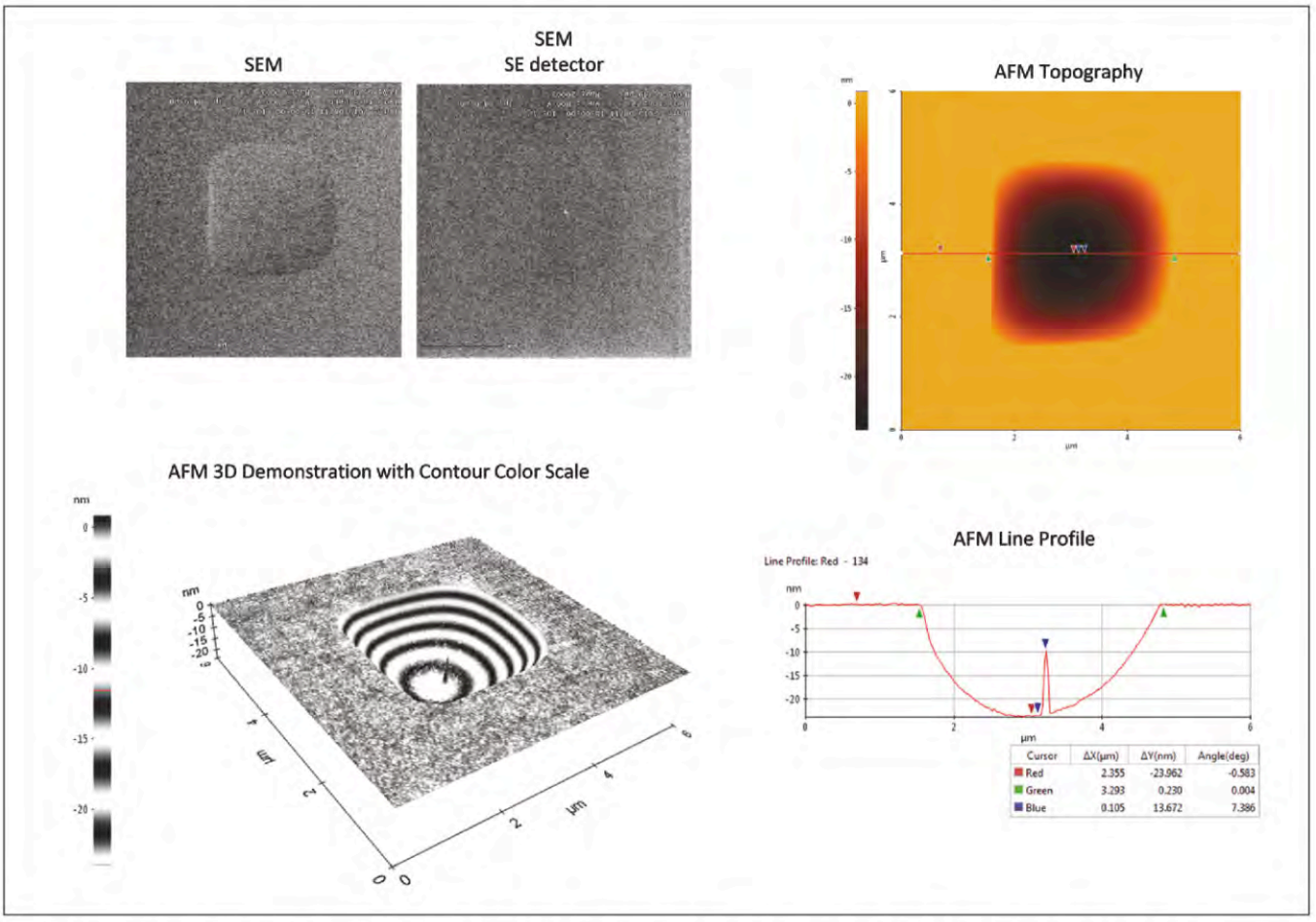


Figure 6: Comparison of data collected by SEM vs. ADR AFM. SEM shows a 2D, aerial view, while ADR AFM includes 3D data, thereby enabling a line profile, 3D construct and contoured colour scale.

smaller or shallower than defects that the SEM could identify. The SEM also had issues identifying defects that had less edge sharpness, whereas the AFM in its automated scanning mode found everything (see figure 6) .

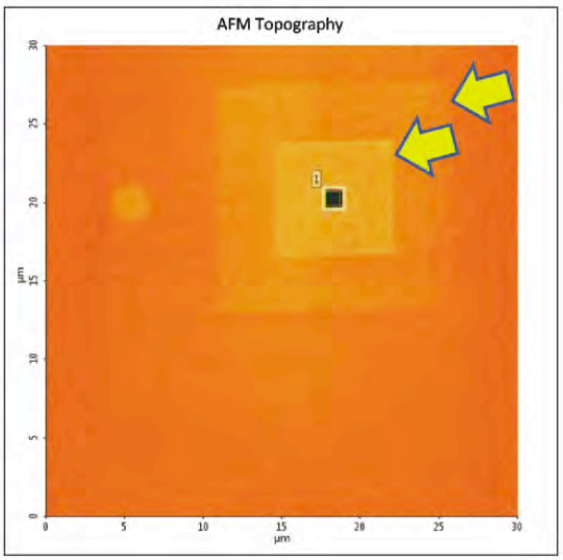


Figure 7: AFM image of a facet defect with several SEM burn-marks is shown; burns are marked by arrows.

"From the customer perspective, locating the defects of interest during the review process and determining size and depth can be critical. While SEM-based techniques can locate larger defects, it does not find them all and in fact missed 13 of 34 in this case. The lack of 3D information and SEM's inability to image the shallow and small defects matters to manufacturers. With Park's automatic defect review manufactures can have high quality 3D data of DOIs more quickly using a turn-key solution that any technician can operate," said Zandiatashbar. Automatic defect review from Park Systems maximizes productivity by up to 1,000 percent as reported by customers. But what satisfies customers most is the unprecedented level of accuracy including 3D imagery and detailed topographic information of even the smallest defects. With ever-shrinking semiconductor device geometries reaching beyond 14nm, defects critically impact microelectronic device performance. Park's approach to automating 3D imaging is revolutionary because it makes the benefits of AFM practical for leading device manufacturers and researchers pushing future product generation boundaries.

Mastering the marriage of III-Vs and silicon

Defect-trapping pockets enable the growth of high-quality films of GaAs on large-area, conventional silicon substrates

BY QIANG LI AND KEI MAY LAU FROM HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

IN 1965, GORDON MOORE, at the time director of research and development at Fairchild Semiconductor, published a now-famous article in *Electronics*. In his four-page piece he outlined the benefits wrought from shrinking the dimensions of silicon transistors, and how fast this level of miniaturization might occur. Hindsight highlights the greatness of Moore's insight, which has been captured by a law named after him.

It is now just over 50 years since the publishing of Moore's seminal paper. And for most of that time, by simply scaling device dimensions, engineers have delivered gains in speed and cost while trimming the power required to operate each transistor. But recently, shrinking device size has not been enough – introducing new materials has held the key to maintaining improvements in performance while trimming dimensions. In this regard, the biggest modification so far has been the shift from SiO_2 to high-κ HfO_2 as a gate dielectric, to prevent leakage currents from escalating to unacceptable levels when the thickness was scaled to a few angstroms.

This revolution in the range of materials employed within the transistor is driving a new era for digital and memory devices. The age of 'more-than-Moore' has arrived. This is a time when both new materials and three-dimensional non-planar architectures are viewed as the way forward. There is also the promise of system-on-chip solutions that dramatically improve capability, while trimming size, cost and power dissipation.

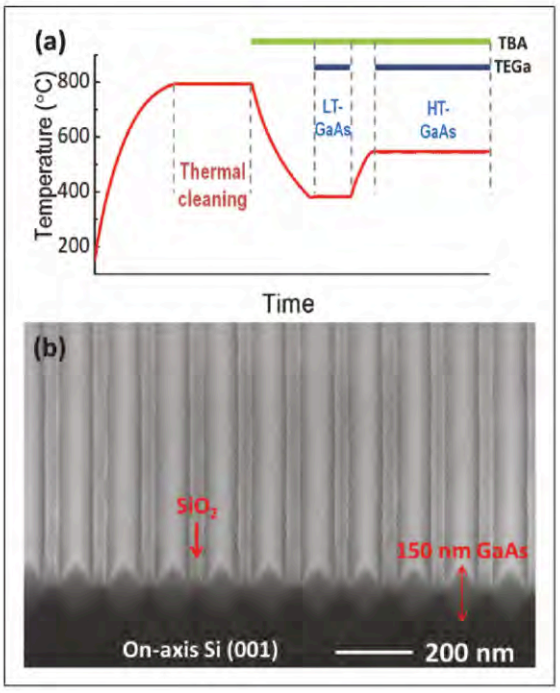


Figure 1: (a) Gas flow and temperature sequence for planar GaAs nanowire growth on silicon using a two-step procedure. The precursors that are used are triethylgallium (TEGa) and tertiarybutylarsine (TBA) (b) tilted-view scanning electron microscopy image of planar GaAs nanowires on silicon.

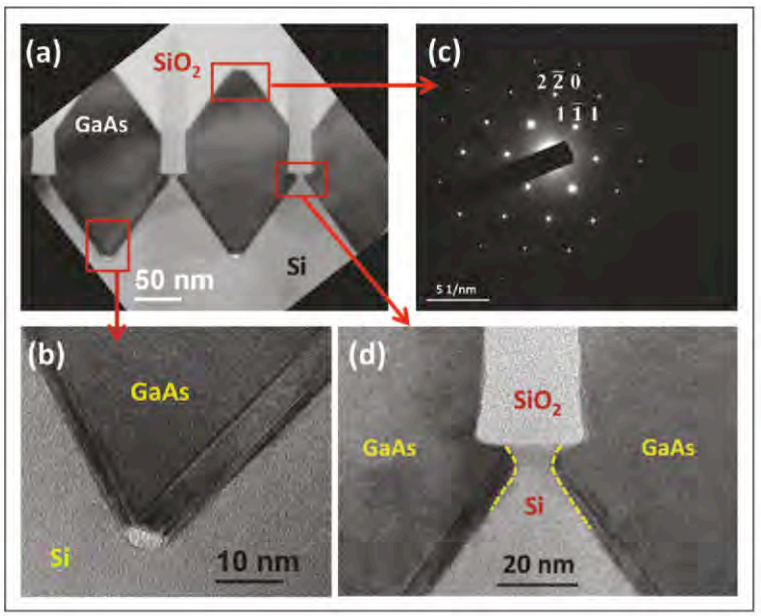


Figure 2: (a) Cross-sectional transmission electron microscopy image of GaAs nanowires; (b) high-resolution transmission electron microscopy image of the GaAs-silicon interface; (c) selective diffraction pattern taken at the apex of the nanowires; (d) transmission electron microscopy image of the stacking faults trapped by a 'tiara'-like structure made of silicon.

Advances in the age of 'more-than-Moore' will require the heterogeneous integration of broad classes of materials that are traditionally not present in silicon fabs. Silicon is great for electronic switching and memory, but its indirect bandgap precludes its use in efficient light emission and photon interaction. This weakness is a major flaw in the 'big data' era, where there is explosive growth in demand for data transmission. But hopefully silicon's deficiency can be addressed by integrating it with photonic semiconductors, such as III-Vs. Such a marriage could revolutionize future on-chip and chip-to-chip communication technologies with optical interconnects.

The most attractive option for bringing these two classes of materials together is to grow an epitaxial III-V film on a silicon substrate. There are challenges associated with this, primarily arising from differences in the lattice and thermal mismatch and crystal polarity. Attempts to succeed in this endeavour date back to the 1980s, but despite a great deal of effort by researchers from all around the globe, progress has been slow, and breakthroughs few and far between.

One group that has made significant strides in this direction is our team from Hong Kong University of

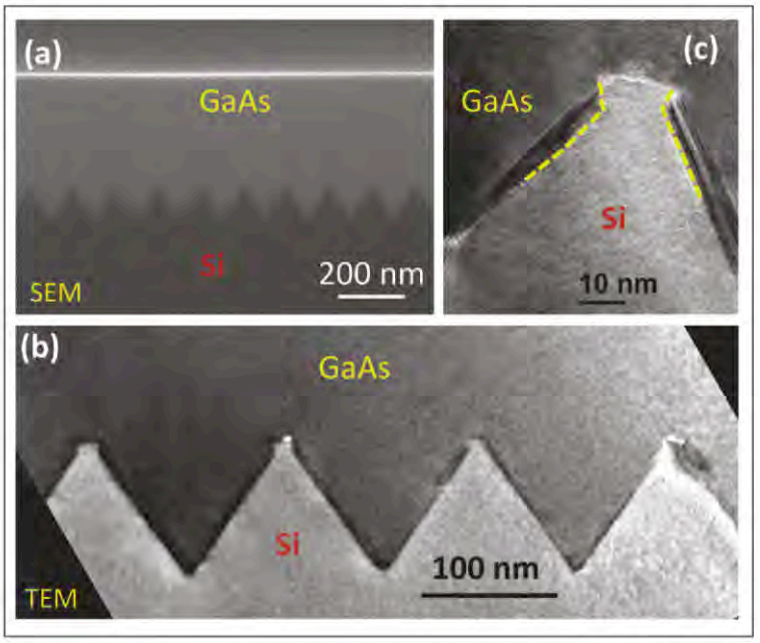


Figure 3: (a) Cross-sectional scanning electron microscopy of a 300 nm coalesced GaAs film using the nanowires as a special buffer; (b) transmission electron microscopy image showing that stacking faults at the hetero-interface are localized and trapped by silicon pockets; (c) transmission electron microscopy image highlighting the defect trapping effect by patterned silicon after coalesced thin-film growth.

Science and Technology (HKUST). We are exploring technologies for growing III-V nanostructures and thin films on CMOS-compatible silicon substrates by MOCVD. We are by no means alone in pursuing this approach. However, while most groups are using catalysts and focusing on vertically orientated nano-structured materials, we are working on compliant substrates, which are highly compatible with the well-established silicon planar processing technology. Our great strength is that we can close the gap between the material growth schemes and the ultimate device implementation.

Our efforts can be traced back to the 2000s, when we first took the lead in the metamorphic growth of InP on planar (001) silicon substrates. Instead of using conventional techniques such as compositional grading of III-V alloys or a germanium buffer, we developed a two-temperature growth process and optimized intermediate GaAs buffers. We overcame the problems associated with an 8 percent lattice mismatch, and achieved device-quality InP featuring a smooth surface. This led to the demonstration of InAlAs/InGaAs based HEMTs and MOSHEMTs on planar silicon. Both of these types of device exhibit state-of-the-art characteristics.

A two-pronged attack

To further improve the material crystal quality, we have adopted a hybrid approach to forming III-Vs on silicon. We combine selective-area heteroepitaxy with epitaxial lateral overgrowth, which is undertaken on nanometre-scale, patterned silicon substrates. One of the strengths of using this particular form of substrate is that it allows the use of recessed pockets – designed correctly, they offer a unique, defect-trapping capability that is not possible with conventional blanket heteroepitaxy.

Taking this approach, we produced ultra-low-defect antiphase-domain-free GaAs thin films on silicon. These were formed via deposition on highly ordered in-plane GaAs nanowires on V-grooved silicon. To produce these GaAs films, we began by taking planar silicon (001) wafers, and patterning them with [110]-orientated SiO_2 stripes with a line-opening width of 90 nm and a line pitch of 130 nm. This created regions in the silicon substrate with a shallow recess, which defines the defect-containing silicon pockets. This approach is notably different from traditional blanket heteroepitaxy, which does not employ the exactly orientated substrates that we use, but rather off-cut silicon, which minimises the formation of anti-phase domains.

We avoid anti-phase domains by etching V-shaped grooves at the bottom of the trenches. This technique, which has been demonstrated by a team of researchers from imec, Belgium, enables the deposition of III-V materials on exposed {111} silicon facets. On these side walls, the films that form tend to be free from anti-phase domains.

By adopting a two-step growth method for the epitaxy of planar GaAs nanowires on V-grooved silicon, we are able to realise a superior crystalline quality (see Figure 1 (a)). After thermal cleaning at 800°C in an MOCVD chamber, we begin by depositing a GaAs nucleation layer at 385°C. This is followed by the growth of a GaAs main layer at typically 550°C.

Strengths of our highly-ordered, site-controlled GaAs nanowires, which are separated by SiO_2, include smooth facets and uniform morphology (see Figure 1(b)). Analysis of X-ray diffraction ω-rocking curves indicates that nanowires with a thickness of 150 nm yield a full-width-at-half-maximum that is comparable to that of 1 μm-thick GaAs thin films on planar off-cut silicon. In other words, switching from planar growth to our novel defect reduction approach slashes buffer thickness by more than a factor of six for the same crystalline quality.

Scrutinising our structures with cross-sectional transmission electron microscopy uncovers some peculiar defect-trapping phenomena (see Figure 2 (a)). Close examination of the GaAs-silicon hetero-interface reveals that the 4.1 percent lattice mismatch is not accommodated by propagation of threading dislocations, but by formation of stacking-disordered layers just a few nanometers thick (see Figure 2 (b)). Thanks to this novel strain-relief mechanism, the GaAs bulk layer has a high crystalline quality, as evidenced by the selective diffraction pattern taken at the apex region (see Figure 2(c)).

A tremendous tiara

Looking more closely at the glide of the few-layer stacking faults at the GaAs-silicon hetero-interface reveals that the disordered layers are stopped by a 'tiara'-like structure (see Figure 2(d)). This is made of silicon beneath the SiO_2 walls, and it originates from silicon recessing by combined dry etching and potassium hydroxide wet etching.

Blocking of defects by this type of hetero-epitaxial approach is often referred to as aspect ratio trapping (ART), or the epitaxial necking effect. Although research on ART is not new, it has traditionally focussed on the growth of high-quality crystals in small cavities, which are defined by a patterned dielectric. There have also been a handful of attempts to produce large area planar films by combining ART with epitaxial layer over-growth. However, the dielectric patterns have spawned hard-to-control asymmetries and irregularities in faceted growth regions. The upshot is a high density of coalescence defects, a rough surface morphology and even more defects originating from the dielectrics.

Our films do not suffer from the same fate, because our tiara-like structure enables the diamond-shaped silicon pocket to localise and confine most of the hetero-interface defects. Another way to look at this is that by removing SiO_2, our nano-sized wires coalesced into planar thin films with a smooth surface, while retaining the defect trapping capability associated with the epitaxial necking effect.

Removing SiO_2 between the merging nanowires improves the surface morphology of the resulting planar thin films. According to images obtained by scanning electron microscopy, just 300 nm of GaAs overgrowth is needed to realise a flat surface (see Figure 3 (a)). Further inspection of the structure by transmission electron microscopy reveals that the silicon pockets can prevent interfacial defects from extending into the upper layers (see Figure 3(b) and (c)). Meanwhile, atomic force microscopy uncovers a surface roughness of 1.9 nm across a 5 μm by 5 μm scan area, and shows that the surface is free of antiphase-domain boundaries (see Figure 4).

> "Blocking of defects by this type of hetero-epitaxial approach is often referred to as aspect ratio trapping (ART), or the epitaxial necking effect. Although research on ART is not new, it has traditionally focussed on the growth of high-quality crystals in small cavities, which are defined by a patterned dielectric"

We have assessed the crystalline quality of the coalesced GaAs films with X-ray diffraction. Peaks from ω-rocking curves have a full-width at half-maximum that decreases from 230 arcsec to 154 arcsec as the thickness of GaAs increases from 1 μm to 2 μm. The ω-2θ linewidth is 72 arcsec. These values indicate good material.

One way to look at the success that we have had is that compared to GaAs films grown on non-patterned,

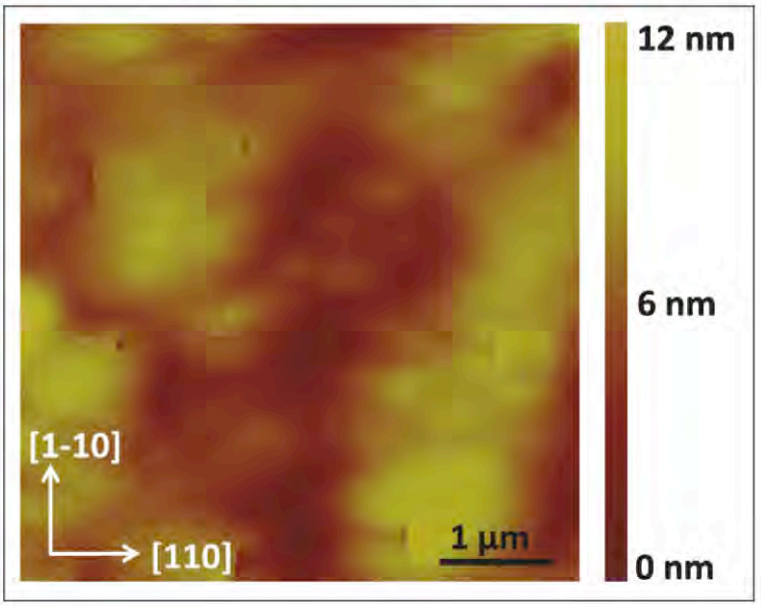


Figure 4: Atomic force microscopy image of a 300 nm-thick coalesced GaAs film grown out of high-ordered nanowires.

off-cut silicon, the X-ray linewidth is cut by more than 50 percent with the same buffer thickness. Alternatively, a comparable X-ray linewidth is possible with a three-fold reduction of buffer thickness (see Figure 5).

Characterising our structures demonstrates that the benefits of our growth scheme are not limited to removing the need to use off-cut silicon to suppress anti-phase domains – they also include a superiority over traditional blanket hetero-epitaxy, when it comes to trapping and reducing defects. What's more, our efforts show that low-defect-density GaAs can be deposited on silicon without the need for other intermediate buffers, such as those based on germanium or graded SiGe.

Additional improvements in the crystalline quality of our as-grown GaAs films are possible by introducing other defect reduction techniques. For example, undertaking three-cycle thermal annealing on 1 μm GaAs on V-grooved silicon cuts the full-width at half-maximum of the ω-rocking curve from 230 arcsec to 180 arcsec.

Another lever for increasing material quality is the nanowire pitch size. Get this right and the overall defect density in the coalesced films can be further reduced in the epitaxial layer overgrowth process. Note that if the lateral overgrowth distance is too long, it introduces coalescence defects and increases surface roughness. For each material one would expect that the optimal growth conditions and the shape of the silicon pockets could be different. We are now looking at materials with an even larger lattice mismatch with silicon, such as InP, because this combination would enable the fabrication of long-wavelength lasers and HEMTs on silicon. These efforts have already led to some success – we have produced some InP-on-silicon compliant substrates.

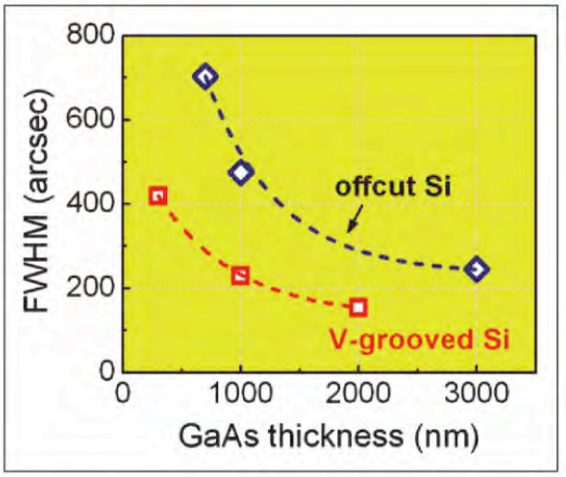


Figure 5: Comparison of the full-width at half-maximum of X-ray diffraction ω-rocking curves for GaAs thin films grown on non-patterned, off-cut silicon and V-groove patterned silicon substrates.

Further opportunities for our technology are associated with using our epitaxial planar nanowires to construct a wide variety of heterostructures on industrial-standard (001) silicon substrates. Combining these nanostructured materials with a nanofabrication process should provide opportunities to develop novel devices and improve and refine conventional devices in three-dimensional geometries.

Using the nanowire as a starting point for forming micro-scale crystals and large-area thin films should unlock the door to the fabrication of a range of devices on large-area, inexpensive and abundant silicon substrates. They include those requiring thick hetero-epitaxial layers, such as monolithically integrated quantum dot lasers, detectors and multi-junction solar cells. If our work kicks-starts a global effort in this direction, it may also light a path towards the long-dreamed-of convergence of electronics and photonics on a common platform.

Further reading

Q. Li *et. al.* Appl. Phys. Lett. **106** 072105 (2015)
Q. Li *et. al.* J.of Crystal Growth **405** 81 (2014)

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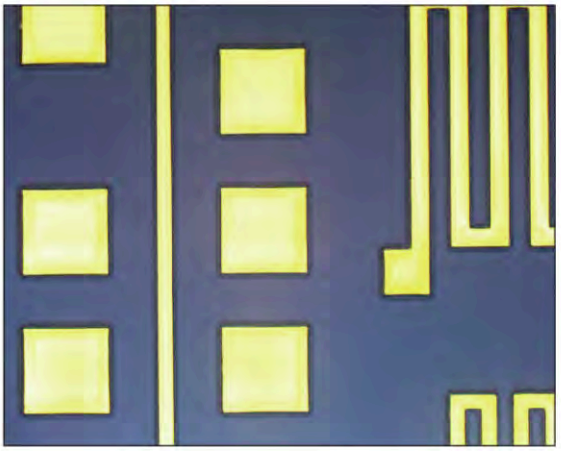
REDUCE GOLD USAGE

Nothing surpasses gold's inherent semiconductor performance benefits. But ClassOne Technology explains how its electroplating system can keep performance high at a fraction of the cost.

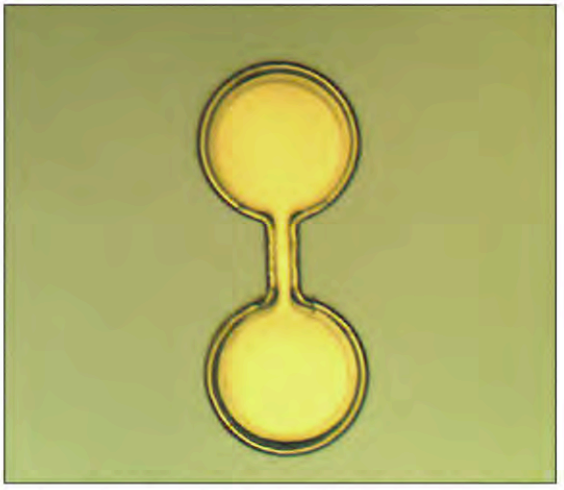
GOLD, despite its high cost, has long been an essential element in semiconductor processing because it is a highly efficient and reliable electrical conductor that also resists oxidation and corrosion. These qualities make gold ideal for connectors, switches and relay contacts in a vast array of applications, which is why in 2015 the electronics industry used more than 290 tons of this precious metal.[1] However, a newer generation of electroplating tools is starting to reduce that usage in certain sectors.

Addressing the problems of PVD, CVD and wet bench deposition

In semiconductor processing, gold is often deposited by physical vapor deposition (PVD) and chemical vapor deposition (CVD) methods. While those techniques sufficed for a time, they also brought certain significant problems such as material wastage, slow deposition rates and downtime for necessary equipment cleanings. Some have tried to use wet benches for gold plating, but with limited success due to the high non-uniformity inherent in that approach. Also, manually operated wet benches were prone to undesirable levels of variation and the risk of human exposure to open baths of toxic chemistry.



Gold plating by the Solstice S8 system



Many semiconductor applications require gold layers ranging in thickness from 3 to 35 microns

However, a newer generation of electroplating systems, exemplified by the Solstice family from ClassOne Technology, is designed to overcome those limitations. The systems provide fast, waste-free, cost-efficient, and production-oriented solutions with uniformities in the 1 percent range.

Eliminating gold loss, reducing gold expenditure

For gold deposition, one fundamental challenge with PVD and CVD was that those techniques did not coat just the wafer, they also coated the entire inner surface of the deposition chamber — in this case, with a very costly material. Theoretically, the 'oversprayed' gold could be recaptured and reclaimed. But in practice, cleaning and reclaiming processes have proved to be very difficult, time-consuming, potentially dangerous (perhaps requiring the use of hazardous chemicals such aqua regia) and ultimately inefficient. Consequently, a great deal of the oversprayed gold

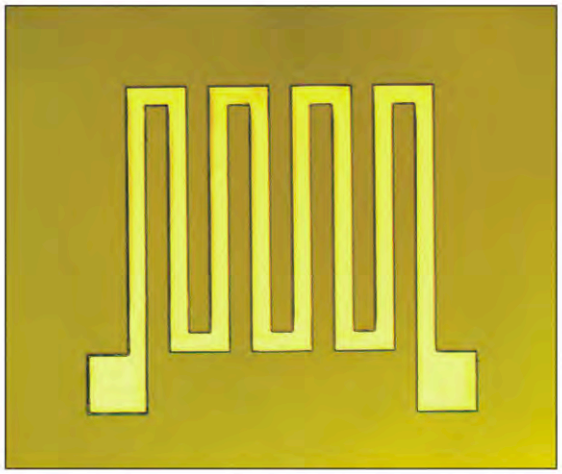
was permanently lost, which significantly increases the total cost of ownership of the process.

By contrast, new electroplating systems only deposit gold onto the wafer, specifically where it is needed. There is no 'overspray' or waste of gold. Also, there is no equipment downtime for chamber cleanings and no need for reclamation efforts. The new electroplating process is cleaner and simpler; it is also more precise and efficient. It reduces costs substantially by cutting gold usage and eliminating waste. The amount of gold needed is further reduced by the fact that electroplating is a self-purifying process, so it requires only four nines of purity in the electrolyte solution instead of the six nines required in evaporation pellets or sputtering targets.

Faster deposition, more streamlined processing

In addition to the gold loss problem, PVD and CVD processes have also been limited by relatively slow deposition rates — typically between 10 and 30 nm/min. This had been acceptable for creating relatively thin layers; however, as applications began to require thicker gold layers, the long deposition process times became increasingly problematic. Today, many emerging markets such as lasers, LEDs, RF and MEMS have requirements for gold layers as thick as 3 to 35 microns, so manufacturers are actively seeking faster deposition solutions.

New Solstice electroplating systems provide deposition rates in the order of 150 to 300 nm/min, or roughly 10 times faster than previous deposition methods. In addition, the new tools are specifically designed for ≤200mm wafer processing and are thus strategically positioned to serve the needs of many emerging markets that use smaller substrates.



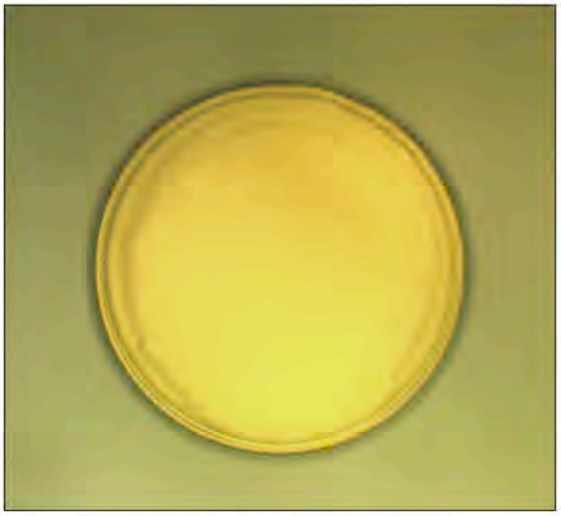
The Solstice S8 can electroplate device features, reducing the amount of pure gold needed by up to 10 times

A view inside ClassOne Technology's Solstice S8 electroplating system showing the tool's eight processing chambers

New electroplating tools further reduce cycle times because no vacuum is required, so processing can start immediately. There is no pump-down wait time before processing can begin. Also, one wafer can be run at a time if desired, without incurring any overhead penalty. The resultant savings in time and increased throughput can add a further level of cost efficiency.

Innovative layering technique can reduce gold usage substantially

Because of its unique 8-chamber design the Solstice S8 electroplating system enables it to replace a solid gold layer with a multi-metal stack, and use much less gold than would otherwise be required.
For example, a feature that previously required a 5μm layer of solid gold can be replaced with a 'sandwich' of 0.25μm Au, 1μm Ni, 2.5μm Cu, and another 1μm Ni – all topped with 0.25μm Au – to achieve equivalent functionality while reducing gold usage by a factor of ten. The multi-chamber equipment design enables it to deposit the Au / Ni / Cu / Ni / Au layers all in a single cycle; no additional process steps or time are



Gold contact points made of an electroplated 'stack' using Au, Ni and Cu instead of pure gold

required to gain significant cost savings.

The magnitude of potential gold savings can be estimated by extending the example above: Assume that a fab is running 1,500 wafers per week through a metal lift-off process where 5 μm of gold is deposited over 50 percent of a 150 mm wafer area. Further assume that all oversprayed gold is recovered and that the price of gold is $1200 per troy ounce with no additional processing fees for the purity.

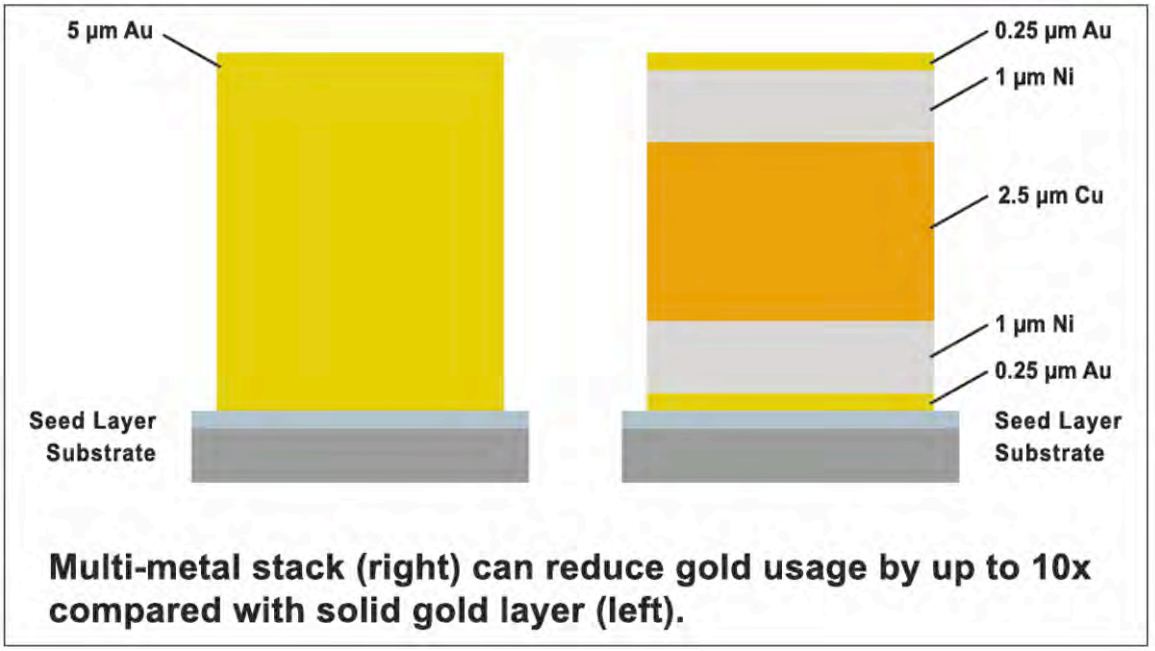
Under those conditions, using a solid gold layer, the user's annual gold cost would be approximately $2,150,000. However, with the same operational assumptions, if the Solstice's Au / Ni / Cu / Ni / Au 'sandwich' technique were used, the total deposited metal costs (Au + Ni + Cu) would be reduced to just over $108,000 per year — yielding an annual savings of over $2,042,000. Thus, the gold cost reduction in the first year alone would more than pay back the cost of the electroplating tool! And if gold were to rise in price, the payback would be reached even more quickly.

Substantially reduce costs while increasing performance

In summary, Solstice electroplating systems are able to deposit thicker gold layers more quickly and efficiently while eliminating gold waste. The process requires no downtime for cleaning vacuum chambers, and it provides increased uptime and more cost-efficient processing. Perhaps most significantly, the tool's chamber design enables innovative layering techniques that can potentially yield enough reduction in gold usage to pay back the equipment purchase cost within a year.

Solstice is a registered trademark of ClassOne Technology.

Reference
1. World Gold Council, (www.gold.org)



Multi-metal stack (right) can reduce gold usage by up to 10x compared with solid gold layer (left).

A side view 'cut-away' illustration showing the composition of an electroplated device feature that uses 10x less gold than a pure gold analog

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Researchers seek elusive pellicle solution

Readying extreme ultraviolet lithography (EUVL) for high volume manufacturing has presented many challenges along the road to creating next-generation semiconductors. Imec researchers believe they are a step closer in delivering a much needed pellicle solution.

WITHIN A FEW YEARS, the lithographic community needs a suitable pellicle to protect photomasks during extreme ultraviolet (EUV) exposures in high-volume manufacturing. While developing a new technology involves many vexing challenges, some seemingly innocuous aspects have far-reaching implications. Developing a pellicle to protect photomasks is very challenging since EUV light is absorbed by most materials. Whatever pellicle is chosen must be greater than 90% transmissive at EUV's 13.5nm exposure wavelength. Materials that work for other lithographic processes do not work well in EUV. Thermal, chemical and mechanical requirements complicate pellicle development.

Emily Gallagher, principal engineer at imec, and her team are screening many candidate materials from both imec and partner organizations to assess suitability. In this article Gallagher explains the imec approach to pellicle development, and highlights carbon nanotubes as one of the promising solutions.

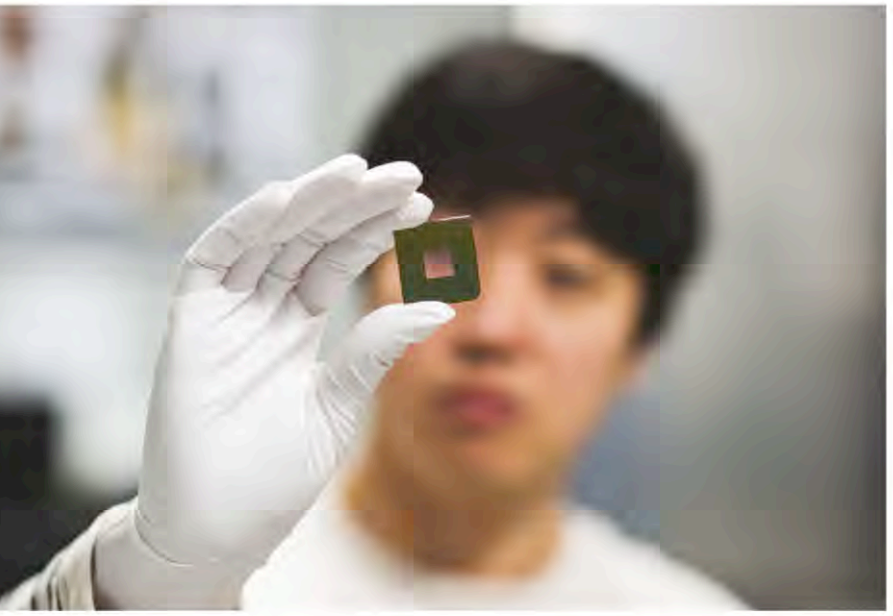
Why a pellicle?

Employing a pellicle is common practice in deep ultraviolet (DUV) lithography utilizing 193nm and

Imec researchers discussing a pellicle sample in development for use in extreme ultraviolet lithography.

248nm wavelength exposures. The pellicle membrane protects the photomask from contamination. But the different exposure wavelength in EUV complicates pellicle choices.

"(The pellicle) is mounted a few millimeters above the surface of the photomask so that particles that land on it will be too far out of focus to print. For DUV, thin film pellicles can be fabricated from low-cost fluoropolymers. They are inexpensive and transmit over 99 percent of the light, ensuring that the imaging impact is minimized," Gallagher explained. "But extreme ultraviolet lithography (EUVL) is a different story. The 13.5nm EUV light is absorbed strongly



Jae Uk Lee from imec's pellicle membrane development team, handling a EUVL pellicle sample.

by most materials, including fluoropolymers. Also, the pump-down sequences in the EUVL vacuum system and the high intensity of the EUV light source complicate the development of a suitable pellicle solution."

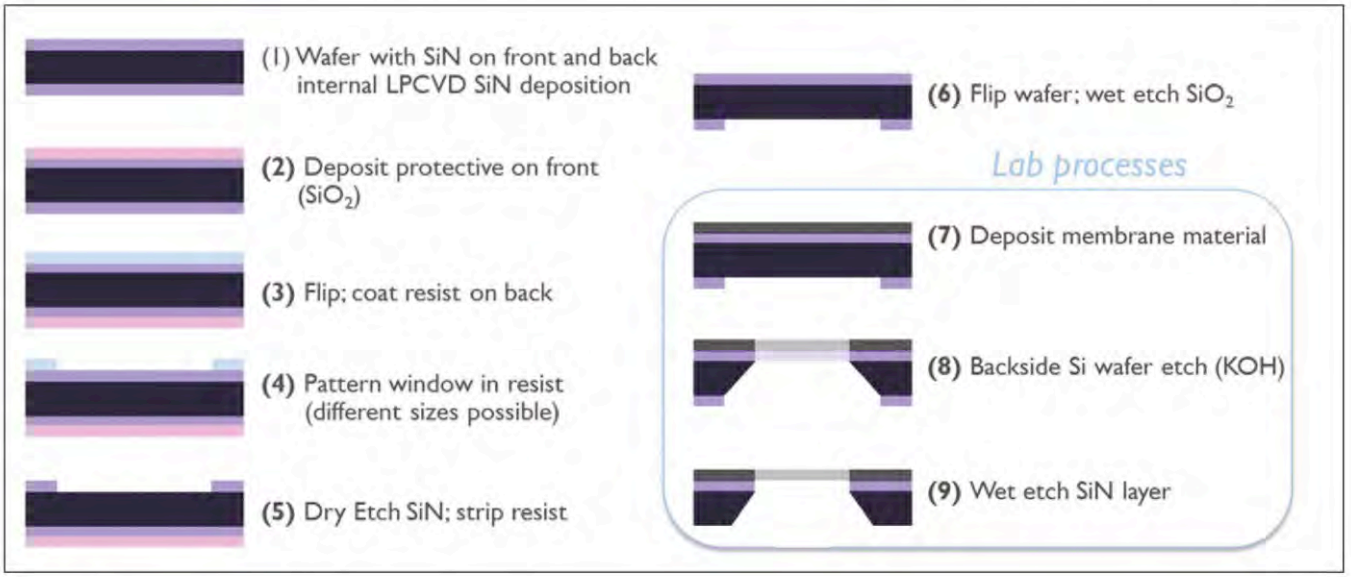
Gallagher added that the industry initially planned to introduce EUVL into manufacturing without any pellicle. The idea was to make the photomask handling and exposure vacuum chamber particle-free, eliminating the need for a protective membrane. However, after defectivity assessments, the chip industry is convinced that a pellicle solution is mandatory for high-volume EUV exposure tools. The pellicle is currently considered a major area for EUVL development.

"While considerable progress has been made in improving the EUV source power, resist sensitivity and mask blank defects – areas that are also considered major challenges – a suitable pellicle for high power exposure (greater than 250 W) has not yet been found. That's why we initiated a project for pellicle membrane development as part of imec's Advanced Lithography Program. Our goal is to have a solution ready within two or three years from now, the time when the IC industry will need a pellicle for their high-volume EUV lithography tools," she said.

Optical, mechanical, chemical and thermal challenges

One of the most important requirements for the EUV pellicle is related to the transmission of EUV light. Gallagher noted that during EUV exposure, single-pass transmission (including light passing through the pellicle) must be at least 90 percent in order to ensure the productivity of the EUVL tool at a targeted source power of 250 W. Too low of a transmission would reduce the effective exposure power, hence the productivity of the tool (measured as wafers exposed per hour,) would be negatively impacted.

Finding a material with sufficient transmission qualities is very challenging since EUV light is absorbed by almost all materials. The pellicle also needs to be mechanically stable, which is difficult to achieve for membranes that are thin enough to meet light transmission requirements. In practice, thin pellicle membranes are mounted on a frame and fixed to the photomask. During use in the EUVL scanner vacuum chamber pellicles are subjected to handling and periodic pump-down/vent cycles, which enhance the risk for bulging and finally breaking membranes. Pellicle lifetime could also be affected by the presence of hydrogen radicals in the scanner since highly



Imec's SiN membrane platform for fabricating thin pellicle solutions.

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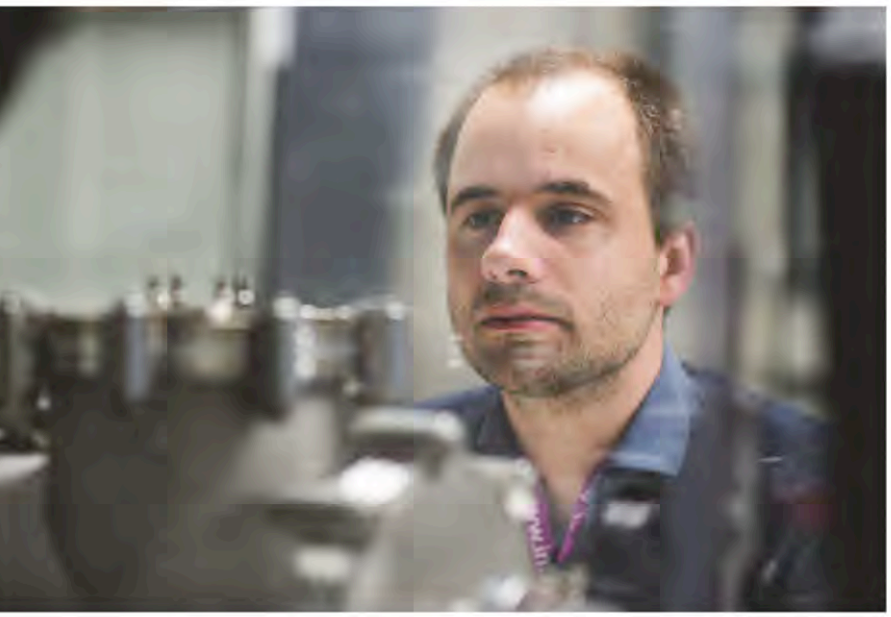


Johannes Vanpaemel from imec's pellicle membrane development team photographed at the experimental bulge tester.

reactive hydrogen is used to keep the chamber sidewalls and optics clean, but it could also react with the pellicle material. Thermal considerations also complicate pellicle choices.

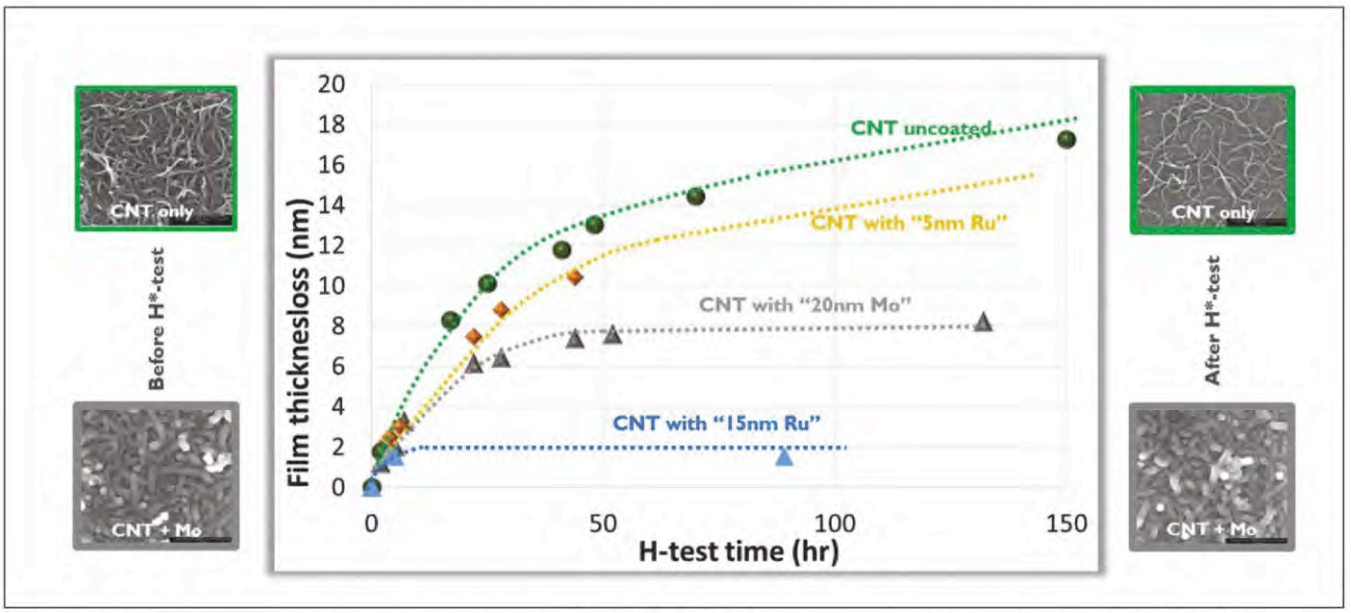
"We need to (also) take account of some thermal considerations. Some of the light that is not transmitted is absorbed, heating the membrane considerably. However, heat transfer options through evaporation or convection are minimal for a material in vacuum; heat conduction is very limited for a thin membrane. The only way to transfer heat is radiation. For some materials, additional emissivity layers will be needed to enhance radiation and decrease the peak temperature of the pellicle. These capping layers can also serve to protect the pellicle from hydrogen etching if selected appropriately," Gallagher said.

Imec's approach to pellicle development

To meet transmission requirements, it is logical to start with low absorption materials. This translates into selecting a material with a low EUV absorption coefficient k. Both silicon (Si) and carbon (C) fulfill this requirement.

"After choosing the right material, we can reduce the absorption even further by thinning and by reducing the density of the material. The latter can be done by either inducing voids (e.g. by etching into a continuous film), or by depositing a material that is inherently porous, like carbon nanomaterials," Gallagher explained. EUV pellicles have been in development for more than a decade. Reasonable options have already been proposed, but they all have their issues. Either the pellicle development is too immature (as is the case with graphene), or the pellicle membranes break at higher source powers (as is the case with poly-silicon or silicon nitride-based pellicles). A key element of imec's strategy is developing alternative solutions. "Building on existing solutions brings no additional value to our partners," Gallagher observed. One of many potential pellicle materials tested by imec are carbon nanotubes (CNTs). Carbon nanomaterials, like CNT films, can have an extremely low density, so the transmission is likely to be high.

"We also expect them to add to the membrane's mechanical strength. Another nice thing about carbon



Results from the hydrogen tests with coated and uncoated CNTs. Coated CNT demonstrate a flat response after exposure to H radicals as required.

nanotubes is that their properties are tunable. This means that issues with the material can possibly be solved by careful engineering," she said.

Carbon nanotube pellicles can be fabricated using imec's 300mm process flow and can be scaled for larger wafer sizes. The pellicle process starts with a silicon wafer. Deposition, patterning and strip processes are deployed to create a flexible platform for membrane development. Silicon nitride (SiN) can serve several functions. It can either be thinned and used as a part of the final membrane stack, or it can be etched away so it is not part of the final membrane. The 300mm platform is compatible with scaling-up membrane sizes, targeting 10 x 10cm^2 and even larger, which is important for developing 450 mm silicon wafer technologies. CNTs process ed on this membrane platform successfully passed several tests that have been established at imec to evaluate potential pellicle solutions.

"The transmission of a stack of three to four layers of nanotubes (~50nm thick) was measured to be higher than 95%. The CNT-based pellicle was also subjected to mechanical testing. At imec, we built an experimental bulge tester that (can) apply a differential pressure across the membrane to test the point at which the pellicle bursts. This burst pressure is then compared to identical SiN membranes without additional layers. The measurements clearly show an improved durability when CNTs are added to the membrane.

"We also looked at the impact of hydrogen (H), which is particularly worrisome since hydrogen is known for etching carbon. The results from our hydrogen tester indeed showed that CNT films loose thickness after long exposure to hydrogen radicals. Fortunately, we can solve this issue by coating or encapsulating the CNTs with a suitable material that has minimal impact on EUV transmission, such as ruthenium or molybdenum," she explained.

Advancing EUVL pellicle development

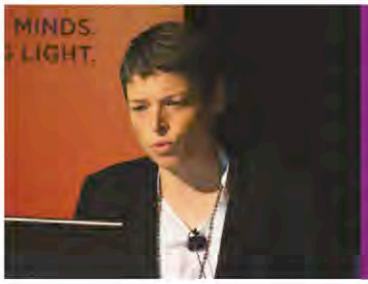
Besides developing and evaluating its own pellicle solutions, imec is also screening pellicle materials developed by partners and other external suppliers. Gallagher said that EUVL pellicle development is a very complicated and challenging activity.

"Carbon nanotube pellicles can be fabricated using imec's 300 mm process flow and can be scaled for larger wafer sizes. The pellicle process starts with a silicon wafer. Deposition, patterning and strip processes are deployed to create a flexible platform for membrane development. Silicon nitride (SiN) can serve several functions. It can either be thinned and used as a part of the final membrane stack, or it can be etched away so it is not part of the final membrane"

To accelerate development, imec believes it is important to have many companies exploring multiple paths in parallel, and to engage the EUVL community. For this reason, imec has made its testing processes available for partners including its in-house capabilities for optical, mechanical, chemical and thermal testing. This puts imec in a unique position.

"If we need a solution within two to three years, we must exploit this infrastructure to the maximum. With our carbon nanotube-based pellicle, we have a promising path forward, but we remain open to alternatives since enabling an industry solution constitutes a success for imec and for our partners," she concluded.

- "Collaboration is the centerpiece to push the limits of lithography", vision by Greg McIntyre in imec's 2015 annual overview.



EMILY GALLAGHER has been a principal engineer at imec since 2014. Her work currently focuses on pellicle membrane development, EUV imaging and photomasks. Prior to this position, she was a senior technical staff member at IBM leading the extreme ultraviolet lithography (EUVL) mask development effort there. She grew up in Montreal, Canada, studied physics in the US, earning her PhD from Dartmouth College with a thesis on free electron lasers. She has authored over 70 technical papers, written two book chapters on photomasks and holds 18 patents.

Legos for next-generation semiconductor devices

Combining disparate technologies inside innovative packages holds great promise, but will challenge current approaches to inspection and metrology. Gurvinder Singh, Director, Inspection Product Management at Rudolph Technologies, explains.

THE SUCCESS of smartphones has led to massive investments in processors, sensors and communications components as well as requisite packaging technologies to integrate devices into the smallest possible space. These investments, coming from both traditional semiconductor manufacturers and from a whole new crop of outside developers, have spawned a nascent ecosystem that will fuel tomorrow's innovation and become a significant industry driver even as smartphone growth itself levels off.

It is not an exaggeration to compare the current situation with smartphone components to the seeding of the early electronics industry by spin-offs from the space program. If you look at the devices incorporated into a modern drone, virtual reality headset, or internet of things (IoT) product, you'll find mostly repackaged smartphone components. This mix and match approach—much like space program spin-offs—has led some to characterize the collection of smartphone components as a Lego set for next-generation devices, including IoT, wearables, autonomous cars, drones, virtual reality/artificial reality headsets, and much more.

Combining repurposed components and technologies to create a virtually limitless variety of new products will present significant challenges to inspection and metrology methods. This will occur because creating those new products will be accomplished primarily by using advanced packaging processes at the back-end of semiconductor manufacturing. Until recently this had been relatively straightforward, but let's look at some of the challenges and sketch out the desirable features of potential solutions.

Submicron sensitivity

The same market forces that continue to drive the reduction of structural dimensions within the die will drive the miniaturization of packages and their components. Dimensions of some redirect layers (RDLs), through silicon vias (TSVs), MEMS-based filters and other components have already reached the size where micrometer-scale defects can be killers. Avoiding 'killer' defects requires sub-micron sensitivity for reliable detection. At the same time, sensitivity requirements for macro defect inspection in middle and back-end of line processes in the wafer fab are also being pushed to the sub-micron level. But sensitivity alone is not always paramount, making a solution that allows the operator a choice of magnifications to optimize the trade-off between sensitivity and throughput is highly desirable.

Warped substrates

Some advanced packaging techniques use ultra-thin wafers or singulated die positioned on reconstituted substrates, both of which can introduce large variations in surface topography. Maintaining sub-micron sensitivity over such surfaces will require specially-designed optical systems with large depth of focus and autofocus mechanisms that can track fast and slow variations in surface height across the die and substrate. These advanced substrates also present challenges to handling subsystems. At the wafer or substrate scale, the system should be able to accurately measure the rotation and position of die on reconstituted substrates.

Rectangular substrates

Much like the front-end fabrication process where economic benefits have driven a steady increase in wafer size, larger substrates in back-end packaging processes promise significant reductions in cost per package. Unlike the front-end, back-end processes are not constrained to the use of silicon wafers, raising the prospect of larger, rectangular substrates often referred to as panels. A number

of large manufacturers are actively exploring panel-based processes, and would benefit greatly from an inspection/metrology solution that accommodates both wafers and panels and offers a clear and reliable transition pathway.

Nuisance defects

Nuisance defects, false positives that should be ignored, are particularly costly in the back-end where the sunk cost of each finished, known-good-die (KGD) is extraordinarily high. The intelligent combination of multiple illumination modes, sophisticated segmentation algorithms and automatic defect classification could greatly reduce the number of nuisance defects, eliminating costly and unnecessary product losses.

Defect escape

Some classes of contaminants and residues, such as organic materials, can escape detection under conventional white light (bright-field or dark-field) illumination schemes, creating a need for innovative illumination modes that highlight these types of defects.

Such an approach could also be useful in distinguishing low contrast organic defects from the high contrast grain structure of underlying metals, or conversely, in finding shorts or 'opens' in metal lines that overlie highlighted organic layers.

Throughput

All other factors being equal, increasing throughput reduces unit cost. An inspection and metrology solution that combines both functions in a single system could increase throughput significantly, while also lowering initial capital investment requirements. Fast and early identification of non-killer nuisance defects, as described above, would also increase throughput by reducing the time spent on further review or diagnosis of inconsequential anomalies. Finally, wide-field camera optics will become an increasingly important determinant of throughput as substrates grow larger.

These are exciting times. Some would compare them to the early days of our industry when the potential for new products and applications seemed unlimited. We have looked here at only one small corner of this new universe.

Still, we have been able to define a short list of challenges and solutions that need to be addressed. That's how progress happens, one step at a time.

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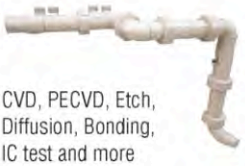

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