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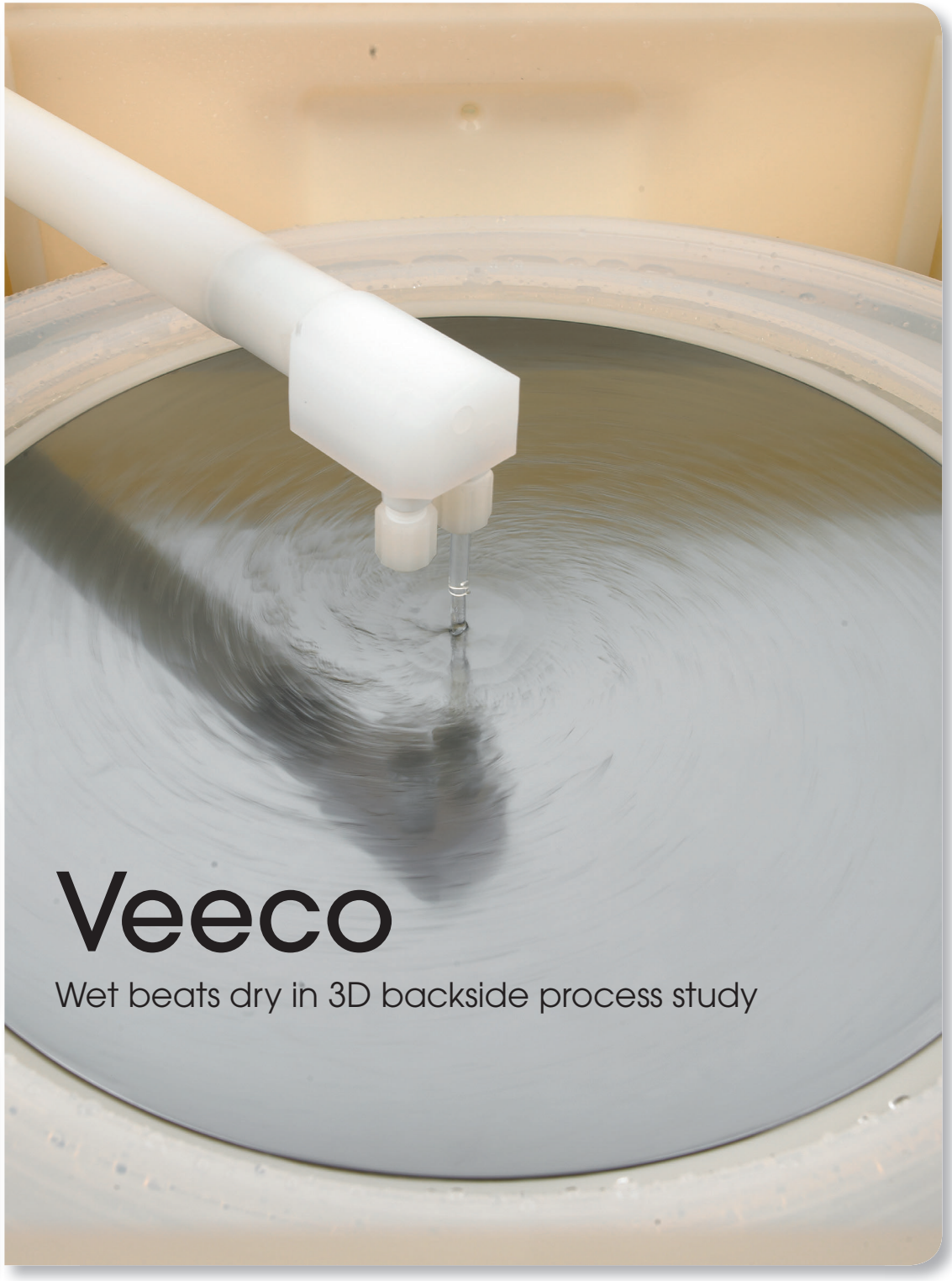

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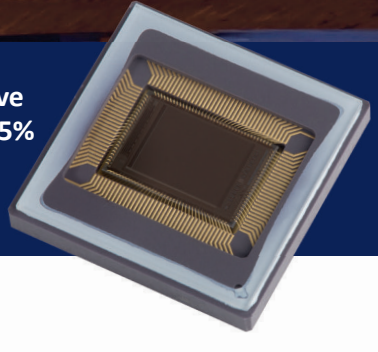

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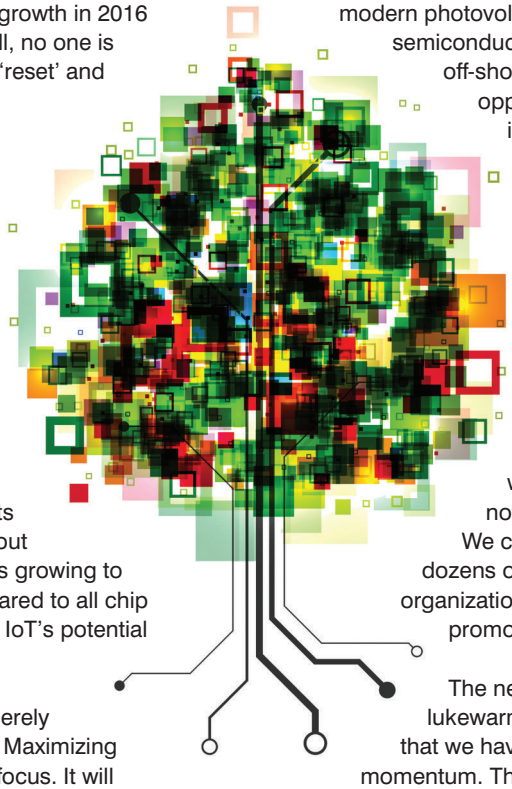
editorialview

Big opportunities on the home front

THE BEST THING about semiconductor growth in 2016 is that it beats the sour notes of 2015. Still, no one is singing 2016's praises. It is time to push 'reset' and break this muck-mired cycle.

Semiconductor sales have long been driven by major waves of technological innovation such as the ascendency of personal computing and smartphones. Gone are those glory days, so what is next? The market awaits a third wave: universal device connectivity through the Internet of Things (IoT). But like any new market, the IoT has not arrived fully formed and laden with generous margins.



The IoT is in its relative infancy. IC Insights projects IoT related sales will finish at about USD $18 billion in 2016; they forecast this growing to $26.9 billion annually by 2019. But compared to all chip sales in 2016 (about USD $335.6 billion,) IoT's potential is slowly unfolding.

Will semiconductor growth return if we merely wait-out today's lackluster cycle? Hardly. Maximizing IoT's potential will take groundwork and focus. It will take learning from winners and studying those who dropped out. And it may require partnering with those already making IoT products. Pick a strategy and get involved. The time is right, the opportunity is ripe. IoT represents the best means to reset semiconductor manufacturing paradigms since the advent of modern photovoltaic power. Unlike the majority of silicon semiconductor manufacturing that has moved off-shore, the IoT presents huge greenfield opportunities for Europe since the industry is still evolving; there are no clearly established IoT centres of excellence.

Most production today focuses on the industrial IoT, leaving other markets largely untouched. What market is yet to be served? Practically anything to do with smart devices for home, work and recreation. What does it take to get involved? Innovation and a willingness to develop products in a wide-open environment. We can win because decisive advantages are not limited to low-cost labour markets. We can win because we already have many dozens of European manufacturers and research organizations working to develop, manufacture and promote IoT devices.

The next time you hear statistics about a lukewarm semiconductor market, remember that we have the potential to restart positive momentum. There is no impossibly huge IoT incumbency to overcome. We have the researchers, manufacturers and security wherewithal to win. If we move proactively, we will see our counterparts in China, the US, Taiwan and elsewhere take notice and start emulating us. That's change we can all support.

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EV Group extends volume manufacturing to biotechnology and medical devices

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, has announced that it is increasing its focus on bringing its high-volume manufacturing process solutions and services to the biotechnology and medical device market. EVG products supporting this market include the company's substrate bonding, hot-embossing, micro contact printing and UV-based nanoimprint lithography (NIL) systems.

In addition, EVG will offer its world-class applications support, rapid prototyping and pilot-line production services. Customers in the biotechnology and medical markets can now leverage these patterning and sealing solutions--which have been production-proven in other industrial markets such as semiconductors, MEMS and photonics--for volume production of next-generation biotechnology devices featuring micrometre or nanometre-scale patterns and structures on larger-format substrates.

EV Group nanoimprint lithography solutions enable parallel processing of biotechnology and medical devices on large-area substrates.

Over the past several decades, miniaturization of biotechnology devices has significantly improved clinical diagnostics, pharmaceutical research and analytical chemistry. Modern biotechnology devices--such as biomedical MEMS (bioMEMS) for diagnostics, cell analysis and drug discovery--are often chip-based and rely on close interaction of biological substances at the micro- and nanoscale.

According to the market research and strategy consulting firm Yole Développement, an increasing number of healthcare applications are using bioMEMS components, while the bioMEMS market is expected to triple from US$2.7 billion in 2015 to US$7.6 billion in 2021. Microfluidic devices will represent the majority (86 percent) of the total bioMEMS market in 2021, driven by applications such as Point-of-Need testing, clinical and veterinary diagnostics, pharmaceutical and life science research and drug delivery. * Precise and cost-effective micro-structuring technologies are essential to successfully commercialize these products in a rapidly growing market that has stringent requirements and high regulatory hurdles.

Traditional process approaches such as injection molding are often unable to produce the extremely small structures and surface patterns with the precision, quality and repeatability increasingly required for these demanding applications, or they require extensive effort in process development. At the same time, solutions are needed to scale up from discrete production of devices to batch processing of multiple devices on a single substrate in order to achieve the economies of scale required to commercialize these products.

NIL has evolved from a niche technology to a powerful high-volume manufacturing method that is able to produce a multitude of structures of different sizes and shapes on a large scale--such as highly complex microfluidic channels and surface patterns--by imprinting either into a biocompatible resist or directly into the bulk material. In addition to structuring technologies, sealing and encapsulation is a central process for establishing confined microfluidic channels. Thus, bonding of different device layers, capping layers or interconnection layers is a key process that can be implemented together with NIL in a cost-effective large-area batch process. As the pioneer as well as market and technology leader in NIL and wafer bonding, EVG is leading the charge in supporting the infrastructure and growth of the biotechnology market by leveraging its products for use in biotechnology applications.

EVG's NIL solutions can produce a wide range of small structures (from hundreds of micrometres down to 20 nm) on a variety of substrate materials used in biotechnology applications, including glass, silicon and a variety of polymers (e.g., COC, COP, PMMA and PS). Each EVG NIL solution is uniquely suited for different production applications. For example, hot-embossing allows precise imprinting of larger structures as well as combinations of micro- and nanostructures, and is superior when replicating high-aspect ratio features or when using very-thin substrates. UV-NIL provides very-high precision, pattern fidelity and throughput in the nanometre-range. Micro contact printing, which is another NIL option, can transfer materials such as biomolecules onto a substrate in a distinct pattern.

With its established wafer-scale bonding equipment, EVG can also offer sealing and bonding processes that are well-aligned with NIL structuring technologies. A variety of different bonding options are available, ranging from advanced room-temperature bonding techniques to plasma activated bonding as well as high-quality hermetic sealing and vacuum encapsulation. Examples of typical solutions include EVG's thermal bonding equipment for glass and polymer substrates, which provides excellent results by enabling high-pressure and temperature uniformities over large areas.

EVG also offers its room-temperature selective adhesive transfer technology, which eases incorporation of bio-molecules prior to the encapsulation of the device.

"EVG has a long history of providing products and solutions for biomedical R&D, having installed the first hot embossing system for emerging bioMEMS and microfluidic research applications more than 15 years ago," stated Dr. Thomas Uhrmann, director of business development at EV Group.

"The knowledge that EVG has built up in this space coupled with our experience in bringing innovative technologies into volume production in other markets has positioned us well to provide proven high-volume manufacturing processes and services to the bio-medical industry to support the production of next-generation biotechnology devices."
* The source for this market data is the "BioMEMS: Microsystems for Healthcare Applications 2016" report, released by Yole Développement in April 2016.

Renesas delivers contactless wireless charging for wearable devices

RENESAS ELECTRONICS, a supplier of advanced semiconductor solutions, has announced a contactless wireless charging solution for low-power applications, such as hearing aids and other wearable devices that require resistance to water and dust.The new wireless charging solution consists of a power receiver integrated circuit (IC) (RAA457100) and a power transmitter IC (RAA458100). Each IC includes all functions needed for wireless charging on a single chip. Renesas will also offer an evaluation kit to help manufacturers with their wireless charging designs.

Wireless charging technology eliminates the need to change batteries or connect a power cable. This convenience has wide appeal for a variety of applications, such as smartphones and wearable devices. Wireless charging technology is of particular interest in low-power applications such as hearing aids that require small form factors as well as resistance to water and dust. However, existing wireless charging technologies have been considered unsuitable for

charging systems employing compact lithium-ion (Li-ion) secondary batteries for these low-power applications associated with the difficulties in achieving smaller form factors with the antenna size mandated by the current standards; and heat dispersion due to large charging currents that are required to charge low-power applications.

With the new wireless charging solution, Renesas has combined its wireless charging system expertise with its proven microcontrollers (MCUs) to enable all key system components in a small space for easier design implementation. In general, contactless power transmission involves applying a 125 kHz alternating current to the antenna coil of the power transmitter to excite the antenna coil of the power receiver and generate AC power. Renesas' newly developed power transmitter IC drives a bridge circuit and controls the alternating current to obtain the transmission power value required by the power receiver. The power transmitter IC integrates a bridge circuit overcurrent protection function and a two-line external overheating protection function. System manufacturers can modify parameter values by programming the read registers with external EEPROM data via an I2C interface to meet their application needs. In addition, they can further customize the solution to their requirements by connecting an external MCU.

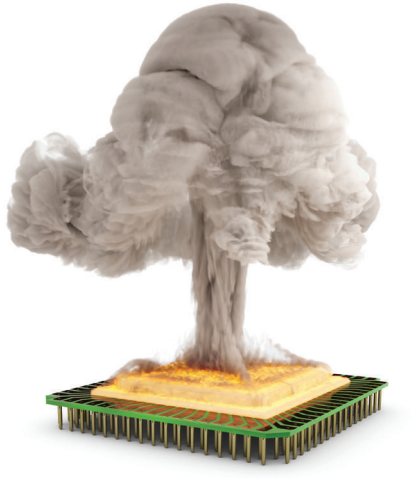
The μPA2690T1R power MOSFET from Renesas is recommended for configuring the bridge circuit. When it is combined with the RAA458100, the system manufacturer can choose between half-bridge and full-bridge circuit configurations to match the power level of the power transmitter.

Picosun patents ALD nanolaminate to prevent electronics from overheating

PICOSUN OY, provider of ALD (Atomic Layer Deposition) technology, has patented a novel ALD nanolaminate to protect electronics such as smartphones, tablets, computers, and lighting devices from overheating.

As both consumer and industrial electronics become faster, smaller, and more efficient day by day, overheating of the components such as batteries, microprocessors, and LEDs has become one of the key problems in the industry. Overheating leads to performance losses, failures in operation, and shortening of the device lifespan – and even to direct dangers, as heated batteries pose a risk of explosion.

Picosun's patented (*) 'phonon superhighway' nanolaminate coating conducts heat efficiently away from the device interior, decreasing its



temperature even 20 degrees. The heat is distributed through the casing of the device, along its surface. The coating can be applied at low temperatures on large batches of items with fast and cost-efficient processing in Picosun's fully automated production ALD reactors. "Our aim at Picosun is to utilize the ALD method not only to advance technological development, but also to improve the usability, safety, and lifetime of technical devices. Our new, patented nanolaminate coating addresses directly these challenges by solving one of the key problems in today's electronics – overheating of the components. Many world-leading electronics manufacturers have already expressed interest towards our invention. We are excited to present this novel ALD solution to our customers to help them improve the performance, reliability, and safety of their products," states Juhana Kostamo, Managing Director of Picosun.

(*) Application no. WO2016146881; "Heat-conductive ALD Coating in an Electrical Device"

Applied Materials brings E-Beam review technology to display Industry

APPLIED MATERIALS has introduced the display industry's first high-resolution inline e-beam review (EBR) system, which the company says will increase the speed at which manufacturers of OLED and UHD LCD screens can achieve optimum yields and bring new display concepts to market.

Applied is the semiconductor industry leader in EBR with more than 70 percent market share in 2015. The company has combined its leading-edge SEM* capabilities used in semiconductor device review with a large-scale display vacuum platform, resulting in an inline EBR technology that is the fastest, most effective method to discover and address the root causes of killer defects in advanced mobile and TV displays.

Applied's EBR system has received orders from 6 of the top 10 largest display manufacturers in the world and demand is increasing as manufacturers look to quickly and cost effectively optimize their yields and bring new types of displays to market faster. "Our new EBR system is the latest in a strong pipeline of display products that enables customers to solve critical OLED and LCD manufacturing challenges," said Ali Salehpour, senior vice president and general manager, Display and Adjacent Markets and Applied Global Services, Applied Materials. "Applied's unique ability to combine semiconductor yield techniques and panel-level SEM technology expands our addressable market and avoids costly yield excursions for our customers. Emerging applications such as augmented and virtual reality and smart vehicles require better displays with new form factors. These applications are driving demand for solutions like our EBR tool that give customers significant time-to-market advantages."

"As a worldwide leader in display, Tianma values the strong relationship with Applied Materials to help us develop new technologies required to produce the high-quality, high-performance mobile displays that consumers have come to expect," said Dr. Jun Ma, vice president, Tianma Micro-electronics Co., Ltd. "Applied's EBR system will enable us to reduce the start-up time at our Wuhan fab and accelerate our ability to bring more advanced display technologies to market. In addition to EBR, we look forward to working with Applied to introduce other semiconductor yield techniques to mobile display manufacturing."

Advanced display technologies require an increasing number of process steps resulting in more and smaller contaminates, and new types of defects. Current inline automated optical defect inspection tools for displays are not as effective as SEM analysis in distinguishing killer from non-killer defects, or in determining systematic root causes of defects. Prior to the introduction of Applied's EBR system, conducting SEM analysis on displays required breaking the glass substrate into pieces and examining each piece separately under a microscope. This is not only costly and time consuming but also makes it nearly impossible to determine the location of the defect on the full panel. Applied solves these limitations by providing inline SEM review at the industry's highest resolution and throughput without requiring the panel to be broken.

Lam Research expand ALE capability

LAM RESEARCH has announced that it is expanding its atomic layer etching (ALE) portfolio with the addition of ALE capability on its Flex dielectric etch systems.

Enabled by Lam's Advanced Mixed Mode Pulsing (AMMP) technology, the new ALE process has demonstrated the atomic-level control needed to address key challenges in scaling logic devices to 10 nm and below.

First in the industry to use plasma-enhanced ALE in production for dielectric films, the latest Flex system has been adopted for high-volume manufacturing of logic devices.

"From transistor and contact creation to interconnect patterning, a new level of precision is needed by logic manufacturers to continue scaling beyond the 10 nm technology node," said Vahid Vahedi, group vice president, Etch Product Group. "For device-enabling applications like self-aligned contacts, where etch helps create critical structures, conventional technologies do not provide sufficient control for the stringent specifications now demanded. Our latest Flex product with dielectric ALE delivers atomic-scale control with proven productivity to meet customers' key requirements."

To continue logic device scaling, chipmakers are adopting new integration schemes such as those using self-aligned contacts (SACs) in order to address issues like RC delay.

As a result, contact etch has become one of the most crucial processes, directly impacting both wafer yield and transistor performance. In order to define critical device structures with high fidelity, the etch process requires directional (anisotropic) capability with ultra-high selectivity, while also delivering the productivity needed for manufacturing.

Qualcomm opens test facility in Shanghai

QUALCOMM has announced the opening of Qualcomm Communication Technologies (Shanghai) Co. Ltd., a semiconductor test facility in the Waigaoqiao (WGQ) free-trade zone in Shanghai, and its first foray into providing manufacturing services for semiconductors. By working with Amkor Technology, the new company will combine Amkor's test services experience and cleanroom facilities with Qualcomm Technologies' experience in product engineering and development.

The new manufacturing facility demonstrates Qualcomm Technologies' commitment to continue to invest and help develop semiconductor expertise in China, and is indicative of growth in semiconductor market leadership in the country. Through the ownership and operation of a semiconductor test center, Qualcomm Technologies will enhance its focus on customer service, continue to develop its expertise in operational excellence, and increase its business presence in China. "The test facility is part of our continued mission to streamline supply chain operations and improve operational efficiency," said Roawen Chen, senior vice president, QCT global operations, Qualcomm Technologies, Inc.

Qualcomm Technologies continually strives to improve our manufacturing footprint in China and the formation of Qualcomm Communication Technologies in Shanghai is another example of this dedication," said Frank Meng, chairman, Qualcomm China.

"We are excited to work with Qualcomm Technologies in their new test operation in China," said Steve Kelley, Amkor's president and chief executive officer. "Amkor offers the most advanced outsourced assembly and test technologies in China, and this expanded relationship is a natural extension of the long history of close collaboration between our two companies."

Kulicke & Soffa enhance hybrid wedge bonder

KULICKE & SOFFA has announced the launch of its new extended version of the Asterion wedge bonder, Asterion EV. The Asterion EV is built on a new architecture with capability to address the industry's growing and changing applications needs. Its single platform can handle a multitude of interconnect materials such as large aluminium wire, PowerRibbon and interconnects for battery cells.

"The Asterion EV solution is well accepted in new application fields such as interconnects for battery cells manufacturing. With the combination of the configurable bond head and enhanced algorithms on placement repeatability, the Asterion EV has demonstrated stable process capability and performance. This is an exciting new launch for us and we anticipate a wide market adoption with the growth of battery cell interconnect technologies", said Chan Pin Chong, Kulicke & Soffa's Vice President of Wedge Bonder, Capillaries and Blades Business Line.

Von Ardenne supplies Fraunhofer IPMS with cluster system

THE FRAUNHOFER INSTITUTE for Photonic Microsystems IPMS has placed an order with VON ARDENNE for a new cluster sputter system CS400S for the deposition of thin films. The investment is part of the extension of the clean room of the Dresden-based institute to accommodate the 200 millimetre wafer technology. By installing the CS400S, Fraunhofer IPMS and VON ARDENNE seek to advance the development and production of highly reflective layer systems for micro (opto) electromechanical systems, the so-called MEMS and MOEMS. The MEMS that will be produced on the system are, for instance, micromirror arrays that will be used for semiconductor lithography and scanner mirrors, which are tailored for industrial applications.

This CS400S is one of the largest cluster systems that VON ARDENNE has built so far. It consists of two magazine load lock chambers, one pre-treatment chamber and five process chambers. The chambers are grouped around a central handling unit with an integrated alignment station. The cluster design of the system enables the sequential in situ deposition of several layers, without the necessity to remove the substrate from the vacuum.

VON ARDENNE has managed to prevail against some renowned competitors during the bidding process. “Two factors were critical for our decision”, said Dr. Matthias Schulze, head of the engineering department at Fraunhofer IPMS. “On the one hand, we are already using VON ARDENNE equipment for the coating of 150 millimetre wafers. Given the many years of good cooperation and shared experiences, we expect the CS400S to be an excellent system. On the other hand, this tool offers the greatest flexibility for the development of new processes for MEMS and MOEMS applications”, he continued. “The new machine platform combined with the strategic partnership with VON ARDENNE are key success factors for the sustainable expansion of our R&D and pilot fabrication activities”, said Prof. Dr. Harald Schenk, director of the Fraunhofer IPMS.

The high flexibility of the process modules is one of the benefits of the system. The chambers can be used for DC, pulsed DC and RF sputtering processes to achieve the best layer properties for MEMS. The VON ARDENNE process chambers ensure that the process is stabilized quickly during the use of reactive sputtering methods. In order to maintain the stability of the processes in the long run and to achieve a high layer homogeneity, the target-to-substrate distance can be adjusted in a wide range. The PID sputtering pressure control system is another feature of the CS400S that ensures high-quality layers. Fraunhofer IPMS and VON ARDENNE plan to establish a close cooperation so that both parties can develop more applications for industrial use and make them marketable. This can either be done in cooperation with each other or together with customers. Thanks to the expertise of both partners and the flexibility of the sputter system, it will be easy to adjust it to new requirements.

“Our cooperation with the Fraunhofer IPMS is very important for VON ARDENNE”, said Thomas Krischke, the CEO of the company. “Fraunhofer IPMS is a worldwide leading institution in developing MEMS and will help us open new business areas in the semiconductor industry.”

MosChip acquire three companies to expand IoT opportunities

MOSCHIP SEMICONDUCTOR TECHNOLOGY, a Hyderabad-based leading semiconductor company, has signed final agreements for the acquisition of three companies: elitePLUS Semiconductor Technologies Pvt. Ltd., and Orange Semiconductors Pvt. Ltd., both located in Bangalore, India, as well as Maven Systems Pvt. Ltd. of Pune, India. MosChip has made the acquisitions as part of the company’s growth plans in the Internet of Things (IoT) area and semiconductor industry.

elitePLUS Semiconductor Technologies has significant presence in the US and UK, and the company’s core competencies are focused on advanced verification, mixed signal, and low power verification. Orange Semiconductor provides offerings in verification, very-large-scale integration (VLSI) services, and embedded software.

The acquisitions of elitePLUS Semiconductor Technologies and Orange Semiconductor will strengthen MosChip’s end-to-end capabilities in VLSI services by adding more than 75 experienced resources in Bangalore. Maven Systems has several award-winning product and service offerings in M2M, IoT domains of remote monitoring, smart lighting, smart metering, smart cities and analytics with clients in more than 20 countries. Maven Systems is part of the growth strategy to allow MosChip to be a leading player in the IoT area.

The three acquisitions will help MosChip to increase the company’s global headcount to more than 250 experienced engineers across Hyderabad, Bangalore, and Pune in India; London; and Silicon Valley. MosChip also plans to add another 150-200 engineers across all locations. With multiple orders from the defense market and clients in the US, MosChip is set to record a very positive top and bottom line for the current fiscal year. The consolidated top line along with the acquisitions may show more than ten times the sales of previous years.

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Diamond proves useful material for growing graphene

Researchers develop method to grow graphene that contains relatively few impurities and costs less to make, in a shorter time and at lower temperatures

GRAPHENE is the stuff of the future. For years, researchers and technologists have been predicting the utility of the one-atom-thick sheets of pure carbon in everything from advanced touch screens and semiconductors to long-lasting batteries and next-generation solar cells. But graphene's unique intrinsic properties – supreme electrical and thermal conductivities and remarkable electron mobility, to name just a few – can only be fully realized if it is grown free from defects that disrupt the honeycomb pattern of the bound carbon atoms.

A team led by Materials Scientist Anirudha Sumant with the U.S. Department of Energy's (DOE) Argonne National Laboratory's Centre for Nanoscale Materials (CNM) and Materials Science Division, along with collaborators at the University of California-Riverside, has developed a method to grow graphene that contains relatively few impurities and costs less to make, in a shorter time and at lower temperatures compared to the processes widely used to make graphene today. Theoretical work led by Argonne nanoscientist Subramanian Sankaranarayanan at the CNM helped researchers understand the molecular-level processes underlying the graphene growth.

The new technology taps ultra nanocrystalline diamond (UNCD), a synthetic type of diamond that Argonne researchers have pioneered through years of research. UNCD serves as a physical substrate, or surface on which the graphene grows, and the source for the carbon atoms that make up a rapidly produced graphene sheet.
"When I first looked at the [scanning electron micrograph] and saw this nice uniform, very complete layer, it was amazing," said Diana Berman, the first author of the study and former postdoctoral research associate who worked with Sumant and is now an Assistant Professor at the University of North Texas. "I'd been dealing with all these different techniques of growing graphene, and you never see such a uniform, smooth surface."

Current graphene fabrication protocols introduce impurities during the etching process itself, which involves adding acid and extra polymers, and when they are transferred to a different substrate for use in electronics.

"The impurities introduced during this etching and the transferring step negatively affect the electronic properties of the graphene," Sumant said. "So you do not get the intrinsic properties of the graphene when you actually do this transfer." The team found that the single-layer, single-domain graphene can be grown over micron-size holes laterally, making them completely free-standing (that is, detached from the underlying substrate). This makes it possible to exploit the intrinsic properties of graphene by fabricating devices directly over free-standing graphene.

The new process is also much more cost-effective than conventional methods based on using silicon carbide as a substrate. Sumant says that the 3- to 4-inch silicon carbide wafers used in these types of growth methods cost about $1,200, while UNCD films on silicon wafers cost less than $500 to make. The diamond method also takes less than a minute to grow a sheet of graphene, where the conventional method takes on the order of hours. The high quality of graphene was confirmed by the UC Riverside co-authors Zhong Yan and Alexander Balandin by fabricating top-gate field-effect transistors from this material and measuring its electron mobility and charge carrier concentration.

"It is well known that certain metals, such as nickel and iron, dissolve diamond at elevated temperatures, and the same process has been used for many years to polish diamond," said Sumant. He and his team used this property to employ nickel in converting the top layer of diamond into amorphous carbon, but it was not clear how these freed carbon atoms converted instantly into high-quality graphene. After Sumant's and Berman's initial breakthrough of growing graphene directly on UNCD, Sankaranarayanan and his postdocs Badri Narayanan and Sanket Deshmukh, computational material scientists at the CNM used resources at the Argonne Leadership Computing Facility (ALCF) to help the team better understand the mechanism of the growth process underlying this interesting phenomenon using reactive molecular dynamic simulations.

Computer simulations developed by Narayanan, Deshmukh and Sankaranarayanan showed that certain crystallographic orientation of nickel-111 highly favour nucleation, and subsequent rapid growth of graphene; this was then confirmed experimentally. These large-scale simulations also showed how graphene forms. The nickel atoms diffuse into the diamond and destroy its crystalline order, while carbon atoms from this amorphous solid move to the nickel surface and rapidly form honeycomb-like structures, resulting in mostly defect-free graphene.

The nickel then percolated through the fine crystalline grains of the UNCD, sinking out of the way and removing the need for acid to dissolve away excess metal atoms from the top surface.
"It is like meeting a good Samaritan at an unknown place who helps you, does his job and leaves quietly without a trace," said Sumant.

"The proven predictive power of our simulations places us in a position of advantage to enable rapid discovery of new catalytic alloys that mediate growth of high-quality graphene on dielectrics and move away on their own when the growth is completed," added Narayanan.

In addition to the utility in making minimally defective, application-ready graphene for things like low-frequency vibration sensors, radio frequency transistors and better electrodes for water purification, Berman and Sumant say that the Argonne team has already secured three patents arising from their new graphene growth method. The researchers have already struck a collaboration with Swedish Institute of Space Physics involving the European Space Agency for their Jupiter Icy Moons Explorer (JUICE) program to develop graphene-coated probes that may help exploratory vehicles sense the properties of plasma surrounding the moons of Jupiter. Closer to home, the team has also crafted diamond and graphene needles for researchers at North Carolina University to use in biosensing applications.

The Argonne researchers are now fine-tuning the process – tweaking the temperature used to catalyze the reaction and adjusting the thickness of the diamond substrate and the composition of the metal film that facilitates the graphene growth – to both optimize the reaction and to better study the physics at the graphene-diamond interface.

"We're trying to tune this more carefully to have a better understanding of which conditions lead to what quality of graphene we're seeing," Berman said. Other Argonne authors involved in the study were Alexander Zinovev and Daniel Rosenmann. The paper, "Metal-induced rapid transformation of diamond into single and multilayer graphene on wafer scale," is published in *Nature Communications.*

The study used resources of the CNM and the ALCF as well as the National Energy Research Scientific Computing Center at Lawrence Berkeley National Laboratory, all DOE Office of Science User Facilities. Additional support was provided by the U.S. Department of Energy's Office of Science.

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Credit: Argonne National Laboratory

New optofluidic platform features tunable optics and novel 'lightvalves'

UC Santa Cruz engineers use flexible silicone material to build an integrated optofluidic platform for biological sample processing and optical analysis

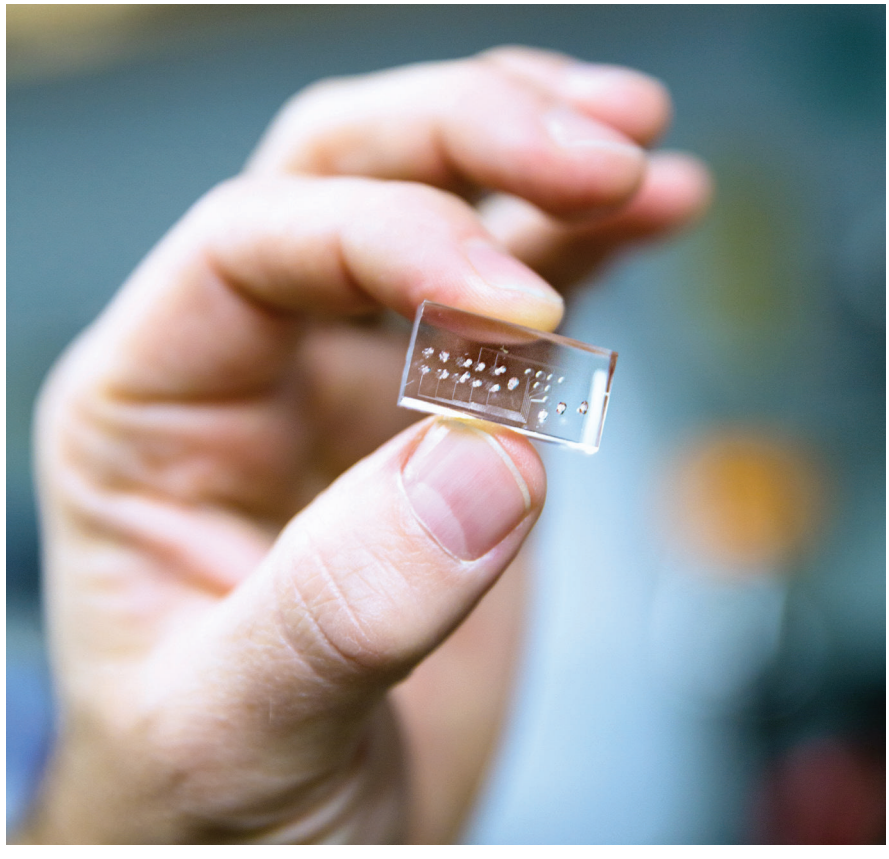

Photo Credit: Carolyn Laguttula/University of California, Santa Cruz

A NEW optofluidic platform for biological sample processing and optical analysis is made of polydimethylsiloxane (PDMS) and features tunable optics and novel 'lightvalves.' (Photo by C. Lagattuta)
For well over a decade, electrical engineer Holger Schmidt has been developing devices for optical analysis of samples on integrated chip-based platforms, with applications in areas such as biological sensors, virus detection, and chemical analysis.

The latest device from his lab is based on novel technology that combines high-performance microfluidics for sample processing with dynamic optical tuning and switching, all on a low-cost "chip" made of a flexible silicone material.
In previous devices from Schmidt's lab, optical functions were built into silicon chips using the same fabrication technology used to make computer chips. The new device is made entirely of polydimethylsiloxane (PDMS), a soft, flexible material used in microfluidics as well as in products such as contact lenses and medical devices.

"We can use this fabrication method now to build an all-in-one device that allows us to do biological sample processing and optical detection on one chip," said Schmidt, the Kapany Professor of Optoelectronics and director of the W. M. Keck Centre for Nanoscale Optofluidics at UC Santa Cruz.

The flexibility of PDMS allows for novel ways of controlling both light and fluids on the chip. Using multilayer soft lithography techniques, senior graduate student Joshua Parks built chips containing both solid-core and hollow-core waveguides for guiding light signals, as well as fluidic microvalves to control the movement of liquid samples. Schmidt and Parks also developed a special microvalve that functions as a "lightvalve," controlling the flow of both light and fluids. "That opens up a whole new set of functions that we couldn't do on a silicon chip," Schmidt said. "The lightvalve is the most exciting element. In additional to a simple on-off switch, we built a moveable optical trap for analysis of biological particles such as viruses or bacteria."

Parks and Schmidt reported the results of initial experiments with the new device in a paper published September in Nature Scientific Reports. In a previous study, Schmidt, Parks, and colleagues at BYU and UC Berkeley demonstrated a hybrid device in which a PDMS microfluidic chip for sample preparation was integrated with a silicon-based optofluidic chip for optical detection of viral pathogens. The new device combines both functions on the same chip. In addition, Schmidt said, the materials are relatively inexpensive, allowing rapid prototyping of devices. "We can do the full chain of fabrication here in our lab, and we can make new devices very quickly," he said.

Schmidt said the potential applications for this technology include a wide range of biological sensors and analytical devices. For viral diagnostic assays, for example, fluorescently labelled antibodies can be used to tag specific viral strains for optical detection.
This work was supported by grants from the National Science Foundation and National Institutes of Health.

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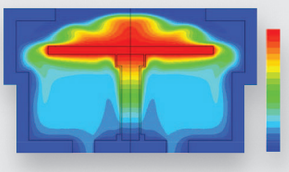

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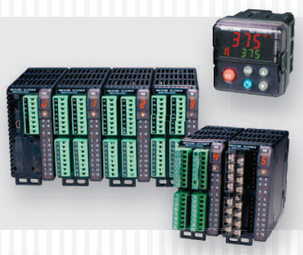

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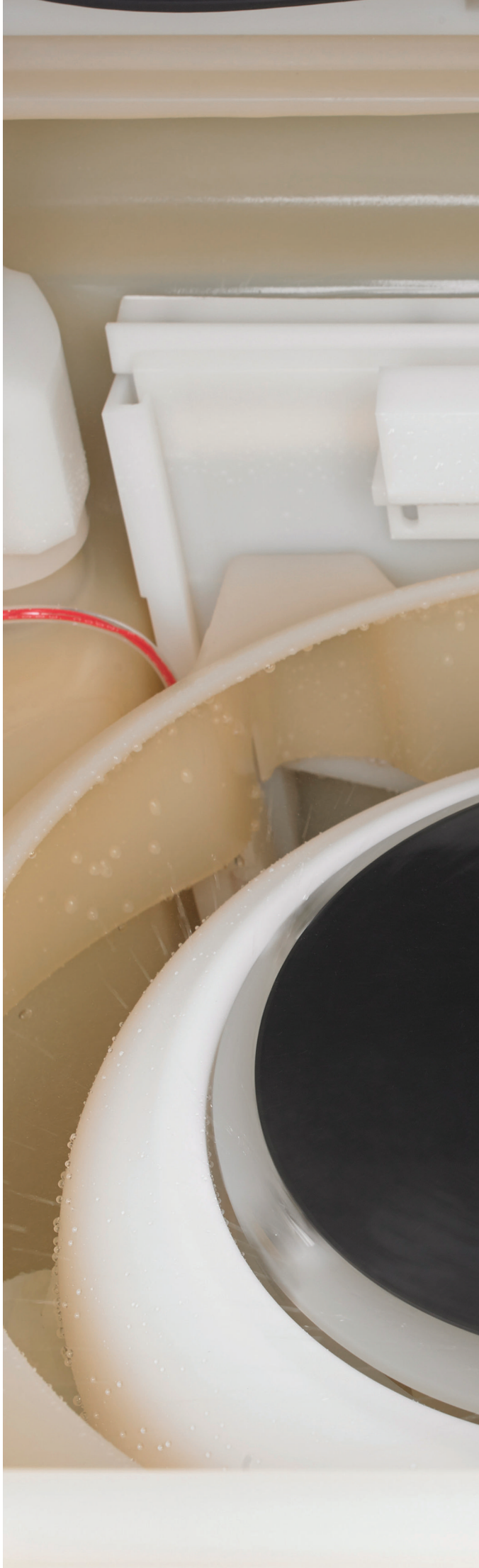
WET BEATS DRY IN 3D BACKSIDE PROCESS STUDY

With 3D integrated circuit wafer stacking entering mainstream HVM, backside processing has become a more critical step for device manufacturers. A study commissioned by Veeco Instruments points to clear advantages of wet etch processing. By Mark Andrews, technical contributor, Silicon Semiconductor.



Right: Veeco's silicon etch system is configured with Profile Match Technology for adaptive process control

FOR 3D-IC strategies to succeed, critical manufacturing processes need to maintain productivity and efficiency without extending costs and complexity to the point where negatives outweigh positives. A recent study commissioned by Veeco Instruments points to clear advantages for wet etch processes worthy of consideration by manufacturers looking for ways to optimize performance while reducing factory floor space and overall costs.

Careful and highly precise backside processing is an area of 3D-IC production that manufacturers pay particular attention to since success (or defects) have a multiplying effect. Backside processing is so important since through-silicon vias (TSVs) finished during these and subsequent steps are hands-down favorites for creating interconnects. TSVs also provide the greatest number of interconnection points compared to other strategies and can be produced with mature, cost-effective technologies.

While there are various points along the production process where TSVs can be made (first, middle or last,) the so-called 'via-middle' position has emerged as the most favored for etching vias into silicon. This point is somewhere between the contact and BEOL layers; approaches may differ from one manufacturer to another. (See Figure 1) In via-middle processing, the wafer has been bonded to a carrier and has gone through an initial grinding to thin the bulk of the silicon wafer.

Process tool manufacturers have focused on the steps that actually reveal the vias as a point of differentiation since the two major approaches are quite different and choices at this point represent options to reduce costs and complexity while improving results.

The figures and details documented in the study referenced in this article were produced by SavanSys Solutions LLC in cooperation with Veeco Instruments. SavanSys is a group of respected and specialized semiconductor industry supply chain cost modeling analysts that use the company's patented software and extensive process flow library to create activity-based cost models for assembly and/or fabrication plant operations.

Veeco's WaferEtch System enables uniform etching on multiple process levels for semiconductor and advanced packaging manufacturers

Two primary approaches to TSV reveal

After mechanically grinding silicon to remove the bulk of unneeded material, additional thinning is required to safely reveal the vias. This takes place to eliminate surface roughness and any defective silicon that may have been released during grinding. The final etch and surface conditioning can be done with a combination of chemical-mechanical planarization (CMP) and plasma dry etching, or wet chemical etching. One approach that is not typically used is simple CMP as a solo step due to the potential for contamination if copper particles come into contact with the silicon wafer backside.

CMP or dry-etch processes utilize costly slurries and involve cleaning steps to remove slurry particles and other contaminants not used in wet etch. They also include expensive plasma equipment and etching gases with much higher consumable and maintenance costs. Plasma etch processes also require a separate wet cleaning following intermediary steps. The SavanSys researchers found that Veeco's wet etch equipment and processes could replace four tools commonly used in the dry etch process of record (POR) including the CMP, plasma etch, cleaning and silicon thickness measurement tools. The key to making the wet etch approach most economical is eliminating the CMP step in the overall sequence. They found that Veeco's two-step wet process (all performed inside one advanced WaferEtch® tool,) accomplishes this in a simpler, more cost-effective manner.

Accelerating production/cutting costs

How can the wet etch approach to TSV reveal involve fewer steps and yield better results while it cuts costs? Essentially, the tool and processes were built from the ground up to do all these things along with delivering greater flexibility. Veeco Vice President of Marketing for its Precision Surface Processing BU, Scott Kroeger, explained the genesis of their wet etch approach.

"We were focused on the fact that the industry needs a lower cost silicon etch-to-reveal process in order to help the industry scale. The current competitive solution involves multiple tools, so the Capex associated with that is significantly higher than a single tool solution like Veeco's. Also, we were focused on delivering excellent surface (condition) and uniformity with lower consumables cost, which is also critical to enabling the silicon etch process. One other very important criteria in the design approach was to build a system that could sense incoming wafer profiles and adjust the etch process automatically to compensate without operator intervention. This takes complexity out of the process recipe tuning and puts the system virtually into autopilot," he remarked.

The first step in Veeco's wet processes relies on a high-rate silicon etch to contour and smooth the

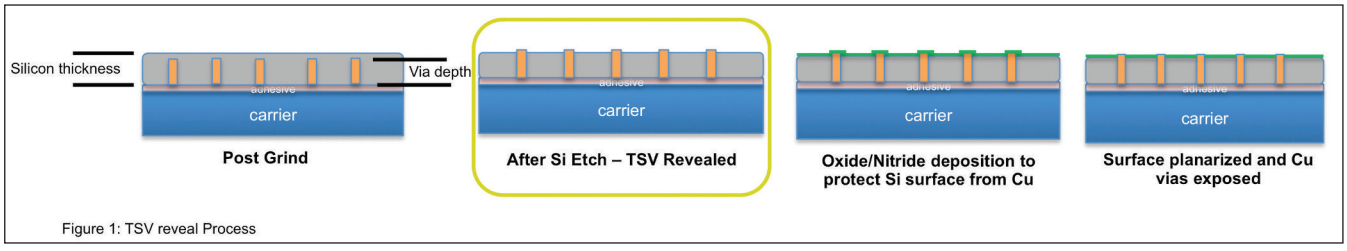


Figure 1: Veeco TSV reveal process

silicon surface to within ~2µm of the TSVs. This step eliminates grind marks from previous processing and compensates for non-uniformities in the silicon wafer. Next, the chemistry is changed to SACHEM Reveal Etch to precisely uncover the vias since this etchant is selective to silicon and does not etch the oxide liner covering the TSVs. Etching is controlled by integrated measurement of the silicon wafer before and after using the company's Profile Match Technology™ (PMT). (See Figure 2)

It should be noted that PMT adds utility beyond establishing and controlling etch rate. The incoming silicon thickness is measured and the program determines the etch profile based on TSV depth data and the reveal height requested by the manufacturer. This ability to precisely and automatically control thickness requirements enables compensation for radial variations for a more uniform reveal height, so it also reduces the amount of reveal needed in many cases. Lower reveal heights translate into lower passivation deposition, and typically, less final CMP to expose the copper surface.

Veeco's Chief Technical Officer for Precision Surface Processing, Laura Mauer, explained that the result of these key, primary wet etch process steps is a smoother wafer with fewer irregularities and a more precise approach to finished thicknesses. Mauer noted that Veeco's new approach does not incorporate TMAH (tetramethyl ammonium hydroxide), an etchant that has been used by other companies and research groups. Veeco replaced TMAH with SACHEM Reveal Etch™.

"TMAH is considered toxic, especially in the high concentrations that are needed for silicon etching. We eliminated it when we invented our approach. Veeco utilizes SACHEM Reveal Etch, which is about 5 times less hazardous than TMAH. The chemistry is one part of the differences in processes. The other is that Veeco's process uses a two-step etch sequence. First, a fast etch smooths the surface followed by the second step using the SACHEM etch to selectively thin the silicon and safely reveal the TSVs," she said.

Another important benefit of Veeco's wet etch compared to a dry etch is the final product: reduced

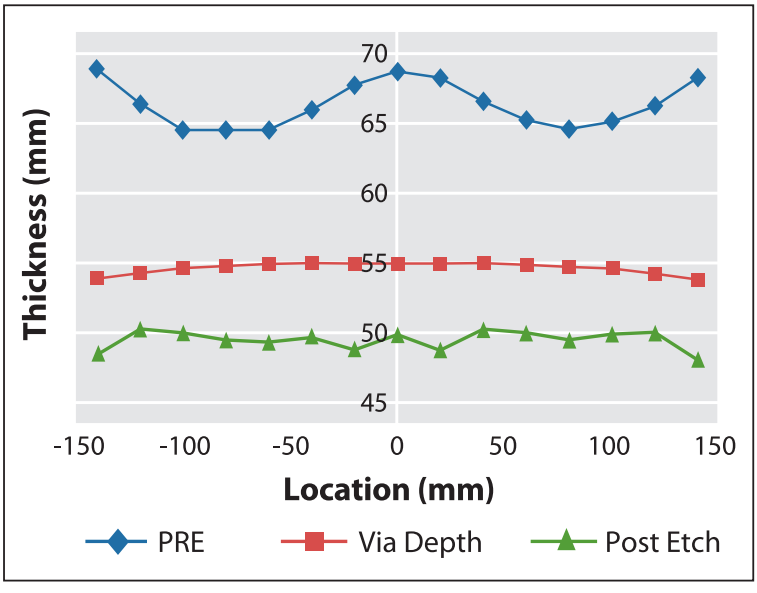


Figure 2: Profile Match Technology chart

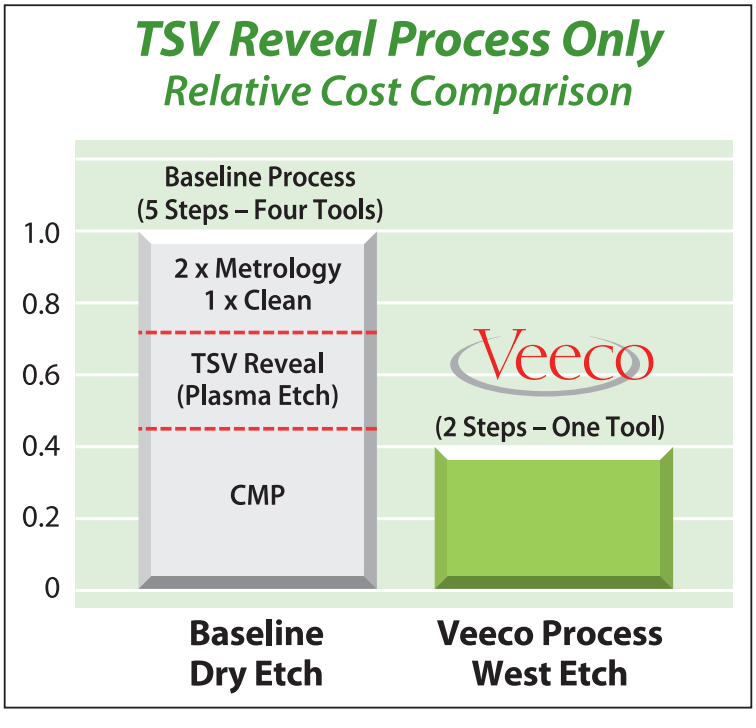


Figure 3: Direct TSV Reveal Process Step Comparison

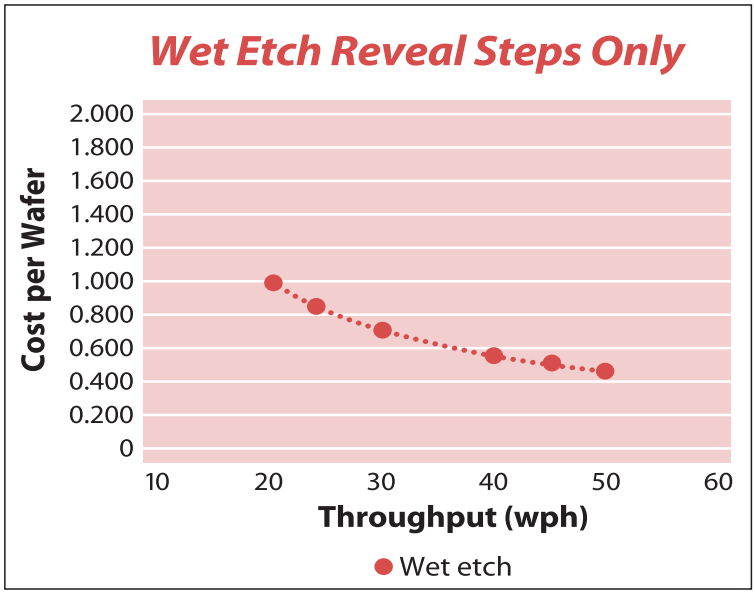


Figure 4a: Wet etch rate sensitivity analysis

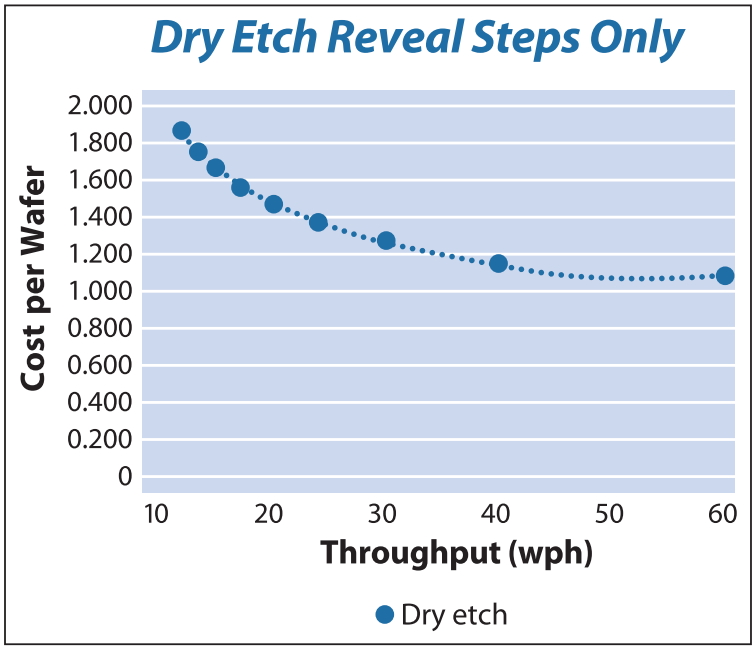


Figure 4b: Dry etch rate sensitivity analysis

surface roughness along with precisely controlled TSV reveal. While post-processing surface roughness can be 4nm or higher with dry etch, Mauer indicated that Veeco's wet etch pushes the benchmark below 4nm.

Cost modeling

Researchers utilized activity-based cost modeling to understand key cost centers of the TSV reveal process with both etching methods. This is a bottoms-up approach that involves breaking down a process flow into individual activities with the costs associated with each item factored into determining how dry vs. wet etch compare on an equal footing. For comparison sake, the TSV reveal process using dry etch begins with bonding to a carrier wafer. The process moves through a series of grinding and CMP steps occurring before and after dry etch, and includes chemical vapor deposition (CVD) passivation once the vias are revealed, along with a few metrology steps. The wet etch reveal process also begins with bonding to a carrier wafer and then proceeds through two major liquid-based process steps within one machine.

Figure 3 shows the cost comparison between the standard four-tool process of record versus Veeco's wet etch process. It is understood that this percentage is heavily dependent on design parameters, type of assembly, the number of redistribution layers (RDLs), etc. However, even with many variables it is clear that TSV-related processes are costly – about 11 percent of the total. Since every factory is somewhat different these numbers may vary; however, the comparison provides insight about relative cost structures and equipment needs as well as materials costs. Yields were assumed to be equal while any potential defect reductions obtained would add to the cost benefits. Determining the baseline is based upon the dry etch POR.

Strikingly, we can see that the two-step wet etch reveal approach delivers the same serviceability as the five-step dry etch baseline processes, yet wet etch costs less than half as much. Secondly, this type of comparison easily identifies where cost is coming from within each incremental step and not just the overall costs. Within the baseline dry etch POR, the plasma etch stage contributes high capital cost while the CMP step contributes high material cost. In the wet etch approach, most of the cost is associated with equipment (roughly 80 percent), which is not surprising since one tool essentially replaces four tools required for TSV reveal in the current POR that includes CMP, dry etch, clean and metrology. The charts in Figure 4a and 4b demonstrate how TSV reveal step costs change as the etch rate changes.

Comparing baseline cost drivers for both etch approaches provides important insights. Cost of ownership is critical to ensuring that an investment like TSV reveal is contributing to a manufacturer's competitiveness and not holding it back. Veeco's Scott Kroeger said that besides reducing the number of tools a factory needs to maintain, his company's approach also delivers better performance and increases throughput, reducing capital costs as well as consumable expenses. The Veeco approach also has long term applicability to a wide range of current and future device form factors.

"The TSV reveal configuration of our WaferEtch tool is well suited for other silicon etch process applications beyond 3D-IC. One main driver for wafer thinning is to reduce the thickness of semiconductor packages such as fan-out wafer level packaging for use in consumer electronic applications, MEMS devices and image sensors.

"There is a growing need for ultra-thin wafers (below 120μm) and we believe that wet etching can achieve

the best results in terms of uniformity and reducing surface roughness. Also, we find that after mechanical grinding and polishing steps, there is subsurface damage in the wafers that causes significant stress and presents a potential for yield loss. We have demonstrated that our wet etch process can remove most of the sub-surface damage and strengthen the wafers," he added.

Better control, smaller footprint, lower costs

The SavanSys analysis of Veeco's wet etch approach to wafer thinning and TSV reveal shows that wet etch can outperform various dry etch processes while reducing the complexity of these critical steps. Since TSV reveal can amount to 11 percent of an interposer-based process like those employed in building 3D-IC devices, controlling costs here has a multiplier effect and direct impact on a manufacturer's bottom line. By choosing an advanced wet etch tool like the Veeco WaferEtch solution, manufacturers can reduce the number of tools they have to maintain as well as the volume of costly consumables while achieving superior performance. Manufacturers can also extend their capabilities into additional wafer thinning operations that are expected to take a larger role in supporting next-generation device designs.

Veeco

Type of Company: Public

Traded as NASDAQ: VECO

Industry: LED, Data Storage, Semiconductors, Power Electronics, Wireless, Optical, MEMS

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Advances in underlying technology extend IGBT performance capabilities

With the adoption of GaN or SiC still some years away for mainstream utilization, power IC vendors need to provide the markets they serve with high voltage switching devices that are still based on established silicon processes and IGBT technology is certainly one that currently holds a lot of promise. Akhil Nair, Technical Marketing Manager for IGBTs, ON Semiconductor explains why.

INSULATED GATE BIPOLAR TRANSISTOR (IGBT) devices are vital components in high performance power conversion (HPPC) circuitry. While power MOSFETs are generally used for low/medium voltage implementations, IGBTs (which have voltage ratings in excess of 1kV) are highly optimized for deployment in challenging higher voltage environments. Improving operational efficiencies and reducing losses are now the fundamental concerns for engineers using these devices. The following article tackles this subject in detail.

While wideband gap technologies, such as gallium nitride (GaN) or silicon carbide (SiC) hold a lot of promise for the future, this is still a long way from being a cost-effective strategy for the vast majority of applications - the unit pricing would just be too high at this stage. It is estimated widespread uptake of GaN/SiC technologies probably remains at least 5-8 years away, as technology maturation and greater economies of scale are needed in order to bring price points down to an acceptable level. So, with this option not yet commercially viable, there is a pressing need for some sort of alternative.
Instead of implementing a move to new semiconductor materials, the industry has to find a way to push the performance envelope of existing IGBT technology. The question is…. how is this going to be done?

Application demands

Advances need to be made so that high voltage IGBT devices can support the elevated frequency levels that are now being demanded, which often extend above the 20 kHz mark as a minimum for many Hi-Performance Power Conversion (HPPC) application. This sort of performance is being expected in a growing number of application areas - among them hybrid/electric vehicles (HEVs), solar infrastructure, uninterrupted power supply (UPS) units and HEV charging stations. Power efficiencies at these higher frequencies has to improve significantly in these applications (heading towards figures of 95 percent in many cases). This implies that switching losses in traditional IGBT technologies needs to come down in order to meet these application demands.

Combating the thermal issues also associated with IGBTs is also of great importance and should not be overlooked. In today's complex power system designs, space is normally quite constrained. By improving switching performance and consequently system efficiency, the area that needs to be taken up by heatsinking mechanisms can be minimized. This leads to better board space utilization, lower bill of materials costs, while still ensuring the reliability is maintained.

The only way to enhance the performance characteristics of IGBTs, while staying with Si technology, is to explore new approaches in relation to how these IGBTs are designed. There are 2 important criteria that define IGBT operation and impact most acutely on its power efficiency.

Firstly, there is the total switching loss (Ets), which is the sum of the turn-on (Eon) and turn-off (Eoff) switching losses. IGBT switching losses can be substantial, especially when the device is running at higher switching frequencies and/or elevated operational temperatures.

Secondly, there is the conduction loss to factor in, which relates to the collector-emitter saturation voltage (VCEsat). An unavoidable trade-off exists between the switching loss performance and conduction loss performance. It does not achieve anything, therefore, to simply concentrate on reducing switching losses. Design engineers need to look at the whole thing, rather than a single element in isolation. It is commonplace to refer to the following figure of merit (FoM):

FoM = VCEsat x Ets

This FoM gives engineers a consistent way by which to benchmark the performance of IGBTs and compare the devices offered by different vendors.

Addressing IGBT switching losses

As mentioned earlier, with IGBT switching performance fundamentally consists of two components Eon and Eoff.

The Eoff of an IGBT can be reduced by two means;
a: by increasing the speed of the device i.e. decreasing the high to low transition time
b: by cutting the tail current.

Figures 1: Two approaches to reducing Eoff

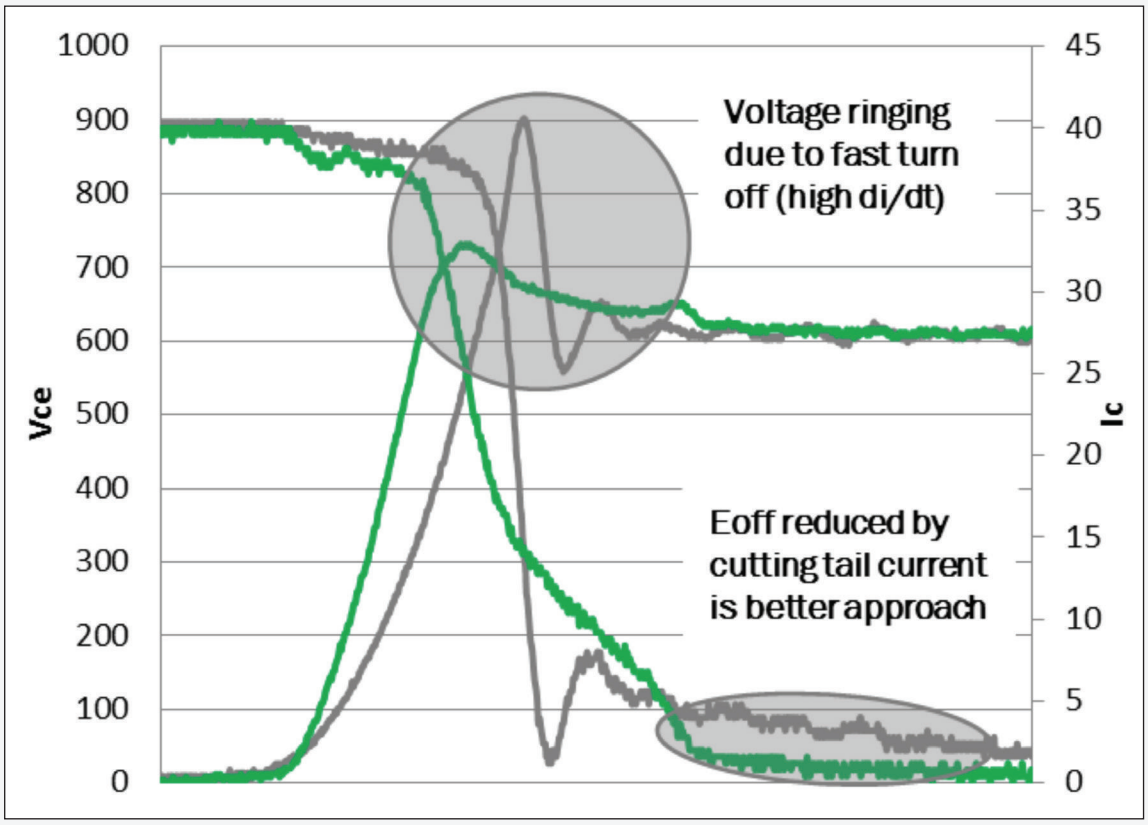
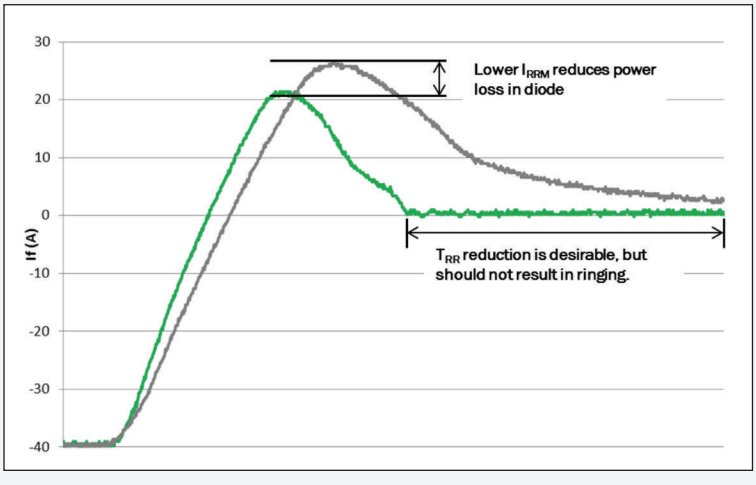


Figure 1 shows the two different scenarios where Eoff is reduced by the methods mentioned above. As seen on the grey waveforms reducing Eoff by increasing the speed (very high di/dt) of the device results in significant ringing.

Not only is this undesirable from an EMI standpoint, but the oscillations also contribute to increasing losses and also there is the added risk of device destruction if the peak voltage exceeds the device breakdown voltage. The alternate approach (green waveforms) of reducing the tail current is clearly more preferable since it allows for reduced losses while keeping maintaining a soft and smooth turn off profile. While Eoff is almost always considered a key measure of IGBT technology and Eon is oft ignored as it is dominated by the co-packaged rectifier. While this is true, when considering the device as a whole and its impact on system performance, it is important to not ignore the Eon since it can significantly contribute to system losses. As seen in figure 2, the diode reverse recovery performance is improved by reducing peak reverse recovery current (IRRM) and reverse recovery time (TRR). It is important to realize that too low a value for TRR would give very high dIRRM/dT, resulting in ringing. Therefore, the best approach to reducing reverse recovery losses (and by extension Eon of the device) is by reducing IRRM.



Figures 2: Fast switching response causing ringing

IGBT manufacturing challenges

Virtually all IGBTs today are designed as 'vertical' devices i.e. the emitter and gate terminals are patterned on one side of the wafer substrate while the collector terminal is on the other side. The FoM of the device is inversely proportional to the thickness of the wafer the device is constructed on i.e. thinner the wafer the higher the FoM of the IGBT. IGBTs today are routinely constructed on wafers <200μm. Essentially the most straight forward way to improve the FoM of an IGBT is by reducing its thickness. However, using thinner wafers has some significant challenges. Obviously, handling wafers that are thin a human hair present major issues during manufacturing.

But, more importantly reducing the thickness also results in a lower breakdown voltage. Most recent IGBT technologies use something called field stop technology to reduce the thickness while maintaining the breakdown voltage. This technology introduces a buffer layer (also called field stop layer) between the collector layer and the bulk of the silicon. The field stop layer, in addition to allowing a higher breakdown voltage also has the added benefit of reducing the Eoff of the IGBT. While a thick field stop layer is very desirable from a device performance standpoint, the silicon processing techniques required to create one are not simple.

Next generation IGBT solutions

Utilizing the company's proprietary Ultra Field Stop (UFS) trench technology, ON Semiconductor has now introduced a series of 1200V IGBTs with a very high FoM. The standard 1200 V/ 40 A device made with UFS technology has ~40 percent lower ETS and 15 percent lower VCEsat than the best most devices available in the market today. This means that these devices can offer the high degrees of performance now being stipulated, curbing system energy losses and boosting power efficiency levels.

The UFS devices are built on SOI (Silicon On Insulator) substrates. UFS is also the first time that wafers which are only 105μm thick have been used by 1200 V IGBTs. The ultra-thin devices are of course enabled by an extra thick field stop layer. The combination of the thick field stop layer and thin wafers contributes to these devices having such a superior FoM.

Another contributor to the performance improvements delivered by these device is the highly advanced platinum-silicon based rectifier that is co-packaged with the IGBT element. This is optimized specifically for operation in conjunction with the UFS technology. It assists in enforcing the desired reduction in reverse recovery losses without ringing.

Figure 3 shows the difference in power losses on a standard half bridge inverter, when comparing the UFS device against OnSemiconductors previous generation industry standard FS2 technology. The details of the application conditions under which the measurement was performed is shown in the figure. The results illustrate how significant reductions in the power losses is experienced with UFS technology. With the adoption of GaN or SiC still many years away, for mainstream utilization at least, power IC vendors need to provide the markets they serve with high voltage switching devices that are still based on established Si processes and IGBT technology is certainly one that currently holds a lot of promise. The combination of newer IGBT technologies such as UFS, combined with advanced fast recovery diode technology has enabled power efficiency levels to be pushed further to satisfy application demands.

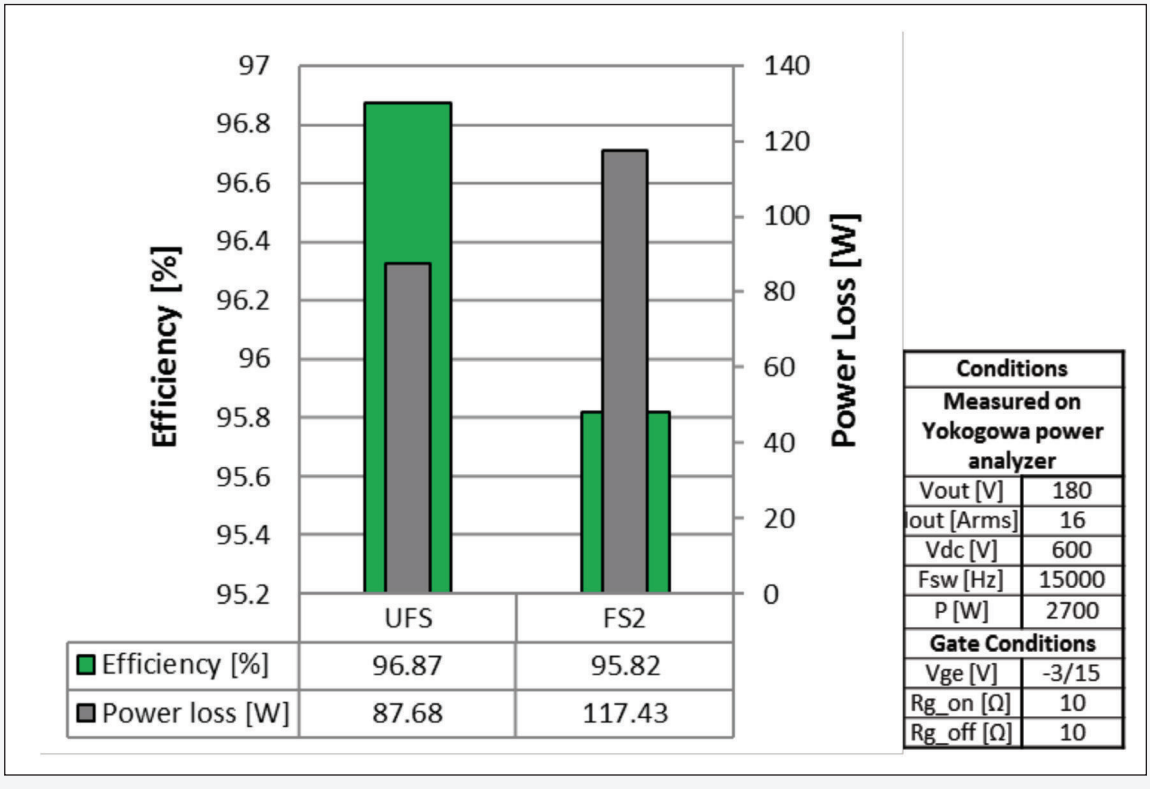


Figure 3: Efficiency and Power Loss Improvements with UFS technology

REINVENTING THE SPRING LOADED PROBE PIN

By reinventing and fully automating the manufacturing process, spring probe pins can now deliver high performance at price of a stamped contact for high density, fine pitch applications

FOR DECADES the spring-loaded probe aka pogo-style pin has delivered excellent mechanical and electrical performance in a highly compliant contact. However, this often came at a high cost given that each pin is constructed of 3-4 discreet parts manufactured and assembled in a laborious, less-than-fully-automated process.

The cost could be so exorbitant, in fact, that when significant volumes of pins are required, many opted to utilize less compliant, lower performance alternative contact technologies to reduce costs.

This approach is becoming less viable, however, with the increasing miniaturization of integrated circuits, electronic components and devices that pack more circuitry into smaller footprints. A single test socket for reliability and burn-in testing, for example, can require hundreds and even thousands of spring-loaded probe pins in a fine pitch configuration. The same applies to board-to-board compression connectors. When factoring in multiples of test sockets as well as production-level quantities of connectors, pin quantities can literally run into the millions.

Enter, or perhaps re-enter, the spring probe. With a new approach to pin design and a complete re-invention of the manufacturing process, miniaturized spring probes as small as 0.2mm are now available that provide a high temperature, current and bandwidth performance pin at the price of a stamped contact.

Traditional pogo-style pins

Although designed and manufactured in subtly different ways, the pogo-style pin is typically constructed of a pin, two plungers and a spring encapsulated in a metal shell.

This style of pin is highly compliant, which means it is designed to compress or "comply" during insertion. This is critical when attempting to maintain a good connection despite potentially uneven surfaces, varying heights, errors in parallelism and flatness, or pivoting or rotating elements.

Although compliancy can be achieved by other techniques, such as bends, buckles, or cantilever-style contacts, additional space between pins is required during compression. Spring-loaded pins operate in a purely vertical fashion, so the maximum space occupied at any time is defined by its diameter. This allows for placement of spring-loaded pins in fine pitch distances as low as 0.2mm.

The trend toward more compact, high density electronics design – defined as the number of pins in a small area or the distance between pin centers – is already impacting several markets. One market that regularly utilizes fine pitch spring probes is for electronics reliability testing, including burn-in, HTOL, HAST, THB and other testing protocols. To conduct this type of testing, sockets are manufactured to provide an intermediate (temporary) connection through an array of pins between the printed circuit

AVAILABLE IN VARIOUS LENGTHS AND PITCH SIZES AS LOW AS 0.2MM, THE PRODUCT IS THE BRAINCHILD OF PLASTRONICS, A GLOBAL PROVIDER OF TEST SOCKETS FOR SEMICONDUCTOR RELIABILITY TESTING. FOR MORE THAN 40 YEARS, THE COMPANY HAS USED SPRING-LOADED PROBE PINS TO CREATE FINISHED SOCKETS FOR BURN-IN, HUMIDITY, FAILURE ANALYSIS AND OTHER TEST REQUIREMENTS

board (PCB) and the components or multi-chip modules being tested. The PCB is then connected to a computer or other device for data capture and analysis to determine pass or fail.

The other market is compression-style board-to-board connectors used in electronics for telecom, automation, medical, aerospace, and military applications. These specialty connectors utilize spring probe technology to create a one-sided connector that is mounted against pads on the PCB. The benefits of spring-loaded connections include the elimination of receptacles to reduce costs, space savings, "one-touch" attachment and removal, and high durability.

Whether creating a temporary connection, such as for testing, or as a permanent board-to-board interconnection, the common denominator is more pins, less real estate.

"Devices used to have 2,000 pins in a two-inch square area. Now they want the same 2,000 pins in a one-half inch square and the only way to do that is to reduce the pitch of the device," says Ila Pal, Chief Operations Officer of Ironwood Electronics, a manufacturer of high speed sockets and adaptors for characterization, burn-in, and production testing.

"We were utilizing spring probe pins on a 1mm pitch design and more recently at .5mm," explains Pal.

"Then, last year, there were requests to shrink the pitch to 0.4mm. Now, we are moving even further down to 0.35mm" Germany-based test socket manufacturer EP Ants GmbH, is experiencing the same market trend. According to Rick Taylor, president and co-founder, 70-80 percent of the test sockets his company manufactures today are for high density applications.

According to Taylor, another market driver is price. Higher density means a higher volume of pins per test socket. Multiply that by the number of sockets required for parallel or serial testing at a single facility and customers expect companies such as EP Ants to deliver the best possible price without sacrificing performance.

"As everything gets smaller and the density gets tighter, pin counts are increasing," says Taylor. "At the same time, our customers expect to reduce their costs. So we challenge ourselves to find ways to manufacture our sockets at an achievable price whenever possible."

So when Taylor heard about a spring-probe called the H-Pin that could deliver high performance at a significantly lower price, he was immediately intrigued.

The H-Pin

The H-Pin is a stamped spring probe that delivers the

Although designed and manufactured in subtly different ways, the pogo-style pin is typically constructed of a pin, two plungers and a spring encapsulated in a metal shell

The H-Pin is a stamped spring probe that delivers the mechanical, electrical and thermal performance of a pogo-style spring probe

mechanical, electrical and thermal performance of a pogo-style spring probe. The highly compliant pin has a working range up to 1mm with a flat spring rate and can be utilized up to 15GHz with -1.0dB loss, carry up to 4 amps of current and withstand temperatures up to 200°C. Although there are a few design tweaks, the real departure is in the manner in which complete pin assemblies are manufactured using a high volume BeCu stamping process and a 100% automated, high speed assembly and inspection process that can produce up to 400 pins per minute.

Available in various lengths and pitch sizes as low as 0.2mm, the product is the brainchild of Plastronics, a global provider of test sockets for semiconductor reliability testing. For more than 40 years, the company has used spring-loaded probe pins to create finished sockets for burn-in, humidity, failure analysis and other test requirements. Depending on quantities, the spring-loaded probe pins can cost 30-50 percent less. With thousands of pins potentially in a single test socket or board-to-board connector, the savings can be significant.

According to Taylor, simply reducing the cost meant little without consistent pin quality. To ensure this was the case, EP Ants conducted extensive testing of the H-pin, which included inviting customers to also test the product and provide additional feedback. "As a test socket manufacturer, we have to rely on the quality of the pins we get from our spring probe supplier," says Taylor. "The H-pins have a very reliable quality level which is extremely important to us and our customers."

Meeting high performance demands

For spring-loaded probes pins, high performance characteristics are defined by the ability to withstand high temperatures required for burn-in and other tests, ability to handle increasing amounts of current over increasingly smaller pins, and the ability to handle high frequencies. According to Taylor, they do not rely on a single pin manufacturer. However, his company uses the H-pins for high temperature burn-in, tri-temp and HAST testing where the spring-probe is regularly subjected to temperatures well in excess of 200°C.

"The H-Pin works well when exposed to the high temperatures we use for burn-in or tri-temp testing," says Taylor. The tests are typically conducted at up to 240°C and, despite cooling the back side, the spring pins still experiences a fair amount of temperature. "We have worked with these pins above 200°C and we did not have a problem where other pins have failed."

The ability of the pins to withstand higher levels of current, despite shrinking in size, is also an increasing concern – particularly with the prevalence of higher power output lithium batteries. "These semiconductor packages and chips have power management features that need to be tested as well," says Taylor. "The H-pins can take a lot of current."

For high performance applications, there can be concerns about the construction of traditional spring-loaded probe pins and how its design can affect the quality of the connection under compression, the potential for unreliable test results requires all finished pins be tested and binned according to performance results. A very costly process step.

According to Ironwood Electronics' Ila Pal, the H-Pin solves this problem by utilizing a leaf spring between the two plungers along with external compression spring that allows the pin to maintain a good connection and pass signal throughout its movement.

Furthermore, the performance of the pin as measured by its contact resistance is also a benefit in high frequency testing. Whereas standard spring-loaded probe pins can experience wide variations in contact resistance, potentially leading to false failures, the variation in the H-Pin is minimal and well within accepted levels.

"For the H-Pins, the variation is very minimal," says Pal. "So, testing is very precise, because we can add a cut-off factor for pass and fail, without having to worry about false failures."

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ELASTOMER SEALS: PURITY OR PLASMA RESISTANCE? CAN YOU HAVE BOTH?

Reducing cost in semiconductor manufacturing is a constant way of life and reducing cost of consumables (CoC) is just one of many ways in which the industry can become more competitive and hence, more profitable. The seal type or material is an integral part of this cost equation. Knut Beekmann, Market Manager for Semicon and Dr Murat Gulcur, Senior Scientist at Precision Polymer Engineering (PPE) explain.

IN SEMICONDUCTOR MANUFACTURING, particle contamination throughout the whole process flow is a significant threat to yield and hence profitability. It's also not just a matter of limiting the total number of particles but, particle size can also be a critical factor. Key manufacturing technologies include vacuum processes such as dry etch and deposition, all of which require elastomer seals to maintain the vacuum integrity. Seals in critical locations, meaning in direct contact with the process and in relatively close proximity to the substrate being processed, are often exposed to extremely aggressive chemistries and variable temperatures.

The net effect is always some kind of physical degradation of the seal over time, the most obvious being erosion. The seal needs to be compatible with the maintenance period of the tool and should not be the limiting factor in determining mechanical intervention or labour intensive additional down time. Furthermore, the seal should not contribute to yield loss through whatever erosion by-products may be formed.

Reducing cost in semiconductor manufacturing is a constant way of life and reducing cost of consumables (CoC) is just one of many ways in which the industry can become more competitive and hence, more profitable. The seal type or material is an integral part of this cost equation.

Background

The choice of seal materials available to end users can be bewildering. Without the luxury of having test chambers or fab production equipment dedicated to testing a multitude of seal materials in the various applications, the choice becomes a potentially risky one, which involves making a change and running live product using a new seal.

The effort must therefore be rewarded with a cost saving that is commensurate with the risk or resource required to carry out such a test. Such a saving can be achieved either through an extension of the uptime cycle, a reduction in the part cost or, a combination of the two. In order to greatly alleviate the risk of incorrect seal choice, potentially leading to scrapped product or wasted test resource, a comprehensive study has been carried out to benchmark seal materials from the leading elastomer O-ring suppliers. The creation and maintenance of such a database serves to greatly offset the risk associated with

changing a seal material in order to reduce CoC and increase profitability or competitiveness.

Methodology

End users often run processes that are tuned to individual needs. It is also normal practice for manufacturers to keep such detailed process information confidential. To test every seal material in every process would be an impractical task. There are however, common chemistries used in plasma etch and deposition and this study was designed to test the various different elastomer materials in the more aggressive chemistries and plasma conditions. The process chemistries chosen are commonly used for etching of silicon, metals, compound semiconductors, dielectrics, resist ashing and particularly aggressive deposition chamber etch. Various different plasma modes were also employed, reflecting a variety of different process requirements. This included direct parallel plate, high density remote inductively coupled plasma (ICP) and sources specifically designed to create high radical and in particular, high fluorine radical content.

In all cases, elastomer materials were placed on the substrate holder on a carrier and subjected to the various process chemistries and plasma sources for fixed periods of time. The substrate holder was not biased to more closely represent the case where a seal would sit within a groove or retaining feature and as a result, would not normally be subject to significant ion bombardment. Materials were evaluated for their relative erosion rates or, mass loss and observation of surface particle formation. TGA spectra were also carried out in order to determine the nature of the material compound and in particular whether the material was purely organic and filler free, contained organic filler or, contained inorganic filler. The process chemistries chosen were:

- O2 in a direct parallel plate plasma system
- O2 in a remote ICP system
- Cl2, BCl3, HBr in a remote ICP system
- SF6, O2 in a remote ICP system
- SF6 in a low volume ICP optimized high radical plasma system

Figure 2: Oxford Instruments PlasmaPro ICP high radical etch system

Figure 1: Oxford Instruments PlasmaPro ICP etch system

The fillers used in the compounding play an important role in the plasma resistance of the elastomers. Most organic polymers have higher etch rates than the fillers. In order to achieve optimum, etch resistance, organic polymers are usually compounded with various types of fillers. The filler particles shield the organic backbone of the elastomer from erosion and therefore improve the plasma resistance of the elastomer material.

The filler particles which are dispersed and trapped within the polymer matrix however; can become free after the polymer matrix is etched away. These free particles on the elastomeric seal can cause contamination and therefore reduce product yields in chemically aggressive processes. In order to minimize the risk of particle contamination and decrease erosion rates, some advanced filler systems can be used in the plasma

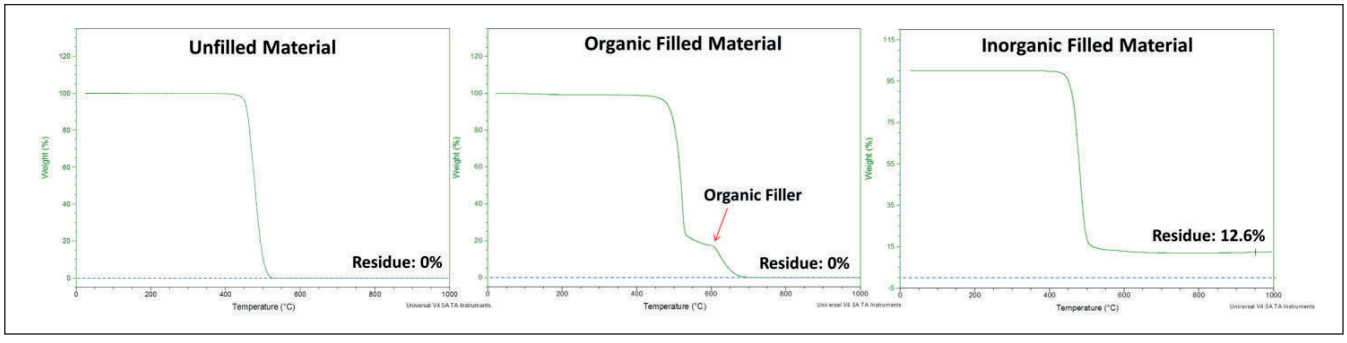


Figure 3. Thermogravimetric analysis (TGA) curves of A filler-free, B organic and C inorganic filled elastomer materials

resistant elastomeric material formulation. Minerals, metal oxides and synthetic fillers are some examples of advanced filler systems. In general, the fillers can be classified in two groups as organic and inorganic fillers. Inorganic fillers provide better erosion resistance when compared with organic fillers because of their rigid crystal structure and relative chemical stability. The chance of contamination however, is generally lower when organic fillers or no fillers are used in the elastomer formulation, with the disadvantage that erosion rates are considerably higher than their inorganic filled counterparts.

Results

The Thermogravimetric Analysis (TGA) curves in Figure 3 show the differences between the elastomer formulations with different filler types. A pure elastomer formulation with no fillers decomposes completely at around 500°C leaving no residue (Figure 3A). Similarly, a formulation prepared using an organic filler also fully decomposes at around 600°C without leaving any residue. In this case, the decomposition of organic filler can be observed in the TGA by a characteristic shoulder at slightly higher temperature than the polymer degradation (Figure 3B). A residue is observed in the inorganic filled elastomer even at high temperature after the organics in the formulation are fully decomposed (Figure 3C). The amount of remaining residue corresponds to the amount of filler used in the formulation. As mentioned above, the chance of particle formation and hence contamination, by using an unfilled or organic filled elastomer is lower than that from a traditional inorganic filled material but the etch rates of inorganics are lower than the organic filled or the unfilled polymers.

This paradox can be resolved by using an advanced inorganic filler system which also significantly minimizes the risk of contamination. The use of lower amounts of filler with maximized surface area is an ideal solution. A filler system with very high surface area has very small particles, ideally in the nanometer size range and they need to be well dispersed. In Figure 4, the plasma erosion rates of several different

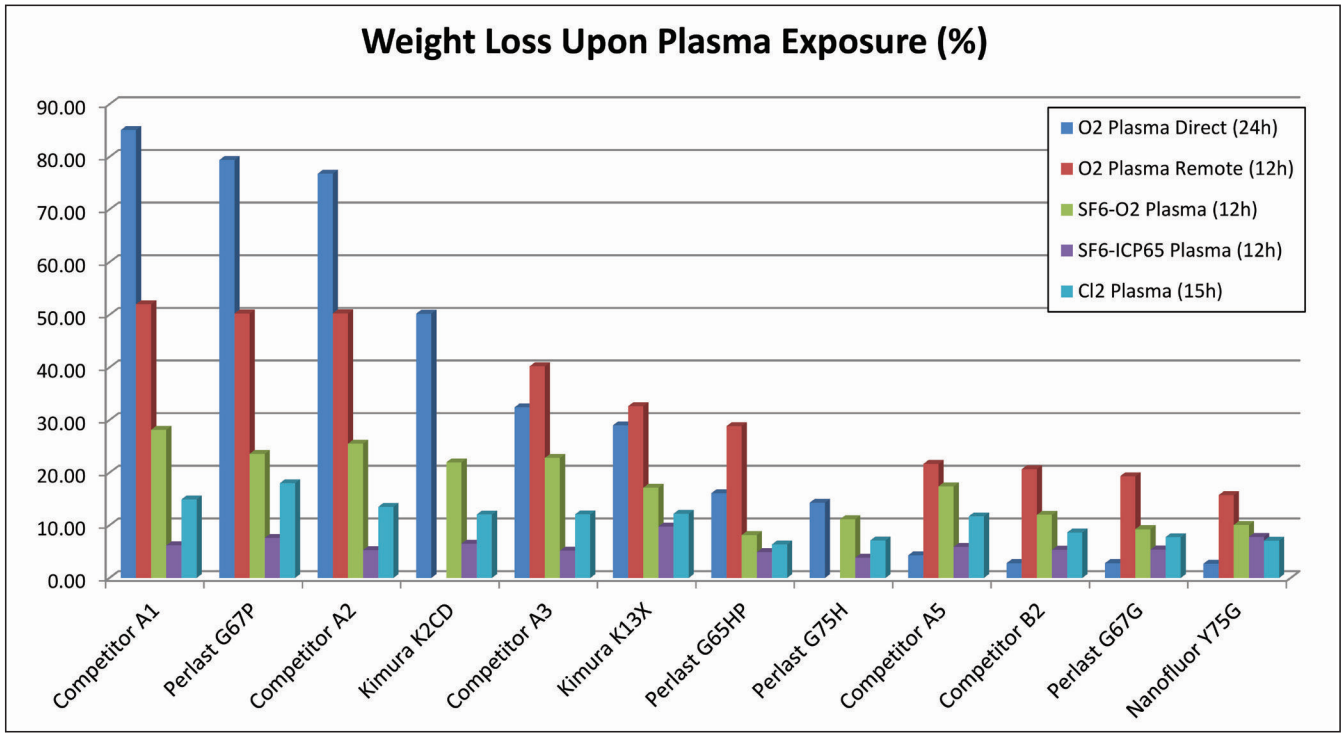


Figure 4 - Summary of the weight loss of various competitor, current and development PPE grades upon exposure to O2 (Direct and remote), SF6/O2, Cl2 (BCl3 / HBr) and high radical SF6 plasmas.

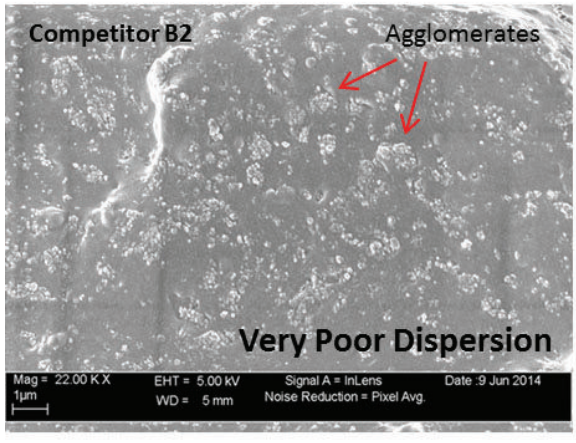


Figure 5a

Figure 5b

fluoroelastomers are graphically presented. Perlast® G67G and Nanofluor® Y75G have been found to provide very good plasma resistance in a variety of chemistries. These grades have been uniquely compounded with relatively low levels of an advanced, non-metal oxide, nano-filler system which has an average particle size of 25-40 nm.

The dispersion of nano-fillers[1] in the elastomer formulation is another very important factor for determining the plasma etch resistance and potential for particle contamination upon plasma exposure. Nano-fillers must be perfectly dispersed in the polymer matrix to achieve maximum plasma etch resistance and minimum chance of contamination of the wafer or substrate being processed.

Nanoparticles have very high surface energy and very large surface area. In order to diminish this energy, they naturally prefer to form agglomerates or clumps which consist of several or up to several hundreds of individual nanoparticles.[2] These agglomerates must be broken into single nanoparticles when compounding and dispersed uniformly in the polymer matrix. If this is not achieved, these agglomerates will behave as macro sized particles and can be released as micron sized defects upon plasma erosion. This phenomenon can be seen in the cross-sectional SEM image of an unused sample, Figure 5A, which is a very good example of poor filler dispersion. As can be seen in Figure 5B, Nanofluor® Y75G however, exhibits excellent Nano filler dispersion and therefore provides significantly reduced chance of contamination or, generation of killer defects.

Providing a smooth surface after plasma erosion is also very important for critical sealing applications. Excellent dispersion results in a smooth surface even after plasma exposure. Poor dispersion causes a rough and uneven surface as a result of inconsistent etch rates on the surface (Figure 5). The TGA analyses of grade B2, Perlast® G67G and Nanofluor® Y75G in Figure 7 shows that the amount of nano-filler used in grade B2 is 20-35 percent higher than in either G67G or Y75G respectively. This therefore leads to a higher risk of particle contamination from grade B2.

Summary

During aggressive vacuum wafer processing, elastomer seals

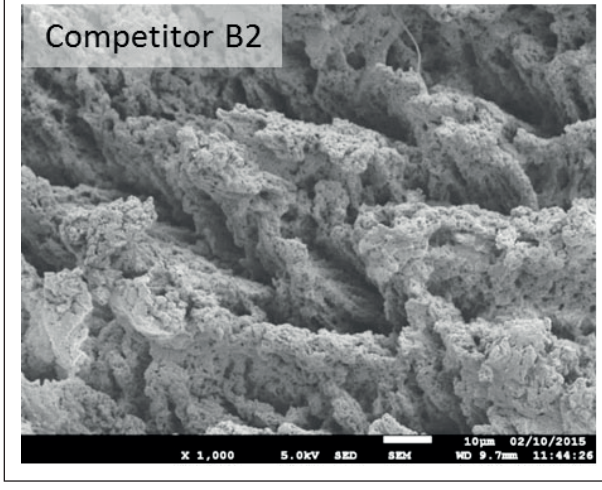


Figure 6a

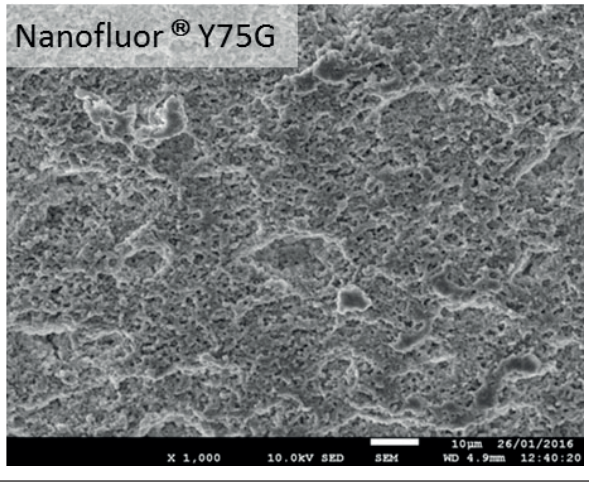


Figure 6b

in key tool locations will be subject to wear during normal operation and will expose the wafer to the degradation by products of the elastomer material and also to any compounded materials contained within the elastomer. As evidenced by the erosion rates, there is inevitably a compromise between using seal materials that are completely free from any filler and organic fillers and those that use inorganic filler systems although some overlap between materials can be seen.

The best solution is generally to use inorganic materials which have well dispersed nano-fillers in the compound, which therefore offer optimized erosion and hence seal lifetime and greatly reduced chance of yield limiting particle contamination.

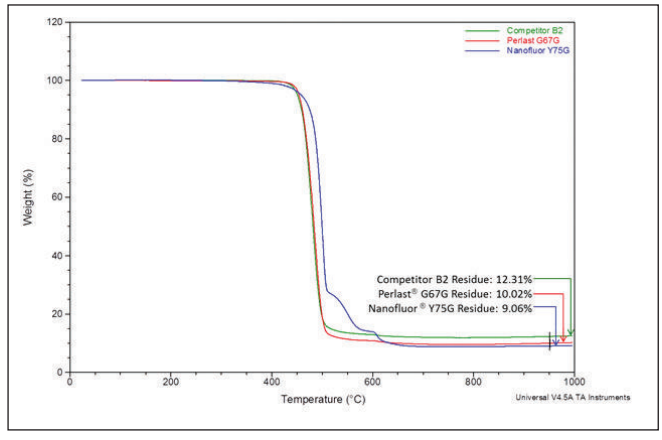
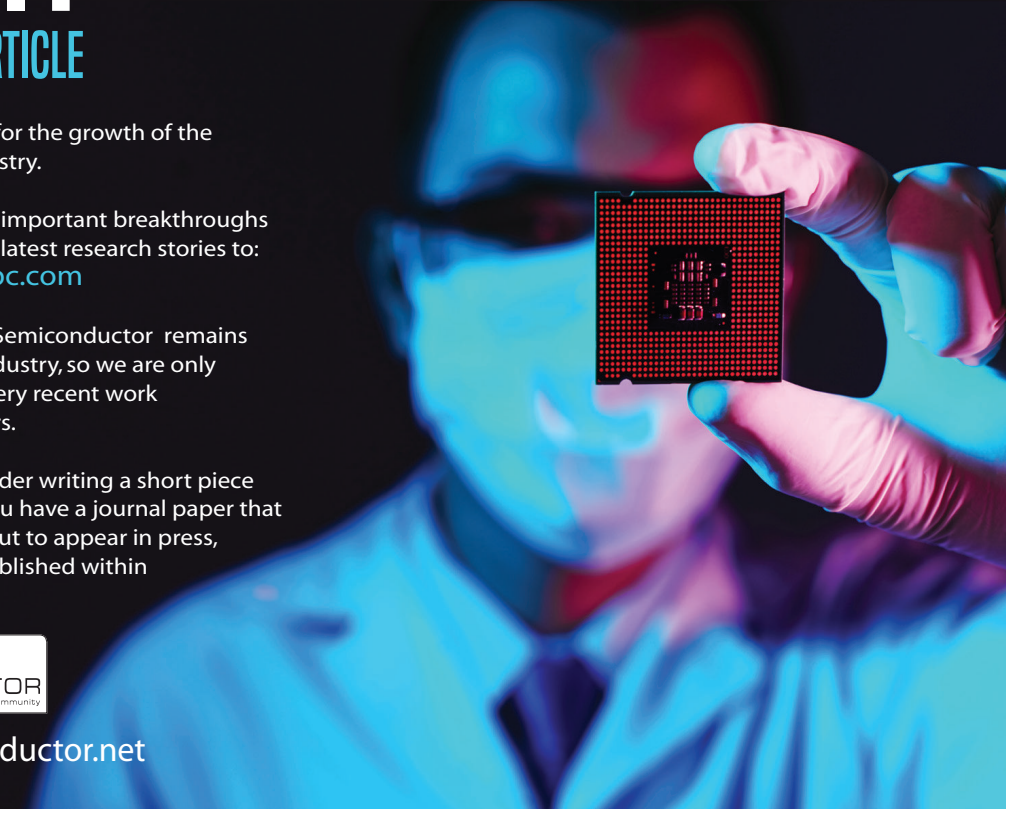


Figure 7 - TGA curves of Nanofluor® Y75G, Perlast® G67G and Grade B2.

Reference

1- Mark, J. E.; Erman, B.; Eirich, F.R. (Eds.) (2013) The Science and Technology of Rubber (4th Ed); Elsevier Inc., Oxford, UK. ISBN: 978-0-12-394584-6

2- Walter, D. (2013) Primary Particles – Agglomerates – Aggregates, in Nanomaterials (ed Deutsche Forschungsgemeinschaft (DFG)), Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, Germ



JST Mfg has an on-site applications laboratory where end users can develop their process with various chemistres and do tests on real equipment ranging from immersion and spray tools to dryers

Dialing-In' wet processing parameters for MEMS, nano manufacturing and R&D

Technology companies experience benefits from using wet processing equipment designed to handle a variety of application parameters. JST Manufacturing explains.

AS THE MARKET for nanotechnology (nano) and MEMS (Micro-Electro-Mechanical Systems) solutions continues to ramp up, the rate of organizations seeking to get involved with this sector is also burgeoning. Yet there are still significant challenges that are, in many cases, posing difficulties in entering this market.

For example, many developers who would like to enter the MEMS or nano field lack the resources, including development time and equipment, to do so. Also, specialized packaging in these areas, which requires simultaneous contact with its own environment while being isolated from other environments, is often expensive and difficult to achieve.

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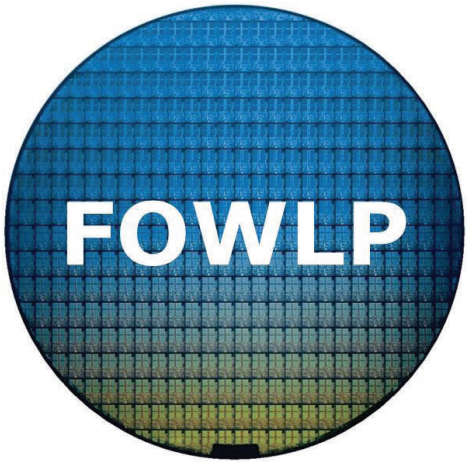

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"MEMS research and manufacturing organizations are meeting those challenges in unique ways," says Louise Bertagnolli, president of JST Manufacturing (Boise ID), a specialist in wet processing equipment for the MEMS, nano, photovoltaic, wafer and related industries. "An increasing number of universities and institutions offer the facilities, including equipment and instrumentation, to conduct MEMS and nano research and even produce prototypes and modest production runs."

Wet processing systems, one of the areas that organizations focus their attention on, are used for such procedures as etching, photoresist wet stripping, photolithography, metal lift-off, and related polymer removal processes.

Those processes aid researchers and manufacturers in improving product quality and throughput in a wide range of MEMS and nano applications such as microsensor- and microactuator-based devices. Some of these capabilities are used in contemporary applications such as the screen rotation of today's cell phone displays and the optical switches and mirrors to redirect or modulate light beams. Future applications will provide complete "system-on-a-chip" capabilities.

A wide variety of equipment designs is available to accomodate the many different wet process requirements

Making research more available

Although the cost of MEMS and nano application development can be very expensive, some institutions are installing facilities and making them available to both educational and commercial researchers. The University of Michigan's Lurie Nanofabrication Facility (LNF) is one example.

The LNF is a world-class facility in all areas of semiconductor device and circuit fabrication, integrated microsystems and MEMS technologies, nanotechnology, nanoelectronics, nanophotonics and nanobiotechnology. The LNF is an open-use facility with hundreds of users from various UM departments, as well as many other universities and businesses. According to Dennis M. Schweiger, Senior Director of Infrastructure, soliciting the opinion of equipment manufacturers regarding equipment design for such facilities can be highly beneficial.

"Since we essentially rent lab space and equipment to our diverse users, it is important that we provide them with wet processing equipment that suits their purposes well," says Schweiger. The original equipment design for the new lab area's wet processing benches was very specific, and determined by the LNF staff.

"We had looked at it in terms of process flow, from start to finish, not really taking into account the variety and variation of process samples that our user community might be working with, how we'd accommodate non-standard sample sizes, or what the impact might be in total cost of ownership with respect to chemical usage," adds Schweiger.

In addition, some of the new equipment had its decks reconfigured once the tools were installed. Several of the earlier wet benches, some of which were purchased over 20 years ago, were also modified to allow for more flexibility in meeting the process needs of the user community.

"In retrospect, our initial plan for the deck space, and processing capability of the benches, wasn't adaptable or flexible enough, and we worked with JST Manufacturing to implement modifications so that the bench decks were simpler, and could provide more working space," Schweiger concluded.

"Although there are similarities in the wet processing techniques used to create a broad variety of MEMS and nano devices, each process might not be identical in concentration, time, temperature and chemicals used," JST's Bertagnolli explains. As a result, there are a wide variety of equipment designs available that include process modules for solvents, acid, bases, deionized water rinse and drying. Mechanical, ultrasonic or megasonic agitation as well as high-pressure spraying and other processes may also be incorporated, if needed. Another consideration is safety and there are many mandated requirements for items such as ventilation, fire suppression, chemical handling and explosion prevention.

Dialing-in equipment design

Although manual wet benches are available, with the growth of the MEMS and nano markets many manufacturers are turning to automated equipment to increase throughput and ensure process repeatability. Fully automated process equipment often includes multiple stations or modules as well as robotics, sophisticated control, data logging and monitoring systems.

Since the design of many wet processing systems is proprietary, specifications are protected by the equipment manufacturer and user alike. Therefore, considering all of the possible design variables, it may be advisable to visit an equipment manufacturer with design capabilities and an application laboratory.

One of the prominent designers and builders of wet processing equipment, JST Manufacturing, has an on-site applications laboratory where end users can develop their process with various chemistries and do tests on real equipment ranging from immersion and spray tools to dryers. The laboratory includes sophisticated metrology equipment including a scanning electron microscope and a Tencor particle counter.

By visiting applications labs such as those provided by JST, end users can "dial-in" and optimize their processes, and can minimize the amount of chemicals required and/or determine the tool features they need for their applications. This can save the customer money by eliminating features they do not need. "Even though a manufacturer arrives with a good idea how they want to handle the wet processing, we are often able to recommend modifications after we have a chance to review the project," says Bertagnolli. "Sometimes design variations will perform the cleaning or etching work in the manner required, but will also save money, reduce the floor space requirement, simplify maintenance or provide other benefits," she adds.

"Since the design of many wet processing systems is proprietary, specifications are protected by the equipment manufacturer and user alike. Therefore, considering all of the possible design variables, it may be advisable to visit an equipment manufacturer with design capabilities and an application laboratory"

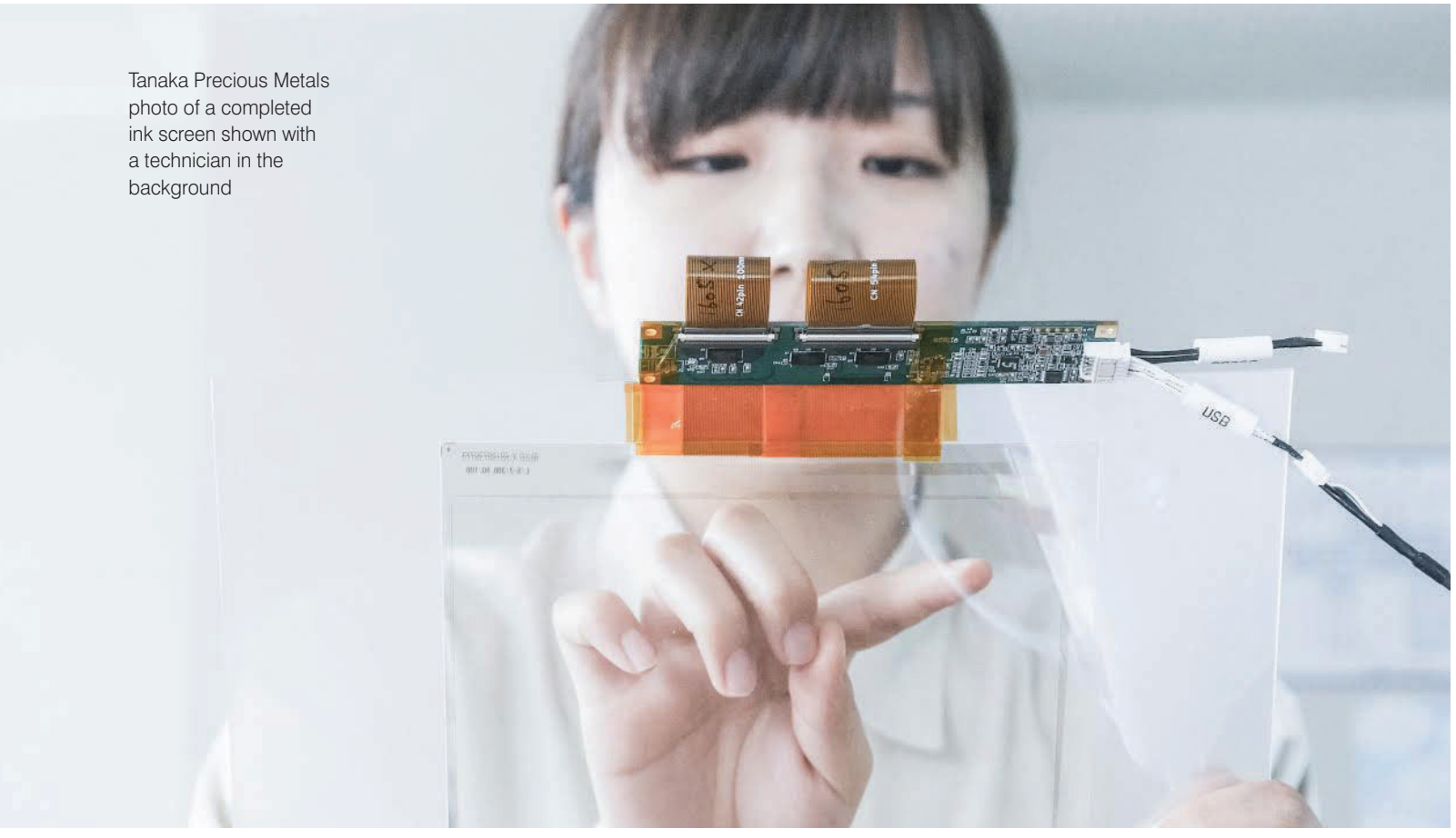
Dialing-in parameters

To facilitate the economical design and building of a wet processing equipment solution, many users insist on a standardized approach with customizable features that will best handle their applications parameters.

For example, JST utilizes standard products and standard methodologies to design and manufacture equipment. Using SOLIDWORKS 3D-modeling software, the company can make minor changes and modifications to meet the needs of each application. Also, the equipment is modular by design, allowing for easy changing and reconfiguration should the process or product requirements change.

Another powerful feature: each unit is designed with software that is capable of performing all tool functions, including those that are not required. With this, end users can create their own process, or recipes, with all sub-routines at their disposal.

"We like to give customers added flexibility by programming their equipment to do everything that the equipment is capable of doing," explains Louise Bertagnolli, JST president. "This enables them to dial in applications, such as chemical concentrations. They can also turn various features on or off, depending on their process requirements. Even though they may not need some of the features today, they may want to turn them on in the future, which can be both economical and powerful."



Tanaka Precious Metals photo of a completed ink screen shown with a technician in the background

Anxiously anticipating big opportunities

A relatively flat semiconductor market in 2016 has led to more consolidations and longings for the advent of IoT devices to impact the global chip marketplace. Mark Andrews technical editor at Silicon Semiconductor discusses.

THE SILICON semiconductor equipment market in 2016 remains relatively flat while chip revenue continues on a slight downward track, according to the SEMI trade organization. At SEMICON West and subsequent industry events, hopes for strong growth are pinned to new internet of things (IoT) device sales in 2017 and beyond.

Semiconductor manufacturers find themselves in another recovery year in which uneven global economic news keeps downward pressure on silicon IC prices as well as the tools that make them. The SEMI group expects by the time we close the 2016 books, fab equipment for wafer processing, test, assembly and packaging may see about 1 percent annualized growth compared to 2015, which was off substantially compared to more robust sales in 2014.

While Taiwanese fabs are expected to retain the top-spot in new equipment investments this year, more that USD $9 billion, they will be followed closely

by China at nearly $6.5 billion and Korea at about $6.1 billion. China leads in terms of fab equipment investment, up more than 30% compared to last year. Non-traditional semiconductor markets—areas outside Europe, North America and Asia—contributed a whopping 59 percent increase this year. Although small compared to the deep-pocket spending elsewhere, the so-called Rest of the World (RoW) spending hints that non-traditional semiconductor manufacturing centers are looking to gain a share of the IoT growth potential

With so much riding on expected growth of IoT spending— connected 'smart devices' of every imaginable shape and function, why isn't the market already churning along at a robust pace? According to Future Horizons founder and CEO Malcolm Penn during his autumn industry forecast seminar in London (September), current revenue levels have little to do with IoT prospects. Penn said the far-from-stellar chip market performance can find its roots in the lackluster global economic recovery that has stymied investors of every stripe. Penn said he believes that because the industry is now driven by a relatively few high-volume chipmakers (4 to 5 depending on who is counting,) as a group they do not throw money into the fray until economic trends move solidly upward.

Penn pointed out that ICs are now an inescapable part of a global economy. Whether good or bad, this means that equipment and device-level sales performance ties closely to worldwide economic conditions. This global influencer status helped buoy semiconductor markets for economies during the worst days of the Great Recession. But during a period some call 'economic malaise,' it swings the other direction when emerging economies trim spending, energy sectors trend lower, wars engulf some regions and major political events (like the upcoming US presidential election) make headlines.

Poor growth has also led to semiconductor industry consolidation (USD $100 billion in 2015,) which further tends to dull enthusiasms for risk-taking. While consolidation slowed to half the 2015 rate this year, Penn's forecasts for 2017 chip sales range widely between nearly 3 percent positive to the possibility of backsliding as much as 3 percent if worse-case scenarios play out.

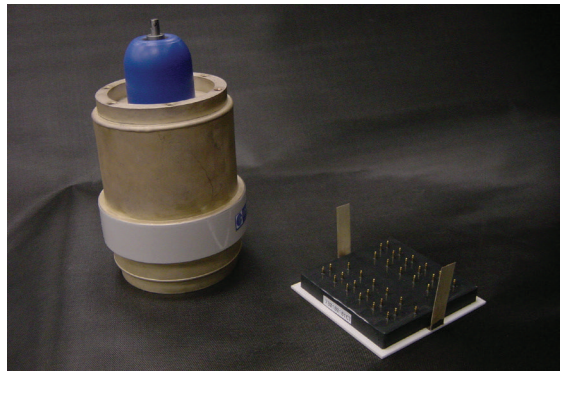
Semiconductor sales have long been driven by major waves of technological innovation such as the ascendency of personal computing and smartphones. Market watchers are now awaiting a third wave—universal device connectivity through the IoT. But IoT is in its relative infancy, so its influence is small compared to other electronics mainstays. IC Insights (in their September updated market report,) projects IoT related sales will finish at about USD $18 billion in 2016; they forecast this growing to $26.9 billion per year by 2019. The entire semiconductor chip sales market should be about USD $335.6 billion this year. IoT's potential is clear.

Reno Sub-Systems show one of their complete systems. Although replacements for legacy devices need to be the same size/ footprint, new installations could be substantially smaller. All Reno RF power systems are more stable, much faster and perform with very little reflected power compared to legacy solutions.

Exhibitors at recent SEMICON West and Intersolar events aren't waiting for 2017 to get excited. New ideas abounded, with many companies showcasing new approaches at these events and others in third quarter across the semiconductor supply chain.

Leti, a CEA institute, led-off with its next-generation 3D network on a chip (3D-NoC) that researchers in Grenoble, France said substantially boosts performance while reducing energy consumption. An earlier generation of the 3D design premiered as a demonstrator project early in 2016. The updated design is called IntAct, which means ACTive INTerposer, playing-off the fact that Leti's design places active components inside a silicon interposer whereas competing 3D designs frequently utilize solid silicon without embedded actives. There are two essentially different approaches to achieve 3D benefits. The first uses stacked chips relying on interconnections to speed signal processing. In the second, chips are designed with vertical structures to increase density. The Leti design is essentially a chip stack, but with a difference.

Let's differentiator is placing active components like electrical pathways inside the interposer; they have plans for future designs using optical connections. In its latest demonstration project, Leti showed chip-



An EVC matching network component from Reno Sub-Systems (left) is compared to its counterpart in a traditional plasma system.

A portion of KLA-Tencor's new inspection portfolio

to-chip data transmission speeds-in the hundreds of megabits per second (M/bs) in a chip measuring just 40 μm x 40 μm. Along with high speed processing, the new design needs 20 times less energy for data transmission than chips on electronic circuit boards. Leti indicated that their new IP is compatible with standard remote direct memory access-type software used for data transmission as well as virtual-server migration applications.

The wafer inspection and process control leaders at KLA-Tencor announced six new products for advanced defect inspection and review at SEMICON West followed by a suite of three new reticle inspection systems. All new products focus on devices at the 10nm node and below.

KLA-Tencor's new inspection and review products include the 3900 Series (previously referred to as a 'Gen 5' product); the 2930 Series broadband plasma optical inspectors; the Puma 9980 laser scanning inspector; the CIRCL 5 all-surface inspection cluster; the Surfscan SP5XP unpatterned wafer inspector and the eDR7280™ e-beam review and classification tool. KLA said these new systems employ a range of innovative technologies to form a comprehensive wafer inspection solution that enables discovery and control of yield-critical defects at all stages of IC manufacturing.

KLA Tencor's new reticle inspection device family.

KLA pointed to performance advantages in all of its new systems such as decreasing time for the delivery of usable data, eliminating nuisance defect reports as much as 4x, and continually tightening control mechanisms. The new tools also utilize improved algorithms for better identification, classification and signature ID with no throughput loss. VP for Customer Engagement Mark Shirey called out the new 3900 and 2930 inspectors as examples of what the entire suite could offer. In the case of these new patterned wafer inspectors they achieved a "…sweet spot for yield enhancement. An entire wafer of 10nm devices can be scanned in an hour, so throughput is the real value along with high reliability at that speed. This makes (the tools) indispensable for accelerating ramp."

KLA-Tencor followed its SEMICON West announcements with three new reticle inspectors to address 10nm and below mask technologies: the Teron 640, Teron SL655 and Reticle Decision Center (RDC). The company described all three systems as enabling present and next-generation mask designs by more efficiently identifying lithographically significant and severe yield-damaging defects.

EV Group (EVG) announced significant additions to its metrology and wafer bonding tool line-ups, including the EVG50 automated metrology system. The new

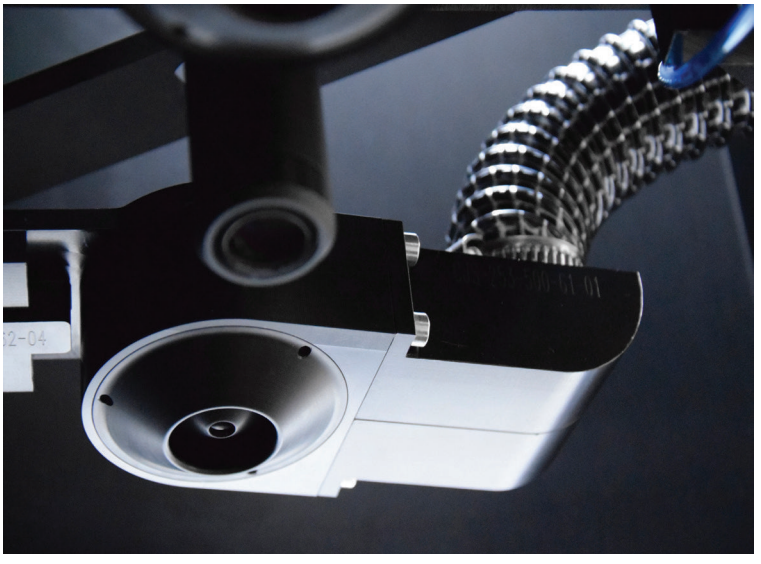
EVG50 is designed to support increasingly stringent manufacturing requirements for advanced packaging, MEMS and photonics applications. It complements the company's versatile EVG40NT measurement system, which has become an industry standard for bond overlay inspection. The EVG50 performs high-resolution non-destructive multi-layer thickness and topography measurements, as well as void detection in both bonded wafer stacks and in lithographic photoresists. The system measures down to two microns in layer thickness, and can inspect up to one million points, achieving throughputs (with 300 mm substrates) of up to 55 wafers per hour. The EVG50's high throughput and unparalleled accuracy and repeatability, even at ultra-high resolutions, enables cost-effective, 100-percent inspection of production wafers, resulting in improved process control.

EVG has also expanded its line of wafer bonding solutions with two new ComBond modules designed for automated high-vacuum wafer bonding in high volume production environments producing such as the latest MEMS devices. The products include a new vacuum bond alignment module that provides sub-micron face-to-face alignment accuracy, which is essential for wafer-level MEMS packaging. EVG also announced a new bake module that performs critical process steps with what they describe as outstanding bond quality and performance of encapsulated MEMS devices. The tools use a modular approach to augment production lines and enable greater levels of accuracy. EVG's latest innovations add new capabilities, such as bonding at room temperature through the ComBond Activation Module (CAM) designed to bond temperature sensitive materials.

In discussing the new capabilities, EVG VP and general manager of North America, David Kirsch, said that the company's ability to control or eliminate oxidization of metal layers is especially appreciated by customers working with aluminum. EVG uses a preheating step prior to bonding, and that offering these benefits all under vacuum is a significant advantage. "The new products fill a void that has existed in the industry—to create bonds without oxidization with extreme accuracy under vacuum. Offering this in a modular system greatly enhances customer advantages," he noted.

EVG's new tools also can provide vacuum encapsulation, which is increasingly needed for certain MEMS devices in order to reduce power consumption caused by parasitic drag, reduce convection heat transfer, or prevent oxide corrosion. Maintaining the required vacuum level for the entire wafer bonding process has been a key challenge for ramping these devices into high-volume production.

New innovations were also announced by 3D Micromac, with a focus on their micoDICE system that leverages thermal laser separation techniques. 3D Micromac calls their adaptation TLS-Dicing; this has been productized in their microDICE system, a high throughput platform designed specifically for hard and brittle wafer substrates, thin wafers at high risk for breakage, new packaging technologies and smaller devices on larger substrates. A material perfect for the new laser technology is silicon carbide (SiC) with a rating of 9.2 on the Mohs scale, the company said.



3D Micromac shows a close up from inside its new MicroDICE thermal laser separation system that is ideal for hard/ brittle substrates such as SiC wafers.

At the heart of 3D Micromac's new microDICE system is their new ultraviolet laser in combination with microbursts of deionized water that seamlessly cleave a wafer into individual devices. Unlike diamond embedded saw blades that create a wide kerf as they singulate devices, or other laser approaches that can ablate wafer surfaces, the TLS-Dicing approach is fast (up to 200mm/s,) requires just one cleaving pass per 'street,' involves no tool wear and leaves a virtually perfect side wall.

3D Micromac's semiconductor market development manager, Hans-Ulrich Zuhlke (PhD) noted that the only consumable product, '…is water. No saw blades, no particle contamination. It is clean and very quick."

3D Micromac saw the opportunity to leverage its work with the Fraunhoffer IISB as a means for speeding the development of next-generation power devices and other product types that rely upon hard and brittle substrates, including SiC. "Using a conventional saw, a diamond blade cannot cut a six inch wafer without having to be changed prior to finishing. Sawing a wafer involves significant materials cost, damage and cleanup issues; our TLS technique has none of these concerns."

Another breakthrough was announced by Reno Sub-Systems, which specializes in radio frequency matching networks, RF power generators and gas

Kulicke and Soffa showing the K&S Hybrid 3 machine

delivery for semiconductor manufacturing. Mention Reno and people in the know talk about speed. The typical RF plasma setup for atomic layer etch (ALE) and atomic layer deposition (ALD) takes one to three seconds for completing RF match and gas stabilization. Once match and stabilization are complete, it takes 30 seconds to finish the entire process. That sounds fast until you consider Reno's approach: just 50 microseconds for RF match and gas stabilization, and 10 seconds for the overall process. Reno delivers speed, repeatability, and predictability as well as more precise control thanks to the company's solid-state design. What is the market? According to Reno, there are roughly 100,000 plasma systems in service across industry, a figure calculated by multiplying the number of RF systems shipped in the past two decades: about 9,000 to 10,000 each year. Given the growing significance of these units in semiconductor manufacturing, they estimate a compound annual growth rate (CAGR) of 5-7 percent. Dramatically improving cycle time while maintaining quality and consistency is huge for these markets as device geometries shrink and the importance of ALE and ALD increases.

Kulicke and Soffa also released new products that again establish the company as a leading resource for pick and place packaging requirements. The new K&S Hybrid line includes the Hybrid 3 and Hybrid 5; both are designed to place active and passive devices at the same time in the same machine in multi-chip modules, system in a package (SIP) modules, wafer level packages and flip-chip products. The new Hybrid 3 can deliver up to 99,000 applications per hour while the Hybrid 5 can output up to 165,000 modules per hour. The K&S vice president of wedge bond, capillary and blades business, Chan Pin Chong, said the benefit for customers is the combination of speed and the fact that the robot assembly units are interchangeable. Using a Hybrid, customers can complete various pick and place operations and then rapidly shift to entirely different devices between shifts or whenever needed.

K&S and shows a device attach taking place

"It saves space on the factory floor to have one machine that can perform two major operations," remarked Chan Pin. "Another aspect that customers enjoy is that there is no impact force delivered during pick and place. Components are constantly monitored, so we deliver 'first time right pick' with very high consistency. Every operation is constantly monitored, so yield is increased even further."

Tanaka Precious Metals also debuted an innovative solution to the development of touch screen and wearable electronics with its new SuPR-NaP (Surface Photo-Reactive Nano metal Printing) technology that uses silver nanoparticles and industrial screen printing techniques to create conductive films. The new technology's ultrafine wire widths are less than one micron across. Due to the precision possible with Tanaka's printing techniques along with its silver-based nano ink, the company believes it could have applications across semiconductor and solar industries. The challenge with current conductive inks and their incorporation into LCD, LED, OLED and other advanced screen types is the need for greater transparency and uniformly thin wires. Tanaka indicated that their new ink is 'virtually invisible' compared to legacy products. Tanaka expects sample distribution at full scale early in 2017 with a production ramp later in the year.

While 2016 remains a challenging year across the global semiconductor market, process technology, materials and device manufacturers are continuing their efforts to enhance competitiveness and ensure that the supply chain supports existing market needs and the prospects of a growing IoT marketplace. As the IoT market matures, manufacturers will be ready to support a changing semiconductor ecosystem with innovative solutions to improve control and efficiency while supporting growing consumer expectations.

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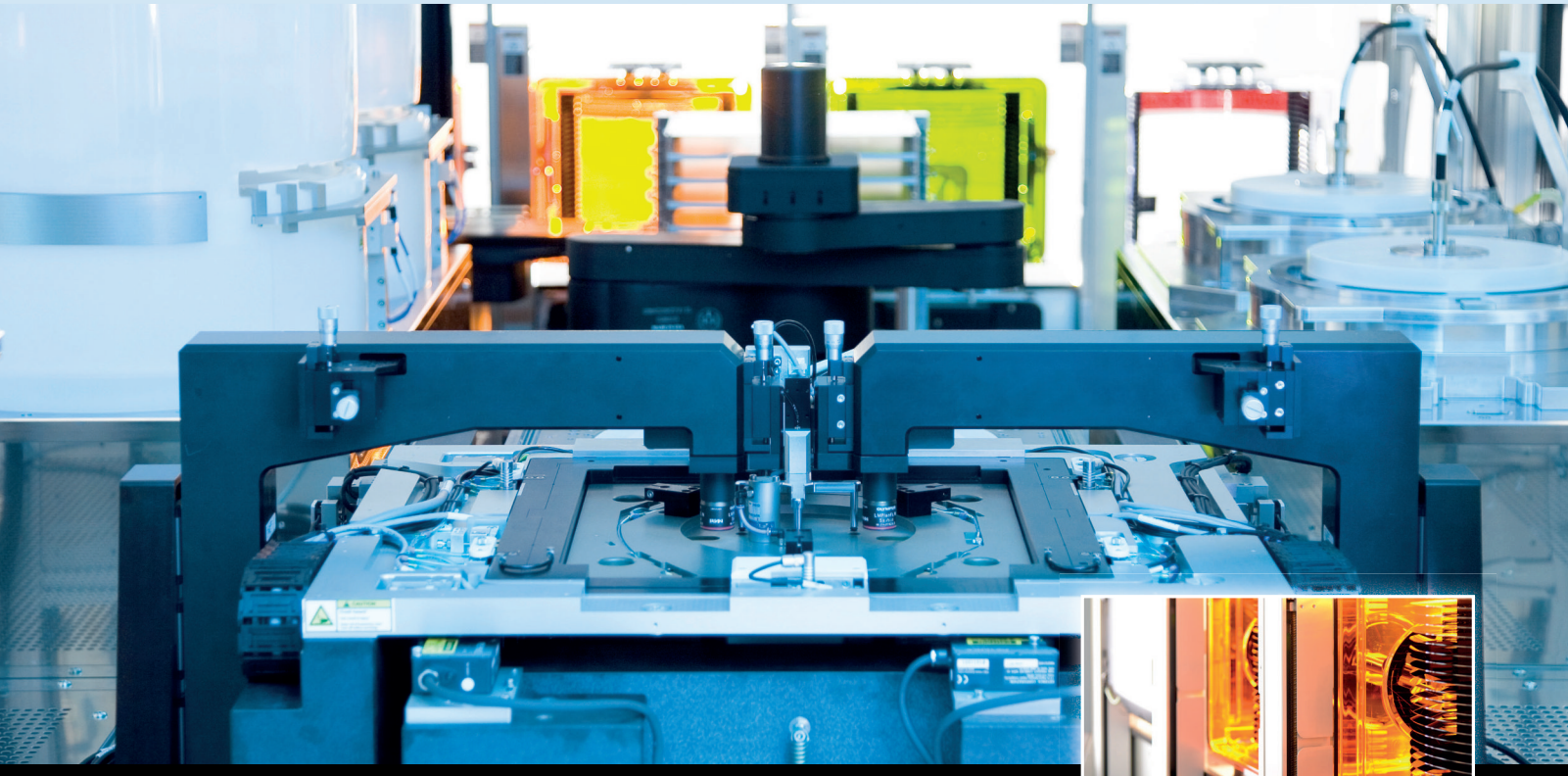

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