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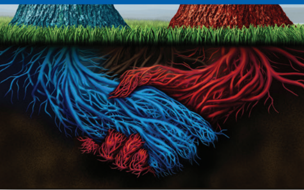
Linde: On-site generated fluorine

The year that was 2015



Imec's wearable technology

Flemish companies to merge

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An innovative plating system

for next generation packaging technologies

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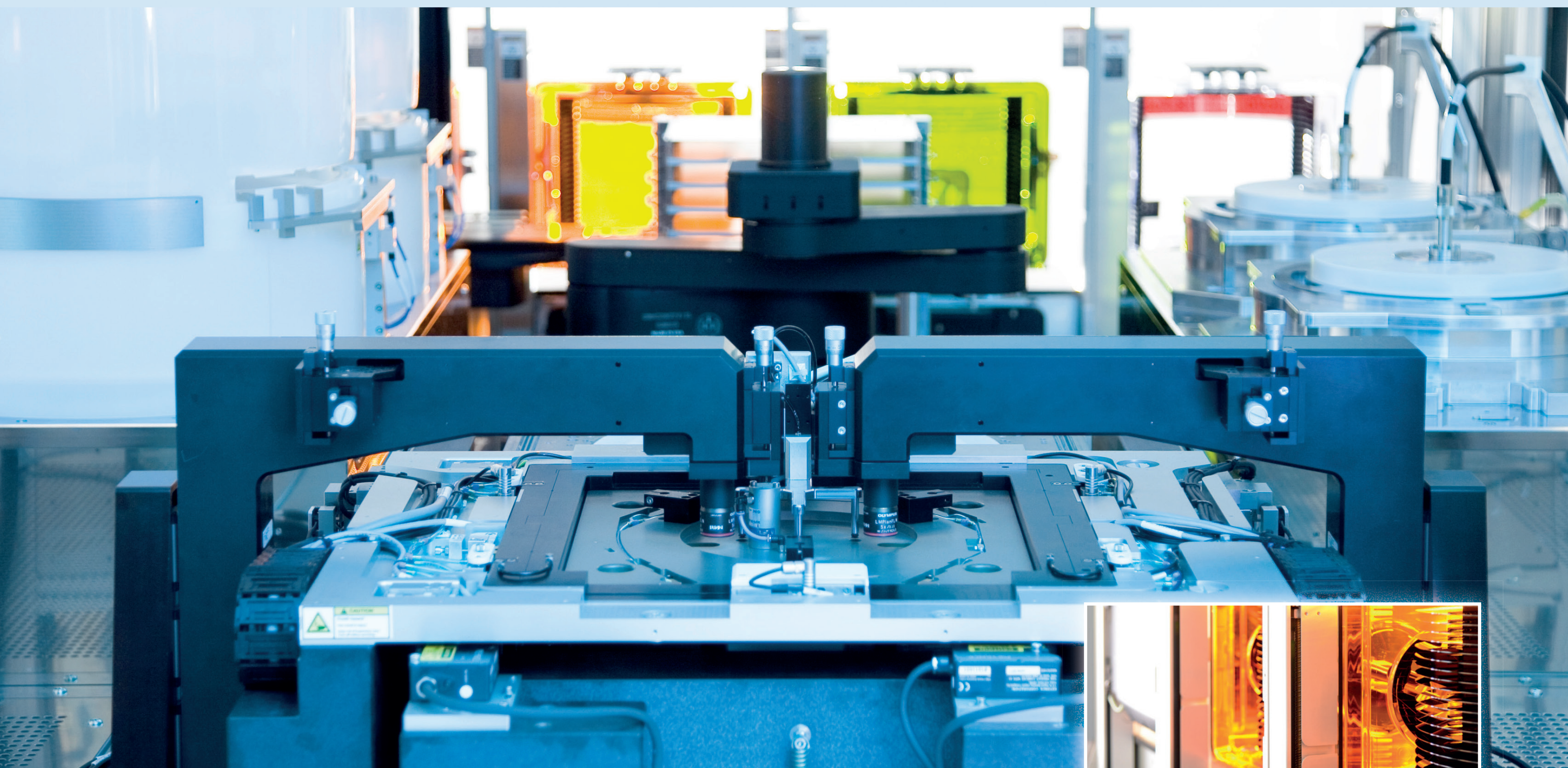

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editorialview

2016: Remaking Growth

ISN'T IT AMAZING how the present colors our past? When 2015 was still on the horizon, analysts predicted up to 11 percent growth. Optimism faded by mid-year; by 4Q forecasts were in full retreat.

Take heart: 2016 should be somewhat better. Sorry this can't sound more upbeat, but the industry is digging itself out of a hole. The positive news is that 2015's 'hole' is not deep and most 2016 broad market indicators are positive.

2016 projections by the World Semiconductor Trade Statistics (WSTS) organization will not send champagne corks popping. But a 'sparkling wine' forecast is better than bread and water rations.

The WSTS admitted that they were among the most enthusiastic forecasters who saw 2015 wrongly. But as 2015 became a fact not a forecast, the WSTS lowered its projections to 3.4 percent growth. They finished the year closer to reality than most, but admittedly were the 'least wrong' of their peers.

While questions about what drove 2015 into the red will no doubt be debated from Beijing to Brussels, the culprits were easy to identify: continued slumps in PC/laptop sectors; smartphone buyers holding onto dollars, euros and RMBs for sake of future revolutionary devices, and slower growth in emerging economies, plus turmoil in the Middle East including Syria and its impacts on the EU. This was all compounded by China cutting forecasts while massive slumps in the energy (oil) sector drove broader economic indicators lower.
In reviewing WSTS' 2015 Table of Corporate Pain, almost every major chip maker reporting data had negatives in 4Q 2015, 1Q 2016, or both. MediaTek won the Unofficial Greatest Seesaw category by falling from 8.3 percent growth in 4Q 2015 to negative 11 percent in 1Q 2016.

Where is there room for optimism? WSTS says 2016 should end with 1.4 percent growth. Not all analysts agree and IBS sees 2016 as another loser. But most believe that 2016 will finish up and I support WSTS projections. There is potential for IoT; better smartphones/mobiles are coming, VR is being productized and a host of anticipated, market-leading devices support the idea that 2017 will be better than 2015 and 2016 combined.

Hold on tight as we look to see if the amazing products and research shown at the SPIE lithography conference and GSM Mobile World Congress will impact semiconductor markets this year or next.

2016 will see modest growth. But as 2015 demonstrated, moving forward is better than sliding back.

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contents

CONNECTING THE SILICON SEMICONDUCTOR COMMUNITY

features

12 Imec advances in wearable technology

Imec researchers made advances in 2015 supporting new wearable and ultra-portable technology in IoT, radar, flexible circuits, medical and related nanoelectronic applications

20 MultiPlate: An innovative solution for next generation packaging technologies

As device geometries continue to shrink, semiconductor packaging technologies face constant challenges to remain relevant and economically viable. Need of the hour is to develop innovative approaches that cost-effectively address the emerging requirements.

26 2015: A year of merger mania in semiconductor manufacturing

2015 set records for merger activity as the China slowdown created global economic headwinds. While some markets contract, new opportunities are poised to strengthen 2016 growth

34 On-site generated fluorine: Effective, safe, and reliable source of fluorine for electronics for over 15 years

On-site fluorine generation has proven a safe alternative to greenhouse gases often used in electronics manufacturing. Linde delves into its makeup, history, and how fluorine is effectively used to clean CVD chambers and in many other applications.

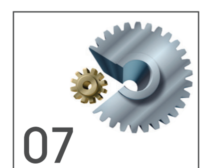
news

06 Advantech, ARM, Bosch Sensortec, Sensirion, Texas Instruments Cooperate on IoT sensor platform

07 Merger between Flemish research centres imec and iMinds

08 Nova and imec developed innovative scatterometry approach for SAQP process control

10 Samsung begins mass producing world's fastest DRAM



Advantech, ARM, Bosch Sensortec, Sensirion, Texas Instruments cooperate on IoT sensor platform

ADVANTECH, along with ARM, Bosch Sensortec, Sensirion and Texas Instruments (TI), have announced the collaboration of a new Internet of Things (IoT) sensor platform called M2.COM; to be unveiled at Embedded World 2016. The IoT era brings new opportunities to traditional industries and drives business evolution for the next-generation of products and services.

To enable a diverse range of IoT applications, and to standardize different platforms and technologies, an open platform for IoT sensors and sensor nodes was established by sensor makers and module makers for more efficient IoT development. By joining M2.COM, participants will define and drive the leading platform to empower the Internet of Things.

Miller Chang, VP of Advantech Embedded Computing Group said, "Data collection will be one of the main challenges for IoT. Sensors, wireless technology, and embedded computing will be the three major core abilities for data acquisition, and that's the reason Advantech worked closely with industrial partners to define the M2.COM open standard. With this standardization, we envision M2.COM will accelerate IoT sensor device deployment."

"A standards-based industrial computing and sensor format is key to fulfil the changing demands of the IoT market," said Zach Shelby, vice president of marketing, IoT business, ARM. "The ARM mbed OS provides the perfect foundation for this new format, supporting the needed communication protocols and formats to securely and easily integrate M2.COM based sensor devices with IoT cloud applications."

"One of the key challenges hindering a fast growth of sensor enabled devices in IoT relevant markets today is the lack of widely adopted open Platform" said Jeanne Forget, VP Marketing of Bosch Sensortec. "For Bosch Sensortec as the leader in MEMS and other sensor technologies it's therefore essential to actively participate in developing open platforms like the M2.COM. We believe that through the collaboration of these competent partners the M2.COM open platform will become a strong driver for sensors in IoT markets."

"Collecting Data and creating wonderfully smart systems and devices will only move the IoT forward if those things are able to interoperate or communicate with one another. Therefore we are proud and convinced, that we are doing the right thing by defining a standard -M2.COM to simplify the integration of sensors IoT development" says Pascal Gerner, Director Product Management of Sensirion.

"In order to accelerate the change and new business opportunities created by the IoT, it's important to have a platform that saves development time and cost with a with standardized sensor interface, like M2.COM, where developers can connect anything anywhere," said Olivier Monnier, marketing director wireless connectivity solutions/IoT, Texas Instruments. "By leveraging TI's low-power SimpleLink Wi-Fi CC3200 wireless microcontroller, M2.COM IoT developers have access to award-winning hardware that will enable them to get their design to market quickly and easily."

Advantech reinforces its vision of "Enabling an Intelligent Planet' in order to accelerate the practice of smart city and IoT solutions, and in the spirit of "Partnering for Smart City and IoT Solutions" it will continue to collaborate with worldwide partners. Through Advantech, ARM, Bosch Sensortec, Sensirion and TI's joint promotion, we believe the M2.COM will realize more IoT sensing possibilities and accelerate the practice of smart city and IoT solutions.

Toppan Printing develops next-generation EUV photomask

TOPPAN PRINTING has announced that it has developed a next-generation EUV photomask for leading-edge semiconductors.

The new photomask minimizes the unwanted reflection of light to peripheral sections during EUV exposure, a next-generation semiconductor manufacturing technology. Testing using EUV exposure machinery manufactured by ASML has verified that this new EUV photomask can reduce dimension variability on silicon substrates by two-thirds.

As a result, it enables improvements in quality and yield for semiconductor patterns. Practical application of the technology will enable further miniaturization of semiconductors and the manufacture of processors that are smaller, faster, and require less power than current models. This development marks the first time anywhere in the world that a structure to suppress the unwanted reflection of light to peripheral sections has been created on the surface of an EUV photomask, and the areas around the pattern have been miniaturized. Toppan developed the conventional EUV photomask that has become the industry standard in 2012 and has successfully developed the new next-generation mask based on further miniaturization. Through ongoing R&D activities, Toppan intends to continue contributing to the evolution of semiconductor manufacturing technology.

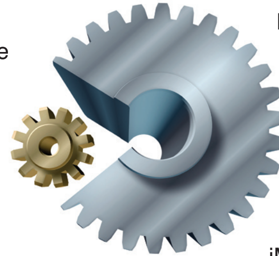
Sample shipments to semiconductor manufacturers will begin in fiscal 2016, with the start of full-scale mass production slated for fiscal 2017. Based on this technology, Toppan is aiming to establish the industry standard for next-generation EUV photomasks.

Merger between Flemish research centres imec and iMinds

THE NANOELECTRONICS RESEARCH CENTRE, imec, and digital research and incubation centre, iMinds, have announced that its respective board of directors have approved the intention to merge the research centers. As they join forces, a world-class, high-tech research center for the digital economy will be created. As a result, the new research center will fuse the technology and systems expertise of more than 2,500 imec researchers worldwide with the sophisticated digital competencies of some 1,000 iMinds researchers from over 50 nationalities. This high-tech research center will further strengthen Flanders' authority as technology epicenter and region focused on creating a sustainable digital future, whilst targeting maximum regional impact.

Imec has been a global leader in the domain of nanoelectronics for more than 30 years, and has innovated applications in smart systems for the Internet of Things, Internet of Health, and Internet of Power. It has built an extensive and worldwide partner network, as well as in Flanders, and has generated successful spin-offs. iMinds' activities span research domains such as the Internet of Things, digital privacy and security, and the conversion of raw data into knowledge. Its software expertise is widely renowned and its entrepreneurship activities in Flanders are first-rate.

"The proliferation of the Internet Everything has created a need for solutions that integrate both hardware and software. Such innovative products that optimally serve tomorrow's digital economy can only be developed through intense interaction between both worlds. There are infinite opportunities in domains such as sustainable healthcare, smart cities, smart manufacturing, smart finances, smart mobility, smart grids, or in short: smart everything. Research centers such as imec –with its widely acclaimed hardware expertise– and iMinds –an expert in software and ICT applications– are uniquely positioned to bring these concepts to life," stated Luc Van den hove, President and CEO of imec. "Furthermore, iMinds is widely recognized for its business incubation programs as well as for making its expertise easily accessible. As such, this merger provides us with a unique opportunity to jointly reach out to the Flemish industry and to further elevate Smart Flanders on the global map."



"Flanders faces the enormous challenge of realizing a successful transition towards tomorrow's digital society; a transition that must happen quickly, considering the urgency to reinforce Flanders' industrial position," commented Danny Goderis, CEO of iMinds. "The merger between imec and iMinds is Flanders' answer to this rapidly accelerating digitization trend. We have a clear ambition to pair more than 3,500 top researchers across 70 countries with an ecosystem of Flemish companies and start-ups, thereby significantly increasing our economic and societal impact. Together, we can help Flanders boost its competitiveness and claim a strong international position." The boards of directors of both organizations have approved the intention to merge. As a next step, this intention needs to be translated into a merger protocol. The merger will safeguard the unique strengths and assets of the two research centers. iMinds flagships such as the ICON research model (in which academic researchers and industry partners jointly develop solutions for specific market needs), the iStart entrepreneurship program (supporting start-up businesses) and iMinds' user research (Living Labs) will be reinforced.

Imec's authority as a global player in high-tech research will further strengthen both Flanders and the international industry. The ambition is to operate as one organization by the end of 2016. Flemish Minister of Innovation Philippe Muyters welcomes the fact that iMinds and imec join forces: "Thanks to their pioneering work in their respective fields, they have put themselves on the world map. When they were founded, the line between hardware and software was still very clear.

Today, and especially in the future, this line is increasingly blurring – with technology, systems and applications being developed in close conjunction. The merger anticipates this trend and creates a high-tech research centre for the digital economy that keeps Flanders on the world map. The gradual integration of both research centres, and the agreement to preserve their respective strengths and uniqueness, will make for a bright future."

Robust sales on commercial grade plasma cleaning system

PLASMA ETCH INC has announced robust sales for 2015 on their entry level plasma cleaner for small research facilities and universities. The company announced Monday that increasing interest in plasma has driven a strong increase in sales of the company's signature PE-25 plasma cleaning system.
The PE-25 low cost plasma cleaner is an affordable, entry level option for plasma treatment. The company hails it as a robust machine which is perfect for small production facilities, research labs and universities. This $5,900 machine was designed for plasma cleaning and surface modification. "The PE-25 is very popular with the research community, as well as universities, due to its low cost and easy to use interface…it's a great value." says company president Greg DeLarge. "Many of our PE-25 customers come back to purchase larger machines after they get their process nailed down and decide exactly what they need for production runs."
This opening price point system also includes industry leading features such as automatic plasma control and a built in control panel with a plasma timer. The PE-25 is easily upgradable to be controlled by any PC or laptop and can even include a light tower for easy to read indication of the steps of the plasma processing sequence.

Nova and imec developed innovative scatterometry approach for SAQP control

NANO-ELECTRONICS research centre Imec and Nova Measuring have announced at SPIE advanced lithography conference that they are jointly developing an innovative scatterometry approach to enable SAQP process control. The initial results will be presented during the conference.

As 193nm immersion lithography is reaching its optical resolution limit using single exposure, advanced multipatterning concepts are studied to reach lower nodes.

Targeting the N7 node, self-aligned quadruple patterning (SAQP) is an advanced patterning approach that uses pitch splitting to extend the capability of double patterning (SADP) 193nm immersion lithography. Nova and imec jointly developed an approach based on scatterometry technology to determine the main contributors to the CD (critical dimension) variation between different populations of lines and spaces. Using parallel interpretation of multiple scatterometry targets with slightly variable pitches, the researchers revealed that scatterometry is capable of measuring different space populations, and the developed metrology solutions can be utilized to monitor and control each process step of SAQP patterning.

"Collaborating with Nova has enabled us to develop a method to improve process control in SAQP for the most advanced nodes," said An Steegen, senior vice president process technology at imec. "Such collaboration is helping the entire semiconductor industry to lower risks and shorten the time to market for the next generation technologies by delivering innovative metrology solutions for the key process control challenges ahead."

"We are excited with the opportunity to collaborate with imec, join its Affiliation Program, and demonstrate the value of our optical CD for early R&D stages," said Dr. Shay Wolfling, Nova's CTO. "We believe that the growing process challenges arising from the advance technology nodes require close partnership between research centres, customers and vendors, and this is part of Nova's stated long-term strategy. Such collaboration with imec , early in the development cycle, allows us to align our technology roadmap accordingly and contribute to our customers' success."

Wika Group goes with EV Group for lithography track system

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, has announced that WIKA Group, a supplier of pressure, temperature and level measurement technology, has placed an EVG HERCULES lithography track system into production for manufacturing pressure sensor devices. The HERCULES system has already been installed and is in operation at WIKA's fabrication headquarters in Klingenberg, Germany.

The EVG HERCULES system combines spray coat, development, wafer prime and bake/chill modules with a mask alignment and exposure tool in a fully automated production platform. To meet WIKA›s unique high-product-mix manufacturing needs, EVG has implemented several new features to this highly customized system.

These include fully automated mask selection, handling and alignment capabilities, which allow users to keep the system in continuous operation while switching out substrate lots that require different geometry masks and carrier sizes for variable customer demands. This mode is also supported by optimized smart scheduling software, which automatically manages process recipes and ensures optimal process flow by pre-calculating the estimated process duration and time of transfer between process steps for each carrier substrate or lithography mask. The smart scheduling software ensures that critical process steps are carried out with repeatable, fixed durations, and can adjust to changes in material or process flow in real time. Benefits include improved process control, throughput optimization and productivity.

"Our business involves the lean production of a wide variety of specialized sensors that include many different materials and design features for customized requirements. As a result, we need manufacturing solutions that are stable, flexible and can be easily adapted to our diverse production needs," stated Dr. Lorenz A. Kehrer, Sensor Development at WIKA. "EV Group has been our supplier of choice for lithography track systems, and adding their fully automated HERCULES system to our production flow allows us to increase manufacturing capacity and yield to meet the growing demand for our high-quality products from our versatile customers. EV Group's expertise in providing world-class automated process solutions for MEMS and sensor manufacturing makes them an ideal partner to support our premium production needs."

"EV Group's integrated HERCULES system is a key component in our lithography product portfolio not only in the field of nanoimprint lithography but also for our MEMS customers applying photolithography processes," stated Hermann Waltl, executive sales and customer support director at EV Group.

"HERCULES leverages our expertise in mask alignment, resist processing, automation and software engineering to provide customers with a comprehensive future-proof lithography track solution for their volume production needs. Adoption of our lithography solutions, including HERCULES, has been driven not only by commercial applications such as advanced packaging and MEMS, but also by highly specialized applications where the customizable nature of our products coupled with our process and engineering expertise allows us to tailor our solutions to meet each of our customer's unique requirements."

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Samsung begins mass producing world's fastest DRAM

SAMSUNG ELECTRONICS CO., LTD has begun mass producing the industry's first 4-gigabyte (GB) DRAM package based on the second-generation High Bandwidth Memory (HBM2) interface, for use in high performance computing (HPC), advanced graphics and network systems, as well as enterprise servers.

Samsung's new HBM solution will offer unprecedented DRAM performance – more than seven times faster than the current DRAM performance limit, allowing faster responsiveness for high-end computing tasks including parallel computing, graphics rendering and machine learning.

"By mass producing next-generation HBM2 DRAM, we can contribute much more to the rapid adoption of next-generation HPC systems by global IT companies," said Sewon Chun, senior vice president, Memory Marketing, Samsung Electronics. "Also, in using our 3D memory technology here, we can more proactively cope with the multifaceted needs of global IT, while at the same time strengthening the foundation for future growth of the DRAM market."

The newly introduced 4 GB HBM2 DRAM, which uses Samsung's most efficient 20-nanometer process technology and advanced HBM chip design, satisfies the need for high performance, energy efficiency, reliability and small dimensions making it well suited for next-generation HPC systems and graphics cards. Following Samsung's introduction of a 128 GB 3D TSV DDR4 registered dual inline memory module (RDIMM) last October, the new HBM2 DRAM marks the latest milestone in TSV (Through Silicon Via) DRAM technology.

The 4 GB HBM2 package is created by stacking a buffer die at the bottom and four 8-gigabit (Gb) core dies on top. These are then vertically interconnected by TSV holes and microbumps. A single 8 Gb HBM2 die contains over 5,000 TSV holes, which is more than 36 times that of a 8 Gb TSV DDR4 die, offering a dramatic improvement in data transmission performance compared to typical wire-bonding based packages.

Samsung's new DRAM package features 256 GBps of bandwidth, which is double that of a HBM1 DRAM package. This is equivalent to a more than seven-fold increase over the 36 GBps bandwidth of a 4 Gb GDDR5 DRAM chip, which has the fastest data speed per pin (9 Gbps) among currently manufactured DRAM chips. Samsung's 4 GB HBM2 also enables enhanced power efficiency by doubling the bandwidth per watt over a 4Gb-GDDR5-based solution, and embeds ECC (error-correcting code) functionality to offer high reliability.

In addition, Samsung plans to produce an 8 GB HBM2 DRAM package within this year. By specifying 8GB HBM2 DRAM in graphics cards, designers will be able to enjoy a space savings of more than 95 percent, compared to using GDDR5 DRAM, offering more optimal solutions for compact devices that require high-level graphics computing capabilities.

The company will steadily increase production volume of its HBM2 DRAM over the remainder of the year to meet anticipated growth in market demand for network systems and servers. Samsung will also expand its line-up of HBM2 DRAM solutions to stay ahead in the high-performance computing market and extend its lead in premium memory production.

Tokyo Electron begin accepting orders for single-wafer metallization system

TOKYO ELECTRON LIMITED (TEL) announced at the end of 2015 that it will begin accepting orders for the Triase+TM EX-IITM TiN Plus HT single-wafer metallization system in April 2016.

Its base model, the Triase+ EX-II TiN, is a high-speed single-wafer ASFD system with an optimized reactor chamber and unique gas injection mechanism.

Since its introduction in January 2013, the Triase+ EX-II TiN has established itself as the standard for single-wafer ASFD TiN metallization systems, and has been adopted by memory and logic device manufacturers throughout the world. The Triase+ EX-II TiN Plus, an upgraded model that became available for booking in July 2015, has also been enthusiastically received in the market. The continued scaling of semiconductor technologies has required that TiN processes in advanced device manufacturing become more detailed and diverse than ever before. TiN deposition systems must now overcome new technical challenges at highly sophisticated levels.

The EX-II TiN Plus HT, which will soon be available to order, has specialized hardware for high-temperature processes and is capable of depositing TiN film of a lower resistance and lower impurity-key technical requirements for advancing semiconductor scaling. Customers already using the Triase+ EX-II TiN or the EX-II TiN Plus can upgrade to the EX-II TiN Plus HT by modifying their existing systems, thereby reducing investment costs.

"The Triase+ EX-II TiN Plus HT is the latest generation system in the series," said Takeshi Okubo, Executive Officer and General Manager, SDBU at TEL. "It is equipped to perform high-temperature processes to satisfy new technical requirements resulting from the scaling of semiconductors, while maintaining the excellent within-wafer uniformity and step coverage achieved by the preceding EX-II TiN Plus. TEL will keep tackling difficult technology development issues to deliver high value-added products for broad-ranging thin film deposition applications."

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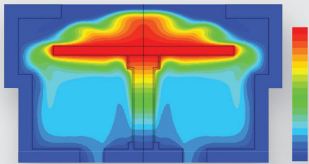

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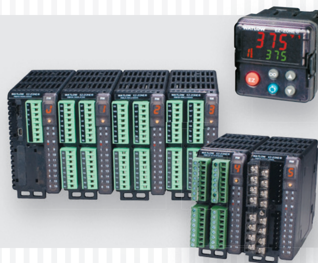

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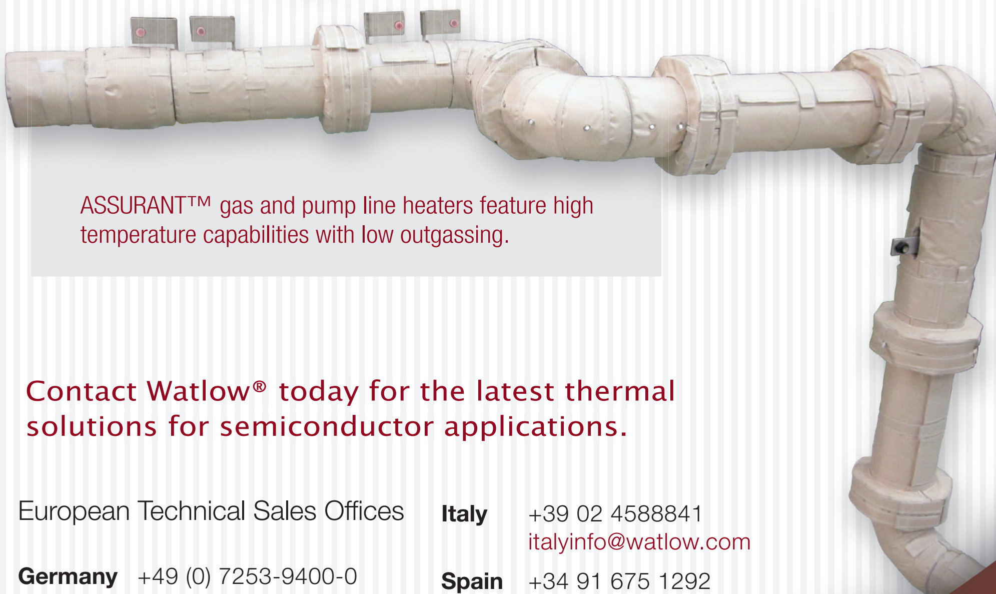

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Imec advances in **wearable technology**

Imec researchers made advances in 2015 supporting new wearable and ultra-portable technology in IoT, radar, flexible circuits, medical and related nanoelectronic applications. Silicon Semiconductor reviews their 2015 successes and where research is headed in 2016.

2015 was a busy year from imec researchers in Leuven, Belgium and throughout the international organization. Imec is renowned for its contributions to microelectronic and nanoelectronic technology that have already transformed daily living.

Results of this collaboration are recounted in the following article prepared by imec researchers (Belgium).

IMEC RESEARCHERS are showing that the ability to wear or easily carry advanced diagnostic, sensor and actuator devices will define ways that people interact with technology and how it interacts with people. While many different devices are moving from labs into the marketplace, Internet of Things (IoT) devices are rapidly evolving; their wireless connectivity will be transformative. But great devices do nothing without power, so new generations of batteries are in development. Sensor technology capable of highly reliable and secure data transmission will also be key for clinical, home and business applications.

Some new and emerging technology is not wearable in the literal sense, yet advances in chip technology that make electronic devices flexible or ultra-portable also create possibilities to radically alter the way diagnostic, safety and monitoring equipment performs. Portability and interconnectivity are key to these developments.

As wearable and highly accurate portable sensing technology emerges, will we soon have hand-held blood analyzers that deliver immediate results that once took days? Challenges exist, and not everything that can be conceived will be created, yet imec's advances in 2015 set the stage for more exciting discoveries to come.

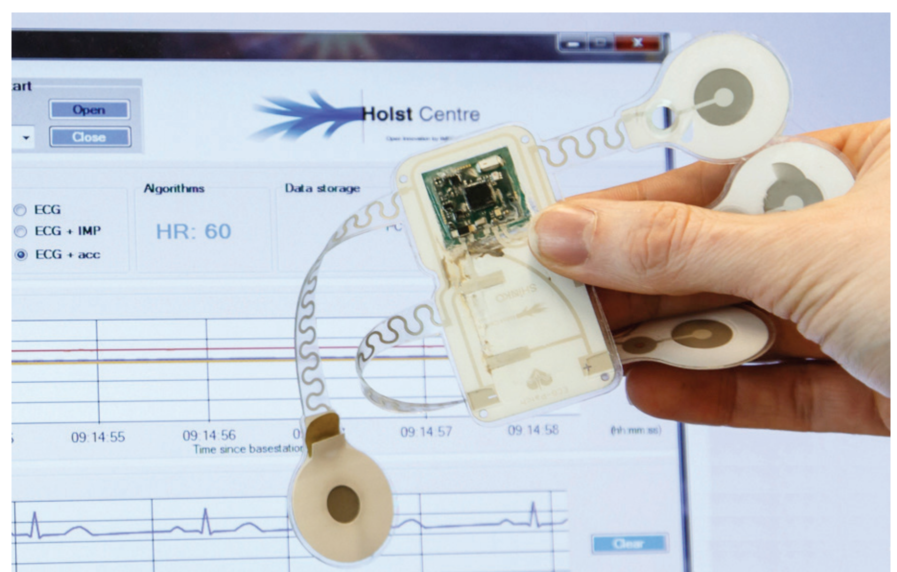
Detecting and dealing with stress using sensors is quite a challenge

By Chris Van Hoof, Program Director, Wearable Healthcare and imec Fellow

Chip technology enables us to improve existing measurement and diagnostic methods for cardiac conditions, neurological disorders and other medical treatment needs. It makes the equipment more compact, more economical and more comfortable for the patient, too. In 2015, we carried out a number of projects in this area. You need to have the right expertise, but in itself, this is not the greatest challenge in terms of medical sensor systems.

What is the greatest challenge?

Developing new methods! For example, our research group is looking at how sensor systems can make a contribution in the diagnosis and/or monitoring of heart failure, stress, sleep apnea and head trauma. Working with medical specialists, we're examining which parameters are relevant and how we can measure them accurately. The difficult



thing in all this is that the method has to be demonstrated and approved in trials with a sufficient number of patients. Which of course means that you need a robust and mature demonstrator – and that is by no means straightforward in the research phase. But it's not impossible: this year we succeeded in setting up trials for heart failure (30 patients) and stress detection (1,500 people).
In the area of sensor systems for lifestyle applications, there are all sorts of other challenges. These include genuine ease of use, the personalization of algorithms and the creation of convincing applications that help persuade us to change our behavior.

Most of the end user devices you find on the market today tend to be disappointing when it comes to accuracy. They are very good for checking whether fit people manage to do their 10,000 steps or cycle enough kilometers, but they are of no use at all for the other 90% of the population. For example, they are simply not accurate enough for measuring whether an elderly relative is getting up and moving about the house enough, or whether an overweight person is increasing his level of fitness by doing the extra exercises recommended by his doctor. Overall, current devices are not at all inspiring and don't actually anticipate your individual needs and habits.

Many of today's devices are in their infancy compared to mobile phones or other sophisticated portable technology. Truly useful devices will address peoples' actual needs, and help answer questions such as: how to use sensors to encourage older and obese people to exercise more? How can you get someone to stop smoking? How can you help a person to keep their stress levels under control?

We at imec and Holst Centre are confident that sensors can help to recognize habits and make adjustments to behavior based on the progress already being made to enable these capabilities. But it is certainly no easy task: not technologically, but also because psychologists and behavioral scientists tend not to be very familiar with modern technology. As a result, there is still some skepticism about whether or not sensors are of any value in changing people's patterns of behavior. We are currently working with some enthusiastic behaviorists from UZ Leuven and KU Leuven to investigate the usefulness of sensors for stress management.

One of the main problems with using sensors to change behavior is the personalization required for the sensors themselves. Take stress, for example, which expresses itself differently in each individual. One person may start sweating, while another gets heart palpitations – and so on. This is in stark contrast with heart rhythm measurements, for instance, where all of the signals are more or less the same. They are also well known and any discrepancies are clearly identifiable.

Personalized sensors and algorithms are needed to identify behavior correctly with any accuracy and then make adjustments. In practical terms, imec and Holst Centre took the first steps in 2015 to validate the measuring technique used for stress and to recognize people's habits and 'trigger' moments using sensors and artificial intelligence technologies. In 2016, the emphasis will be on providing feedback, for example, to reduce stress. A project will also be started to help smokers quit their bad habit with a 'virtual coach', which is what we also call our sensor approach. Because one thing is certain: if we were all to have a personal coach who kept an eye on us 24/7, we wouldn't have to make a list of New Year's resolutions any more. Or maybe we would – even if it was simply to pass them on to our virtual coach.

What if radar could recognise us from the way we walk?

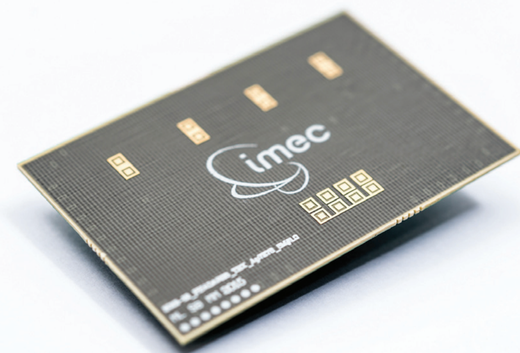
By: Wim Van Thillo, Program Director, Perceptive Systems

The future Internet of Things (IoT), with its intuitive applications, will operate based on a broad stream of data supplied by sensors placed everywhere. These will be sensors that are many times smarter and more sensitive than the ones we have today. They will also be produced and installed in far greater numbers and be much cheaper than they are now. One example of such a sensor is radar, a simplified version of which is already used in high-end automobiles to enable the vehicle to take over a number of tasks from the driver. Current radar sensors still much resemble the radars that are used to regulate aircraft flight paths and see traffic. They are mostly manufactured using specific SiGe (silicon-germanium) technology. The resulting sensors are rather large and expensive, which makes them unsuited for unobtrusive integration into applications such as self-driving cars or drones.

At imec we develop radar chips based on CMOS technology. Ultimately, our aim is to arrive at a compact radar-on-chip, a chip that offers far greater performance at a much lower power consumption than is the case at the moment – plus we want to incorporate a number of additional features and capabilities. For example, over time, we envisage a radar that is capable of distinguishing pedestrians from cyclists. That technology might even allow identifying individuals by the way they walk. Making that radar, based on what we already have developed today is our challenge for the years ahead.

Over the past three years we have been working on the building blocks for just such a radar-on-chip using 28nm CMOS technology. So far we have developed an effective 79 GHz transceiver, which in 2015 we also integrated with antennas on a micro-PCB.

The result is a fairly complete radar system measuring just a few square centimeters. The next step in our program is to make those building blocks even better, with additional

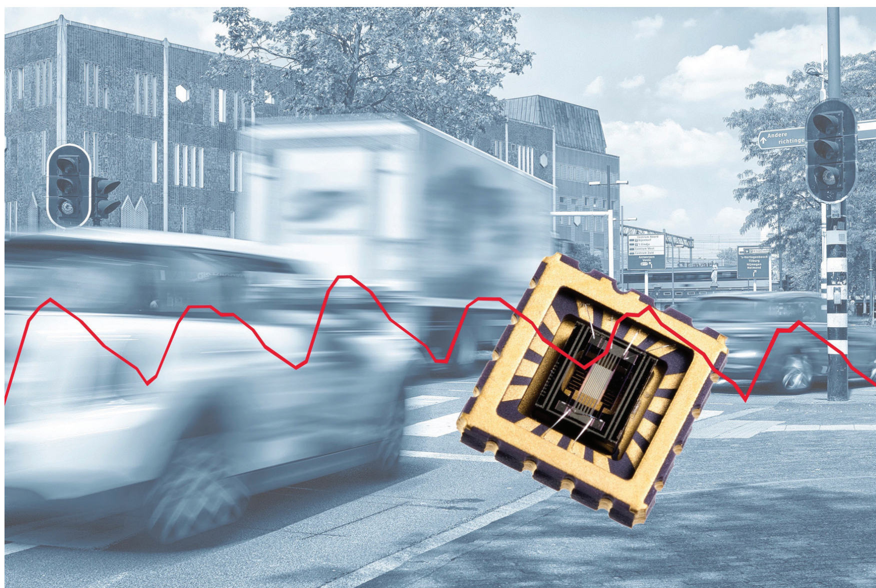


features and an even better resolution. And at a system level, we plan to develop applications that far exceed the capabilities of today's radars.
One of the ways to make our radar sensor smaller and more sensitive is to work with an even higher signal frequency. Which is why, in 2016, we will start to develop the building blocks for a 140 GHz radar. We will be using even smaller antennas integrated onto the chip itself, resulting in an enhanced Doppler resolution and a better depth resolution. In parallel, we are implementing smart signal processing for 79GHz and 140GHz systems.

The reflected signal received by our radar not only contains information about the position of the objects around the radar, but also about their movements. This "micro-Doppler" information makes it possible to distinguish pedestrians from runners, cyclists or animals. It might eventually even be used to distinguish individuals from one another. So, for instance, a car would be able to identify its driver and allow access based on the radar information.

To make this micro-Doppler information accessible, we will deploy algorithms for pattern recognition and automatic learning, algorithms that are currently used in image processing. With these our radar will learn to recognize and distinguish the micro-Doppler signature of individual objects. In a subsequent stage, we will then combine the signals of multiple radars to create a full 360-degree image of what is going on around the car. Finally, to make the picture more complete and even smarter, our aim is to combine the radar information with that of other applications such as cameras or ultrasonic sensors.

Each type of sensor has a field of application for which it supplies unique information, and image sensors are typically better at recognizing markings on the road or traffic signs. This "sensor fusion" is what we ultimately want to arrive at, with applications affecting many aspects of daily living including health, safety and quality of life issues.



Enabling IoT applications with more value

By: Harmke De Groot, Senior Director, Perceptive Systems

There is a tsunami of connected smart systems coming at us, with millions of sensors that generate data and gather information about the world around us, ourselves, our movements, the things we buy, our health and so on. But how do we ensure that these systems are truly connected, secure, and deliver applications that bring real value for their users? That is the major challenge facing everyone involved with the Internet of Things (IoT). This challenge also includes a number of technical aspects for which imec and its partners are developing appropriate solutions.

The main technical issue is that all of these systems have to be properly and seamlessly connected with one another, regardless of how much they may differ. Imagine, for example, trying to connect ultra-efficient sensors, extremely fast and broad data flows, complex industrial infrastructures and privacy-sensitive medical devices. To do so, we still have to overcome scores of interoperability and network problems for which we need to devise technical solutions.

A second important challenge is ensuring that we have tight security for all those systems, paying particular attention to privacy issues. Obviously you don't want everyone to be able to view the data generated by your sensors. But at the same time you do want to have a home in which appliances are connected and interacting intuitively with all the people who live there. But who exactly are these people? Which applications can children access? And what to do with someone who comes to stay for just one night?

Third, we will want to combine all of the knowledge provided by our sensors and systems so that we can create smart, intuitive applications. All too often at the moment, the data gathered from sensors is simply displayed on a device, after which the application waits for some kind of input from the user. In the future, the application will be able to improve itself and its environment autonomously, based on the intelligent combination of all sensor feedback.

We also need to make our applications future-proof. Every solution that is based on the raw power of number-crunching will be overtaken soon by Moore's Law. But a sensor incorporated into a building may be required to operate for thirty years. Which is why we have to come up with smart concepts, e.g. in the area of security, that are not dependent on processor speed.

In 2015 for these reasons we built a development platform for distributed

IoT applications, a platform on which applications can be tried out and simulated at an early stage. Everyone using the platform can also plug in their own sensors and transmitters, which is handy when it comes to testing concepts for networking and security, or for simulating what happens if an application is expanded to using 10,000 sensors. We are using the platform to set up partner consortiums on certain applications, such as the precise measuring of air quality.

We have begun working on R&D for security and privacy – an area that is relatively new for imec. For example, we are looking at solutions capable of using location to decide whether someone is allowed to access an application. This prevents the smart sensors and actuators in your car or home from being manipulated remotely. And in the area of secure hardware, we are examining how we can develop PUF solutions (physical unclonable functions) without making the ICs larger or more expensive. In 2015 we also continued working on highly sophisticated building blocks for communication in the future IoT. We are developing low-power sensors for specific applications, as well as a series of transmitters that cover the wide range of needs in the IoT (extremely economical, very flexible, high data rates).

“We have begun working on R&D for security and privacy – an area that is relatively new for imec. For example, we are looking at solutions capable of using location to decide whether someone is allowed to access an application”

What will be needed in five years' time

By: Paul Heremans, Technology Director, Large-Area Electronics

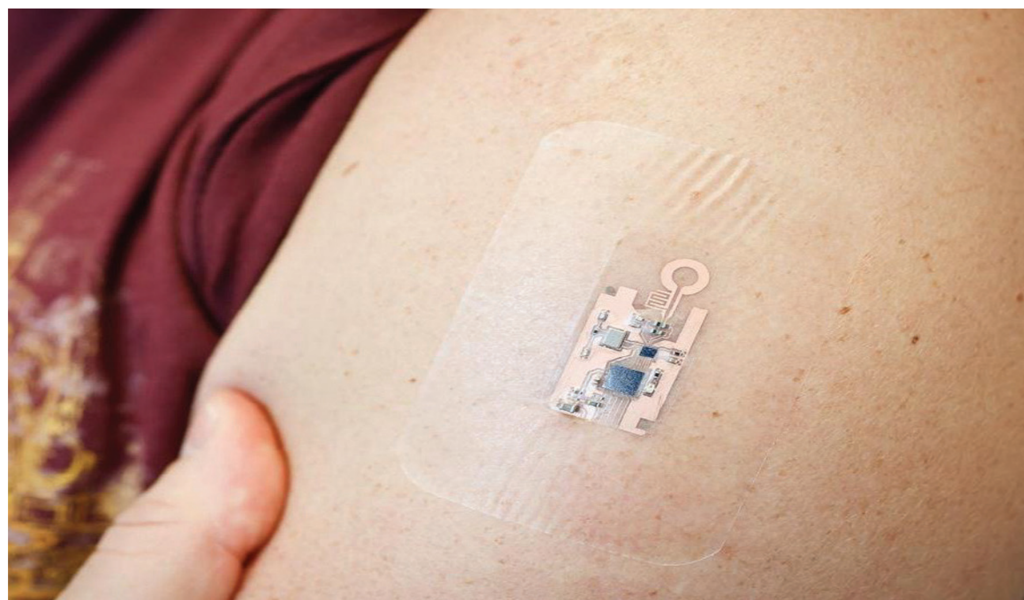
Our task as a research center is to offer our partners technical solutions for their future applications, two to three product generations ahead in time. But when it comes to flexible electronics, the industry does not follow predetermined roadmaps that we can base our research upon. Therefore, the big challenge that faces us every year is to accurately assess what our partners will need in five years' time.

One of the technologies that we are pretty sure will be a winner, is an improved 'haptic' user interface for displays. Haptic or kinesthetic communication are devices that recreates the sense of touch. While touchscreens have become standard these days, they don't give users any touch feedback; the screen simply feels the same wherever you touch it. But with haptic feedback, you can e.g. make users actually feel that they have pressed a key. One way of doing this is with a large number of ultrasonic sound sources embedded in the surface of the display – which will be a really nice application for our flexible large-area technology.

For a number of years now, we have been working on flexible chips. We have managed to produce electronic circuits and applications using the same technology developed to enable flexible displays. There is a sizable interest from the industry for these kinds of chips. But what we need to do now in 2016 is make sure that they are ready to be mass-produced, for example using the same infrastructure that is also used to manufacture displays.

Another important part of our R&D involves producing comfortable wearable electronics. We are working on applications that are incorporated into clothing, as well as on electronics worn on the skin.

In 2015 we succeeded in producing a T-shirt with a built-in LED display that is not only flexible, but that also stretches. These displays are still low-resolution, comparable to digital signage applications. But if there is sufficient demand, we will start developing a higher-resolution technology.



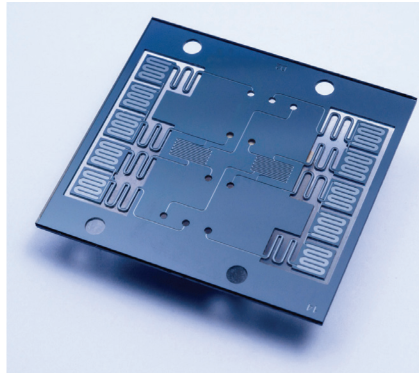
We also made progress with our comfortable health patches. The next generation will consist of a disposable patch with the electrodes that contact the skin, and a small reusable module in the form of a card that is inserted into the disposable patch and that contains a.o. the readout electronics. In 2016, we'll research how we can replace the vulnerable connectors to the readout electronics with a contactless design using our NFC (near-field communication) technology.

A large part of our efforts in 2015 was in the area of display technology. Our program on flexible display technology only started three years ago, yet we are already recognized as innovators. We have achieved this status by focusing on a number of key technologies where we really make a difference, e.g. the patterning of very small OLED pixels to produce high-resolution displays. We are also designing energy-efficient, high-quality pixel drivers, for which our partners show great interest.

One of the driving forces for innovation is the way we can mix and match technologies with the other areas in which imec excels. For example, we are developing infrared photo detectors to complement silicon image sensors. By combining these two types of image sensors, we plan to produce hyperspectral cameras with particularly broad-spectrum coverage. We are also looking into using thin-film transistors derived from our display transistors as switches in the CMOS backend.

Another fruitful example of a cross-domain development is with healthcare technology: by combining our flexible electronics with low-voltage sensors that measure health parameters, we can create some particularly useful health applications. Reversely, the CMOS engineers involved with resistive RAM, which also uses on oxides for the active layers, are looking at how to apply these in flexible oxide electronics, and perhaps even in future energy-efficient displays.

Such R&D that crosses the boundaries



of different fields will keep on growing in importance!

Chip technology enables us to make medical instruments smaller, faster and more cheaply

By: Peter Peumans, Program Director, Life Science Technologies

The Apple A9 chip used in the latest iPhones contains more than three billion transistors. That's pretty impressive on its own – but when you look at its price of around 20 euro, it becomes even more remarkable. For decades the chip industry has succeeded in offering more and more functionality at increasingly low prices. It is our aim to bring the enormous power of silicon-based chip technology to the life sciences, too.

Why would we want to do that? First and foremost to make medical instruments smaller and less expensive. In doing so, we can bring them within the reach of consumers. A good example of this is our project in which we integrate an entire medical laboratory onto a chip measuring just a few cm².

The chip will be capable of analyzing the molecules or cells contained in body fluids (DNA, proteins, viruses, blood cells, etc.) totally autonomously. This will make it possible to carry out sophisticated tests quickly in places where it was previously impossible: in the hospital ward, at a doctor's practice and even in the patient's home. As an example, DNA tests could become mainstream as a result.

A second reason for bringing chip technology to the world of the life sciences is to increase the speed or throughput of medical instruments. Imagine if you were able to read (or sequence) DNA using a chip. Then it would become possible to integrate a large number of these sequencing components onto a small area, enabling high throughput DNA sequencers.

Companies that specialize in DNA sequencing are truly convinced by the power of silicon technology. This is demonstrated by the partnerships that imec currently has with these companies (such as with Pacific Biosciences). Chip technology is also of interest

"The Apple A9 chip used in the latest iPhones contains more than three billion transistors. That's pretty impressive on its own – but when you look at its price of around 20 euro, it becomes even more remarkable"

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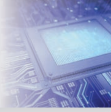

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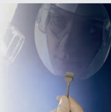

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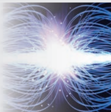

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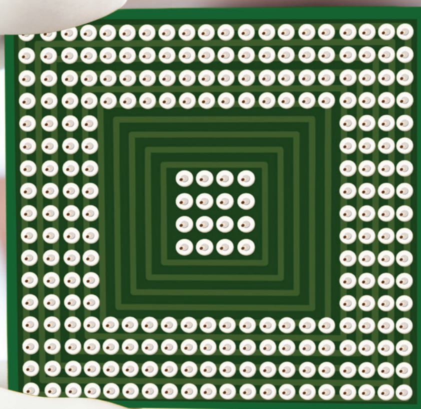

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for cytometric devices (counting and examining cells) because the devices themselves can be made smaller and more compact (and hence become mainstream), or because their throughput is enhanced. Counting and examining cells may be of value, for instance, in following-up leukemia treatment: a disposable chip that could quickly count the number of blood cells would help the doctor to tell the patient on the spot whether the treatment is working.

Another application is cell therapy in which human cells are used as medicine. One risk with this treatment is that wrongly programmed cells might be injected inadvertently, which could lead to tumor formation. Cytometric devices are needed to be able to check all of the cells to be injected before they are administered to the patient. Thanks to chip technology, this can be done faster, better – and also cost less.

Imec's lens-free microscope technology can also be extremely useful in this area, too! Up until now, we have worked mainly with 'older' chip technologies for the life science applications mentioned above.

More specifically with 0.18 and 0.13 micrometer technology on 200mm silicon wafers. In 2016, we aim to go a step further and test scaled chip technologies. At the present time, no one knows what these more advanced chip technologies might mean for medical instruments. After all, if the 'old' technologies already mean such a revolution for equipment manufacturers, doctors and patients, who knows what the newer technologies will bring.

The best electrolyte material for solid-state batteries hasn't been found yet

By: Philippe Vereecken, Principal Scientist, Electrochemical Storage

These days, we all walk round with a smartphone and laptop – which has mainly been made possible by lithium-ion batteries. At the moment, these batteries still operate with a liquid electrolyte which limits miniaturization.

The flammable liquid also poses safety risk especially for use in wearables and medical implants. But because we also intend using sensors just about everywhere in our environment soon, we need to find a worthy successor to replace it. And this is the solid-state lithium-ion battery. This new type of power unit will be more compact, as well as safer. And if you manage to combine this battery with thin film technology, it will also be possible to recharge that battery very quickly. This makes a handy solution for small batteries, which will always have a limited capacity. In a larger format, this battery would also be ideal for flexible electronics and who knows, eventually maybe even for powering electric cars. In fact, you could say that it is the holy grail of rechargeable batteries.

The main problem with solid-state batteries is that we have not yet found the ideal electrolyte. Of course, we have made plenty of progress in this direction – just look at the many scientific papers that have already been published on the topic. But the fact remains that the world of batteries is still not much further down the road than the first generation of lithium solid-state batteries of the type that are used in pacemakers, for example, which only deliver a very small amount of current.

Our research center (imec) is on a quest to find the best electrolyte material for solid-state batteries. We are currently focusing on composite electrolytes. There are two other types of electrolytes that could meet the needs, but they still have quite a few disadvantages. The first of these types, polymer electrolytes, do not have sufficient conductivity. The second, inorganic electrolytes, require a high process temperature, which results in the electrodes becoming damaged.

Last year, we succeeded in developing a composite electrolyte that not only has good conductivity ($2x10^{-4}$ S/cm), but is also compatible with the materials used for electrodes (lithium-manganese-oxide as a positive electrode and lithium-titanium-oxide as a negative electrode in our lab). This electrolyte is made mainly from silica, a material with which we have a great deal of experience in the chip industry.

Now the challenge is to combine our 3D electrodes and our silica-based composite electrolyte to produce a genuine 3D thin film solid-state battery. If everything goes to plan, we will have a first demonstration set ready in 2016. And hopefully we will then be able to demonstrate that 3D thin film solid-state batteries are more than just hype and are a real new step forward in battery technology that will enable us to produce ultra-small electronics and batteries that will recharge in no time at all!

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MultiPlate:

An innovative solution for next generation packaging technologies

As device geometries continue to shrink, semiconductor packaging technologies face constant challenges to remain relevant and economically viable. Need of the hour is to develop innovative approaches that cost-effectively address the emerging requirements.

PRESSURE on the entire supply chain is rising and the drivers are clear – enhanced performance, more functionality, and reduced costs. Investments in next generation node technologies are perhaps too substantial and precarious and thus, the industry is turning to advanced packaging to enable improved performance and functionality.

While it is still unclear which of the advanced packaging technologies offer the best performance at the lowest cost, it is imperative that companies actively engage and peruse the multiplicity of options, as opportunity costs are significant.

Therefore, the industry and companies are evaluating a range of technical solutions to meet the current demands for advanced packaging. Accordingly there are many R&D assessments being undertaken using a variety of applications: fan out/in wafer level packaging (FOWLP, FIWLP), flip chip, fan out panel level packaging (FOPLP), embedding dies, 2.5D interposer, wafer level chip sized package (WLCSP), among many others. The challenge for packaging researchers and manufacturers is to develop technologies that are leading edge, relevant for contemporaneous market trends, and profitable, all while minimizing opportunity costs.

There is certainly one thing on which all agree – there is a dire need to develop new solutions to meet the future challenges for advanced packaging. This article will explore some of the those challenges and how they can be overcame by rethinking traditional manufacturing approaches.

High speed copper pillar plating for flip chip

As the “More than Moore” approach gains momentum, advanced packaging applications are more heavily scrutinized. Once a mainstay, traditional wire bonding is being surpassed by flip chip as the preferred packaging application for sub 45nm node technologies. Since its introduction flip chip has gained considerable market share and has proven to be technically superior to traditional wire bonding which requires a larger footprint and offers limited

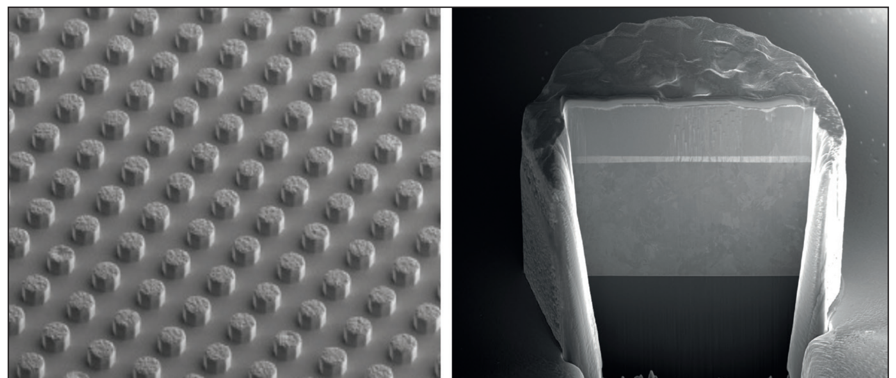


Figure 1: Example of Cu pillars with Ni barrier and Sn solder layers: (left) Top down view; (right) FIB SEM

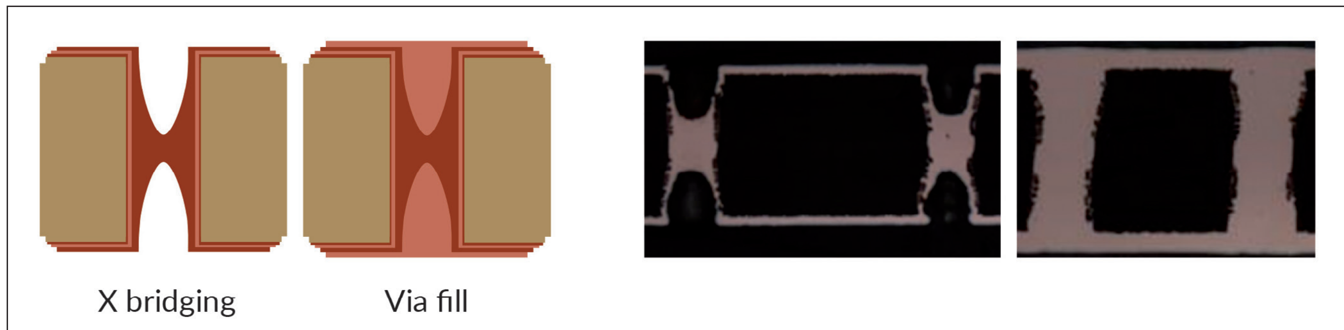


Figure 2: Atotech's patented "X bridge" through hole filling process; (left) graphic representation; (right) FIB cut of 200x100 μm through holes in panel size organic substrate

I/O density. More importantly, thermal and electrical performances are significantly improved with flip chip. Already in high volume manufacturing, flip chip currently represents roughly 16 percent of the overall packaging market (200mm equivalent). The projected flip chip growth is sizeable, with a steady increase in wafer starts over the next five years.

There are several ways to connect the flip chip to the substrate prior to packaging. The primary two methods are soldering and using Cu pillars. Soldering is utilized in flip chip BGA which uses SnAg balls to connect the chip to the substrate. The different soldering methods have a few limitations – C4 side paste printing is limited by solder paste and printing equipment, while micro ball placement has proven to be both slow and expensive.

For the most advanced technology nodes, the preferred interconnection technology in flip chip is Cu pillar. Market estimates suggest that in the coming years, Cu pillar technology has great potential and will lead the flip chip market segment in terms of growth.
Two layers of Cu pillars connect the die to the IC package – a large pillar layer on the substrate side and a small pillar on the die side, followed by an optional RDL layer to further improve the I/O count. During plating, the Cu is electrochemically deposited to form the pillar according to the process requirements for height, diameter, and shape. Typically a thin electrolytic Ni layer (up to 3μm) is deposited on top of the Cu for the purpose of inhibiting diffusion and electromigration. Finally, the pillar is capped with electrolytic Sn or SnAg.

The standard process requirements for pillar plating include exceptional void performance, nonuniformity of less than 5 percent, and high current density plating at 10+ ampere per square decimeter (ASD). Each of these parameters contributes to the overall throughput, reliability performance, and yield for the plating process. Therefore, it is essential to develop a pillar plating technology that can deposit pure Cu with high deposition speed, without impacting the voiding performance and uniformity, both of which influence the electrical performance.

Atotech's unique MultiPlate in combination with their Spherolyte process satisfies all of the performance requirements for Cu pillar applications and provides a higher throughput than standard process of record, with a system throughput capacity of 50 wafers per hour. Using reverse pulse plating, the process is optimized to the desired pillar profile and shape, thereby reducing doming or dishing, and improving the overall uniformity of the deposited Cu (< 5 percent WIP/WID/WIW). In MultiPlate, deposition is significantly faster (≥20 ASD) than traditional fountain platers (≤10 ASD) and voiding performance is enhanced. Pure Cu depositions are made by possible by use of high purity chemistries and close monitoring of the bath components during plating. All of this is achievable because of the technically superior design of the system.

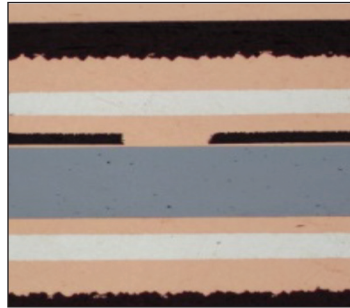
Cu through hole filling for interposer technologies

Although not currently used in standard wafer manufacturing, through hole filling (THF) is seen as a promising alternative for interposer manufacturing with large through silicon vias (TSV) as used in MEMS and image sensor applications. MultiPlate's THF technology allows for direct plating through substrates using the patented "X bridge" filling process, during which the deposited Cu forms an "X" at the center of the through hole, subsequently creating two vias that are then simultaneous filled using double side plating. This through hole filling process has been proven on glass, and Atotech also offers feasibility on wafer upon request. The primary advantage of the through hole filling process is the reduction of up to 30 percent of the process steps.

Double side plating for embedding components

For assembly technologies, embedding dies has been identified as a good solution for enhancing performance and reducing manufacturing costs. Embedding dies refers to the integration of components (passive components and integrated circuits) within the layers of a die package. Market research on embedded active and passive dies demonstrates that this technology will witness wide acceptance in the coming years, particularly for mobile

applications. Substrates with embedded dies offer smallest form factor and footprint, as the die package is significantly denser and therefore takes up less space on the PCB or IC substrate. Moreover, the process sequence, and in particular the number of plating steps, is shortened when dies are embedded and electroplated on both sides.



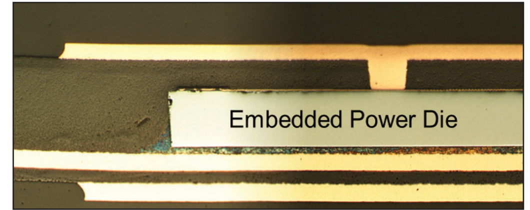


Figure 3: (left, right) Double side plated embedded power die; source: Fraunhofer IZM in collaboration with EmPower program

There are a number of other benefits of embedding dies, including higher levels of integration and improved thermal and electrical performance. Embedding dies facilitates a shorter electrical path, which results in a faster signal and overall electrical performance for the entire package. Embedding dies also presents the opportunity for increased levels of integration and the ability to house multiple dies, of various functionalities, in a single package.

Typically, during the embedding process, RDLs and backside metallization are done by sputtering and plating each side of the wafer or panel individually. This is a costly and equipment intensive exercise that can also slow down the production flow. MultiPlate's double side plating capability enables simultaneously plating of vastly different structures on each wafer or panel side, such as large pads for the back side metallization and fine lines of the RDL structures. This double side plating technique is successfully proven and well recognized for embedding power dies as part of the EmPower program.

Advanced Cu deposition will continue to be a mainstay in advanced packaging, but not without some limitations. A primary concern regarding Cu deposition is the fact that as the substrate thickness decreases and thicker Cu RDL layers are required (in FOWLP, for example), warpage is a critical processing challenge. Double side plating is able to overcome the warpage which is typical in high end processing with stress compensation achieved by simultaneous Cu depositions.

The advantage here is significant, as warpage has a major impact on yield. Yield is also a challenge for panel-based manufacturing of embedded components. Notwithstanding, high volume manufacturers have already adopted embedded technologies for low I/O dies on panel-level. This will be discussed further in the next section.

RDL plating for fan out wafer/ panel level packaging

One example of embedding dies is fan out wafer/panel level packaging in which the die is placed on a wafer carrier and the package is built up around it. Fan out has been around for years and is a leading prospective trend for packaging manufacturing. More players are expected to increase capacity in the coming years for both ≥300mm

ATOTECH MULTIPLATE ATOTECH

THF DSP RDL Pillar

Compatible with:

- 150, 200, and 300mm wafers
- Various panel sizes up to 510x510mm
- Large variety of substrates
- Various electrolytes
- Thin Taiko wafers

Designed for:

- Single and double side plating
- Through hole filling
- Higher speed pillar plating

Figure 4: Tool process capabilities of the manual system offered by Atotech's MultiPlate. THF: Through Hole Filling, *DSP: Double Side Plating, RDL: Redistribution Layer, and Pillar

*Double side plating refers to the simultaneous plating of both substrate sides

wafer and panel applications. Fan out is a preferred packaging approach as it is designed to considerably increase I/O density with a reduced footprint and profile, partly due to the fact that it's thinner than flip chip, as it does not require a package substrate. In fan out processing, the redistribution layers are plated partially on the die and the molding resin. Using a metal or glass wafer carrier which is removed after plating, the RDLs and second layer interconnect (SLI) pads are left open to connect with solder balls to the PCB.

Warpage is a critical processing challenge in fan out due to the use of molding resins, thinner substrates, and thicker Cu depositions. Yet another challenge is posed by the lack of infrastructure. Both the equipment and complete fabs are unable to handle the large wafer and panel sizes, while continuing to provide desired yield.

Fan out processing may soon be done on panel level, as the price per piece significantly decreases from larger wafer sizes to panel. However, standard panel tools are not designed for processing wafers and tend to have a significantly lower yield than their wafer counterparts. This is partly due to the design of panel tools and the fact that they have not been engineered to satisfy the highest ISO standards.

MultiPlate is designed to satisfy the stringent requirements for next generation advanced packaging applications, both on wafer and panel level, and can also be customized according to the customers' production requirements. With its double side plating capability, it also effectively addresses the warpage issues.

MultiPlate: designed for performance

As manufacturing costs and yield become progressively critical for all members of the supply chain, performance of each process is of utmost importance. For high end ECD processes in packaging applications, yield, throughput, and reliability performance are optimized when the process, chemistry, on-line analytics, and plating equipment are in synchronization.

The primary requirements for high end, next generation ECD processes in packaging applications, as previously noted, include high purity deposits, nonuniformity of less than 5 percent, good voiding performance, and higher current density plating compared to what is currently available in the market.

The main processing challenges already discussed – the migration from wafer to panel, the issue of warpage when processing thin substrates, time sensitive production, yield, and most importantly – being able to quickly adapt for next generation technologies – can be overcome with MultiPlate.

MultiPlate is a next generation plating tool which offers the versatility and multi-functionality necessary to address the current and future challenges for optimal performance in advanced packaging technologies. It is an innovative electrochemical deposition plating system designed for flexible R&D and superior performance of high end application-specific production, and can be customized for through hole filling and both single and double side plating on RDLs and pillar structures which are required processes for many packaging applications such as flip chip, embedded power components including fan out, among many others.

MultiPlate's superior design includes the following features:

- **Dimensionally stable inert anodes for Cu plating:** An optimized uniformity within wafer/panel is enabled by an adjustable current distribution over the entire surface. This is possible due to the implementation of a segmented inert anode - two segments for 150 or 200mm and three segments for 300mm or panel.

- **Advanced fluid system:** Optimum electrolyte flow distribution is achieved with the advanced fluid system (AFS). The short distance from the cathode (wafer/panel) to the segmented anode provides a direct flow and superior agitation. Both of these are needed for high speed plating (current densities ≥20 ASD) and superior thickness uniformity.

- **Cu dissolving unit:** Voiding performance and uniformity are optimized by maintaining a bath with minimal impurity incorporation. By monitoring and replenishing the Cu concentration with an external unit while plating, there is no need to interrupt the production. Using intelligent software, algorithms, limits and frequencies of the measurements are specified in order to maintain an optimal plating result.

- **Free programmable mechanical agitation:** Overall uniformity is improved with the use of a freely programmable mechanical agitation mechanism. This mechanism allows for the movement of the wafer holder – down to just 35mm from anode to cathode – which eliminates the risk of spray and flow pattern, thereby improving uniformity.

Figure 5: Images of a manual MultiPlate system; (left) front view; (middle) plating baths; (right) chemical distribution units

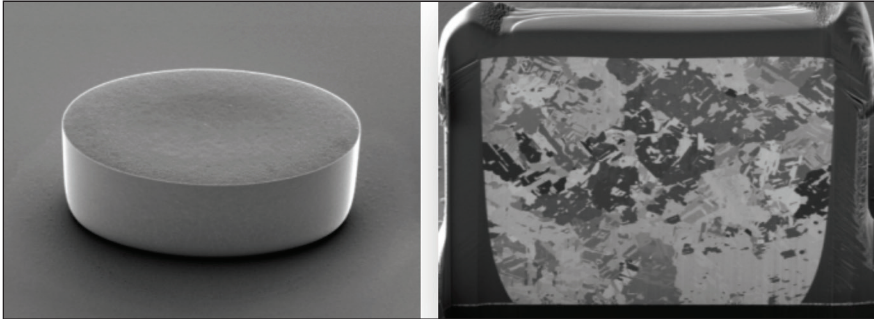


Figure 6: (left) Example of a 20 μm Cu pillar plated at 3.8 μm per minute; (right) FIB cut through the pillar

- **Multipurpose rectifier:** Reverse pulse plating is essential for high speed pillar plating to achieve an ideal profile (no doming or dishing), and to obtain Atotech's patented "X bridge" technology in through hole filling. The "X bridge" is achieved by double side plating the wafer/panel to form two blind vias on each wafer/panel side. Next the vias are filled using a standard electrolytic plating process. For double side plating processes, the current parameters can be independently adjusted for each wafer or panel side to support different design layouts and plated thickness requirements.

- **Substrate holder:** For dry contacting of 150, 200, or 300mm wafers and panels, substrate holders for both single and double side plating are available and are capable of handling thin Taiko wafers as well as glass.

- **Fast wafer handling:** The automated load/unload station is designed for high throughput – approximately 50 wafers per hour – with the final rinse and dry station after unloading.

- **Easy maintenance:** MultiPlate was designed for ease of use, employing intuitive human interface, and complying with the latest ISO and clean room standards. A completely encapsulated line and modular approach means that maintenance is streamlined with quick access to subunits.

Designed to deliver exceptional results

MultiPlate effectively complements Atotech's proven Spherolyte process to deliver unmatched ECD processes which enable an improved, cost effective manufacturing flow and better performance.

High speed copper pillar plating

- High speed pillar plating (≥20 ASD or 4 μm/min)
- Excellent uniformity (<5 percent WIW, WID, WIP)
- High purity Cu deposit
- Homogeneous Cu grain structure
- Superior voiding performance eliminates the need for Ni diffusion barrier on Cu pillar

Through hole filling capability

- Reduced process steps (≥30 percent) which means higher throughput
- Pulse reverse option allows filling of through holes

Double side plating for next generation assembly technologies

- Warpage compensation by simultaneously plating on both wafer or panel sides
- Reduced process steps (≥30 percent), eliminating manufacturing complexity
- Excellent uniformity (≤10 percent WIW)
- High purity Cu deposit
- Homogenous Cu grain structure

Planned market entry

Currently installed at the Berlin Technical Center, Atotech's MultiPlate system is fully operational and ready for additional wafer scale feasibility studies and POR determination on 150, 200, and 300mm wafers. The first automatic wafer system will be shipped in April 2016, while the first semi-automatic panel system will be delivered in July 2016.

Next generation packaging technologies

With the addition of MultiPlate, Atotech now holds the unique position of offering customers a one-stop-shop when it comes to electroplating, providing high purity chemistry, plating equipment, and process development for ECD packaging

Substrate and Dimensions	Process Results
Organic substrate Panel 200 µm by 100 µm through holes 2 : 1 aspect ratio (AR) 60 min process time	
Organic substrate 200 mm wafer 275 µm by 115 µm through holes 2.4 : 1 AR 80 min process time	
Glass substrate 200 mm wafer 290 µm by 80 µm through holes 3.6 : 1 AR 95 min process time	

Figure 7: Various images of through hole filling with corresponding filling times, dimensions, and aspect ratios

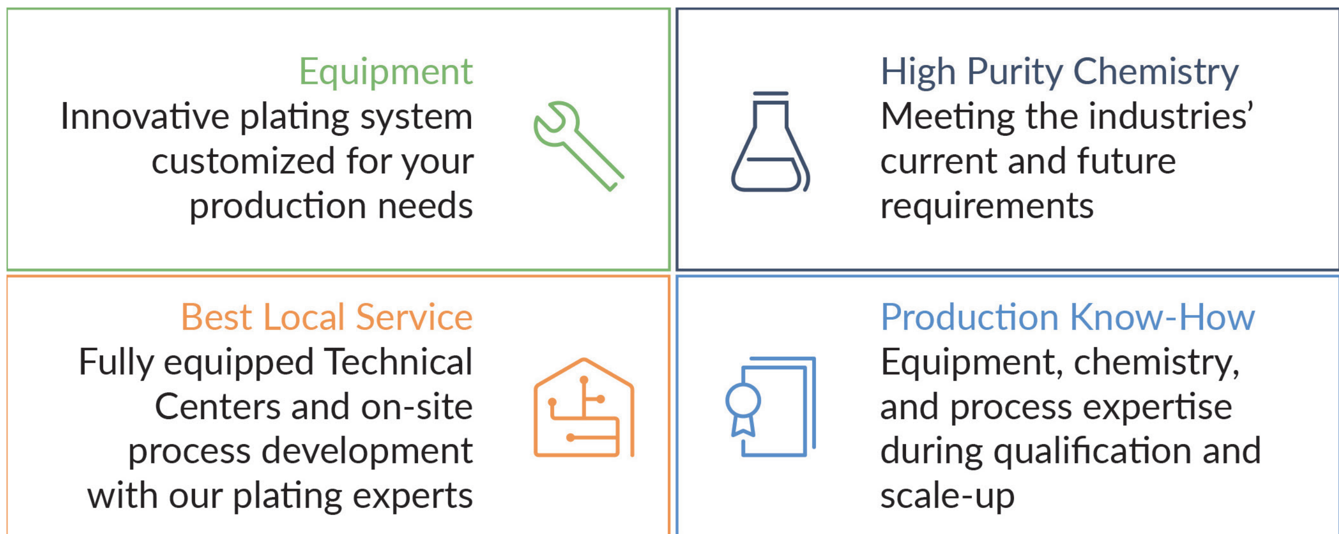


Figure 8: The four pillars of Atotech's semiconductor business strategy

applications. The company's journey began with the transfer of know-how from their industry leading plating processes and equipment for single and double side plating on printed circuit boards, to the optimization of these technologies for semiconductor packaging applications at their Berlin Technical Center.

Atotech has provided the electronics industry with leading technology solutions – including highly specialized chemistries and plating equipment – for over a century. Their in depth plating know-how is built on a comprehensive legacy of M&T Chemicals and Schering Galvonotechnik. Over the years, Atotech has remained committed to developing technologies which are measurably superior, ecological, and competitively priced. Staying ahead of the competition and being able to address the industry's demands for next generation technologies has always been the foundation of Atotech's global strategy. Thus, the migration to the semiconductor equipment market was only a natural and essential undertaking. Atotech's semiconductor capabilities have steadily grown since its inception in 2006. The success of its semiconductor division is reflected in their consistently expanding global network and client base.

The company's strength lies not only in their comprehensive know-how and leading technology solutions, but also in their highly trained team of experts and an ability to stay close to the customer.

Their Technical Center and Systems approach – with regional Technical Centers equipped with plating manufacturing equipment and managed by technology experts – enables them to support customers at all key locations globally.

Their decision to expand focus to include advanced packaging equipment was made primarily with the intent to offer customers a one-stop-shop, and to explore unchartered territories in semiconductor manufacturing: double side plating on wafer and panel, plating on glass and organic substrates, and high speed pillar plating using the well-known reverse pulse system.

With MultiPlate, Atotech has yet again raised the bar in providing pioneering solutions to tackle key challenges facing the industry today. It is decidedly superior to conventional plating tools available for standard RDL or pillar plating on the market, and offers key features and capabilities for overcoming the obstacles that next generation technologies will present.

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"Over the years, Atotech has remained committed to developing technologies which are measurably superior, ecological, and competitively priced. Staying ahead of the competition and being able to address the industry's demands for next generation technologies has always been the foundation of Atotech's global strategy"

2015

A year of merger mania in semiconductor manufacturing

2015 set records for merger activity as the China slowdown created global economic headwinds. While some markets contract, new opportunities are poised to strengthen 2016 growth.

2015 WAS A RECORD-SETTING YEAR across the semiconductor industry. Merger mania hit new highs, with 18 deals of $100 million or more making headlines. Mergers closing by October 31st were valued at $110 billion. Yet some major deals did not happen, as was the case with the Tokyo Electron/Applied Materials match-up. Meanwhile, the acquisition of KLA-Tencor by Lam Research Corporation announced in fourth quarter moves forward with the approval of most industry watchers even though regulators have not officially weighed-in.

Contributor Mark Andrews saw that some of the biggest headlines came from China, where the country's long-standing expansionist business climate ran into substancial headwinds that shook financial markets this past summer. World markets largely recovered thanks to infusions of capital by the Chinese central bank and the resilience of the United States' economy. Despite China's negative pull, Asia is still on-track to be the world's major producer of semiconductors by 2020.

While technological advances continue to drive product innovation, headlines in 2015 often spoke of incremental advances for many applications. That having been said, new ground was broken in memory, photonics, 5G, IoT and progress towards 450mm technologies.

As 2015 draws to a close, industry analysts remain optimistic that growth—perhaps at a slower pace—will continue in the New Year thanks to the ever-inventive minds of the world's best manufacturers, suppliers, researchers and entrepreneurs.

2015 Year in Review

January

Researchers at IC Insights got off to a busy start, forecasting seven percent growth in semiconductor manufacturing. This prediction was within the range of SEMI's forecasts as well.

While several researchers foresaw a China slowdown, none were looking for the fall-off that markets would experience by the summer.

Taiwan Semiconductor Manufacturing Company (TSMC) announced record quarterly 2014 profits, but also signalled that a slowdown might be coming. As if they heard the forecast in Taiwan and wanted to exert their own influence, leaders in Beijing signalled that China intended to fund semiconductor expansion to the tune of $10 billion (USD.) Meanwhile a new report from IC Insights listed the top 50 foundries of 2015; nine were in China. At the Consumer Electronics Show in Las Vegas (USA), Intel announced a new chip family that included 14 new designs targeting PC and notebook applications. Intel also showcased what it claimed to be the smallest wearable system on a chip (SoC) device that was clearly targeting the wearables market.

February

A week into leading the SEMI trade group, John Neuffer helped celebrate record setting revenues in 2014 of nearly $338 billion, up 9.9 percent over 2013. China was first on his list of stops as the world's number-two economy sought expanded roles in high-tech manufacturing, placing more emphasis on key capabilities that have up to this point typically been located elsewhere across the globe.

As China topped many analysts' must-watch lists, America's Silicon Valley again made news, this time for its continued expansion. Perhaps seeing ahead to the rocky road we'd find by mid-2015, Silicon Valley executives reported continuing expansion of the type not experienced since the 'bubble' days of the dotcom boom that burst in 2001, but of a type that they believed was more sustainable compared to the breakneck pace set before 2000-2001. February saw TSMC announcing a $16 billion investment in its plants. Spoiler Alert: That ambitious plan would be trimmed later in 2015, with capital investment falling from $10.5 to $8 billion, reflecting the reality of a shrinking market.

Even though February saw shouting matches over whose semiconductor fabs might grow the fastest, Internet of Things (IoT) technology grabbed headlines as well. Security experts at ARM outlined what they saw as the road ahead for realizing the technology's potential, putting cash into the gambit by acquiring Offspark, a company specializing in Transport Layer Security (TLS), technology that was already used widely across commerce and communications infrastructure. Elsewhere in the IoT universe, experts meeting at the Boston Embedded Systems Conference said that the competing platforms for realizing IoT secure connectivity were still sorting themselves out and would be for years to come, which could affect how quickly IoT devices are brought to market.

March

Merger mania continued in a big way on March 1st with the announcement by NXP and Freescale that they planned to combine resources, creating a $10 billion revenue machine. If finalized the merger would create the world's 9th largest chip maker, and dominate the market for automotive and general purpose microcontroller semiconductors. NXP and Freescale valued the deal at $40 billion.

As if to put an exclamation point on the issue of global fab hot spots, analyst at IC Insights said that Asia would have nearly 70 percent of all fabs by 2019, with the bulk (40 percent,) located in Taiwan and South Korea. China made the list with a forecast of 10.9 percent of global fabs by 2019.

In a move that surprised no one except those with their heads in the sand, exhibitors at Wearable TechCon noted that smart glasses from Epson, Google and Sony were resetting expectations and were turning their attentions to business applications. The appeal of Google Glass and similar products in work environments that challenge staff to maintain constant contact across multiple applications as well as 'interface' with their human counterparts seems intuitive. One has to wonder why the developers didn't seek those markets at the same time they were promoting smart glasses to mainstream consumers.

Technology news came on several fronts, with researchers at North-eastern University announcing that they had uncovered basic principles that should enable the development of quantum Wigner crystals, predicted as theoretically possible in 1934. The breakthroughs could enable ultra-high-electron mobility several orders of magnitude superior to either silicon or graphene. On the optical front the University of Washington in Seattle and California's Stanford University announced development of nano-scale lasers that could be ideal for transmitting data optically around semiconductor chips.

March ended with analysts 'cooling' to the idea of an Intel/Altera combination. Although speculation about Intel acquiring an FPGA leader has persisted for years, that market is tiny compared to Intel's primary computing markets. Analysts wondered why the chip maker would spend $13 billion for a company with perhaps $2 billion in annual revenues.

April

IoT again made headlines as EuroCPS pledged to fund as many as 30 teams across Europe with up to $25 million to underwrite a three-year initiative in fundamental and practical research. The goal was to enable greater capabilities and market growth for all things wearable tied to Internet of Things applications. The initiative particularly targets smaller research groups that often are challenged when competing against major global enterprises with deep R&D pockets.

At midpoint, engineers commemorated the entry of Gordon Moore's 'simple' assertion that transistors could double in capacity within the same area of a silicon chip every two years. While the ramifications of this idea are still being argued the impact of Moore's Law is undeniable. The successful pursuit of greater computing capacity led to not just faster and cheaper computers, but also myriad applications from communications and the Internet to smartphones, tablets and now the dawn of IoT.

April saw announcements from the Internet Engineering Task Force (IETF) about new, faster chips and the software to drive them, all tied to software-defined networking (SDN). Meanwhile, the Optical Internetworking Forum (OIF) is leading initiatives to create bonded Ethernet channels. The ultimate goal of both groups is to create 400 Gb/s channels bonded to create pipes as 'fat' as 1.6 Tb/s.

Analysts also went out on a limb to predict Intel's process technology of choice for its next two generations, driving toward 10nm devices. Analyst David Kanter (based on the contents of papers released by the company and other assorted data,) predicted Intel would rely on quantum well FETs using two new materials—indium gallium arsenide (InGaAs) for n-type transistors and strained germanium for p-type devices. Only time will tell, but if he is correct Intel could leap frog competitors one more time.

Closing out a busy April was Apple's achievement of yet another sales record: $58 billion in the second quarter compared to the same time in 2014. Although Apple declined at the time to make forecasts on its then-anticipated Watch segment, iPhone and Mac sales dropped. Nevertheless the world's largest electronics company reported a $13.6 billion profit. Not bad for a 'cooling' market.

May

We all know how frustrating it can be to find the right component for a new design, and engineer Javier Solorzano responded by co-founding a new company called Elektet that he believes will aid designers, and manufacturers searching for just the right component. This isn't your basic parametric search engine like many chip vendors have built into their websites. His approach is a 'Google-like' system that could work across the web to help engineers locate parts despite widely varying product IDs and descriptions across the industry.

It was no surprise to discover the industry heavy weights Qualcomm and Broadcom again found something to dispute, this time in how the LTE-Unlicensed (LTE-U) spectrum is being utilized alongside Licensed Assisted Access. The US Federal Communications Commission is interested in whether the two companies are sharing spectrum and not

looking into ways that incumbent Wi-Fi technologies might be infringed upon. The inquiry could potentially pit cellular network providers against the 'cable guys' as well as users of unlicensed spectrum. Stay tuned….

Infineon made additional headlines by announcing that the Munich, Germany based company was looking for a buyer to take over its Newport (Wales) wafer fab that came to the company as part of its acquisition of International Rectifier. Although seen as an eventual blow to the local economy, Infineon stated it expected work to continue in Newport through the end of 2017, indicating that demand is sufficient for a potentially protracted sales process.

News from the wearables market included opinions from the Embedded Systems Conference in California that indicated relatively modest sales figures could be tied to the fact that while devices such as Apple Watch have many capabilities, they haven't achieved the kind of data throughput that medical practitioners would need to use the devices for patient diagnoses or monitoring. One problem lies in the sensor design, which is fine for other systems today but lacks the contextual data that a doctor or other practitioner would need.

Samsung made headlines by announcing it would ramp production of its 10nm devices starting in 2016. The new node is expected to be in full production by the end of next year. International Business Strategies CEO Handel Jones said that if Samsung can achieve 10nm at production volumes, the impact could be very disruptive in the market.

June

The month began with good news for Taiwan Semiconductor Manufacturing Company (TSMC) when MediaTek announced that it would continue using the company as its leading-edge chip foundry. This announcement laid to rest fears that MediaTek might be shifting its business to TSMC rival Samsung.

Defending his company's decision to buy Altera, Intel CEO Brian Krzanich said the combined companies would ship integrated products starting in late 2016 for servers and some still-undetermined embedded systems. His message was met with some scepticism by Linley Gwennap, a principal analyst at The Linley Group and a veteran Intel analyst. Krzanich estimated new business could be "…be quite a bit bigger than a billion dollars…"

'Sanity' became the watchword at an early June conference attended by Internet of Things (IoT) experts who labelled projections of up to 50 billion IoT devices by 2020 as 'Fantasy.' A more realistic projection is 1.9 billion IoT devices shipping by 2020, according to Linley Gwennap who said he took a bottoms-up look at real world stats, such as the global middle class population (about 2 billion by 2020) and the number of homes expected to have Wi-Fi or other broadband connections (around 600 million.)

Analysts at the Computex Taipei event looking for ways to realize maximum penetration for wearable IoT devices stated that 72 million wearable devices worth $17 million will ship this year, pointing to a compound annual growth rate (CAGR) of 18 percent. They projected up to 156 million units worth $39 billion by 2019. Bruce James, director of mobile solutions for ARM, with chip designs in 90 percent of with world's smartphones, is betting on watch and watch-like wearables as emerging leaders.

By mid-month, reports were surfacing noting that demand for semiconductors was weakening in the second quarter with some assemblers in Asia suggesting double-digit fall offs compared to second quarter in 2014. The iPhone supply chain and automotive markets remained a bright spots in 2015 forecasts.

While current semiconductor shipments were falling compared to 2014, China's top foundry, Semiconductor Manufacturing International Corporation (SMIC), forged a joint venture with Huawei, Qualcomm and the imec research institute to develop its own technology for 14nm process production at a SMIC fab by 2020. Beijing had earlier committed to spending $10 billion for domestic semiconductor production, which could include the 14nm development project analysts said.

July

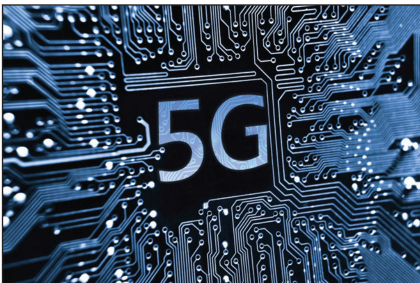
IBM and GlobalFoundries got the month off to a busy start, announcing that they had closed the deal transferring IBM's Burlington, Vermont (USA) foundry to GF. The deal was worth $1.5 billion and as a condition IBM agreed to make

"'Sanity' became the watchword at an early June conference attended by Internet of Things (IoT) experts who labelled projections of up to 50 billion IoT devices by 2020 as 'Fantasy.'"

GlobalFoundries its supplier for the next 10 years while Global also obtained ownership of 10,000 IBM semiconductor patents.

5G took another step towards becoming the next cellular communications standard when it was announced that demonstration projects, trials and specifications work would begin within months of the July announcement. 5G is expected to deliver a number of benefits compared to 4G technologies, including maximum data rates of 10- to 20 Gb/s, likely confined to dense urban areas.

Analysts at Credit Suisse in Taipei said MediaTek (the world's third largest chip designer,) is expected to continue making market share gains in the LTE market at the expense of top-rated Qualcomm because of its position in the fast-growing Chinese smartphone market. MediaTek's market share in LTE is likely to double (up to 45 percent of the China market) by December 31st.



In other news from Asia, the Tsinghua Unigroup (China) bid $23 billion to buy Micron Technology. While the deal would fill one of the biggest strategic holes in China's chip industry it was expected to raise political issues all the way to the US White House. Micron is the second largest chip maker in the US (behind Intel) with revenue of $16.8 billion in 2014.

By mid-July analysts were reporting that semiconductor sales were in a two-year slump due primarily to weak demand for PCs and some smartphones. Gartner Group reported that chip sales rose a mere 2.2 percent by the middle of 2015, with growth of just 1.3 percent predicted by year's end. At the same time, Gartner predicted that growth would return to a more typical 4-5 percent range starting in 2017, thanks to expected growth in IoT, the expansion of smartphone sales in growing markets such as India and China, and more positive momentum in other markets including Europe and the Americas.

"The Consumer Electronics Association, also presenting at the Flash Memory Summit, said that while wearables constitute the fastest growing segment they are also the smallest and most fragmented"

Taiwan Semiconductor Manufacturing Co. (TSMC), the world's largest chip foundry, said the outlook for the rest of 2015 is worse than the company previously expected because customers were digesting an inventory glut built earlier this year. While the company expected an increase in demand for computer, consumer and industrial segment devices, it expected smartphones and other handset device markets to decline.

The impact of declining growth in China was fully felt across global financial markets starting in July. Even though the official sources in Beijing reported 7 percent annual growth, outside economists and analysts pointed to the government's widely observed miscalculation of 'deflator' factors that are a broad measure of prices affecting a country's economy. Economists stated that Chinese gross domestic product (GPD) figures were wrong by up to 2 percentage points.

The vulnerability of devices linked to the internet hit home in July as car maker Jeep and its parent, Fiat Chrysler Automotive (FCA), admitted that Jeep vehicles were vulnerable to hacker attacks. FCA stated that blame for the vulnerability was shared with Sprint, FCA's system integrator, and Harmon Kardon, designer of in-vehicle infotainment systems.

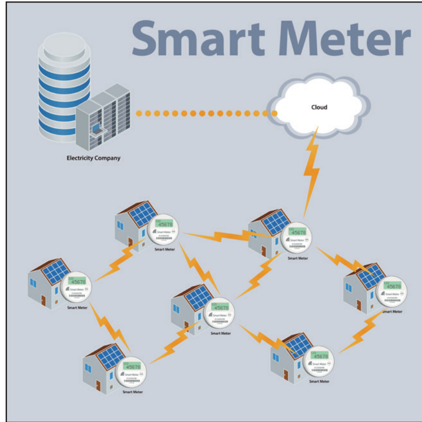
The revelation came at the end of the month when a hacker team succeeded in taking over vehicle functions by exploiting software weaknesses. A sweeping recall of 1.4 million vehicles resulted to proactively address the problem; no driver injuries were reported at the time.
NXP celebrated strong financial performance as the month drew to a close. The company reported $1.506 billion in revenue, a 12 percent increase compared to 2014. High performance mixed signal products for security, connectivity and mobility made the second quarter the 12th consecutive double-digit growth period for the company.

August

At a meeting of IoT professionals at the Embedded Systems Conference (ESC), the group conceded that Internet of Things technology will not take off until two lynchpin requirements are met: development of wide area networks and lower costs for hardware crucial to seamless connectivity. While hardware costs typically decline as deployment accelerates, the lack of networks hinders overall market development. While the group referenced good efforts to create networks by the LoRa Allience led by Semtech, and SigFox (France), the group foresaw that IoT devices would slowly enter the market since cellular networks appear to be, '…the only viable option for that kind of coverage for the next ten years….'

At the Flash Memory Summit Samsung announced solid-state drives (SSDs) and systems geared to drive 3-D NAND into mass markets. But analysts and even other vendors suggested that it may take most of 2016 before the technology is ready for mainstream implementation. The Consumer Electronics Association, also presenting at the Flash Memory Summit, said that while wearables constitute the fastest growing segment they are also the smallest and most fragmented. This led other analysts to conclude that fitness trackers and

smart watches both show signs of gaining traction with consumers, yet they have penetrated just 11 percent of US households, nowhere near the 60 percent penetration of smartphones in the US.



Altera executives seemed edgy about prospects of life under the Intel umbrella. Analysts, speaking with current senior executives and those who have already departed the company, cited fears of how well Intel integrates acquired companies given its PC-oriented leadership. Despite Intel's long-standing attempts to shed its dependence on personal computing, they cited what happened to past acquisition targets including Level One, DSP Communications, Sialogis Corporation, Giga A/S as cause for concern over how well Altera might fare. Smart meters are driving the IC market supporting IoT in utility markets. Global revenues for semiconductors used in water, gas and electric meters reached $1.2 billion in 2014, with growth standing at 11 percent according to IHS researchers. Growth opportunities remain as more public utilities change over to the technology, which better tracks customer utilization. The future points toward integrated ICs to do the work now being done by individual components; manufacturers with integration expertise are best positioned to take advantage of this growing market.

MediaTek's rapid growth in 4G smartphones is likely to be undermined by handset makers in China who are designing their own chips, according to Hong Kong based Bernstein Research. Spreadtrum Communications and Huawei are eroding MediaTek's position because the maturing market is favoring Chinese players that are backed and subsidized by the government. At the same time MediaTek is gaining market share from Qualcomm in the 4G and high-end segment.

September

Chinese upstart Phytium Technology made headlines with is aggressive 'Mars' design that was released at the Hot Chips event. The Mars architecture is designed for ARM-based servers and utilized advanced SoCs not seen before in mass market applications. But despite the fact that Phytium is only three years old, the company has deep roots in Chinese electronics—it is a subsidiary of China Electronics Corporation, one of the oldest state-run enterprises.

Gartner researchers reported that chip sales in September continued to slow largely due to stagnant sales of semiconductors headed into PCs, tablets and smartphones. They forecast that growth could dip to a fraction of one percent, but might rebound once third quarter sales figures were finalized. TSMC announced that it expected to begin early production utilizing a 10nm process later in 2015, and planned to achieve 7nm production capability by 2017. The road map that the company unveiled in Silicon Valley meetings also pointed towards a reduced cost version of its 16nm process in 2016 and a broad portfolio of specialty processes for IoT, automotive and sensor applications.

Perhaps leaping ahead of consumer acceptance and comfort, analysts at the Linley Group announced their research points to the availability of fully autonomous, self-driving cars by 2022. This new technology will help double the size of today's $10 billion automotive semiconductor market by 2025. Feedback from automotive industry insiders suggest that today's driver assistance and automation systems are mere 'appetizers' for the main course of self-driving cars.

The technology is already there and being tested, remarked Linley Gwennap, principal of the Linley Group. The researcher did not elaborate on how willing consumers will be to hand steering wheels over to microprocessors. Anyone for a replay of 'I Robot'?

October

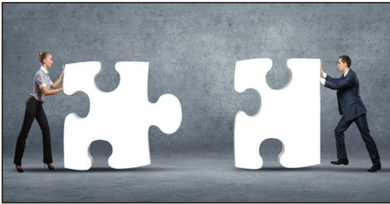
Google's' Nest Labs announced it planned to release its Weave protocol in 2016 and will involve partners that will use it to connect smart home products such as locks, light switches and cameras. The advancement is seen by industry observers as another way that IoT devices are moving into more mainstream applications visible to a wider range of consumers.

The slump in PC market semiconductor sales was reflected in Micron Technology's report of declining sales revenue for a third straight quarter. Even though PC sales remain sluggish, the company reported healthy demand for memory chips in other end markets,

Analysts at the Linley Group announced their research points to the availability of fully autonomous, self-driving cars by 2022. This new technology will help double the size of today's $10 billion automotive semiconductor market by 2025

pointing to the continued shift away from traditional computing and towards other small form factor computer options such as tablets and smartphones.

Marvell announced that it is sampling the first products based upon its MoChi approach to building modular SoCs. One of the company's two new 64-bit ARM processors is the first to implement final-level cache (FLC) technology, which aims to shrink external DRAM requirements. The MoChi design concept is Marvell's approach to creating products that operate like SoCs when interacting with application software, but may actually be composed of multiple die in one or more packages. The concept enables chips made in different processes to work together as closely as if they were grouped together on the same die.



Extreme Ultra Violet (EUV) technology got a boost from imec researchers in Belgium working with Cadence Design Systems. The two organizations partnered to create two 5nm test chips using a mix of 193i and EUV techniques. The researchers believe this approach represents the best alternative to breach the barrier limits of Moore's Law in transistor evolution.

Dell bid $67 billion to buy storage giant EMC in a mid-October acquisition proposal. The deal was billed as the largest high-tech purchase to date, but received mixed reviews from industry watchers. The analysts were unenthusiastic largely because both companies—though large and successful—are seeing flat or declining sales in their segments. Industry insiders wondered how the company would deliver growth to investors given little prospect for innovation beyond the company's existing portfolios.

The town of Bristol, England took innovation to a new height by turning itself into a 'petri dish' for experiments in communications and the Internet of Things (IoT.) Bristol received grants and gifts totally 75 million (GBP) to create wired and wireless infrastructure for a smart city. It aims to build applications ranging from assisted living programs for seniors to driverless cars and solar energy.

Taiwanese semiconductor giant TSMC reduced early-2015 planned capital expenditures of $10.5 billion to $8 billion, a 25 percent cut. The move came on the heels of slowing global demand for semiconductors.

Lam Research Corporation announced its intention to purchase KLA-Tencor, marking the start of the industry's largest merger of high performance process tool makers. The $10.6 billion deal was observed by some analysts as an effort to put the new company ahead of its arch-rival, Applied Materials. The merger was approved by both boards, but comes at a time of increasing regulatory scrutiny of M&A activity. In April Applied Materials and Tokyo Electron cancelled a planned $29 billion mega merger, citing opposition from antitrust interests at the US Department of Justice. Yet most analysts approve of the Lam/KLA deal, saying it will give the combined entity a decisive edge in global competition through pricing power it likely would not enjoy as separate companies.

November

Fears about automobiles being vulnerable to hacking led to more media coverage of the dilemmas facing car makers. While manufacturers have quietly sought to patch firmware and software holes, evidence remains that many newer car infotainment and computing systems are vulnerable to attacks that gain access through radio or cellular frequencies, or piggybacking on the short range signals from a consumer's key fob. According to the US Federal Bureau of Investigation (FBI), between April 2014 and June 2015, there were 992 'ransomeware' related complaints, with victims reporting losses totalling more than $18 million.

The Semiconductor Industry Association (SIA) reported that global chips sales declined 3 percent to $85.2 billion in third quarter. The decline followed trends from earlier reports, with declines in traditional PC sales and smartphones as leading indicators. At the same time sales picked up in September, leading some analysts to hope for a better year-end tally. Qualcomm reported to shareholders that it believed smartphone growth would continue to slow in 2016, and that prices for chips going into handsets will continue to fall, though less sharply than they did in 2015. Qualcomm also expects China OEMs will command a growing share of the market.

While Qualcomm fretted over its future with Samsung and with other key handset makers, its prospects may be looking up when it comes to printed electronics. Raghu Das, CEO or IDTechEx, hosted an industry forum on the subject in Silicon Valley, saying that the technology had matured to a point that engineers need to 'get printed electronics out of the lab and utilize their capabilities.'

Those poised to take advantage of these possibilities include Qualcomm and a handful of other companies. Qualcomm later presented new products at the forum, including a label that can gather data from a golf club and feed info to the player's smartphone. A thin-film battery maker, Blue Spark Technologies, displayed a bandage that can deliver a patients temperature information to a handset.

The strengthening US dollar compared to the position of other world currencies has taken a toll on the semiconductor industry, among many, and is forecast to lead to contraction in worldwide chips sales in 2015.

Samsung is set to make inroads into Intel's position as the world's largest chip maker in 2015, according to market forecasts compiled by researchers at IC Insights. The researchers say that Intel continues to suffer from its dependence on the weakening personal computer market and its limited success breaking into mobile phone applications. IC Insights expects Intel sales to contract 2 percent in 2015 compared to Samsung growing its chip revenue 10 percent, which should bring them in at $6 billion behind Intel's forecast of $50 billion in chip sales.
Merger mania continued in November

as Renesas Electronics became an investment target attractive to a number of suitors outside Japan, including China's Tsinghua Unigroup and Germany's Infineon Technologies. Tsinghua's ambitions in memory chips are well established since it is seeking a foothold in the logic business, especially in automotive and MCU segments.

Infineon is said to regard Renesas as an ideal fit, based on the Japanese chip vendor's strength in infotainment, head unit and digital cockpit technologies and other areas of automotive electronics where Infineon lags. It's also important that Renesas has a strong position with both Japanese and European automakers.

"A rocky 2015 did not deter Taiwanese semiconductor giant TSMC from predicting this month that it will achieve double-digit growth during the coming year and that its 10nm process is on schedule for production in 2016. The company's CEO also predicted similar results for 2015 at the end of 2014, so it remains to be seen how well the company will fare against headwinds now buffeting the industry"

December

T.J. Rodgers, outspoken CEO and President of Cypress Semiconductor, said this month that he expects 'merger mania' which is now driving consolidation across the industry may continue for another two years. The CEO cited a causal relationship between what executives see in the market and fears that not merging with a like-minded company could mean they are losing out on potential market share gains. Chip companies executed more than 18 M&A transactions worth more than $100 million in the last year; M&A activity totalling $110 billion was reported as of October 31st.

A rocky 2015 did not deter Taiwanese semiconductor giant TSMC from predicting this month that it will achieve double-digit growth during the coming year and that its 10nm process is on schedule for production in 2016. The company's CEO also predicted similar results for 2015 at the end of 2014, so it remains to be seen how well the company will fare against headwinds now buffeting the industry. TSMC also announced that its 7nm process was on track; the company could see 10nm as a transitional node leading directly into 7nm.

For only the second time in the last 25 years, business growth for the top chip manufacturers in 2015 is expected to beat the growth of top fabless companies, according to researchers at IC Insights. The change in fortunes is largely credited to Samsung's decision to use its own Exynos application processor in smartphones at the expense of Qualcomm. This growth notwithstanding, IC Insights said they also expect 2015 will be rather flat overall for the top 10 integrated device manufacturers (IDMs), while the top 10 fabless companies are expected to slip into slightly negative figures this year.

The International Electron Devices Meeting (IEDM) in Washington, DC was the setting for word from senior ARM researchers that even though it is getting harder and more costly to make chips smaller and faster, there is hope to be found in advancing Moore's Law. To combat an increasing set of design limitations, engineers will need to employ a host of remedies that could fragment and possibly dilute economies of scale.

This may result in significant sacrifices in density for the sake of schedules, combined with balancing the need for cost effectiveness with market timing. The researchers see hope in what is already being done and will be done to increase productivity and cut costs, noting as an example that multiple passes through lithography will increase costs while new steppers coming online for 7nm will be 50 percent faster than those used at 28nm.

United Microelectronics Corporation (UMC), the world's third largest foundry, said it expects to open a joint venture 300mm fab in China about two months earlier than expected. Production should begin in the third quarter of 2015. A spokesperson credited the aggressive readiness posture to faster than expected construction in China. Meanwhile, UMC arch rival, Taiwan's TSMC, also announced plans to open its first wholly owned 300mm fab in china, slated to begin production in the second half of 2018.

A Chinese government-backed firm has initiated a bidding war for chip maker Fairchild Semiconductor International. In November Fairchild accepted an acquisition offer from ON Semiconductor Corporation. The offer it accepted was for $2.4 billion, while the offer from the unsolicited bidder was for $2.6 billion. While Fairchild said it will review the new offer, its board has already accepted the ON Semiconductor bid, so it is unclear whether the Chinese company has a chance to acquire Fairchild.

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On-site generated fluorine:

Effective, safe, and reliable source of fluorine for electronics for over 15 years

On-site fluorine generation has proven a safe alternative to greenhouse gases often used in electronics manufacturing. Linde delves into its makeup, history, and how fluorine is effectively used to clean CVD chambers and in many other applications.

By Dr. Paul Stockman, Head of Market Development, Linde Electronics

ON-SITE GENERATED FLUORINE (F_2) is a safe and reliable alternative to greenhouse gases for chemical vapor deposition (CVD) chamber cleaning and is currently used in the commercial production of semiconductors and LCD screens in multiple sites in Asia and Europe. In the first of a two-part series, we describe the on-demand production of high-purity fluorine as demonstrated by Linde's installed base of more than 30 generators over the last 15 years. Production capacities ranging from 1 to 100+ tons / year have displaced high-pressure fluorine cylinder and bulk nitrogen trifluoride (NF_3) supplies. Certification by leading safety and engineering authorities document the design details required to effectively deliver fluorine reliably and safely without incident. In Part 2, we will describe the fundamental physical properties of fluorine, which are the basis for significant process and cost of ownership improvements and which eliminate the need for greenhouse gases in chamber cleaning.

History of fluorine

Fluorine was first produced and isolated by the French chemist Henri Moissan in 1886. However, the challenges in production processes and the element's vigorous reaction chemistry limited its use to bench-scale apparatuses for small experimental quantities. Industrial-scale production technology was first developed for the Manhattan Project in 1943 when gas-phase uranium hexafluoride (UF_6) was identified as the preferred method for separating the fissible ^{235}U isotope from the remaining 99 percent of isotopes. After the war, fluorine production technology was further developed and proliferated with the spread of independent nuclear materials capability and from this base further non-nuclear applications were developed.

Today, tens of thousands of tons of industrial fluorine are produced commercially all over world as chemical feedstock for organic fluorides and various inorganic fluorides such as SF_6, NF_3, and boron trifluoride (BF_3). Additionally, industrial fluorine is used for chemical modification of surfaces and to make certain plastics impermeable to water, oxygen, and hydrocarbons.

While industrial fluorine can be transported in large volumes either as a cryogenic liquid or as a compressed gas, safety and logistic concerns dictate that most fluorine is produced and consumed on-site and on-demand at low or atmospheric pressure. This limits both absolute inventory of fluorine, because it is only made as is needed, and also prevents high-energy, high-pressure events because the reactivity of fluorine is directly related to its pressure.

How fluorine is produced

Fluorine is produced by electrolysis of anhydrous hydrogen fluoride (HF) to yield hydrogen (H_2) gas at the cathode and F_2 gas at the anode; the amount of gas evolved is directly proportional to the current applied. The process is similar to the electrolysis of water to produce H_2 and oxygen (O_2); however,

it requires the salt potassium bifluoride (KHF_2) as a charge carrier and transport medium. The HF consumed by electrolysis is replaced by adding HF gas or HF liquid directly to the salt-acid mixture, with an effective composition of $KHF_2 \bullet (HF)_{x \approx 1}$, which melts at 72° Celsius. The electrodes are physically separated to prevent the rising H_2 and F_2 gas bubbles from recombining, and the gases are evolved over the melt and collected through separate vents. Material selection of electrode and cell body components is essential to ensure a long operating lifetime of the fluorine cell with minimum maintenance requirements, and periodic chemical analysis of the salt-acid mixture verifies the integrity of components.

HF dissolved in the molten KHF_2 salt is electrolyzed to produce H_2 at the cathodes and F_2 at the anodes. The HF_2 feed can be introduced either as a gas or a liquid. The evolved streams of both H_2 and F_2 contain 1-5 percent of HGas as a vapor-phase impurity. The H_2 stream is diluted to concentrations below the LEL (lower explosion limit) of 4 percent and scrubbed before being vented to atmosphere. For high-purity applications, the fluorine stream is purified to remove the HGas as well as other low-level impurities. Compression to a working pressure of 1.0 to 1.5 barg and buffering in a temporary tank provides an adequate process supply at constant pressure without creating excess inventory.

Anhydrous HF, either in gas cylinders or larger bulk containers, is used to feed the fluorine cell. The H_2 byproduct is extracted for disposal, while the generated fluorine is further purified before being compressed to 1 to 1.5 barg and temporarily buffered before use in the customer process. All key process modules are enclosed in extracted cabinets as part of the safety design.

On-site fluorine generators

Concerns for safety and reliability have informed the design of on-site fluorine generators for use in the high-tech thin-film industries of semiconductor, display, and photovoltaic manufacturing. As with any chemical introduced into these market sectors, safety risks need to be identified and mitigated. Fluorine is the most electronegative element from the periodic table and this extreme reactivity is the cause for risks to both health and equipment.

Fluorine falls in the middle of the spectrum of the many toxic gas-phase chemicals commonly used in thin-film device manufacturing, a few examples of which are shown in Table I *[Reference: American Conference of Governmental Industrial Hygienists]*. Mitigation strategies focus on three areas: material selection and passivation, containment, and design for minimal inventory.

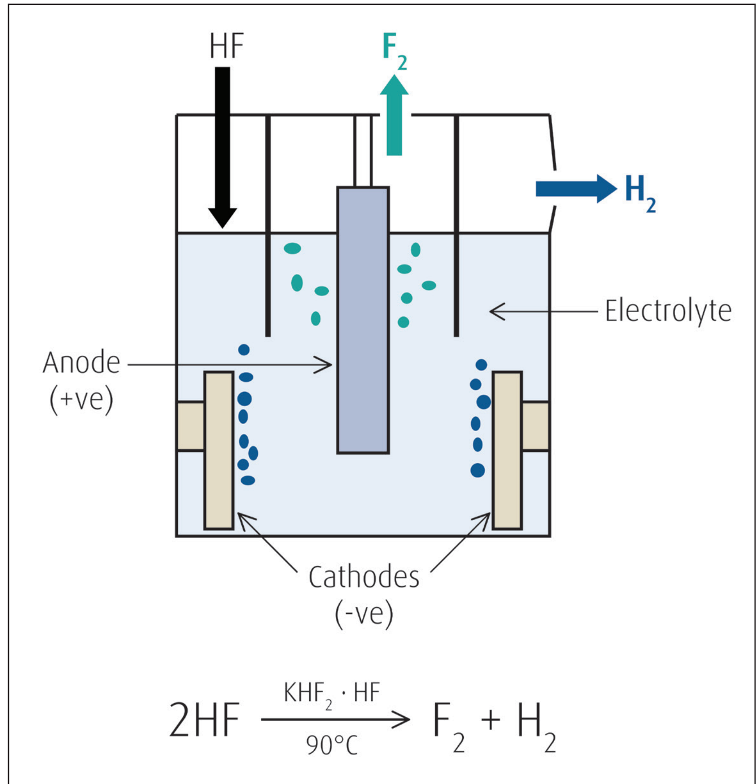

Figure 1: Electrolytic production of fluorine

Comparison of toxicity of electronic gases

Gas TLV/TWA[1]	(ppm)
Arsine	0.05
Diborane	0.1
ClF_3	0.1
Germane	0.2
Phosphine	0.3
Fluorine (F_2)	**1**
HF	**3**
Silane	5
NF_3	10
CO	25

Note1: TLV/TWA is defined as Threshold Limit Value/Time-Weighted Average. It is the maximum permitted workday exposure recommended by the ACGIH.

Table I: TLVs (Threshold Limit Value) for common gas-phase, thin-film feedstocks

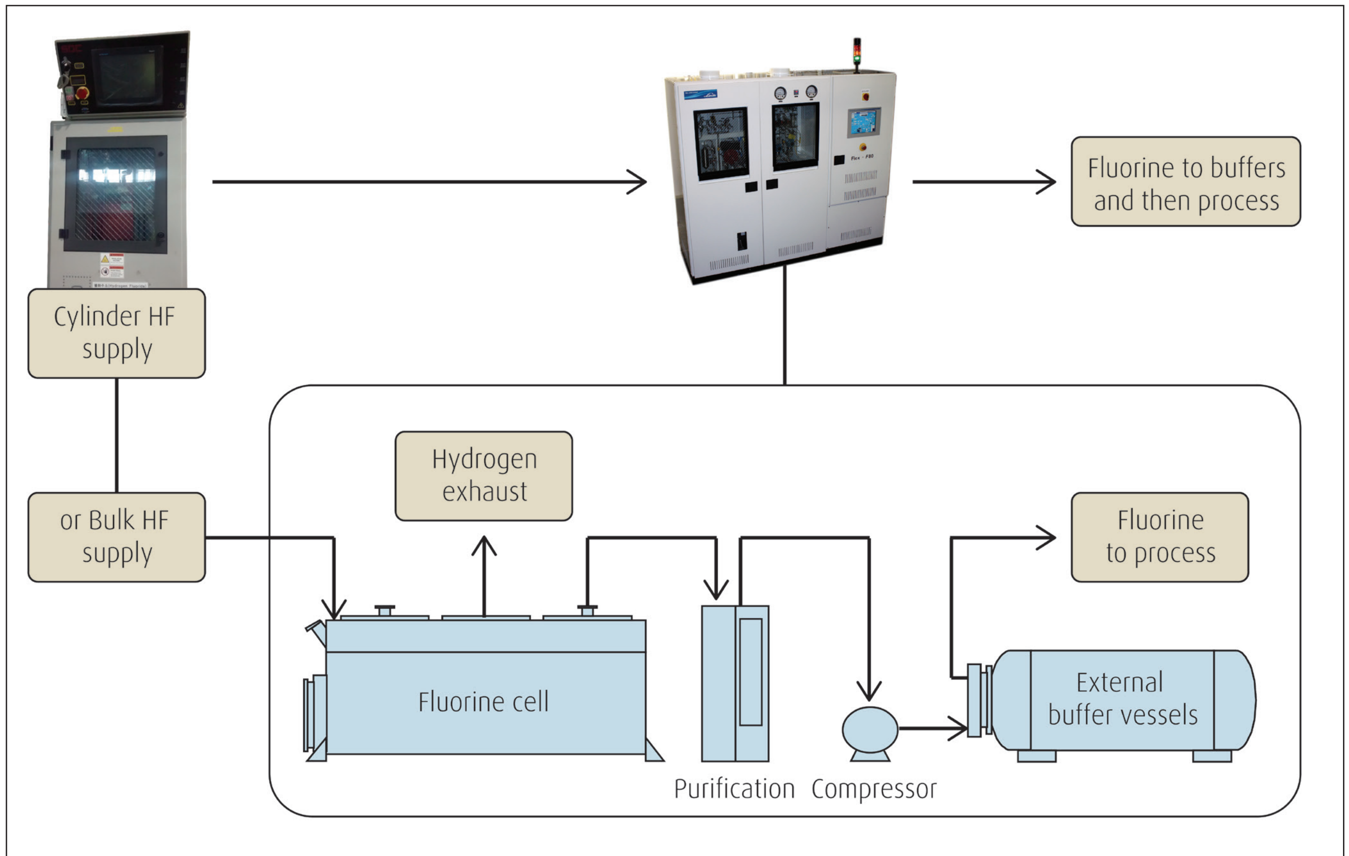

Figure 2: Process flow diagram for on-site generated fluorine

Mitigation strategy: Material selection and passivation
Although fluorine is highly reactive, many common metal constructions are compatible with fluorine at process temperatures. These include brass, copper, nickel, and many steel and nickel alloys, all of which form chemically inert, passivated metal fluoride layers when properly prepared.

Components for the generation, containment, and transport of fluorine should first be cleaned of all particles and residues – the same as for oxygen service – and certified leak-free. They are then exposed to a sub-atmospheric partial pressure of fluorine, often diluted in an inert gas.

Any organic residues are converted to gas-phase fluorides and exhausted to a scrubber, while the native oxide layers of the metal are replaced to form metal fluorides. By gradually raising the partial pressure to the maximum working pressure, the metal fluoride passivation layer is deepened, and the metal surfaces are rendered inert to further reaction with fluorine.

In addition, properly-sized piping and elimination of sharp bends are required to reduce gas velocities below the industry-recognized safe levels *[Reference: Compressed Gas Association CGA publication 9-15; European Industrial Gas Association EIGA document 140/10].*

Mitigation strategy: Containment
Containment forms the second safety risk mitigation strategy. All super-atmospheric sources of fluorine are contained by either ventilated enclosures or sealed and sectioned annular piping.

Ventilated enclosures house all generation and compression equipment, purification and buffer vessels, and valve manifold boxes. Extraction rates are determined to maintain safe external conditions in the event of a rapid release of the limited inventory. Extracted air is treated by either a local or facility acid scrubber.

Toxic gas detectors specific to fluorine are used to monitor all extracted areas. Transport of fluorine within the facility is through double-layered piping. The fluorine flows in the center tube while the annular space is sectioned and pressurized with nitrogen.

A leak from the center tube can be detected as a pressure loss in the annular space, and fluorine is doubly contained by both the outer pipe and the nitrogen barrier. A leak detected by a toxic

gas monitor or by depressurization of the annular containment triggers suspension of fluorine generation and automated closure of fail-closed valves.

Mitigation strategy: Design

On-site fluorine generation has been sized to meet the requirements of a number of thin-film chamber cleaning processes. Originally conceived as a replacement for high-pressure cylinders of F_2 and ClF_3 (chlorine trifluoride) used for cleaning low-pressure chemical vapor deposition (LP-CVD) semiconductor equipment, the smallest sized units have an annual production capacity of 1 ton / year. The equipment is designed in standard modules with form factors similar to gas cylinder cabinets.

Along with the availability of gas blenders with very low pressure-drop components, these units make for a direct replacement of 20 percent F_2 / 80 percent nitrogen (N_2) cylinder supplies. Almost all safety incidents in the semiconductor industry with fluorine are associated with high-pressure cylinder supplies, and in particular, the regulators used. Because a single generator operating at low pressure can replace more than 500 cylinders per year, the safety of the process has been greatly improved.

Maintaining a minimal inventory is integral to the design and safe usage of fluorine. Because the fluorine is generated on-site, there is no need to compress it to high pressures in order to transport it in containers. Instead, a pressure of 1.5 barg is sufficient to supply all gas conditioning and mass flow equipment of the cleaning process. And because fluorine is generated on-demand and proportionally to the current applied to the electrodes, the only vessels used are sized to buffer the generator against the periodic requirement for cleaning gas.

Modeling of randomized demand from multiple tools, sometimes numbering more than 100 for a single on-site plant, ensures that the buffer vessels are sized adequately for all realizable demand without being oversized. For example, a plant with a name-plate capacity of greater than 100 tons / year has an instantaneous inventory of less than 50 kg, which is little more than four hours of supply for a large LCD fab; fluorine supplies for semiconductor process have inventories as low as 2 kg at any time. As well as being made safe, on-site generated fluorine for thin-film chamber cleaning applications must meet the very high industry standards for reliability. Design and operation are essential to achieving high uptime. Beyond proper material and component selection, moving parts are minimized in the system design, electrochemical duty is kept light, and preventative maintenance and monitoring use leading indicators to keep all performance parameters within controlled ranges.

The design of the on-site generation configuration uses n+*1* redundancy of key components and modularization of assemblies. Therefore, preventative maintenance and repairs can be performed quickly without compromising the ability to supply the process, and longer-term service can be accomplished off-site. In addition to on-site operators, most fluorine plants for thin-film chamber cleaning take advantage of remote monitoring. This allows 24 hours per day coverage and diagnostics by fluorine plant experts located on three continents.

The design for safety and reliability have been recognized and accredited by a number of design authorities and awarding bodies: certification to CE, ASME, Korean S-mark, and SEMI S2, and awards by Semiconductor International for Best Product 2009 and from International Solar Technology for Green Solar Manufacturing 2009.

With the advent of the high-volume manufacturing of LCD screens and thin-film photovoltaic modules, the demand for on-site generated fluorine has grown in scale. In these applications, fluorine is used as a chamber cleaning agent for plasma-enhanced chemical vapor deposition (PE-CVD) processes. Larger generators have been designed for supplying 100s of tons / year. And although the process design

"Maintaining a minimal inventory is integral to the design and safe usage of fluorine. Because the fluorine is generated on-site, there is no need to compress it to high pressures in order to transport it in containers"

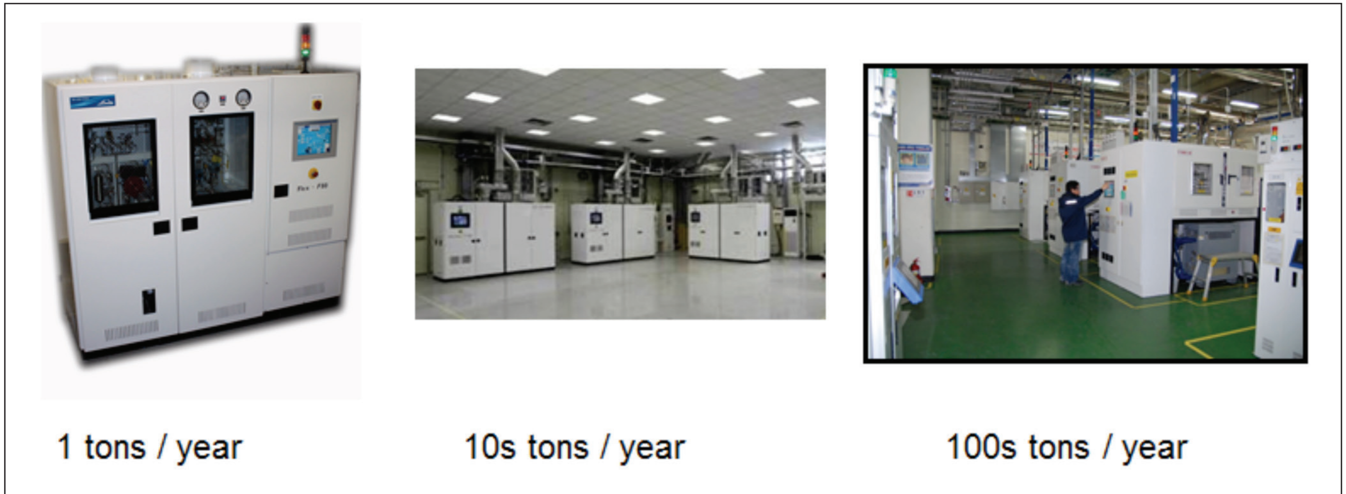

Figure 3: Three generations of on-site fluorine generators. Generators are available in different sizes and configurations to offer a wide range of capacity options.

remains the same, the form factor for these systems has grown to a separate on-site facility. This mirrors the track to other on-site supply schemes, such as those for nitrogen, oxygen, and hydrogen, from which manufacturers benefit as they scale their operations to achieve critical capacity.

The supply of on-site generated F_2 differs in several areas from the use of SF_6 or NF_3 for cleaning thin-film equipment.
On-site supply schemes require different project considerations versus packaged material supplies to ensure proper footprint, utilities availability, and expansion capability.

Planning for safety is integrated with the end user and community at an early stage, and additional activities are required for commissioning and operation. Likewise, permitting and licensing change, with the added benefit that the on-site chemical inventory is substantially reduced. Furthermore, risks to supply chains and pricing volatility are reduced.

Summary

In the last 20 years, Linde has installed over 30 on-site fluorine generators, which are successfully operated in 11 countries. These continue to operate without a single safety incident, and provide supply delivery reliability much greater than 99 percent.

In Part II of this article series, we will discuss the fundamental chemical properties of fluorine that allow it to deliver significant process and cost of ownership benefits while at the same time eliminating the need for the majority of greenhouse gas usage in high-tech, thin-film manufacturing. Used in increasingly higher volumes, gases like NF_3, SF_6, and C_2F_6 have global warming potentials thousands of times greater than CO_2 and are coming under stringent monitoring and reduction regulations as more aggressive measures are enacted to reverse trends in climate change.

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DR. PAUL STOCKMAN joined Linde in 1996. He currently is Head of Market Development, Linde Electronics, where he guides Linde's strategy to anticipate the needs of its customers in the semiconductor, display, solar and LED markets. During his career with Linde, Dr. Stockman has held roles in electronic materials product, purification and analytical development; equipment development; as well as Technology and Commercialisation Manager for Linde's on-site fluorine equipment. Dr. Stockman has been granted 5 U.S. patents and holds a Ph.D. in Chemical Physics from the California Institute of Technology.

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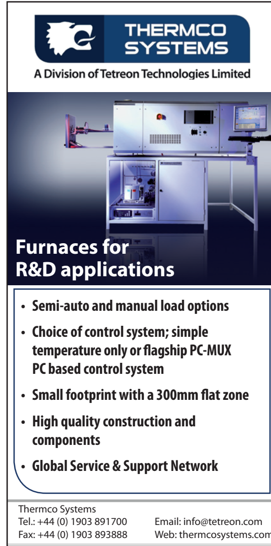

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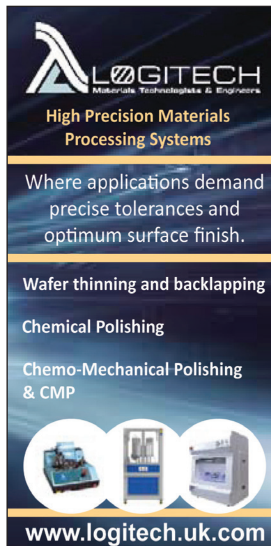
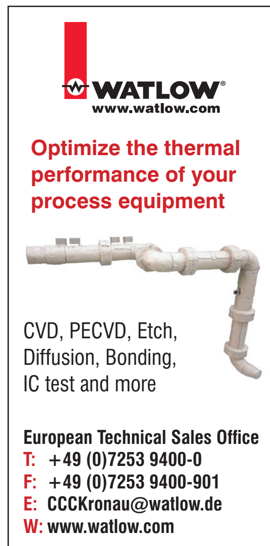


Pump Line Heaters



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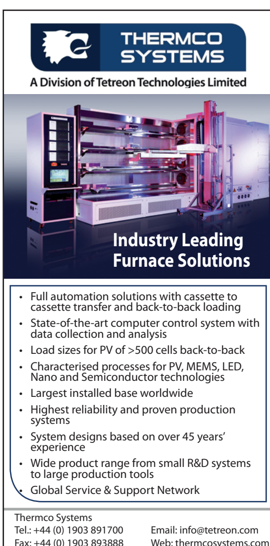
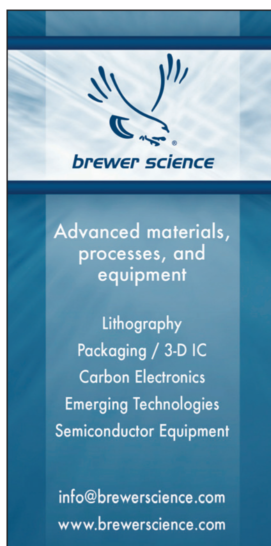


Materials, Processes and Equipment



Solder Rework

Wet Process

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