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Volume 38 Issue 5 December 2016 @siliconsemi www.siliconsemiconductor.net

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How plasma resistant are your O-rings?
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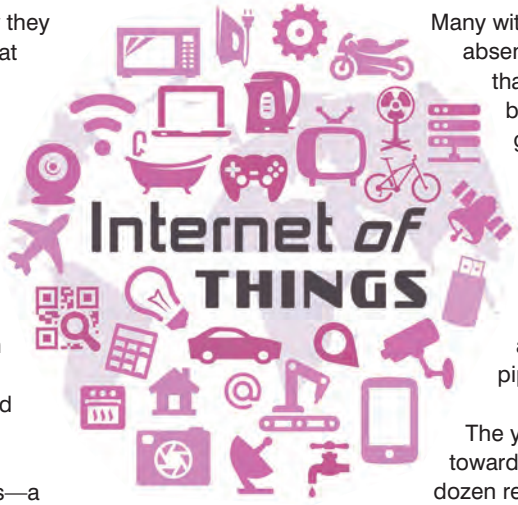
editor's view

By Mark Andrews, Technical Editor

Will IoT set the pace in 2017?

You can't satisfy some people. Some say they would rather do almost anything than what they do each day. Me? I enjoy my days because I work in the semiconductor industry.

Surprised at my satisfaction? Then take a closer look. Where else but in semiconductors could you find the sort of daring that defies (or at least bends) the laws of physics? Where else will you find more than just a few people who can say they started with nearly nothing, but today are driving a Ferrari or have realized other wild and crazy dreams?



2016 in a sense has been like other years—a little up, a little down; some new products / some new processes. But hardly business as usual. 2016 had enough unexpected endings and life-changing discoveries to keep Hollywood writers busy. There were major mergers worth billions that failed, while even bigger deals like the Softbank/ ARM proposal or Qualcomm wedding NXP claimed the spotlight.

Risk and its inherent excitement is what sets this industry apart. Simple ideas can become industry standards. But it is the risky process of putting an idea out there that leads to success. And even though there are no guarantees, it's opportunity that drives our industry, and that is exciting.

Many within semiconductors bemoaned the absence of sustained growth this year, and that's understandable—no one starts a business planning to 'just do OK.' Yet growth crept back into forecasts late in the year and most analysts now believe 2017 will be better. Much hope is again placed on Internet of Things products and services. And while we have heard this song before, more IoT products were introduced in 2016 and still more are moving through the pipeline.

The year fast passing saw serious work towards 5nm silicon chips even as a half dozen research teams announced 'More than Moore' alternative technologies. We saw new solutions for keeping lithium-ion batteries operating safely while other companies announced mobile power solutions that use entirely new chemistries. Energy storage became a product category that leapt from renewable energy to electric vehicles to power electronics and back 'round again.

Why do I find the semiconductor industry exciting? It's the place where virtual reality has become a reality. It's the place where clouds are full of memory, where new circuits are connected by photons, and where computers fit on a wrist. Excitement is all around us – So as we look back on 2016 and ahead to 2017, prepare to be amazed.

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Silicon Semiconductor is published four times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/€158 pa (UK & Europe), £138.00 pa (air mail), $198 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2016. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing.
US mailing information: Silicon Semiconductor is published four times a year for a subscription of $198 by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. Periodicals postage paid at Rahway, NJ. POSTMASTER: send address changes to: Silicon Semiconductor, c/o Mercury International Ltd, 365 Blair Road, Avenel, NJ 07001.
Printed by: The Manson Group. © Copyright 2016. ISSN 2050-7798 (Print) ISSN 2050-7801 (Online).

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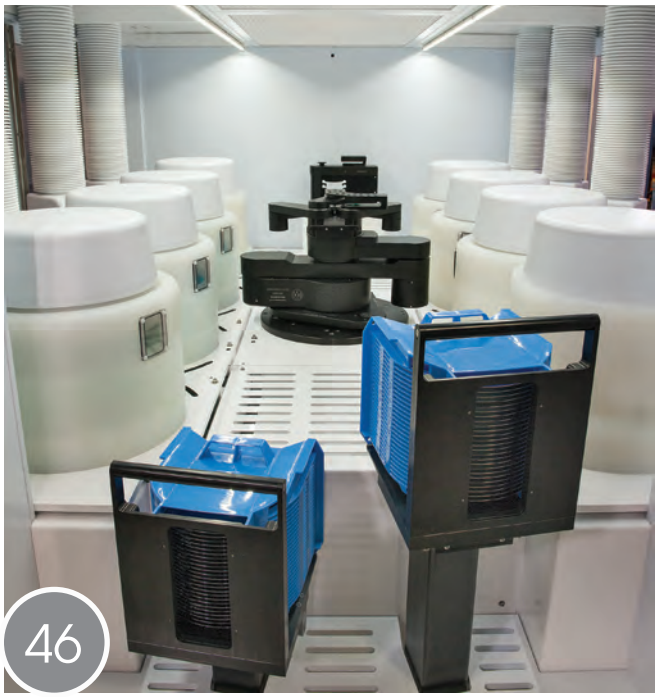
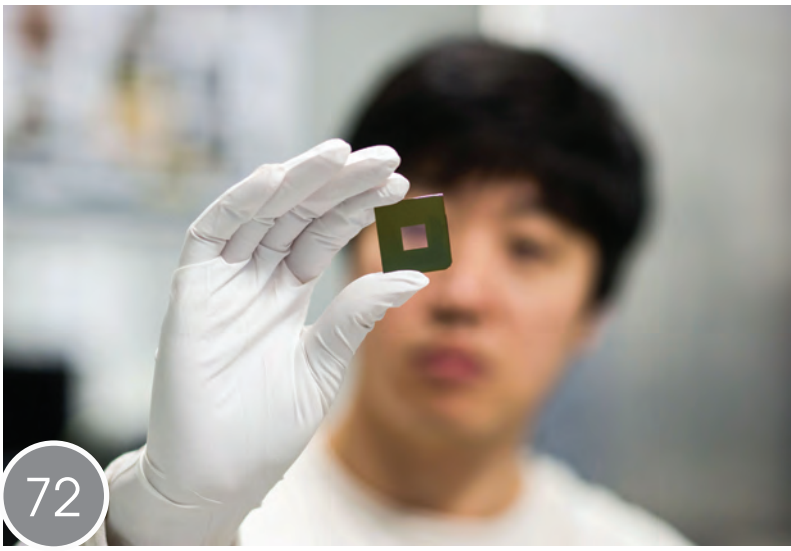




The top headlines in review

2016 saw new records and innovations across the semiconductor industry with late year rebounds and new opportunities poised to spur growth in 2017. Mark Andrews, technical editor looks at the industry highs and lows.

INDUSTRY CONSOLIDATION continued to make headlines in 2016 with the record-setting £24.5 billion (GBP) offer by SoftBank (Japan) for ARM (UK) amongst major multinational deals that became public by mid-year. While growth seemed elusive throughout much of 2016, an unexpected spike in US PC sales joined other gains in non-PC segments to push the needle towards positive in third and fourth quarters. Not to be outdone on the M&A stage, Qualcomm targeted NXP in a late-year acquisition bid driven by desires for a manufacturing foothold in connected world tech. If approved, the deal will encompass a total enterprise value of about $47 billion (USD). But mergers don't always see approval. In 2015 regulators scuttled the Tokyo Electron/Applied Materials marriage. In 2016 they pushed-back against the Lam Research/KLA-Tencor merger; we'll see which deals close in 2017.

2016 was also the year that saw a plethora of new silicon devices entering the market, many targeting the Internet of things (IoT), a segment that most industry watchers believe will be the biggest opportunity for long-term semiconductor growth since smartphones burst onto the scene in 2007. Leading foundries debuted new 10nm and 7nm capabilities in 2016 while talking about their 5nm plans and processes. New solutions were also proposed as 'More than Moore' ways for keeping transistor density and processing speed increasing once silicon reaches its theoretical limit. And power storage emerged as a cross-market product category, bridging silicon photovoltaic (PV) sales, power electronics and legacy electrical grid requirements.

No matter where one might turn in 2016, a nagging question kept rearing its head: when will growth validate the aspirations of so many across the semiconductor supply chain? Positive indicators materialized shortly before SEMICON Europa in late October. But it would take further evidence in November and December to point towards a positive finish for 2016 and an upbeat outlook for the year to come.

JANUARY 2016

Intel's Bumpy Ride
Market leading semiconductor maker Intel Corporation reported record fourth quarter revenue in line with consensus analysts' expectations, but said 2015 sales as a whole declined slightly amid a fourth consecutive year of declining PC sales. Intel executives said the company finished the year strongly, despite a weaker than expected macroeconomic environment and a weak PC market.

Helping 'little' pharma
Professor Yufeng Jane Tseng at National Taiwan University (NTU) announced that NTU had developed a program that eliminates the need for animal testing in drug research and development, which is required today by the Federal Drug Administration (FDA) and other international drug safety agencies. Prof. Tseng said it is believed that NTU's modeling program will help 'little pharm' compete against much larger international pharmaceutical companies, so long as drug monitoring agencies approve the new process.

TSMC forecasts $9.5B in 2016 Capex
Taiwan Semiconductor Manufacturing Co. (TSMC), the world's largest foundry, said it will increase its capital expenditure in 2016 between $9 billion to $10 billion as it aims for greater share of small geometry chips. The company it planned to keep the spending high in order to retain its top spot after slashing capital plans several times in 2015. TSMC estimated that its 2016 revenue growth rate may double the company's expected 5 percent gain for the overall foundry segment this year.

The company also indicated that it has made significant progress on extreme ultraviolet (EUV) lithography, and after a series of setbacks in attempts to utilize it for 10nm and 7nm, it expects to insert

the process for 5nm chips. The company noted it achieved output of 500 wafers per day using EUV during a sample period.

Samsung worker health
Samsung Electronics Co. Ltd. made a concession to worker families and former employees who have died of cancers over the last decade, agreeing to establish an independent committee able to inspect its semiconductor facilities. Families and former workers have argued for a decade that it was the unsafe use of dangerous chemicals in semiconductor wafer fabs that caused anomalous clusters of illnesses and deaths. Samsung has apologized to the families but has also denied responsibility for the deaths and illnesses. The company established a fund in 2015 ($83 million USD) to pay worker medical expenses; there have been 150 claims filed since then.

Global PC numbers fall in 2015
Global PC shipments declined again in 2015, the fourth consecutive year of contraction in what has traditionally been the most important market for the semiconductor industry, according to industry research firms. Just 276.2 million PC units shipped in 2015, the first time since 2008 that the personal computer market did not break the 300 million mark, said International Data Corporation (IDC). It was the fourth consecutive year of declining shipments for PCs.

Chip forecasts / market drivers diverge
Semiconductor revenue forecasts in 2016 and what will likely drive them long-term vary widely among analysts. China will be key factor, but one nearly impossible to predict, said the analysts meeting in a strategy session convened by the SEMI trade group. Bill McClean, IC Insights, was bullish, predicting four percent revenue growth in 2016. Handel Jones of International Business Strategies (IBS) was bearish, forecasting a 1.5 percent decline that could slide to a negative three percent. Gartner was in the middle, expecting 1.9 percent growth for the year. By product group, NAND flash is expected to be a bright spot with an 8.7 percent compound growth rate through 2019. Even faster growth is expected for IoT devices, but it will likely make up less than $30 billion in

semiconductor sales by 2019, about 7.2 percent of the chip market, given average selling prices of a couple dollars per chip.

Manufacturing is top cyber target
While cyber-attacks on networks at Sony, Target, and the US Government made headlines, the greatest cyber vulnerability is in manufacturing, said Chet Namboodri, senior director of Global Private Sector Industries at Cisco. “Financial services gets more press, but industrial networks get more attacks.”

Imec melds flash with III/V performance
Researchers at nanoelectronics research group Imec (Leuven, Belgium) found a way to increase the speed and longevity of flash memories by arranging them vertically along with higher-performance III-V channels that employ indium gallium arsenide (InGaAs). Most flash memories today use planar polysilicon channels controlled by a floating gate and a control gate used to read at low voltages and program at high voltages. Imec found that vertical 3-D NAND gates can be greatly accelerated by using III-V materials such as InGaAs in the channels.

Intel gets deeper into drones
Intel Corporation continued its march into the rapidly growing drone market, announcing it signed a definitive agreement to acquire Germany-based drone maker Ascending Technologies GmbH.

Financial terms were not disclosed. The acquisition was the latest in a series of investments that Intel has made in drone technology over the past year. Intel, other chip vendors and consumer electronics firms are increasingly looking at the drone market as another place where technologies developed mainly for smartphones can be leveraged.

Apple hints at wireless charging future
In an effort to stay ahead of its rivals, and in the face of flagging iPhone and iPad sales, Apple is planning to introduce wireless charging on the two devices as early as 2017, according to a Bloomberg report, which quotes unnamed sources familiar with the plans. Apple is working with partners both in the US and Asia to resolve issues inherent in wireless charging technologies including the present need to increase charging power when a smartphone or similar device is farther from the power source. Apple currently offers wireless charging for its smartwatch, and smartphone rivals such as Samsung, Sony, and Google all offer handsets that boast wireless charging.

FCC wants to cancel cable TV set-top boxes
The era of the set-top box is over, according to officials at the US Federal Communications Commission, which announced a proposal to open up competition for delivering pay television services. A Notice of Proposed Rulemaking was released that aims to let any system or application access pay-TV streams, putting an end to the high cost of renting set top boxes currently defined and provided by cable television providers.

The proposal would require providers to choose open formats defined by industry standards groups to control access to their programming and content guides as well as maintain security. The FCC said all of this is within today's technological capabilities, but that cable TV companies have resisted this due to the loss of STB revenue that they have grown to depend upon.

ST exits the set top box market
STMicroelectronics NV said on the same day that the US FCC announced its new set top box rule making intent that the company will stop developing STB and home gateway products. It also plans to lay off up to 1,400 workers out of its 43,000 employees. In a 2016 that workforce 're-alignment,' about 1,000 employees (150 based in France), will be affected. Moving forward, ST intends to focus on automotive and industrial applications as well as Internet of Things devices including smart home and smart city applications.

Apple forecasts first decline since 2003
Despite another quarter of record sales and revenue, Apple Inc.'s stock traded lower after hours (Jan. 26) after the company reported lower than expected iPhone sales and forecast its first year-over-year decline in sales in 13 years. Tim Cook, Apple's CEO, laid the blame for the lackluster quarterly forecast primarily on the strong US dollar and on 'economic malaise' in China and other areas.

EUV Improves, but still not ready
Extreme ultraviolet (EUV) lithography is making slow progress, re-kindling hopes it could be ready for production use in the 7nm node, while TSMC and other major foundries say they expect insertion at 5nm. The semiconductor industry has placed multi-billion dollar bets the technology will enable smaller, cheaper chips; critics remain skeptical. So far, EUV lacks a powerful and reliable enough light source to produce the number of wafers that major semiconductor manufacturers need on a daily basis.

Intel claims hacker-proof design
Intel Corporation announced it 6th generation core processors at the Gamecon Congress 2015 (Aug. 5-9, Cologne, Germany); however they left out secret details about new vPro on-chip hardware important to business uses. Of the half dozen new hardware capabilities in the latest cores, the more important are 'Authenticate' and 'Unite,' both of which use on-chip hardware Intel claims is not hackable.

Early lung cancer detection
Early detection of lung cancer may become the norm, if the inexpensive table-top detector pioneered by National Taiwan University (NTU) is widely adopted by doctor's offices. The trick is that it can detect the malady when it is only five millimeters in size, which is typically in time for an easier cure by surgery. The product will be spun-off from the Electrical Engineering and Computer Science (EECS) department at NTU) to be licensed and manufactured by a third party such as Delta Electronics International (Singapore) Pte Ltd., according to Lab Director Wei-Cheng Tian.

February – 2016

Taiwan university pursues white LED
To make a white light emitting diode (LED) today, engineers either must use a white phosphor-coated package illuminated by a single color LED or mix red, green and blue LEDs together. However, if researchers at National Taiwan University (NTU) are successful, they will be able to produce white light from a single tiered-column LED at a single pixel. Scanning electron microscopy (SEM) images reveal a single uniform diameter column pixel will emit a single color (left) but by narrowing it at the top tier (right) two different colors can be emitted by the same pixel, and by adding a third even narrower tier a third color can be emitted, permitting a single pixel to emit red, green and blue (RGB) resulting in white light from a single pixel.

Toshiba expands memory factory
Toshiba Corporation said on 2 February that it will pay about $25 million (USD) to acquire land to expand its flash memory production in Japan's Mie prefecture. Toshiba (Tokyo) said it is acquiring 150,000 square meters (about 500,000 square feet) to expand production of its proprietary BiCS flash 3D memory. The company said it expects to break ground on construction by March 2017. Toshiba announced in January it would gut its semiconductor business, save for NAND flash. The company has decided to focus strictly on flash memory and nuclear energy as its core businesses. The move is considered a necessary step to return the Japanese giant to profitability.

Wearables to grow 48 percent
Wearables will achieve over 18 percent growth in 2016, with smartwatches taking the lead for earnings growth potential, reaching 274.6 million units in 2016, predicts Gartner. The group forecasts an 18.4 percent jump from 232 million units sold in 2015. The market is expected to drive $28.7 billion (USD) in revenue in 2016; of that total, $11.5 billion will come from smartwatch sales.

Are Windows phones going 'Zombie'?
Windows Phone doesn't have much of a future, based on the numbers highlighted in Microsoft's fourth quarter (2015) results. Sales of new handsets crashed precipitously, leaving Microsoft with a tiny slice of the global smartphone market. Microsoft says it sold about 4.5 million Lumia smartphones during the fourth quarter of 2015. That's down a whopping 57 percent in volume from the 10.5 million it sold during the fourth quarter of 2014. Revenue for its handset division crashed almost as hard, down 49 percent year-over-year. During a similar period Samsung shipped about 86 million devices and Apple sold 74.8 million iPhones.

Presto expands into Asia
Presto Engineering Inc. announced that it has significantly expanded its turnkey capabilities with the opening of two new manufacturing hubs and a world-wide logistics center in Asia. The company now offers a complete and comprehensive solutions for ICs, from GDSII hand-off (design output) to finished ICs shipped directly to end customers. Presto is targeting the latest high-speed communication, Internet of Things (IoT) and secured elements markets.

2015 chip sale slide not as bad as predicted
Global semiconductor sales totaled $335.2 billion in 2015, a slight decrease of 0.2 percent from 2014, according to the Semiconductor Industry Association (SIA) Trade Group. The final 2015 total was dragged down by a relatively poor month of December, when chip sales dipped to $27.6 billion, a decrease of 4.4 percent compared to November 2015 and a decrease of 5.2 percent compared to December 2014.

Intel's Moore's Law insights
Moore's Law has had a long life, but 'pure vanilla' CMOS process technology has run its course according to top Intel executive, William Holt, who spoke at the International Solid-State Circuits Conference (ISSCC). Holt did assert that new

techniques won't be in Intel's 10nm process that the company is now prototyping; engineers will stretch CMOS as far as possible. But new techniques such as tunneling FETs, ferroelectric FETs, spintronics, new III-V materials and processes not yet discussed publicly, or some combination, will take the industry below 5nm.

NXP reports autonomous driving progress
NXP Semiconductors has been working with Google on self-driving cars and had progress to report. Speaking in the plenary session of the 63rd ISSCC, officials said facsimiles of self-driving cars — "robots with wheels" — are already on the road. High-end vehicles can now speed down highways at up to 130 mph with minimal driver attention, said Lars Reger, chief technology officer of NXP's automotive group based in Hamburg, Germany. Technology that enables these previously impossible feats is actively working its way down-market, pointing to autonomous driving in the not-too-distant future.

Operators push narrowband IoT
Critics say that cellular network carriers, too preoccupied with 4G data-capacity issues, are neglecting their Machine-to-Machine (M2M) and Internet of Things (IoT) opportunities. But despite some skepticism, the cellular industry is aware that non-cellular players such as the LoRa Alliance and Sigfox are ratcheting up their bids for IoT dominance, using unlicensed spectrum as an edge in the emerging IoT network battle. But in response, cellular network operators will return to the Mobile World Congress next week to demonstrate a renewed commitment to Cellular IoT, recently agreed upon and designated as LTE Cat-M1 and LTE Cat-M2.

Micron increases 3D NAND production
2016 may be shaping up to be the year memory makers commit to upping 3D NAND production in a bid to replace its planar predecessor. Micron announced its 3D NAND technology is now available in multi-level cell (MLC) and triple level cell (TLC) products, and expects by the second half of 2016 that the majority of its NAND flash output to be on 3D NAND because designers are creating laptops, tablets and servers that need its increased capacity, performance and power.

Qualcomm unveils new wearable SoC
Qualcomm announced a thinner and lower-power family of SoCs that it has dubbed Snapdragon Wear 2100 that targets the emerging wearables market. The Snapdragon Wear platform is a full suite of silicon, software, support tools and reference designs. The company had previously pushed its mobile chips, such as the Snapdragon 400, into the wearable segment. This represents the first time Qualcomm has created a wearable-specific platform.

US says IoT is emerging intelligence challenge
The US Director of National Intelligence, James Clapper, delivered chilling remarks regarding the Internet of Things, noting there may come a day when spy agencies may tap into IoT for surveillance, network access and more if security concerns are not addressed. Threats surrounding the Internet of Things (IoT) may be looming larger than previously expected, with government spy agencies thrown into the mix along with cyber-criminals looking for new and faster ways to steal personal information.

DARPA puts itself on a diet
Some of the most world-changing technologies—such as the Internet—were spawned by the US Defense Advanced Research Project Agency (DARPA), but the pace of change has accelerated. Instead of concentrating on big, expensive, long-term projects, DARPA's new aim for its $2.9 billion budget will be smaller, more numerous and less expensive innovations that better address the crowd-sourced frontier facing manufacturers in a globalized economy.

EUV to get $500M research center
Globalfoundries and SUNY Polytechnic Institute will spend a total of $500 million (USD) over five years to create a new R&D center to accelerate the introduction of extreme ultraviolet (EUV) lithography into the 7nm process node and beyond. The move is the latest sign EUV will at long last make its way into production fabs, albeit probably not until 2018 or later.

New battery tech promises 10x charging improvement
Scientists from Stanford University and the Department of Energy's SLAC National Accelerator Laboratory have developed a method that makes silicon lithium-ion battery anodes a possibility. Such anodes could store 10 times more energy per charge than existing commercial anodes and make high-performance batteries smaller and lighter. Silicon particles swell to three times its normal size during charging, then crack and shatter. They also react with the battery electrolyte to form a coating that saps their performance. To alleviate these issues, the Stanford-SLAC team wrapped each silicon anode particle in a custom-fit cage made of graphene.

Samsung describes its 10nm SRAM
Samsung provided a look 'inside' its 10nm FinFET technology and an advanced 128 Mbit SRAM in a paper presented at the International Solid-State Circuits Conference (ISSCC). A version of the new 6T SRAM bitcell optimized for size is 38 percent smaller than a similar part made utilizing Samsung's 14nm process. It measures 0.040mm^2 compared to 0.049mm^2 for a version optimized for high current.

Security expert discloses Nissan vehicle hack
The Nissan Connect EV interface designed to remotely read out condition data and control systems information such as air conditioning in Nissan vehicles can be easily accessed and abused by unauthorized persons, says an industry consultant that studied the systems and reported the deficiencies to Nissan. The vulnerability was reportedly addressed shortly after the researcher made his discoveries public after attempting to contact the company privately.

Samsung unveils new memory tech
Samsung has doubled the capacity and speed of its Universal Flash Storage (UFS) memory, announcing what it said is the industry's first 256GB UFS aimed for use in high-end mobile devices at the 2016 Mobile World Congress in Barcelona, Spain. Samsung is now mass-producing the embedded memory based on the UFS 2.0 standard, the company said in a news release. To put its capacity into perspective, one 256GB UFS chip can store about 47 full HD movies.

IoT Networks expand at MWC
Ingenu, the LoRa Alliance and Sigfox announced expanded partnerships for their competing low-power wide area networks at the Mobile World Congress. The low power wide area networks are in a race to connect Internet of Things devices and systems at a time when cellular backers are accelerating their efforts to finish competing IoT standards.

SMIC to increase Capex in 2016
Semiconductor Manufacturing International Corporation (SMIC), China's largest foundry, said it planned to increase capital expenditures for 2016 by a third to $2.1 billion as it aims to capture strong growth

in the world's fastest growing chip market. SMIC is boosting capital expenditures from $1.57 billion in 2015 to increase its 2016 sales 20 percent from $2.24 billion in 2015, the company said on a conference call with analysts to announce results for the fourth quarter of 2015.

3 photonics pilot lines launch with EU funding
The Photonics Public Private Partnership has launched three pilot lines for the production of optoelectronic devices and circuits thanks to €35 million ($39 million USD) of European Union investment. The three manufacturing Pilot Lines are PIX4LIFE, MIRPHAB and PI-SCALE, which are aimed at health applications, mid-infrared imaging sensors for the detection of chemicals in gas and liquids and flexible OLED production respectively.

March 2016

Taiwan tops Korean fab capacity
Taiwan overtook South Korea in 2015 as the world leader in semiconductor fab capacity, according to market research firm IC Insights. Taiwan accounted for 21.7 percent of total capacity, edging out South Korea at 20.5 percent, according to the researchers. IC Insights counts capacity that chipmakers have overseas as belonging to the overseas location. The portion of fab capacity in other Asian locations, North America and Europe has dropped slightly while the rest of the world (ROW,) primarily Singapore, Israel and Malaysia, showed a small gain.

Analog Devices unveils IoT energy harvesting
To address the scarcity of energy in IoT applications, Analog Devices has unveiled a power management unit (PMU) for efficient energy harvesting called the ADP509x. The PMU converts harvested power down to the 16μW to 100mW range with sub-μW operation losses. Devices relying on energy harvesting often have to slowly accumulate enough energy to turn on, resulting in long delays before the device can start sensing, processing, and transmitting. This can result in missed data collection, slow operation, and poor user experience. The PMU solves these problems with a multiple-power-path design, which enables fast start-ups and smooth operation.

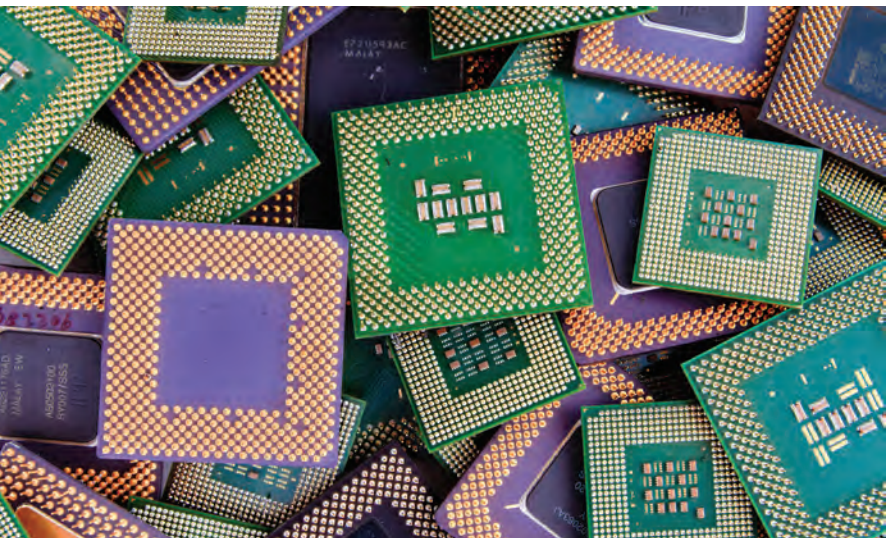
Chip sales off to slow start in 2016
Semiconductor sales started sluggishly across the board in 2016, due largely to softening demand and lingering economic headwinds, according to the Semiconductor Industry Association (SIA) trade

group. Chip sales declined on both a sequential and annual basis across all regions except China, where sales increased compared with January 2015. It marked the third straight month that China was the only region to post year-to-year growth in chip sales. Global chip sales totaled $26.9 billion in January, down 3 percent from the previous month and down 6 percent compared with January 2015, according to the sales numbers, compiled by the World Semiconductor Trade Statistics (WSTS) organization.

Dell expands into IoT market
Personal computer giant Dell is applying its proven quality, reliability, and global reach to the industrial PC market with the introduction of two purpose-built industrial PC families: the Embedded Box PC 3000 and 5000 series. The ruggedized, fanless PCs are part of Dell's IoT product portfolio and target Industrial IoT edge computing and gateway applications. Dell made the announcement at Embedded World.

Flexible battery, electronics market expands
Today's tiny market for thin-film batteries will grow to $470 million by 2026, according to a new report from IDTechEx. The news comes as proponents of all sorts of flexible printed electronics are wrapping up an annual meeting that attracted a record 650 attendees, showing their latest work.

Tablet shipments fall, but future looks better
Shipments of tablets are projected to decline in 2016 for the second consecutive year, according to market research firm International Data Corporation (IDC.) The firm blames the decline in sales of slate styled tablets on the lack of a killer application to spur upgrades.



VR shipments to top 50M/year by 2020
Virtual reality (VR) device shipments will total more than 50 million units by 2020, according to market analyst firm ABI Research. This equates to a compound annual growth rate of almost 85 percent. The dramatic increase is in part due to the relatively small market for the emerging technology in previous years.

Leti solves silicon resonator mystery
The mystery of why silicon resonators can never get close to their theoretical minimum frequency fluctuation has finally been solved by Leti, a division of CEA in Grenoble, France. Since the invention of the silicon resonator for MEMS devices, the source of frequency fluctuations has been a mystery attributed to a half-dozen or more causes by the same number of research organizations. While Jitter (phase noise) has long been attributed to thermal noise, no one previously identified the source of frequency variations, thus limiting the accuracy of the devices. By surveying the literature and designing experiments to discount all the other proposed sources of noise-related frequency fluctuation, Leti and colleagues have concluded that the only remaining possibility must be the answer: mechanical noise.

TSMC and ARM target 7nm at data centers
TSMC and ARM announced the next phase of their collaboration on leading-edge semiconductor process technology will be data center and networking chips that will drive their work on the 7nm FinFET node.

US spurs industrial chip market growth
The industrial semiconductor market is expected to grow at a compound annual growth rate (CAGR) of 8 percent between 2014 and 2019, when it is projected to be worth $59.5 billion, according to a forecast from market research firm IHS Inc. The firm predicts that increased capital spending and continued economic growth, especially in the US, will spur demand for industrial semiconductors. The firm lists commercial aircraft, LED lighting, digital video surveillance, climate control, traction and medical devices as the drivers for most of the global demand for industrial ICs.

Taiwan to build its first 300mm fab in China
Taiwan Semiconductor Manufacturing Company (TSMC), the world's largest foundry, said today that it has signed an agreement with the municipal government of Nanjing to finalize plans for its first 300mm wafer fab in China. TSMC announced the plan for the $3 billion fab investment in December last year.

IHS says wireless charging market is maturing
According to market research firm IHS, the wireless charging receiver market grew more than 160 percent in 2015 compared to the previous year. Annual global shipments reached 144 million units. Annual shipment volume is expected to top one billion units by 2020 and two billion by 2025, according to IHS' latest "Wireless Power Receiver Market Report."

April 2016

Smartphone sales growth contracts
Smartphone sales will grow at the lowest rate on record and PC sales will decline again in 2016, according to market research firm Gartner Inc. The Stamford, Connecticut (USA) research firm said it expects smartphone sales to grow 7 percent this year to reach 1.5 billion units. It would mark the first time that smartphone sales grew at less than 10 percent in a year, Gartner said.

Microsoft backs Sigfox cloud on IoT --
IoT network infrastructure provider Sigfox announced it will integrate the Sigfox Cloud with Microsoft Azure IoT Hub, enabling its customers to use data for real-time analytics. Currently operating in 14 countries including the US with more than 7 million devices in its network, Sigfox provides subscription-based low-power, wide-area (LPWA) communications dedicated to the Internet of Things.

A different 'flavor' of Intel CMOS
Intel's future processors at 10-nanometer and beyond will continue to use CMOS for cores, but the cores will be surrounded by novel circuit architectures using new materials that may extend Moore's Law indefinitely according to IEEE Fellow Kevin Zhang, vice president of Intel's Technology and Manufacturing Group.

'Internet of the Tire' now possible
Silent Sensors has moved to CPI's National Printable Electronics Centre in the UK to scale up the London-based company's patented tire sensor technology which has been developed to measure pressure and temperature. The technology is aiming to transform the way transport fleets currently track, monitor and manage tires, prompting some to call the new expansion of the technology across commercial fleets as the start of the 'Internet of Tires.'

Synopsys says nanowires will be next transistors
Synopsys Inc. claims that the FinFET is dying, III-V on silicon is dead before its time, and that silicon nanowire transistors are the solution that will take Moore's Law scaling all the way to single atom transistors around 2043.

Samsung backs next-gen OLED Pioneer
The Samsung Venture Investment Corporation has taken the lead in a $13.5 million Series A round of venture funding of Kyulux, Inc., a Japanese advanced materials startup that is commercializing the next generation of OLED display and lighting technology. Kyulux is a leader in developing and delivering an advanced OLED material technology, called Thermally Activated Delayed Fluorescence or TADF.

The technology is recognized as the third generation of OLED emitting mechanisms; it enables 100 percent internal quantum efficiency in OLEDs without using rare metals such as iridium that are required for high efficient emission in phosphorescence.

Freescale buy-out makes NXP largest auto chip vendor
According to the latest analysis by market watcher Semicast Research, NXP was the leading vendor of semiconductors to the OE automotive sector in 2015. Infineon passed Renesas Electronics to become the second largest vendor, with STMicroelectronics and Texas Instruments completing the top five. Semicast estimates that revenues for OE automotive semiconductors totaled $28.2 billion (USD) in 2015.

IBM details its plans for brian-like computing
IBM unveiled details about its future plans for TrueNorth, the company's neuromorphic mixed-signal chips that are based on the human brain. Its chip architecture, array of evaluation boards, reference systems and software ecosystem were described by their architect at the International Symposium on Physical Design 2016 (ISPD) in Santa Rosa, California (USA.) IBM expressed it aspirations for its brain-like computers, hoping they will become a household name for applications from ultra-smart Internet of Things (IoT) to similar chip based applications across industrial, commercial and consumer markets.

Chip market decline deepens
A chip market decline that began mid-2015 looks set to continue through the first quarter of 2016 at least, with falling markets on an annual basis in all geographies except China, according to figures from the Semiconductor Industry Association.

The global chip market was down on an annual basis in both Q3 and Q4 of 2015, according to World Semiconductor Trade Statistics (WSTS.) Some forecasters see the chip market continuing to contract throughout 2016 and into 2017; however, others call for a positive bounce as early as fourth quarter 2016.

Samsung says its 10nm DRAM could defy Moore
Rumors about the death of Moore's Law have been greatly exaggerated in recent years, and Samsung Electronics' mass production of what the company said is the industry's first 10nm 8Gb DDR4 DRAM chips shows scaling has yet to hit obstacles that cannot be overcome.

Samsung said it addressed DRAM scaling challenges using currently available argon fluoride immersion lithography without the use of extreme ultra violet equipment. The company began mass-producing 20nm 4Gb DDR3 DRAM in 2014, and said its 10nm class DRAM is in part the result of its process a step further.

TSMC Expects Surge in 2H 2016
Taiwan Semiconductor Manufacturing Co. (TSMC), the world's largest foundry, expects that it will emerge from an industry slowdown sometime during the second half of this year. Foundries have led growth in the semiconductor industry, yet have faced slowing sales resulting from excess IC inventory, poor demand for mobile and computing products and slumping tablet demand. TSMC said its year-on-year sales growth will probably not rebound until the latter half of 2017, driven by demand for high-end smartphones.

Qorvo buys ZigBee IoT specialist Greenpeak Technologies
Qorvo Inc., the RF chip company formed when RF Micro Devices and TriQuint merged at the end of 2014, has agreed to acquire fabless short-range wireless chip company GreenPeak Technologies NV (Utrecht, The Netherlands). Qorvo did not disclose terms of sale. GreenPeak was formed by the merger of Dutch company Xanadu Wireless and the Belgian company Ubiwave in July 2007. The company has specialized in ZigBee and Bluetooth chips for domestic applications and the Internet of Things. In 2015, GreenPeak celebrated the shipment of its 100 millionth ZigBee chip to the smart home market.

Russia and the US inch toward 'universal memory' materials
Researchers from the Moscow Institute of Physics and Technology (MIPT), the University of Nebraska (USA) and the University of Lausanne (Switzerland) have collaborated to grow an ultra-thin ferroelectric film on silicon, which they believe could become the favored 'universal' non-volatile memory material of the future while also serving as memristors in brain-line cognitive neuromorphic computers. The material is an ultra-thin (2.5-nanometer) polycrystalline ferroelectric film on silicon invented through a collaborative effort involving all three institutes.

Intel cuts 12,000, 11 percent of staff
In a sign that the PC is no longer a standard bearer of the silicon semiconductor industry, Intel Corporation announced its plan to cut up to 12,000 employees, 11 percent of its staff, amid a four-year decline in revenues and profits from PC chip sales. The news comes as Intel reported $13.7 billion revenues, down 8 percent from the previous quarter but up 7 percent from the same quarter last year. It made profits of $2 billion, a 43 percent plunge from the prior quarter but up 3 percent from the same quarter last year.

Harvest electricity from magnetism
With microwaves on the rise worldwide, generated by cell phone towers, mobile devices, Wi-Fi, Bluetooth, 5G and on and on, it is natural that researchers would investigate ways to harness these waves to generate energy. Scientists at the University of Utah have discovered a novel way of converting microwave energy into electricity in organic semiconductors. In the lab, they have demonstrated a novel effect—called the inverse spin Hall effect—which can convert magnetic spin current into electrical current using microwaves as their source of magnetic spin.

Carriers Clash over IoT
The Internet of Things is redrawing the competitive map when it comes to low-power wide area (LPWA) networks. Although under the surface of wider IoT talks, this is a looming battle for which operators, OEMs and chip makers are all gearing-up. A handful of service providers including Orange are rolling out IoT networks now based on the LoRa specification for unlicensed 800-900 MHz bands. Many other carriers are expected to start deploying IoT networks in 2017 using an emerging narrowband cellular standard based on LTE being developed by the 3GPP. Meanwhile, Sigfox, the first mover in this sector, is rolling out its own 800-900 MHz service worldwide. Several other players with their own technologies such as Ingenu are trying to deploy competing networks or license others to build them. The battle lines are just being drawn for a battle that will define how IoT data is transported, and who pays what for the privilege.

IoT security spending poised to skyrocket
Global enterprises and consumers will pump nearly $350 million into securing the Internet of Things (IoT)

this year, a figure that is set to grow exponentially in coming years as networks of connected objects expand, according to market research firm Gartner Inc. The researchers say that IoT security spending is set grow from about $232 million in 2014 to nearly $550 million in 2018. Gartner predicts that IoT security spending will expand further after 2020 once improved skills, organizational change and more scalable service options improve execution.

Apple iPhone sales drop 16 percent
Sales of Apple iPhones fell 16 percent, its first decline since the product line was introduced in 2007. The company forecast that 2Q 2016 will be weaker than previously expected, but remained bullish about the iPhone's long-term future , which continues to attract Android users and first-time smartphone buyers, especially in emerging markets.

MediaTek expects growing sales of smartphone devices
MediaTek, Qualcomm's largest competitor in the smartphone silicon business, said it expects to increase shipments during 2Q 2016 compared to the first quarter even as global growth in the segment has stalled for the first time.

Intel to exit mobile SoC business
As it proceeds with a massive restructuring plan announced earlier this month, Intel will exit the smartphone and tablet mobile SoC business by ending its struggling Atom chip product line. The discontinued products include those code-named SoFIA, Broxton and Cherry Trail. As Intel CEO Brian Krzanich explained in his latest blog, the chip giant's focus is now squarely on "Cloud, IoT, memory/ programmable solutions, 5G and Moore's Law."

Samsung counts on smartphone sales to boost bottom line
Samsung Electronics, South Korea's largest company, said an early release of its Galaxy S7 smartphone helped shore up first-quarter earnings while its semiconductor unit lulled and its flat-panel display business recorded a loss. Ironically, the phone would later be recalled (third quarter 2016) due to battery overheating, fires and property damage linked to the flagship Galaxy S7.

May 2016

Chip sales post slight increase
Global semiconductor sales ticked up slightly in March, showing sequential improvement for the first time in five months, according to the Semiconductor Industry Association (SIA) trade group. March chip sales totaled $26.1 billion on a three-month average basis, up 0.3 percent compared with February said the SIA, reporting sales figures from the World Semiconductor Trade Statistics (WSTS) organization. But total first quarter chip sales totaled just $78.3

billion, down 5.5 percent compared to the fourth quarter of 2015 and down 5.8 percent compared to the first quarter of 2015, the SIA said.

Google and Fiat Chrysler join forces
Search giant Google's plans for self-driving vehicles took a new turn with the announcement of a partnership with Fiat Chrysler (FCA), which will integrate Google's self-driving technology into 2017 Chrysler Pacifica Hybrid minivans to expand Google's existing self-driving test program. This is the first time Google has worked directly with an automaker to integrate its self-driving system (sensors and software,) into a passenger vehicle.

Graphene patterned at room temperature
Graphene is easily grown with chemical vapor deposition (CVD) on copper foil, but a simple way of etching circuit patterns and transferring them to a non-metallic substrate has eluded engineers. Now researchers at the University of Illinois (Urbana-Champaign) claim to have a one-step room temperature process for quickly patterning and transferring graphene circuits to flexible substrates using a simple shadow mask.

NXP is top auto chip vendor
Following its takeover of Freescale, NXP Semiconductor has been declared the leading automotive chip vendor for 2015 by market research firm Strategy Analytics. Researchers said they combined the companies' auto chip sales at $3.9 billion and attributed 14.2 percent of a $27.4 billion automotive semiconductor market in 2015 to NXP.

Researchers magnetize graphene
By inserting hydrogen atoms into the lattice of a graphene sheet, researchers from Spain and Egypt say an array of electrons in nanoscale domains encoded with magnetic spin can transform the material into a spintronic successor to silicon by inserting (doping) hydrogen atoms into specific

locations in the graphene lattice. By spreading out hydrogen atoms in an already tightly packed array of carbon atoms (graphene) spintronic circuits could be built at ultra-small nano- or even angstrom-scale (10 angstroms equals a nanometer), enabling a spintronic solution to replace silicon in transistor fabrication.

LEDs lead power electronics growth
Power semiconductor and supply vendors are poised to cash in on strong growth anticipated for LED lighting in coming years, according to the latest forecast from market research firm IHS Inc. The power semiconductor market for LED lighting is projected to grow to 24.3 million units in 2020, up from 7.3 million units in 2015, as LED lights command a larger proportion of the overall lighting market, according to IHS (Englewood, Colo.).

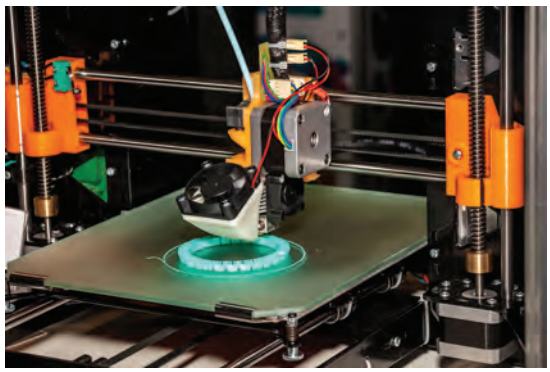
Suppliers feel heat from chip slowdown
Eight of the top 10 semiconductor suppliers saw declines in first quarter sales compared with the first quarter of 2015; several saw sales fall by 25 percent or more, according to a new ranking of chip vendors published by market research firm IC Insights Inc.

The Semiconductor Industry Association trade group said overall first quarter chip sales were down by nearly 6 percent compared to the first quarter of 2015.

Lam/KLA-Tencor deal faces additional scrutiny
Analysts are divided over whether the proposed $10.6 billion merger of Lam Research and KLA-Tencor corporations will go forward after the companies announced late Friday that the US Department of Justice (DoJ) had asked for more information about the deal. Analysts noted that a similar 'second request' for information was made in the Applied Materials/Tokyo Electron merger deal that the DoJ eventually squashed.

Foundry Capex forecast to rise 3 percent
Capital expenditures in the semiconductor industry are forecast to rise by 3 percent this year, led by foundries that are expanding to grab more business according to a report by market research firm IC Insights. "Intense rivalry in the foundry business will push capital spending in this semiconductor manufacturing segment to nearly $23 billion, which will break the previous record high level of $22.1 billion set in 2014," according to IC Insights senior market research analyst Rob Lineback.

HP releases new super-fast 3D printer
Hewlett Packard (HP) launched its long-heralded Multi Jet Fusion (MJF) 3D-printing technology for commercial-scale end-production, plus a supporting ecosystem, at the RAPID show in Orlando, Florida (USA). HP claims, and analysts who have witnessed the machine work and tested its performance agree, that MJF is at least 10 times faster than other 3D printing methods. The system could change the entire industrial market for making end-products through additive manufacturing (AM).



New 'Gigafactory' Opens in Germany
BMZ GmbH (Karlstein-Großwelzheim, Germany) has opened the first section of what will be Europe's biggest lithium-ion battery factory, called by some 'Europe's Gigafactory' who allude to Elon Musk's Gigafactory for producing batteries in Utah for electric vehicles (EV) and energy storage. BMZ plans to more than quadruple production areas in Germany by 2021.

Google may face €3B EC fine
The European Commission is planning to announce it will impose a record-breaking €3 billion (about $3.4 billion USD) fine on Google, according to the UK's Telegraph newspaper claiming EC officials plan to make the announcement prior to the summer holiday season. Google has been under investigation for seven years for allegedly using its search engine to favor results of its vested interests while excluding or minimizing options belonging to rival companies. Google has denied any unfair practices.

TI tops industrial chips market
Texas Instruments was the leading vendor of semiconductors to the industrial sector in 2015, placing it ahead of Infineon Technologies AG, according to analysis at Semicast Research. Semicast's industrial semiconductor vendor share analysis ranks TI as the leading supplier in 2015, with an estimated market share of 8.1 percent, ahead of Infineon with 6.8 percent, Intel (4.9 percent), STMicroelectronics (4.4 percent) and Renesas (3.8 percent).

Foundry sales indicate slump is not yet over
Taiwanese foundries TSMC and UMC, two of the industry's largest circuit makers, have both released sales figures showing that a chip market slowdown that lasted through the winter is not yet over. Both companies announced April 2016 sales that were significantly smaller than those they achieved in April 2015.

Imec announces IoT chip that supports 5 networks
The Imec research institute (Leuven, Belgium) has designed an SoC integrating support for five low power wide area (LPWA) networks for the Internet of Things. The chip supports five networks that run in the 780-930 MHz ISM band and are geared for smart meters or smart cities—802.15.4g/k, LoRa, KNX-RF, Sigfox and Wireless M-Bus.

Flexible electronics and OLED market could be $18B in 2020
According to IDTechEx Research's latest report, the plastic and flexible displays market will reach nearly $2 billion (USD) this year and will grow to $18 billion by 2020. The two main manufacturers of OLED displays have both announced large investments supporting capacity expansion. Samsung Display has said it plans to spend more than $3 billion between 2015 and 2017 for a new production line. Its rival LG Display is trying to lead the industry by committing over $9 billion for two new manufacturing plants.

FDSOI drives ST's automotive business
The fully-depleted silicon-on-insulator (FDSOI) chip manufacturing process championed by STMicroelectronics has become almost the default choice for digital manufacturing within the automotive and discrete group (ADG) business unit at ST, according to that group's senior executive, Marco Monti who is responsible for the ADG business unit.

ARM doubles-down on smartphones
ARM, the world's largest provider of reusable designs for silicon, expects its latest CPU and GPU cores to help revive demand for smartphones by taking games, virtual reality and augmented reality to a new level.

While some industry observers believe smartphone demand has peaked, ARM sees plenty of upside in a segment that has already doubled the number of personal computers in the marketplace. ARM

representatives said they believe enhanced capabilities enabled by their new devices and ongoing OEM product development can revive consumer interests.

June 2016

Xiaomi buys 1,500 Microsoft patents
Chinese smartphone manufacturer Xiaomi will purchase approximately 1,500 patents from Microsoft as it looks to expand its portfolio of intellectual property, according to a 31 May statement from the company. Wang Xiang, Xiaomi's senior vice president of strategic cooperation, said he believed the approach pointed to a long-term effort to grow the company's patent portfolio through collaboration and commitment to mutually beneficial relationships.

FDSOI garners EC IoT development support
Globalfoundries and STMicroelectronics are the leading chip companies in a European Commission collaborative research project that aims to create an ultra-low power platform for Internet of Things (IoT) applications based on 22nm FDSOI chip manufacturing process. The three-year project is led by Belgian research group imec and includes academic and commercial participants across the chip supply chain.

Military startup announces new neural processor
KnuEdge Inc. (San Diego), a company that has raised more than $100 million since it was founded in 2005, has announced a neuromorphic processor called KnuPath intended to accelerate voice recognition and other machine learning applications.

The processor is already in production and in use at customer sites, KnuEdge said. At the same time the company launched KnuVerse, its voice-recognition and authentication software that has been in use by military contractors for five years.

New imec Wi-Fi radio ready for IoT
Nanoelectronics research center imec along with the Holst Centre and Wi-Fi IP provider Methods2Bussiness have demonstrated a complete Wi-Fi HaLow radio. The low-power, long-range radio solution is claimed to use 10 times less power than state-of-the-art orthogonal frequency division multiplexing (OFDM) radios on the market. The radio's compliance with the recently amended wireless networking protocol (IEEE 802.11ah) ensures that it is optimized for IoT-related applications.

Fab Capex billings fall 13 percent in 4Q, rise in 1Q 2016
Global semiconductor capital equipment billings posted a year-over-year decline of 13 percent in the fourth quarter, led by precipitous declines of nearly 50 percent in Europe and more than 30 percent in the US and South Korea, according to the SEMI industry trade group. By 1Q 2016, semiconductor capital equipment billings totaled $8.3 billion in the first quarter, up 3 percent compared with the fourth quarter of 2015, according to SEMI. Tool sale bookings totaled $9.4 billion in the first quarter, up 5 percent from the previous quarter and down 2 percent compared with the year-ago quarter, SEMI said.

Qualcomm offers new connected car reference design
Fabless chipmaker Qualcomm has announced a reference platform for connected cars. Supporting wireless key technologies such as LTE, GNSS, Wi-Fi, DSRC/V2X and Bluetooth, the platform addresses the requirements of a broad range of applications with one sweeping blow.

China dominates smartphone supplier lists
China-based component suppliers represented eight of the top 12 positions for smartphone manufacturers in the first quarter of 2016, according to a report from IC Insights. Chinese companies Huawei, OPPO and Xiaomi were all top five suppliers. Although Samsung and Apple surpass all other companies in total smartphone shipments by a significant margin, both companies are forecast to have slight decreases in overall shipments by the end of 2016. Five of the eight Chinese companies ranked by IC Insights are expected to increase their shipments by at least 5 percent compared with 2015, even though most of their customers are within the PRC home market.

Most new Semi Fabs headed to China
At least 19 wafer fabs will start construction in 2016 and 2017 with most going into China, which is responsible for more than half of new fab starts, according to the SEMI industry trade group. As a result spending on chip making equipment, which had started slowly in 2016, will pick up and result in a market worth $36 billion this, up 1.5 percent on 2015, rising to $40.7 billion in 2017, up 13 percent year-on-year.

ASML to buy Hermes for $3.1B
ASML Holding NV will spend $3.1 billion (USD) to buy Hermes Microvision, Inc. for its e-beam inspection tools, shoring up the ecosystem for ASML's extreme ultraviolet (EUV) lithography systems, which it now says could be used for volume production of semiconductors starting in 2018. According to industry watchers, the deal is significant because after KLA-Tencor dropped its EUV mask inspection program, ASML had to find a way to keep an alternative EUV mask inspection/metrology tool alive to accelerate the market. This deal appears to be another step in that direction.

Solar Impulse 2 begins Atlantic crossing
The Solar Impulse 2 took off from JFK Airport in New York on 20 June and set a course across the Atlantic for Seville Airport in Spain. If it completes this leg of its mission, it will have taken a giant step closer to circumnavigating the globe using only the power of the sun.

Google launches Zurich AI research center
Google is diving deeper into artificial intelligence, with the company opening a dedicated machine learning research center in its Zurich office, the company announced on 16 June. The Google Research Europe center will focus on three areas: Machine intelligence, natural language processing, and understanding and machine perception.

Daimler plans to add EVs to its luxury lineup
Luxury carmaker Daimler intends to add an electric version to all of its model families and develop a specific vehicle architecture for battery-electric cars. Its existing GLC model will be expanded by a new

version that combines fuel cell with plug-in hybrid approaches. The company will invest €7 billion over the next two years.

Swiss team pushes perovskite efficiency
Michael Graetzel and his team at the Ecole Polyechnique Federale de Lausanne (EPFL) in Switzerland have found news ways to grow perovskite materials for larger-size solar cells, reaching over 20 percent efficiency and matching the performance of conventional thin-film solar cells of similar sizes. Their technique involves briefly reducing pressure during fabrication of the perovskite crystals, which enables higher efficiencies with a low cost manufacturing process.

Researchers create first 1,000 core processor
A team of engineering students from the University of California-Davis has designed a 1,000-core processor with 621 million transistors. The "KiloCore," presented at the 2016 Symposium on VLSI Technology and Circuits in Honolulu on 16 June is said to be the most energy efficient many-core processor ever reported. "To the best of our knowledge, it is the world's first 1,000-processor chip and it is the highest clock-rate processor ever designed in a university," said Bevan Baas, professor of electrical and computer engineering, who led the team that designed the chip architecture.

Fab tool book-to-bill remains at parity
The three-month average ratio of bookings to billings for North American semiconductor equipment vendors remained above parity for the fifth consecutive month in May, according to the SEMI trade group. The book-to-bill ratio for North American fab tool vendors in May was 1.09, meaning that $109 worth of orders were booked for every $100 worth of billings, SEMI stated. The SEMI book-to-bill ratio has remained above parity in each month this year.

'Brexit' ripples through tech community
A majority of voters in the UK on 23 June decided to leave the European Union, a move that had been opposed by a number of tech titans from IBM to Microsoft. Britain's exit from the European Union is expected to impact not only that country, but also the companies that do business there. While the stock market reacted negatively to the vote, and the British pound (GBP) fell in valuation against other major world currencies, those losses were largely regained in the months that followed.

July 2016

Micron announces job cuts
US-based semiconductor maker Micron Technology Inc. said on 30 June that it would cut an unspecified number of jobs as part of a series of cost-cutting initiatives in the face of challenging conditions in the global memory chip market. Micron said it expects to save about $80 million per quarter in the next fiscal year through a combination of job cuts and other unspecified measures.

Putting a new spin on MRAM
On the 20th anniversary of its invention at IBM Research, fabled nonvolatile 'universal' magnetic random access memory (MRAM) is getting an upgrade. IBM announced on 7 July that it would collaborate with foundry-giant Samsung in using a spin-transfer torque (STT) design on its MRAM.

FCC paves way for 5G
The US Federal Communications Commission (FCC) voted unanimously on 14 July to approve a set of rules allocating spectrum for 5G wireless broadband communications in the United States. The FCC's vote makes the US the first country in the world to approve rules for communications operating at frequencies above 24 GHz.

Berkley Lab sees path to increased perovskite efficiency
Berkeley Lab researchers at its Molecular Foundry and Joint Center for Artificial Photosynthesis used atomic force microscopy images of the surface of perovskite crystals to show a new path to much greater efficiency in the emerging technology. The study revealed that not all crystal facets are high performers, paving the way to increased perovskite efficiency by eliminating under-performing crystal facets.

Chip sales stagnate
Semiconductor sales showed a modest sequential uptick in May, but remained hamstrung by soft demand and global economic malaise, according to the Semiconductor Industry Association (SIA) trade group. "Most regional markets have struggled to gain traction in 2016, with the Americas falling well behind sales posted through the same point last year," said John Neuffer, SIA's president and CEO, in a statement.

"Sales of analog products were a bright spot in May, notching both month-to-month and year-to-year increases."

Imec and ARM to collaborate on 7nm design
Processor intellectual property licensor ARM Holdings plc (Cambridge, England) has signed on to the INSITE collaborative research program on design at nanoelectronics research institute IMEC (Leuven, Belgium). Developers are now faced by a large number of potential design choices at 7nm including: the required number of lithography exposures, device architecture such as FinFETs or lateral nanowires, the local interconnect scheme, cell architecture and the metallization scheme.

US PC sales show surprising strength
PC shipments increased in the second quarter compared with the second quarter of 2015, the first year-over-year increase for the US PC market after five consecutive quarters of declines, according to market research firms. But the surprise US growth was not enough to offset declines elsewhere, as global shipments contracted for the seventh straight quarter, according to Gartner Inc. and International Data Corp. (IDC).

Leti plans startup accelerator
Philippe Ruffin, who is responsible for startup programs at Leti, disclosed the plan at the Leti Innovation Day on IoT reliability and security, held in Lyon, France, in June. Ruffin said there are more than 150 startup accelerators in Europe but that none are devoted to science and technology and that Leti wanted the IVA to fill that gap with a plan to support 10 companies in 2017 and for that number to rise to 20 by 2020.

TSMC to adopt EUV at 5nm
Taiwan Semiconductor Manufacturing Co. (TSMC), the world's largest foundry, said it will fully implement extreme ultraviolet (EUV) lithography to make 5nm chips by the end of this decade.
"We estimate that EUV will be a cost-effective tool for high-volume manufacturing by 2020, in time for our 5nm ramp," TSMC Co-CEO Mark Liu said at an event to announce the company's second-quarter results. "We plan to use EUV lithography extensively in 5nm to improve density, simplify process complexity and reduce cost."

Leti unveils new 3D 'network-on-chip'
Leti, a CEA Institute, came to SEMICON West (San Francisco) this week to unveil its second generation 3D Network-on-Chip (3D-NoC) technology. Using its new 3D-NoC technology, Leti researchers have developed an on-chip communications system that it says substantially boosts computing performance while reducing energy consumption. This was accomplished by stacking chips in a single enclosure, or by placing the chips side by side on a silicon interposer.

Softbank announces £24.3 bid to acquire ARM
ARM Holdings plc has agreed to be bought by Softbank of Japan for £24.3 billion (about $32.25 billion USD) in an all-cash deal. As part of the deal Softbank has pledged not to change ARM's successful partnership business model, culture and brand. It has also said it will keep ARM's headquarters in Cambridge, England, and to increase employment in the UK from approximately 1,700 to approximately 3,000 over the next five years.

STM returns to profitability
STMicroelectronics second quarter revenues totaled $1.70 billion compared with $1.76 billion in 2Q15. The company made a net profit of $23 million in 2Q16 compared with a net profit of $35 million in 2Q15. The company lost $41 million in the previous quarter. CEO Carlo Bozotti told analysts on a conference call that ST was now well positioned to show year-on-year growth in the second half of 2016.

Daimler demos semi-autonomous bus
It has no mirrors or other typical driving aids, yet its dozens of forward- and backward-looking cameras, long- and short-range radars and high-precision GPS create an exact virtual image of surroundings on Daimler's latest brainchild—a nearly autonomous 'Future Bus' that will roll along a 20-km track (about 12.5 miles) through the city traffic of Amsterdam; driver not required. The technology will enter series production early in the next decade, the company says.

Sensors to dominate wireless markets by 2021
Wireless sensor nodes and connected peripherals will outnumber hub devices such as smartphones and PCs in 2016 and increase their holding through 2021, according to ABI Research. The market research firm

reckons sensors and peripherals will be 65 percent of an installed base of 47 billion units by then, double the 2016 level.

ASML reports EUV progress
ASML announced it received orders for four extreme ultraviolet lithography systems in its latest quarter and anticipates selling a dozen EUV systems next year. The report fueled expectations the long-delayed scanners finally will be ready for mass production in 2020, probably for 5nm chips. Optimism for the new timeline was tempered by concerns the systems used to print lines as fine as 13nm may need a major optical upgrade for work on nodes beyond 5nm.

Vitamins fuel new energy storage system
Researchers at Harvard University (Cambridge, Massachusetts) have identified a new class of high-performing organic molecules inspired by vitamin B2 that can safely store electricity from intermittent energy sources like solar and wind power in large batteries. The development builds on previous work in which the team created a high-capacity flow battery based on a food additive called ferrocyanide instead of metal ions such as lithium. The work resulted in high-performance, non-flammable, non-toxic, non-corrosive, and low-cost chemicals that could enable large-scale, inexpensive electricity storage in flow batteries. Although research and development continues, the Harvard work points to trends away from hazardous and potentially explosive high capacity battery technologies.

ADI to acquire Linear Tech for $14.8B
Analog Devices Inc. (ADI) will acquire rival Linear Technology Corp. in a cash and stock deal worth about $14.8 billion, the companies said on 26 July. The deal, which remains subject to stockholder approval, would bring together two analog semiconductor powerhouses and would be the latest in a string of blockbuster semiconductor deals over the past few years. Combined, the two firms held about 9 percent of the analog IC market in the first quarter, according to IC Insights.

WD and Toshiba claim first 64-layer 3D NAND memory
Disk drive vendor Western Digital Corporation and Toshiba Corporation claim they have developed the world's first 64-layer 3D NAND memory and that it is in pilot production at joint-venture factories at Yokkaichi, Japan. The new NAND memory is based on so-called BiCS3 (bit cost scalable) technology developed by Toshiba and came to Western Digital in its acquisition of SanDisk Corp. in May 2016.

Spray-on perovskites show promise
Photovoltaic (PV) materials that can be sprayed on like paint have been explored before, but researchers at the University of Virginia and Cornell University say they are on the trail of a new perovskite combination that can be commercialized within the next few years.

Self-assembling metal halide perovskite thin film solar cells have been sought for several years and research continues for a means to maintain high efficiency and resistance to environmental factors while keeping costs low.

August 2016

EPC says data proves GaN FET reliability
Gallium nitride power FET maker Efficient Power Conversion (EPC) has published a reliability report documenting GaN technology reliability after millions of device hours of stress testing, and based on analysis of all field returns. EPC's Phase Eight Reliability Report documents a combined total of over 8 million GaN device-hours with zero failures. The report examines, in detail, the stress tests that EPC devices are subjected to prior to release as qualified products and analyzes the physics of failure.

Renesas to exit microwave business
Renesas Electronics announced on 2 August that it will discontinue its microwave device business.

The company plans to stop the production and supply of microwave devices, shutting down the business in the summer of 2018. According to Renesas, its microwave device division has been pulling back from product development for some time. Renesas explained that although the business remains profitable, it has not invested in new product development for some while and feels many of its key products will be incorporated into future system LSIs.

FEI ships 1,000th Helios System
FEI (now Thermo Fisher Scientific) announced that it achieved a milestone of the 1,000th Helios™ DualBeam system shipped since the product family was introduced in 2006. The 1,000th system was manufactured in their Brno plant and was shipped earlier in August to a customer utilizing the system for advanced failure analysis on sub-20nm semiconductor devices.

MediaTek faces chip shortage
MediaTek, Qualcomm's largest competitor, said it is unable to meet demand for 3G and 4G smartphone products because it underestimated the supply of chips needed from its foundry partners. Demand has been better than the company expected earlier this year. MediaTek Chief Financial Officer David Ku said that by 4Q 2016, it would not be able to fulfil all its order, and was addressing the situation with suppliers and customers alike.

New Jeep vehicles still vulnerable
When automotive security researchers Charlie Miller and Chris Valasek took the stage ($ August) at the Black Hat conference in Las Vegas, they outlined new methods of CAN message injection. Earlier the duo had successfully exploited a Harman-made 'head unit' that offers a Wi-Fi hotspot to get into the vehicle's network. The latest invasion exploited the car's unprotected cellular connection via the Sprint wireless network, but had to physically be connected to the car's systems.


3

largest chipmakers will boost Capex
Chipmakers Intel, Samsung and TSMC are likely to increase capital expenditures during the second half of this year while the rest of the semiconductor industry tightens its collective belt, according to market research firm IC Insights. Analysts said in a report that the companies will probably spend $20 billion for Capex, representing a 90 percent increase from the first half of 2016.

IBM 'lab-on-chip' detects cancer
IBM Research (Yorktown Heights, NY) has designed a microfluidic 'lab-on-a-chip' that can separate biological particles down to sizes as small as 20 nanometers. If successful, the chip will make it possible to detect cancer markers before a tumor has even started to grow. The IBM process is based on the idea of ultra-fine filtration with the aim of finding human cell components that are markers for the disease before it has a chance to take root within a human body.

SMIC raises 2016 sales target
Semiconductor Manufacturing International Corp. (SMIC), China's largest foundry, raised its aim for sales this year to the mid-to-high 20 percent range based upon unexpectedly strong demand. Three months ago, SMIC forecast a 20 percent increase in its 2016 sales from $2.24 billion in 2015. Part of SMIC's optimism stems from its acquisition of LFoundry. In June, SMIC agreed to acquire a 70 percent stake in LFoundry, which specializes in analog products for automotive, security and industrial applications, for about $55 million. The deal is SMIC's first expansion of manufacturing outside China.

Laser slicing can slash SiC costs
Japanese ingot processing equipment manufacturer DISCO Corporation has unveiled a new laser-based technique to slice wafers out of a SiC ingot, producing 50 percent more wafers through reduced material losses while slashing production times by a factor of six. While today's wafer production typically involves the use of multiple diamond wire saws, taking several days to slice through an ingot while producing considerable material waste, Disco's KABRA process is not only much faster but also requires less wafer processing steps since it leaves no micro-undulations on the surface, as do wire saws.

Renesas sets sights on Intersil
The Japanese economic newspaper Nikkei reported early Monday that Renesas Electronics is, '…in the final stages of negotiations to acquire Intersil.' Neither company would confirm or discuss the article. The impetus of the deal is believed to be Renesas' desire to reinforce its position in the global automotive chip market.

ARM investors OK SoftBank acquisition
Shareholders of ARM overwhelmingly approved its sale to SoftBank (Japan) on 30 August in a London meeting. In order to allay concerns and political backlash, the Japanese telecom giant promised the UK government that it would at least double ARM's workforce in the UK over the next five years. Softbank also made a commitment to keep ARM's headquarters in Cambridge, and retain its partnership-based business model and culture.

EU sends Apple a $14.5B tax bill
The European Commission has ruled that over several years Ireland has granted unjustifiable tax benefits to Apple worth up to €13 billion (about $14.5 billion USD), which the US computer company must now pay back to the Irish state — plus interest. The ruling is that Ireland allowed Apple to organize its business in a way that allowed it pay substantially less tax than other businesses and that this is illegal under European Union state aid legislation. Apple has protested the decision and said it plans to appeal.

September 2016

iPhone 7 uses Broadcom chips
Broadcom Ltd. will get a bigger bite of the Apple iPhone 7 and can't get enough chips to handle the demand for 4K set-top boxes or data center switches. Nevertheless, the sees the overall semiconductor industry as stable, not booming. The outlook came as Broadcom reported revenue of $3.792 billion, up 7 percent from the prior quarter and a net loss of $315

million, according to generally accepted accounting procedures (GAP).

Sequans claims 'big lead' in IoT chips
With the promise of growth in the cellular IoT market, Sequans (Paris, France) is coming to Las Vegas this week for CTIA's Super Mobility Week to unveil what the company calls, '…the world's first purpose-built Cat M1/NB1 chip.' While competitors such as Qualcomm, Intel and Altair (now owned by Sony) are still working on their cellular band Cat M1 and NB1 chips, Sequans CEO Georges Karam boasted that Sequans is the first in the industry to sample a Cat M1/NB1 chip, called "Monarch."

IC Insights cuts IoT chip market forecast
Although few nameplate products have had time to represent IoT consumer applications, IC Insights just released an updated IoT semiconductor market report in which it has trimmed back its own forecast for Internet of Things products. According to the researchers' latest report, semiconductor sales for IoT system functions in 2019 are now expected to reach $29.6 billion that year instead of $31.1 billion.

Dual lens iPhone is smartphone first
Apple's newly iPhone 7 Plus, with a dual-lens camera designed to provide both telephoto and deep depth of field typical of digital single lens reflex (DSLR) cameras is likely to set a new industry standard for image quality never before imagined for mobile photography. Although unlikely to completely replace DSLRs, Philip Schiller, senior vice president of worldwide marketing at Apple, boasted during the Apple event Wednesday that, '…this is the best camera ever made in any smartphone.'

Tricky transistor beats Moore, says developers
Researchers at Zvi Or-Bach's startup Zeno Semiconductor (Sunnyvale, California) are claiming a power-boosting breakthrough can increase drive by 2x and power-delay by 4x compared with the average 30 percent improvement seeking an advance to the next Moore's node. The key is a new transistor architecture

that could operate as either a low-power metal oxide semiconductor field-effect transistor (MOSFET) or could switch to a high-power bipolar-junction transistor (BJT). The discovery was revealed at the European Solid State Device Research Conference (ESSDRC 2016, Lausanne, Switzerland.)

Linde Opens leading edge Taiwanese R&D facility
Linde Group, one of the world's largest suppliers of specialty gases for the semiconductor industry, has established what it says will be a world-leading R&D facility in Taiwan. The company has invested approximately $5.6 million to establish the new R&D Center for its Asia Pacific region customers with a state-of-the-art analytical and product development laboratory in the central-island city of Taichung. Linde has signed a collaboration agreement with Taiwan's Industrial Technology Research Institute (ITRI), which will contribute 10 of its personnel as part of the project.

Questions remain for Tesla after fatal 'autopilot' crash
A fatal accident in China thrust Tesla's transparency into sharp focus this week, posing fresh and daunting questions as to the safety of Tesla's 'Autopilot' feature. New reports surfaced this week in China about a crash that killed a 23-year-old occupant while driving a Tesla Model S in Handan, a city about 300 miles south of Beijing, four months before Joshua Brown died in Florida, also in a Tesla Model S on Autopilot.

Amazon Echo leads voice control revolution
Whether they are called smart microphones, virtual digital assistants or personal home robots, Amazon Echo-like products are on the rise. The second generation Echo Dot, whose price has been just dropped from $89.99 to $49.99 compared with its first generation version, will be on sale in the US market next month. The products have opened a new Internet of Things market enabling device vendors to compete on better audio quality in voice capture, higher mic audio resolution, more sophisticated background noise filtering, better far field detection, and unflappable connectivity.

Car makers and telecom operators move towards 5G
In a cross-industry alliance, Audi, BMW and Daimler along with telecommunications equipment providers Ericsson, Huawei and Nokia as well as semiconductor vendors Intel and Qualcomm will bundle their research and development resources to evolve, test and promote communications solutions around 5G standards for connected mobility. The '5G

Automotive Association' was announced to develop, test and promote communications solutions, support standardization and accelerate the commercial availability of such solutions is a new visible indication that both groups see huge potential in advanced mobile connectivity.

Reports claim Qualcomm looks to buy NXP
Qualcomm is in talks to buy NXP Semiconductors for more than $30 billion, according to multiple press reports including a Wall Street Journal article. The reports have driven NXP's stock up about 15 percent to an estimated market capitalization of about $33 billion (USD). If the deal goes ahead, it could become one of the largest in a historic period of semiconductor consolidation. NXP itself completed its merger with Freescale Semiconductors in December 2015 that it valued at $40 billion.

October 2016

New approach cuts deep learning in half
Researchers at the University of Massachusetts (UM) have invented a diffusive-memristor that more accurately models the synapses of a human brain by selectively forgetting seldom used information, while allowing vital information to be locked-in no matter how little it is accessed. UM Professor Joshua Yang leads a team that claims to have solved the problem with their diffusive memristor, which does everything that a regular memristor does, plus emulates 'forgetting' old information no longer needed.

Biometrics is replacing passwords
FotoNation (San Jose, California) has developed a suite of biometrics recognition algorithms aimed at eliminating the need for smartphone passwords with face- and iris-recognition. FotoNation has been licensing its 'red eye' reduction algorithms used by Nikon and nearly every other camera and smartphone maker. The company believes its new biometric algorithms are therefore an easy-sell since the techniques are based on their highly successful photo enhancement programs.

FD-SOI makes 1st in-product appearance
Without any visible end products to justify its proponents' ultra-low-energy promise, FD-SOI has struggled to overcome skepticism regarding uptake and the technology's readiness for consumer applications. The wait is over. Sony is using the technology in a new smart watch built using a 28nm Fully depleted silicon on insulator (FD-SOI) process. The new watch was rolled out in China in September by Huami, Xiaomi's sub-brand.

Google debuts first consumer products
October the 4th was a big day for Google: the web search engine giant launched its first OEM products including two smartphones, a smart speaker, a virtual reality headset and a Wi-Fi access point. Its Pixel smartphones and Home smart speaker are the containers for its machine-learning Assistant, the company's most strategic product of all.

Magnetic storage tape still does the job
Despite the advent of cloud computing and a plethora of successful, high speed memory technologies that succeeded it, magnet tape storage perseveres as a mainstay technology used in many industries, and financially, it still doesn't make sense to replace those systems when they can no longer replace the tape. It's a niche market, but one that Solid State Disks Ltd. sees as being viable for the foreseeable future. The family-run business based in Reading, United Kingdom goes back as far as 1982, when the company was founded to provide 19-inch disks to OEM customers, as well as spare heads and media.

FTC study says nuisance lawsuits affecting innovation
A study of so-called 'patent trolls' from the US Federal Trade Commission is raising fresh calls for Congress to take further actions to reform the patent system. The study provided details about the types of companies that acquire and assert typically computer and communication patents — especially in the wireless sector — against a widening set of defendants. Those involved in the majority of cases were litigation patent-assertion entities (PAEs) held small portfolios often with fewer than ten patents. They filed 96 percent of the patent suits in the study and accounted for 91 percent of the licenses but only 20 percent of the total revenue, about $800 million. In the broader, regular semiconductor market, these portfolio

PAEs accounted for only 9 percent of the reported licenses in the study, but generated 80 percent of the revenue or about $3.2 billion.

LAM/KLA merger failure cools M&A fever
In striking down a proposed $10.6 billion deal to merge Lam Research and KLA-Tencor, regulators sent chip makers a message that they will have to rely on vendor collaboration to optimize next-generation processes. The ruling is expected to put a chill on any other larger merger deals in the capital equipment sector despite an historic period of consolidation in the overall semiconductor industry. The deal put together nearly a year ago aimed to create a company with unique abilities to make and measure chip building processes. While multiple companies compete in the deposition and etch systems that Lam supplies, KLA maintains a dominant market share in metrology that regulators said would not be fair to combine with Lam's leadership positions.

TSMC grows its share of foundry business
Taiwan Semiconductor Manufacturing Co. (TSMC) increased its share of the foundry business to 55 percent this year on better than expected demand for smartphones during the third quarter. "In the third quarter, we gained market share across most technology nodes," according to TSMC Co-CEO Mark Liu, speaking at a Taipei event to announce the company's quarterly results. TSMC, which counts Apple as its largest buyer, said that sales growth was driven by its mobile customer's new product launch. TSMC makes the A10 processor for Apple's latest smartphone, the iPhone 7 Plus, introduced in September.

1nm transistor demonstrated
Carbon nanotubes have been used in experimental transistors for decades, but always as the channel for the transistor. Scientists at Lawrence Berkeley National Laboratory (Berkeley Lab) in Berkeley, California have now pioneered the use of carbon nanotubes as the gate, allowing them to claim the world's smallest transistor. According to Berkeley Lab, the laws of physics had been thought to set five-nanometers as the smallest size possible for transistors, but by going to carbon nanotube gates, they have been able to break that limit, according to Professor Ali Javey. His demonstration shows that by changing the material mix, Moore's Law can be extended further than was previously thought.

Largest US carriers and chip makers push for LTE powered IoT links
The two largest US cellular carriers and five module makers said they will use a Qualcomm chip implementing the latest low-power LTE standards for the Internet of Things. The news shows the cellular IoT standards should get strong market penetration in 2017. AT&T will use the Qualcomm's MDM9206 in a San Francisco pilot of Cat-M1 that it expects to be the start of a national service roll out in 2017. Verizon will use the chip in its Thingspace service. Cellular module makers Quectel, Telit, U-Blox, Simcom and Wistron NeWeb Corp. said they will use the chips in modules supporting Cat-M1 and NB-1 services.

Did processor cause Samsung Note 7 meltdown?
It's far from clear what exactly caused Samsung Note 7 to catch fire at this point. Samsung isn't talking until after it finishes its own investigation. But a new report by the Financial Times quoted an unnamed source who has spoken with Samsung that the company, emerged Wednesday that the culprit might not be the lithium-ion batteries themselves, which Samsung initially suspected. Rather, the problem might reside in the underlying technology -- tweaks made to the processor in the smartphone to speed up the rate at which the phone could be charged.

DRAM pushes up chip forecast in 2016
The market for integrated circuits could eke out 1 percent revenue growth this year and 4 percent in 2017, thanks in part to a rebounding DRAM market, according to the latest report from IC Insights. The market watcher estimates unit sales will grow 6 percent this year, up from a previous forecast of 4 percent unit growth and a 2 percent decline in revenues. The upbeat news comes four months after the Semiconductor Industry Association said it expected a 2.4 percent sales decline this year, following similar predictions from a handful or market researchers. After falling "quite a bit in the last 18 months," DRAM prices are stabilizing as demand from smartphones and PCs rise and memory vendors cut

back on capital spending, said Bill McClean, president of IC Insights.

The IoT gets new network provider
A new low power-wide area (LPWA) network for the Internet of Things joined the growing set of options. M2M Spectrum Networks will use over its licensed sub-GHz spectrum in the US technology from Link Labs. Over the next two years, M2M is expected to purchase as many as 10,000 base stations implementing Link Labs' variant of LoRa called Symphony Link. Separately, Link Labs is gearing up a new IoT networking product line based on LTE-M. A handful of startups are rolling out LPWA networks worldwide for IoT including Sigfox, LoRa and Ingenu. Cellular providers are countering with low power versions of LTE going into trials next year.

Qualcomm Targets NXP for connected world foothold
Qualcomm Inc. announced Thursday a definitive agreement to acquire NXP, creating a combined company with annual revenues of more than $30 billion. Qualcomm will offer $110 per share in all cash transaction — a premium of 11.5 percent to NXP Semiconductor's Wednesday's close — for a total enterprise value of approximately $47 billion. Worth roughly $39 billion excluding debt, the agreement would represent the biggest chip deal ever, exceeding Avago's $37 billion agreement to buy Broadcom Corp.

New 'fireproof' lithium-ion batteries?
Lithium ion batteries are indispensable as energy source for millions of electronic devices as well as for electromobility. Their drawback: They are not overly safe in that they are easily inflammable. In a joint research effort, the University of Ferrara and the Karlsruhe Institute of Technology (KIT) have found a way to tame the batteries. The problem with existing lithium ion batteries is that they are utilizing volatile organic solvents with a rather low combustion point. Instead of the commonly utilized organic material they employed inorganic salt that had been liquefied at room temperature, and could significantly improve the batteries' resistance to fire.

November 2016

SMIC to build South China's first 300mm fab
Semiconductor Manufacturing International Corporation (SMIC), China's largest foundry, said it is proceeding with plans to build South China's first 300mm fab at an existing facility in the city of Shenzhen, near Hong Kong. The company said in a press release that the new fab is aimed at meeting demand for internet of things (IoT) chips using mature technology and some second-hand equipment for production. Construction is scheduled to start by the end of 2016, and production will ramp up by the end of 2017.

Broadcom plans to carve up Brocade in $5.9B acquisition
Just before Thanksgiving, Broadcom Ltd. chief executive Hock Tan is at it again, carving up an appetizing company with the skill of a private-equity chef embedded in a semiconductor company. Under the deal, Broadcom will round out its storage networking business with Brocade's Fiber Channel switches and sell its Ethernet networking business for an expected $1-2 billion. The system-level switches are expected to add nearly $1 billion to Broadcom's annual revenues and bolster its overall profit margins by as much as 5 percent.

Chip forecast rises through 2017
Another market watcher is raising its forecast for growth in semiconductors this year and into 2017. International Business Strategies (IBS) predicts a 0.2 percent increase in chip sales this year and a 4.6 percent rise next year. At an industry event in January, Handel Jones, chief executive of IBS, was the bear, predicting a 1.5 percent decline while Bill McClean of IC Insights was the bull, forecasting four percent revenue growth in 2016. Now both are roughly in agreement. The two analysts (now) point to similar dynamics of increasing memory prices and greater memory content in smartphones from growing Chinese suppliers.

Siemens to Buy Mentor for $4.5B
Siemens on Monday agreed to buy Mentor Graphics in a $4.5 billion deal. Siemens, which has been increasing its industrial software capabilities lately, said it sees Mentor's electronics IC and system design, simulation and manufacturing solutions as critical for developing "smart" and "connected" products — including autonomous vehicles. Mentor helps companies design and manufacture circuit boards and semiconductors with specialist software, notably for the aerospace and automobile industries. Siemens is Europe's largest engineering conglomerate, best known for its power systems. But the company is keen on playing a big role in the so-called *fourth* industrial revolution — big data and IoT

SMIC expects sales records to continue
Semiconductor Manufacturing International Corp. (SMIC), China's largest foundry, said it expects strength in its business to continue as it rides a wave of demand in China. The company forecast in a conference call to announce its third-quarter results that sales in the current quarter will rise as much as 7 percent from the record $774.8 million in revenue it posted during the July to September period this year.

China support IoT interop Plan
China has agreed to align any national standards for the industrial Internet of Things with the work of the manufacturing dominated Industrial Internet Consortium (IIC). The deal is the latest of a handful that the IIC hopes to knit into a global framework for IoT. The IIC signed the memorandum of understanding with an academy under China's Ministry of Industry and Information Technology on Wednesday. It already struck similar deals with German officials responsible for its Industrie 4.0 initiative as well as officials in Japan with a similar program.

Samsung makes $8B bid for connected car leader Harman -- Samsung will pay $8 billion for the US car technology group Harman. The Korean electronics giant sees the Harman deal gives them the dominance in a growing automotive tech market in one fell swoop. Today, carmakers and tier ones face an unprecedented level of challenges in dealing with the complexity in vehicles' system designs and security that needs to be placed at the heart of the connected vehicles. Harman is best known for its connected car technology through its high-end multimedia, navigation and visual display systems. Lately, Harman has been beefing up its automotive security portfolio by buying up a suite of automotive security technology companies. Harman's group sales were $7 billion during the 12 months to October and its order backlog as of June was $24 billion, according to the company.

Researchers claim optical computing breakthrough
All-optical computers using photons traveling at the speed-of-light in theory could make the electronics we know today obsolete. All the subsystems are in place, but one key obstacle remained — optical losses. Now the Moscow Institute of Physics and Technology (MIPT) claims it may have cleared that last hurdle. According to the journal, Nature, a new method that can compensate for losses just by carefully designing dual waveguides to match the wavelength of the light traveling through them. By doing so, the traveling waves can reinforce each other along the way, thus introducing a slight gain that compensates for the normal losses.

Imec claims new 1st in photonic circuits
Photonics may be the future of the post-Moore's Law era, with electronic design automation (EDA) tools already available to make the transition. Now IMEC research institute (Leuven, Belgium) claims that it has demonstrated sub-micron spin-wave devices (SWDs) integrated with state-of-the-art FinFETs, announcing it this month at the Annual Conference on Magnetism and Magnetic Materials 2016.

'Dr. Watson' may see you
IBM's Watson has identified cases of heart disease previously undiagnosed by human inspection of ultra-sonic imaging, clinical tests and case notes, according to the company at a Conference on Medical Image Computer Assisted Intervention (MICCAI, Athens, Greece). As a result, IBM is offering five new Watson modules to doctors aimed at improving the accuracy of diagnoses for stroke, mammography, radiology and cancer. So far, IBM has proved the concept by using Watson to inspect diagnoses, echocardiograms and ultra-sonic images of past patients. By training on a large database of correctly diagnosed cases — including unstructured data such as doctor's notes — Watson was able to automatically spot 25 percent more heart disease from a dataset sample of cases it had never before seen, according to IBM Fellow Dr. Tanveer Syeda-Mahmood.

Coatings can stop Li-ion battery fires
The exploding battery debacle of Samsung's Note 7 eventually led to the phones recall and the ignominy of having one of its products treated as an object of scorn. It was recalled, replaced, recalled again and now permanently cancelled. But yet another company said it could have all been avoided if Samsung had only used a product like theirs for eliminating the possibility of a lithium-ion related fire. Forge Nano (Denver, Colo., formerly PneumatiCoat Technologies), said that if their nano coating had been used the coatings would have boosted the breakdown temperature of flammable electrolyte Li-Ion batteries, putting it way far into the safe zone for nominal environmental usage. The key, according to Forge Nano (Denver) is nano-pattern atomic layer deposition (ALD).

Leti claims 1st qubits on 300mm Si Wafer
As major electronics laboratories worldwide rush to invent a complementary metal oxide semiconductor (CMOS) quantum computer, Leti lays claim to the first quantum bit (qubit) fabricated on a standard 300mm CMOS line. Leti (Laboratoire d'électronique, Grenoble.) It planned to present all the details at the International Electron Devices Meeting (IEDM 2016, Tuesday, Dec. 6) in a paper titled, SOI Technology for Quantum Information Processing. "We have proved the concept of using a standard CMOS line to fabricate the quantum-dot qubits for a future quantum computer," Maud Vinet, Leti's advanced CMOS manager told EE Times in an exclusive interview.

December 2016

IBM matures nanotube connectors
IBM has surmounted one of the last hurdles to a future of carbon nanotube electronics by developing a method of connecting them to traditional electronics with nanoscale nickel end-contacts. IBM foresees a carbon nanotube future where wearables, Internet of Things (IoTs), implantable medical monitors as well as More-than-Moore semiconductors will all use carbon nanotubes as their base, because they are cheap and easy to fabricate at low temperatures.

US blocks China's Aixtron acquisition
US President Barack Obama's move to block the sale of a German semiconductor equipment supplier to a Chinese government-backed investment firm is likely to exacerbate growing tensions between the US and China over trade and China's place in the $335 billion global semiconductor industry. Obama on 2 December took the extraordinary measure of issuing an executive order prohibiting the acquisition of the US businesses of Aixtron SE by a shell corporation established by China's Fujian Grand Chip Investment Fund on the grounds that it presents a threat to US national security. Grand Chip is a Chinese investment firm partly owned by China's central government. The company derives about 20 percent

IBM, TSMC detail their 7nm work
Separate papers on 7nm process technology from TSMC and IBM energized a packed ballroom on the first day of the International Electron Devices Meeting (IEDM). They showed results that they believe nudge forward both Moore's law and extreme ultraviolet lithography (EUV). TSMC reported the smallest 6T SRAM to date in a process that it aims to put into risk production by April. IBM described the smallest FinFET made to date in a research device made with EUV. IBM showed FinFETs with contacted poly pitch of 44/48 nm, a metallization pitch of 36 nm, and a fin pitch of 27 nm. One device included a source-to-drain contact opening of about 10 nm and a gate length of about 15 nm.

Nissan learns a lot by towing its own cars
Car maker Nissan Motor Corporation announced it is using a fully automated vehicle towing system at its Oppama Plant that it named Intelligent Vehicle Towing (IVT). The system relies on mapping and communication technologies to link an intelligent and all-electric car to Nissan's production infrastructure and command it to tow newly produced cars to their dedicated wharf for shipping. The wholly automated system does not rely on conventional sensors that actually help guide the vehicle—the vehicle itself navigates around obstacles and picks up/delivers vehicles to their next production stop.

Leti details its 5nm node at conference
Researchers from CEA-Leti presented two papers unveiling promising nanowire architectural blocks for the 5nm node at the 2016 IEEE International Electron Devices Meeting (IEDM) in San Francisco. One of the papers, "NSP: Physical Compact Model for Stacked-planar and Vertical Gate-All-Around MOSFETs," presents a predictive and physical compact model for NanoWire/NanoSheet (NW/NS) Gate-All-Around (GAA) MOSFETs. By using a novel methodology for the calculation of the surface potential including quantum confinement, the researchers claim the model is able to handle arbitrary NW/NS cross-section shape of stacked planar and vertical GAA MOSFETs (circular, square, rectangular), providing an excellent tool for design exploration.

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GROWTH SIGNS SPUR OPTIMISM AT SEMICON EUROPA

Global semiconductor companies met in Grenoble, France for SEMICON Europa 25-27 October in a bid to shake off the doldrums that had stymied growth for nearly two years. While positive reports encouraged attendees, most companies are looking to Internet of Things (IoT) products to move the needle most in 2017.

AS INDUSTRY-LEADING COMPANIES, start-ups and every-size company in between met in Grenoble, France for SEMICON Europa there was no escaping an essential question: were recent growth indicators the start of a trend, or will it take the IoT to drive real growth in 2017 and beyond?

To take a reading of the mood across industry in 4Q 2016, one needed only visit a major conference in late October. Positive growth indicators materialized shortly before the event, but few companies reported seeing strong evidence so soon afterward despite the SEMI organization's recent positive announcements. A glimmer of good news in October was followed in November and December by analysts in overall agreement: the market is starting to improve.

Silicon Semiconductor technical editor Mark Andrews and publisher Jackie Cannon met with companies across the supply chain including EV Group (EVG) director of communications Clemens Schutte who said that his company had seen an increase in orders, and that new process tools announced earlier in 2016 were catching the attention of customers across the supply chain.

EVG had previously announced significant additions to its metrology and wafer bonding tool line-ups, including the EVG50 automated metrology system and the new ComBond Activation Module (CAM) designed to support room temperature bonding of sensitive materials. MEMS applications were recurring themes for EVG as was a wide range of IoT device and process tool solutions.

Edwards Vacuum launched its new Smart Thermal Management System (TMS) at SEMICON Europa. The system adds feedback control to accurately maintain gas temperature in vacuum pump fore lines and exhaust lines. Unheated lines can be clogged by condensed process materials and by-products. In addition to semiconductor/IoT product manufacturing, the system is designed to improve performance for manufacturers of flat panel displays and solar cells

Right: Alain Astier, President of IoT Planet

Representatives from across the IoT supply chain participated in a panel discussion regarding efforts to deliver seamless, intuitive and reliable security across Internet of Things applications. Companies represented included Gemalto, Mentor Graphics, Objenious, STMicroelectronics and Synopsys.

using chemical vapour deposition, epitaxy and etches with the potential for condensation. Alain Astier, President of IoT Planet, remarked that the growth industry is expecting from an expanding universe of connected devices is indeed occurring. But like any major force impacting industrial expansion, IoT is still largely in its embryonic stages, which is good news for those with products still in development, but not the avalanche of good tidings many would like to see capturing headlines. Nevertheless, a reordering of business-as-usual takes time since, "…we are talking about a major shift in the way people interact not only with one another, but the devices they use: the internet and the products that they use today that are not yet connected – this is a revolution in the making," he said.

Stephane Allaire, president of Objenious, remarked that while it is easy to think of IoT as a 'product' the concept of connecting devices to one another through the internet to expand their usefulness, enhance control features and enable whole new industries goes beyond any product class, type or category that the industry has so far created.

"IoT isn't just a product – it's a revolution. It is also an ecosystem. It is many, many things beyond a sensor or a battery that lasts 10 years to power that sensor. It is also an ecosystem because we use the internet and the cloud and 'Big Data'… And if you don't think that this will be big, you will be killed in the market," he elaborated.

The role that Europe already plays and can play in the evolution of the IoT was repeated almost everywhere throughout the Grenoble conference, emphasizing that IoT represents a new era in semiconductor manufacturing. Exhibitors and attendees seemed to share the sentiment that as an evolving marketplace without scores of IoT incumbents, and given the role European companies and researchers are already playing in IoT development, manufacturing opportunities for Europe are significant, especially for those who take a chance and seek them now.

Marie Semeria, CEO of CEA-Leti, one of Europe's largest research organizations, stressed the need for groups such as hers to continue their initiatives to strengthen public-private partnerships that are leading to more companies entering the business, bringing new ideas that lead to new products as well as solving the vexing challenges of industry. In an interview, Semeria said she noted that Leti's vision to anticipate the needs of industry and to 'sense' where new markets might be found has never been more critical.

"I believe the message is to think differently and to provide differentiation and value to our industry partners. My goal is to add value including competitive advantages with differentiated technologies. We did that with FD-SOI, which was very different from what was offered at the time when FinFET was emerging. FD-SOI is the right technology for low cost/low energy consumption devices which will see growth as IoT grows."

Semeria said that the fully depleted-silicon on insulator (FD-SOI) technology Leti originated can have

Stephane Allaire, president of Objenious, told SEMICON Europa attendees that while we are in the early days of IoT adoption, the technology will revolutionize many aspects of health, business and daily life.

a substantial impact as designers and manufacturers create more IoT products for existing and new markets, reshaping the way people interact with each other and their mobile devices. She also foresees a greater role for integrating key intellectual property (IP) at the device level by co-engineering products with software that increases a device's worth before it ever reaches production – an example of the 'value-added' approach she mentioned earlier.

"We have to think about the hardware and software together, whether that is finding better ways to use the FD-SOI technology such as lowering energy consumption, and embedding the IP right inside the package. Security is especially a concern for IoT devices, which is why we moved forward to add more designers such as (those in) the INRIA center – it is compelling research for the design centers to develop the software close to the hardware. We now have a dedicated team working on IoT security both at the device level and at other points along the value chain. Consumers need to have confidence that the new IoT-enabled devices they may consider purchasing will benefit their lives and not pose a security risk."

"The key is to consider security from the device level all the way up to the cloud. We at Leti are good at technology and communications at the hardware level, also we need to make sure that our partners are ensured of security and the most advanced technology no matter what they are looking to manufacture."

"An important initiative for us is to continue to expand the global portfolio including a high degree of integration and interconnection; with more interconnects we can gain time and speed as well as a smaller size. When interconnects go up we gain in many ways…We can be a low cost solution like we are now with FD-SOI in the Global Foundries plant in Dresden (Germany). This is still in Europe as well as at Samsung (in Korea). This is not yet in China, and if we want Europe to maintain a competitive advantage in developing IoT devices and other products we need to think about the best way to develop these technologies. The key is research to develop the technology. We have the tools and the expertise. We just need to execute on the plan," she remarked.

(Below) Silicon Semiconductor Technical Editor Mark Andrews at SEMICON Europa.

From the perspective of major research organizations such as Leti to supply chain vendors, OEMs and contract manufacturers, they believe sizeable growth across the semiconductor industry will resume when consumers 'get excited' about new products including next-generation IoT and mobile devices. As Semeria and other leaders remarked at SEMICON Europa, the IoT isn't merely a portfolio of new products, it is the universe of technologies, wireless interfaces, networks and applications that empower the concept of connectedness that has the power to revolutionize society. Even though 70 percent of the $10 billion (USD) in revenue from IoT this year is tied to industrial

CEA-Leti chief executive Marie N. Semeria in the Leti stand at SEMICON Europa. Semeria said Leti's role across research and product development areas will focus on advancing the evolution of IC technology and the many ways Internet of Things products need to evolve as core technologies and products mature.

applications, more visible consumer products are entering the market all the time, and this will continue to increase. The recent rising consumer awareness of connected devices like Amazon's 'Echo' and its 'Alexa' interface – and growing purchases of such technology – are steps towards new levels of connectivity that will impact public perception just as earlier products created a whole new industry as evidenced by Apple's iPhone and Samsung's Galaxy product lines.

Days before SEMICON Europa, trade organizations and analysts presented data suggesting 2016 could end on a positive note, a far better result than earlier when market watchers expected something between backsliding and modest growth. By November multiple industry trackers forecast small increases this year, with 2017 expected to outpace it by a significant margin. International Business Strategies (IBS) was amongst those forecasting a fractional uptick for now, with growth as high as 4.6 percent in 2017. Almost everyone agreed that a surprising surge in US PC sales combined with replacement smartphone sales was driving 2016 numbers positive. What's in store for 2017 will depend on legacy market growth and excitement around newer smartphone models replacing Samsung's failed Galaxy Note 7 and the prospect of Apple having new tricks in its iPhone bag. The wild card is how quickly the semiconductor market feels IoT's heft – the '800 pound gorilla' that so many expect to do so much for semiconductor makers. If the IoT starts significantly capturing consumer imagination in 2017 the Champagne corks will start popping.

On-site generated fluorine:

Effective, safe, and reliable source of fluorine for electronics for over 15 years

On-site fluorine generation has proven a safe alternative to greenhouse gases often used in electronics manufacturing. Linde delves into its makeup, history, and how fluorine is effectively used to clean CVD chambers and in many other applications.

By Dr. Paul Stockman, Head of Market Development, Linde Electronics

ON-SITE GENERATED FLUORINE (F_2) is a safe and reliable alternative to greenhouse gases for chemical vapor deposition (CVD) chamber cleaning and is currently used in the commercial production of semiconductors and LCD screens in multiple sites in Asia and Europe. In the first of a two-part series, we describe the on-demand production of high-purity fluorine as demonstrated by Linde's installed base of more than 30 generators serving global industries over 20 years and electronics manufacturers for more than 15 years. Production capacities ranging from 1 to 100+ tons / year have displaced high-pressure fluorine cylinder and bulk nitrogen trifluoride (NF_3) supplies. Certification by leading safety and engineering authorities document the design details required to effectively deliver fluorine reliably and safely without incident. In Part 2, we will describe the fundamental physical properties of fluorine, which are the basis for significant process and cost of ownership improvements and which eliminate the need for greenhouse gases in chamber cleaning.

History of fluorine

Fluorine was first produced and isolated by the French chemist Henri Moissan in 1886. However, the challenges in production processes and the element's vigorous reaction chemistry limited its use to bench-scale apparatuses for small experimental quantities. Industrial-scale production technology was first developed for the Manhattan Project in 1943 when gas-phase uranium hexafluoride (UF_6) was identified as the preferred method for separating the fissible ^{235}U isotope from the remaining 99 percent of isotopes. After the war, fluorine production technology was further developed and proliferated with the spread of independent nuclear materials capability and from this base further non-nuclear applications were developed.

Today, tens of thousands of tons of industrial fluorine are produced commercially all over world as chemical feedstock for organic fluorides and various inorganic fluorides such as SF_6, NF_3, and boron trifluoride (BF_3). Additionally, industrial fluorine is used for chemical modification of surfaces and to make certain plastics impermeable to water, oxygen, and hydrocarbons.

While industrial fluorine can be transported in large volumes either as a cryogenic liquid or as a compressed gas, safety and logistic concerns dictate that most fluorine is produced and consumed on-site and on-demand at low or atmospheric pressure. This limits both absolute inventory of fluorine, because it is only made as is needed, and also prevents high-energy, high-pressure events because the reactivity of fluorine is directly related to its pressure.

How fluorine is produced

Fluorine is produced by electrolysis of anhydrous hydrogen fluoride (HF) to yield hydrogen (H_2) gas at the cathode and F_2 gas at the anode; the amount of gas evolved is directly proportional to the current applied. The process is similar to the electrolysis of water to produce H_2 and oxygen (O_2); however,

it requires the salt potassium bifluoride (KHF_2) as a charge carrier and transport medium. The HF consumed by electrolysis is replaced by adding HF gas or HF liquid directly to the salt-acid mixture, with an effective composition of $KHF_2 \bullet (HF)_{x\approx1}$, which melts at 72° Celsius. The electrodes are physically separated to prevent the rising H_2 and F_2 gas bubbles from recombining, and the gases are evolved over the melt and collected through separate vents. Material selection of electrode and cell body components is essential to ensure a long operating lifetime of the fluorine cell with minimum maintenance requirements, and periodic chemical analysis of the salt-acid mixture verifies the integrity of components.

HF dissolved in the molten KHF_2 salt is electrolyzed to produce H_2 at the cathodes and F_2 at the anodes. The HF_2 feed can be introduced either as a gas or a liquid. The evolved streams of both H_2 and F_2 contain 1-5 percent of HGas as a vapor-phase impurity. The H_2 stream is diluted to concentrations below the LEL (lower explosion limit) of 4 percent and scrubbed before being vented to atmosphere. For high-purity applications, the fluorine stream is purified to remove the HGas as well as other low-level impurities. Compression to a working pressure of 1.0 to 1.5 barg and buffering in a temporary tank provides an adequate process supply at constant pressure without creating excess inventory.

Anhydrous HF, either in gas cylinders or larger bulk containers, is used to feed the fluorine cell. The H_2 byproduct is extracted for disposal, while the generated fluorine is further purified before being compressed to 1 to 1.5 barg and temporarily buffered before use in the customer process. All key process modules are enclosed in extracted cabinets as part of the safety design.

On-site fluorine generators

Concerns for safety and reliability have informed the design of on-site fluorine generators for use in the high-tech thin-film industries of semiconductor, display, and photovoltaic manufacturing. As with any chemical introduced into these market sectors, safety risks need to be identified and mitigated. Fluorine is the most electronegative element from the periodic table and this extreme reactivity is the cause for risks to both health and equipment.

Fluorine falls in the middle of the spectrum of the many toxic gas-phase chemicals commonly used in thin-film device manufacturing, a few examples of which are shown in Table I *[Reference: American Conference of Governmental Industrial Hygienists]*. Mitigation strategies focus on three areas: material selection and passivation, containment, and design for minimal inventory.

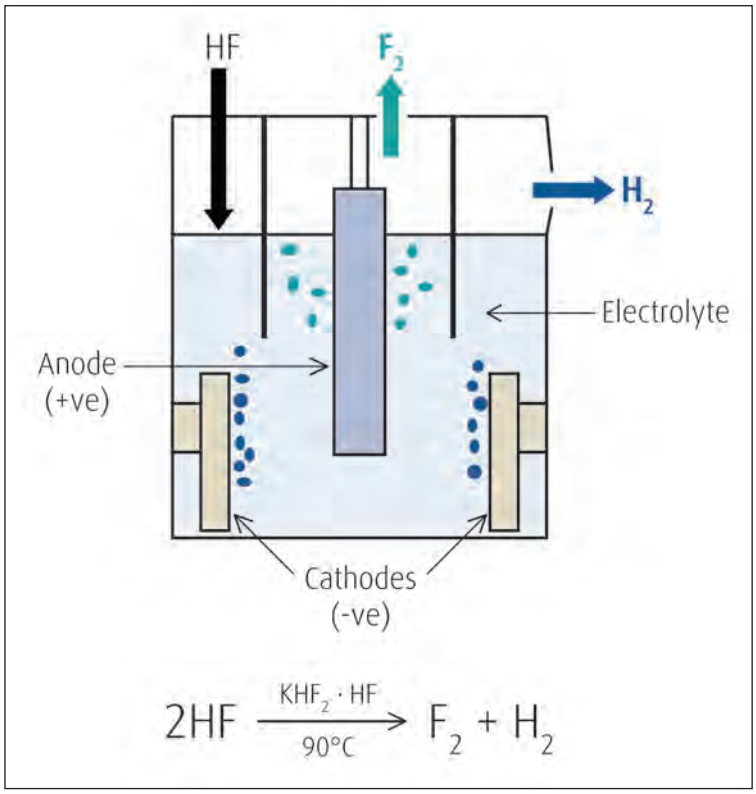

Figure 1: Electrolytic production of fluorine

Comparison of toxicity of electronic gases

Gas TLV/TWA[1]	(ppm)
Arsine	0.05
Diborane	0.1
ClF_3	0.1
Germane	0.2
Phosphine	0.3
Fluorine (F_2)	1
HF	3
Silane	5
NF_3	10
CO	25

Note1: TLV/TWA is defined as Threshold Limit Value/Time-Weighted Average. It is the maximum permitted workday exposure recommended by the ACGIH.

Table I: TLVs (Threshold Limit Value) for common gas-phase, thin-film feedstocks

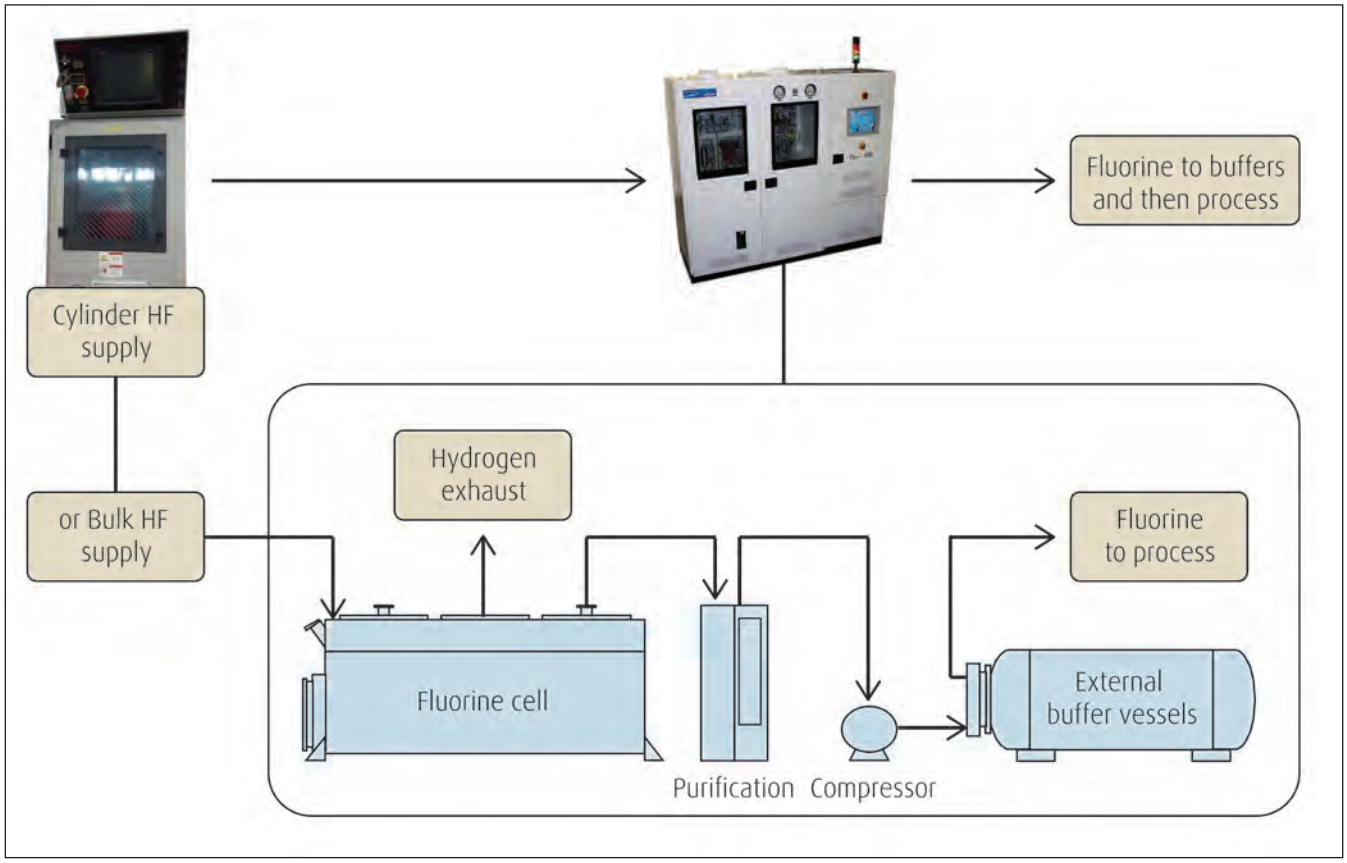

Figure 2: Process flow diagram for on-site generated fluorine

Mitigation strategy: Material selection and passivation

Although fluorine is highly reactive, many common metal constructions are compatible with fluorine at process temperatures. These include brass, copper, nickel, and many steel and nickel alloys, all of which form chemically inert, passivated metal fluoride layers when properly prepared.

Components for the generation, containment, and transport of fluorine should first be cleaned of all particles and residues – the same as for oxygen service – and certified leak-free. They are then exposed to a sub-atmospheric partial pressure of fluorine, often diluted in an inert gas.

Any organic residues are converted to gas-phase fluorides and exhausted to a scrubber, while the native oxide layers of the metal are replaced to form metal fluorides. By gradually raising the partial pressure to the maximum working pressure, the metal fluoride passivation layer is deepened, and the metal surfaces are rendered inert to further reaction with fluorine.

In addition, properly-sized piping and elimination of sharp bends are required to reduce gas velocities below the industry-recognized safe levels *[Reference: Compressed Gas Association CGA publication 9-15; European Industrial Gas Association EIGA document 140/10].*

Mitigation strategy: Containment

Containment forms the second safety risk mitigation strategy. All super-atmospheric sources of fluorine are contained by either ventilated enclosures or sealed and sectioned annular piping.

Ventilated enclosures house all generation and compression equipment, purification and buffer vessels, and valve manifold boxes. Extraction rates are determined to maintain safe external conditions in the event of a rapid release of the limited inventory. Extracted air is treated by either a local or facility acid scrubber.

Toxic gas detectors specific to fluorine are used to monitor all extracted areas. Transport of fluorine within the facility is through double-layered piping. The fluorine flows in the center tube while the annular space is sectioned and pressurized with nitrogen.

A leak from the center tube can be detected as a pressure loss in the annular space, and fluorine is doubly contained by both the outer pipe and the nitrogen barrier. A leak detected by a toxic

gas monitor or by depressurization of the annular containment triggers suspension of fluorine generation and automated closure of fail-closed valves.

Mitigation strategy: Design

On-site fluorine generation has been sized to meet the requirements of a number of thin-film chamber cleaning processes. Originally conceived as a replacement for high-pressure cylinders of F_2 and ClF_3 (chlorine trifluoride) used for cleaning low-pressure chemical vapor deposition (LP-CVD) semiconductor equipment, the smallest sized units have an annual production capacity of 1 ton / year. The equipment is designed in standard modules with form factors similar to gas cylinder cabinets.

Along with the availability of gas blenders with very low pressure-drop components, these units make for a direct replacement of 20 percent F_2 / 80 percent nitrogen (N_2) cylinder supplies. Almost all safety incidents in the semiconductor industry with fluorine are associated with high-pressure cylinder supplies, and in particular, the regulators used. Because a single generator operating at low pressure can replace more than 500 cylinders per year, the safety of the process has been greatly improved.

Maintaining a minimal inventory is integral to the design and safe usage of fluorine. Because the fluorine is generated on-site, there is no need to compress it to high pressures in order to transport it in containers. Instead, a pressure of 1.5 barg is sufficient to supply all gas conditioning and mass flow equipment of the cleaning process. And because fluorine is generated on-demand and proportionally to the current applied to the electrodes, the only vessels used are sized to buffer the generator against the periodic requirement for cleaning gas.

Modeling of randomized demand from multiple tools, sometimes numbering more than 100 for a single on-site plant, ensures that the buffer vessels are sized adequately for all realizable demand without being oversized. For example, a plant with a name-plate capacity of greater than 100 tons / year has an instantaneous inventory of less than 50 kg, which is little more than four hours of supply for a large LCD fab; fluorine supplies for semiconductor process have inventories as low as 2 kg at any time. As well as being made safe, on-site generated fluorine for thin-film chamber cleaning applications must meet the very high industry standards for reliability. Design and operation are essential to achieving high uptime. Beyond proper material and component selection, moving parts are minimized in the system design, electrochemical duty is kept light, and preventative maintenance and monitoring use leading indicators to keep all performance parameters within controlled ranges.

The design of the on-site generation configuration uses n+*1* redundancy of key components and modularization of assemblies. Therefore, preventative maintenance and repairs can be performed quickly without compromising the ability to supply the process, and longer-term service can be accomplished off-site. In addition to on-site operators, most fluorine plants for thin-film chamber cleaning take advantage of remote monitoring. This allows 24 hours per day coverage and diagnostics by fluorine plant experts located on three continents.

The design for safety and reliability have been recognized and accredited by a number of design authorities and awarding bodies: certification to CE, ASME, Korean S-mark, and SEMI S2, and awards by Semiconductor International for Best Product 2009 and from International Solar Technology for Green Solar Manufacturing 2009.

With the advent of the high-volume manufacturing of LCD screens and thin-film photovoltaic modules, the demand for on-site generated fluorine has grown in scale. In these applications, fluorine is used as a chamber cleaning agent for plasma-enhanced chemical vapor deposition (PE-CVD) processes. Larger generators have been designed for supplying 100s of tons / year. And although the process design

“Maintaining a minimal inventory is integral to the design and safe usage of fluorine. Because the fluorine is generated on-site, there is no need to compress it to high pressures in order to transport it in containers”

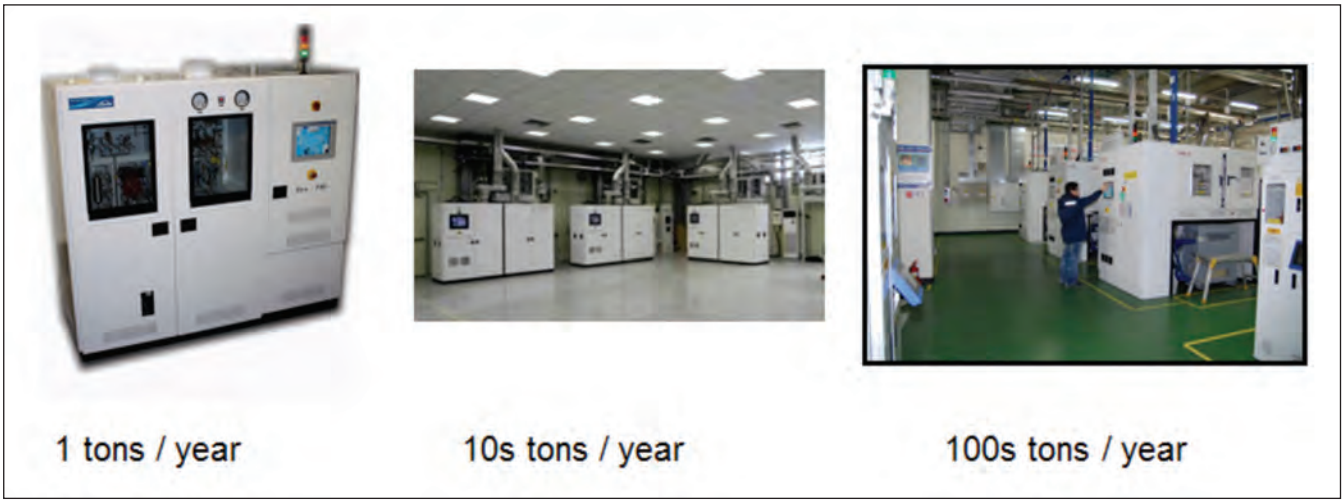

Figure 3: Three generations of on-site fluorine generators. Generators are available in different sizes and configurations to offer a wide range of capacity options.

remains the same, the form factor for these systems has grown to a separate on-site facility. This mirrors the track to other on-site supply schemes, such as those for nitrogen, oxygen, and hydrogen, from which manufacturers benefit as they scale their operations to achieve critical capacity.

The supply of on-site generated F_2 differs in several areas from the use of SF_6 or NF_3 for cleaning thin-film equipment. On-site supply schemes require different project considerations when compared to packaged material supplies to ensure proper footprint, utilities availability, and expansion capability.

Planning for safety is integrated with the end user and community at an early stage, and additional activities are required for commissioning and operation. Likewise, permitting and licensing change, with the added benefit that the on-site chemical inventory is substantially reduced. Furthermore, risks to supply chains and pricing volatility are reduced.

Summary

In the last 20 years, Linde has installed over 30 on-site fluorine generators, which are successfully operated in 11 countries. These continue to operate without a single safety incident, and provide supply delivery reliability much greater than 99 percent.

In Part II of this article series, we will discuss the fundamental chemical properties of fluorine that allow it to deliver significant process and cost of ownership benefits while at the same time eliminating the need for the majority of greenhouse gas usage in high-tech, thin-film manufacturing. Used in increasingly higher volumes, gases like NF_3, SF_6, and C_2F_6 have global warming potentials thousands of times greater than CO_2 and are coming under stringent monitoring and reduction regulations as more aggressive measures are enacted to reverse trends in climate change.

DR. PAUL STOCKMAN joined Linde in 1996. He currently is Head of Market Development, Linde Electronics, where he guides Linde's strategy to anticipate the needs of its customers in the semiconductor, display, solar and LED markets. During his career with Linde, Dr. Stockman has held roles in electronic materials product, purification and analytical development; equipment development; as well as Technology and Commercialisation Manager for Linde's on-site fluorine equipment. Dr. Stockman has been granted 5 U.S. patents and holds a Ph.D. in Chemical Physics from the California Institute of Technology.

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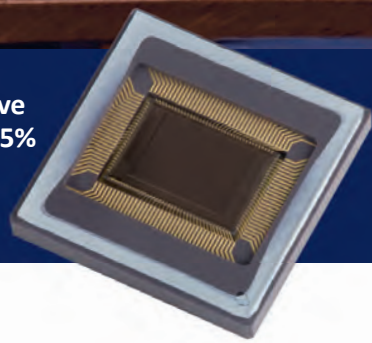

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On-Site Generated Fluorine:

High-speed chamber cleaning with zero global warming potential

On-site generated fluorine enables faster chamber cleaning and eliminates the need for the largest use of restricted greenhouse gases in semiconductor manufacturing processes.

Dr. Paul Stockman, Head of Market Development at Linde Electronics, explains the chemical properties underlying the benefits.

IN PART 1 OF THIS ARTICLE [1], we described the safe and reliable on-demand production of fluorine as demonstrated by Linde's on-site fluorine generators, with an installed base of more than 30 systems over the last 20 years and more than 15 years serving electronics manufacturers. With production capacities of one to hundreds of tons per year, these systems first displaced cylinder sources of F_2 and ClF_3 used for chamber cleaning of semiconductor processes, and have subsequently become the preferred bulk supply of chamber cleaning agents for large LCD and thin-film photovoltaic manufacturing. In Part II, we discuss the fundamental chemical properties of fluorine that allow it to deliver significant process and cost of ownership benefits, while at the same time eliminating the need for the majority of greenhouse gas (GHG) usage in high-tech manufacturing.

Chamber cleaning requirement

Chemical vapor deposition (CVD) processes used in high-tech thin film manufacturing require periodic cleaning to remove particles and films from the

surfaces of the vacuum chamber and process equipment. The frequency of the cleaning can be as short as once per deposition cycle, or may range up to once per several days, depending upon the thickness of the film deposited and the sensitivity of the devices being made. Without cleaning, these films and particles lead to defects that render semiconductor chips inoperable, displays with dark pixels, and solar modules with degraded efficiencies.

Most high throughput CVD processes employ automated, on-line cleaning with gas-phase chemicals as a time-saving alternative to off-line manual and wet processes. These gases must not only react with compounds in the deleterious films and particles, but also must be non-reactive towards the chamber materials of construction. In order to maximize the availability of the costly CVD equipment, chamber cleaning processes must be quick. And increasingly, device manufacturers are looking for processes that have low environmental impact and long-term sustainability. Most importantly, the cleaning processes must be very low cost per process cycle: it's cleaning, after all.

F-gases and activation

Fluorine-containing gases, or F-gases, meet all of the technical and cost requirements for chamber cleaning agents. The gases are activated to release the fluorine atoms as neutral radicals, which subsequently react with residual thin-films to form a gas-phase waste stream and are removed through the vacuum exhaust system of the chamber. While very reactive towards the thin-film compounds, fluorine radicals are inert towards most of the metals and ceramics used in CVD equipment, provided that moisture and oxygen are excluded.

Historically, the electronics industry has used fluorocarbons (C_xF_y): sulfur hexafluoride (SF_6), and nitrogen trifluoride (NF_3) as feedstocks to supply the fluorine radicals. These gases are easy to compress and transport in cylinders, and the cost to supply has been reduced through higher-volume manufacturing and packaging. However, these gases have certain process inefficiencies inherent to the high bond strengths and side reactions associated with the carbon / sulfur / nitrogen carrier atoms. These gases have also been the target of environmental scrutiny and regulation because they are all very strong greenhouse gases with global warming potentials thousands of times that of CO_2. As a cost-effective alternative, fluorine (F_2) has zero global warming potential (GWP) and none of the process inefficiencies of the earlier chamber cleaning agents.

Three methods can be used to activate the F-gases to release fluorine radicals [Figure 1]. In low-pressure CVD (LPCVD) process equipment operated at very high temperature, greater than 700°C, the thermal

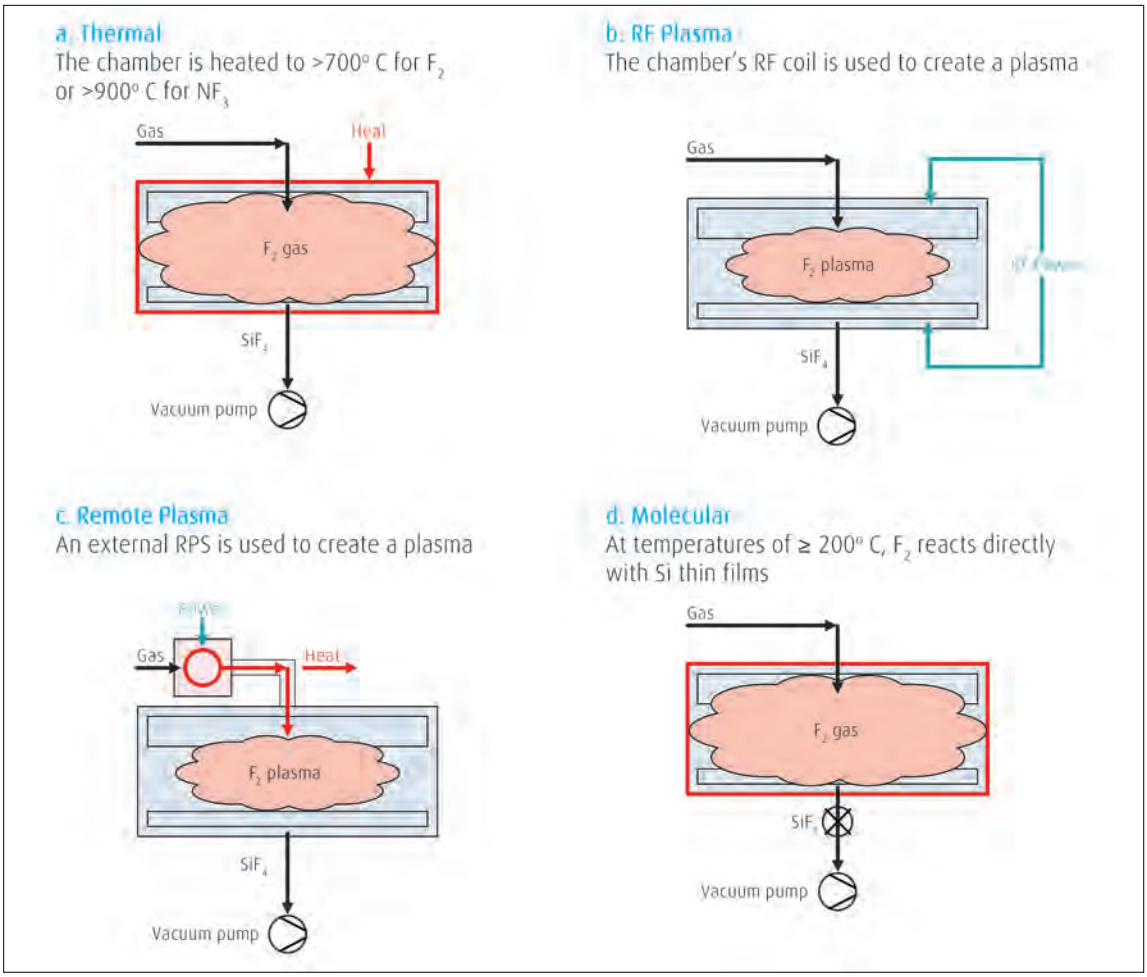

Figure 1: Activation methods for CVD chamber cleaning

> In order to maximize the availability of the costly CVD equipment, chamber cleaning processes must be quick. And increasingly, device manufacturers are looking for processes that have low environmental impact and long-term sustainability. Most importantly, the cleaning processes must be very low cost per process cycle: it's cleaning, after all.

energy from the chamber walls is sufficient to break the molecular bonds and release fluorine radicals. In plasma-enhanced CVD (PECVD) equipment, process temperatures are much lower, and too much time would be spent to heat and then cool the chamber for cleaning. Instead, the internal RF coil used to activate the plasma of the thin film reactants is also used to activate the F-gas cleaning agent. The cleaning rate is limited by the amount of energy that can be supplied by the RF power source.

With the advent of larger, more expensive 300 mm PECVD equipment, external remote plasma sources (RPS) were introduced in order to increase the energy available for cleaning gas activation, thereby decreasing the cleaning time. Most current generation PECVD tools use this method to increase the tool availability. Importantly, argon is not required to support the plasma in the RF or RPS methods. Finally, a fourth method using a low temperature direct reaction between molecular F_2 and the silicon thin film has been demonstrated as a very fast alternative method for this application. [2]

Thermodynamics and kinetics: Theory

Both the thermodynamics – or chemical energy – and kinetics – or chemical pathways – of cleaning gas activation need to be considered to understand and exploit the significant process advantages available when using F_2 vs. other F-gas alternatives. After a short look at this fundamental science, we will present process data from a variety of tools and applications that demonstrate these advantages.

As the most electronegative atom in the periodic table, fluorine forms strong bonds with most other atoms, including some stable compounds with rare gases. It is not surprising then that C_xF_y, SF_6, and NF_3 all have very high bond energies – the amount of energy required to release fluorine radicals. In contrast, fluorine forms a very weak bond with itself, and therefore F_2 requires very little energy for activation. Table 1 shows the energy required to remove individual fluorine radicals from a given F-gas and summarizes the average energy of activation. In the subsequent examples, we will see how this translates into much higher cleaning rates achievable with F_2.

Once the fluorine radicals are created through activation, chemical simplicity maximizes the amount of fluorine radicals that are available for cleaning from F_2. There is only one chemical

$$F_2 \text{ --> } F\cdot + F\cdot \qquad (1)$$

pathway (1) that can be followed, and recombination in the gas-phase to reform F_2 is kinetically forbidden. Therefore, almost all of the fluorine radicals created from F_2 go on to react with the thin films and particles targeted for cleaning. With the addition of different atoms, there is more than one available pathway during activation. For example, with NF_3 and RF activation, at low

$$NF_3 \text{ --> } \cdot NF_2 + F\cdot \qquad (2)$$

$$\cdot NF_2 \text{ --> } :NF + F\cdot \qquad (3a)$$

$$\cdot NF_2 + \cdot NF_2 \text{ --> } N_2F_4 \qquad (3b)$$

	F_2	NF_3	SF_6
Bond energies	F---F 159 kJ/mol	F_2N---F 248 kJ/mol	F_5S---F 387 kJ/mol
		FN---F 278 kJ/mol	F_4S---F 229 kJ/mol
		N---F 316 kJ/mol	
Activation energy for each F atom produced	F from F_2 80 kJ/mol	F from NF_3 281 kJ/mol	F from SF_6 308 kJ/mol

Table 1: Bond strengths and activation energy of CVD chamber cleaning gases

pressures, the desired pathway (3a) dominates. However, as the flow of NF_3 and the RF power increase, recombination of the intermediates (3b) competes, with a result that only approximately 50 percent of the fluorine atoms become effective cleaning radicals [3].

With SF_6, the effect is even more pronounced, and oxygen is added to prevent the deposition of sulfur during the cleaning.

$SF_6 + {}^1/_2\ O_2 \rightarrow SOF_4 + 2\ F\cdot$ (4)

The effective net reaction (4) means that only 33 percent of fluorine atoms are actually used.

Thermodynamics and kinetics: Results

Now we take a look at the process effects of the thermodynamics and kinetics on commercial PECVD tools for Gen 5 LCD processes from AKT/AMAT, Oerlikon, and Ulvac. In each case, a silicon thin film has been deposited on the chamber walls at an operating temperature of 200°C.

The cleaning gas flow has been normalized to atomic F· in units of standard liter per minute (slm). The endpoint for the cleaning was determined by OEM recommended methods. The cleaning rates have been normalized to the OEM recommended method, which is set at 1.

In Figure 2 [2] and Figure 3, RF activation of F_2 vs. SF_6 and NF_3 is compared, and the RF power used is noted in the figures. The results confirm the kinetics limitation on efficiency: 33 percent for SF_6 and 50 percent for NF_3 vs. F_2. Furthermore, for the same cleaning rates, F_2 consumes one-third of the electrical power for activation.

And finally, for the same equipment set, F_2 can achieve a much faster cleaning rate: 5x vs. SF_6 and 3x vs. NF_3. This is due ultimately to the limitations of the power required for activation. Similar results have been published by others on 300 mm semiconductor tools [4].

Results in Figure 4 from a similar experiment using a tool with an RPS [5] demonstrate the improved utilization of NF_3 with this method of activation. Because the RPS completely decomposes the cleaning gas, all the fluorine is converted to fluorine radicals and the cleaning rates are the same for F_2 and NF_3 for the same amount of atomic F· flow.

However, because the F_2 bonds are so much weaker than those from NF_3, the RPS can convert much more F_2 into F· radicals and the achievable cleaning rate for F_2 is 3x to 4x that of NF_3. And for the same cleaning rate, F_2 cleaning requires 50 percent of the RPS electrical power required for NF_3. Finally, because there is no carrier atom in F_2, 20 percent less mass is used to achieve the same clean vs. NF_3.

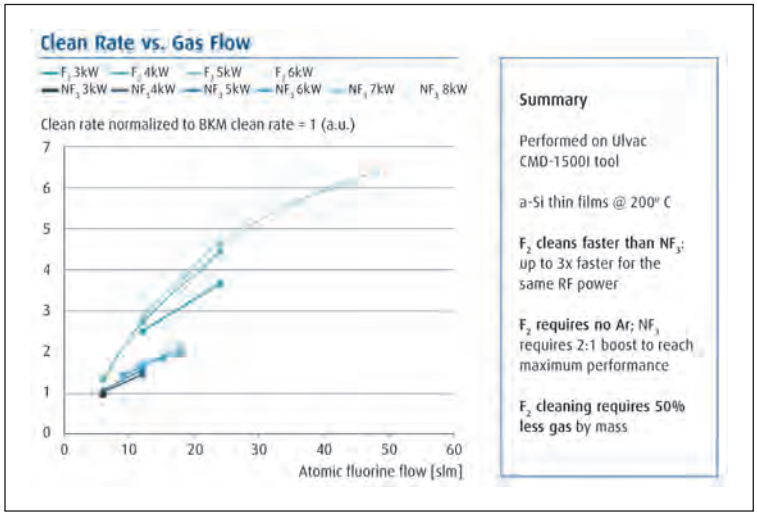

Figure 2: RF Plasma cleaning on an Ulvac tool: F_2 vs. NF_3

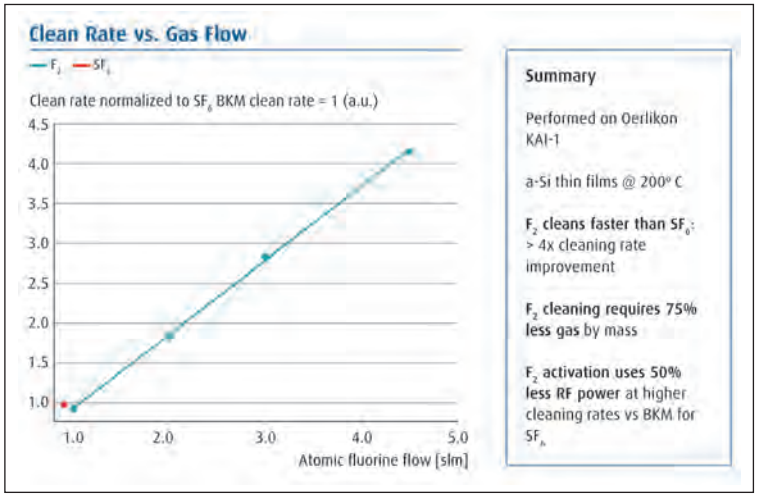

Figure 3: RF plasma cleaning on an Oerlikon tool: F_2 vs. SF_6

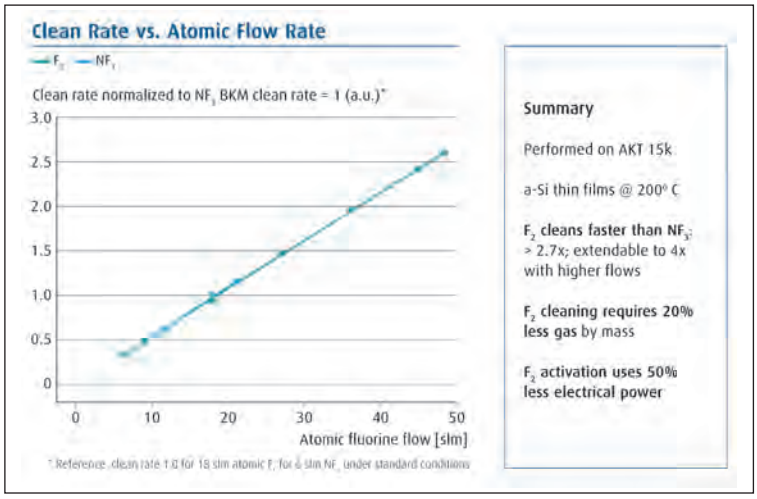

Figure 4: RF plasma cleaning on an AKT tool: F_2 vs. NF_3

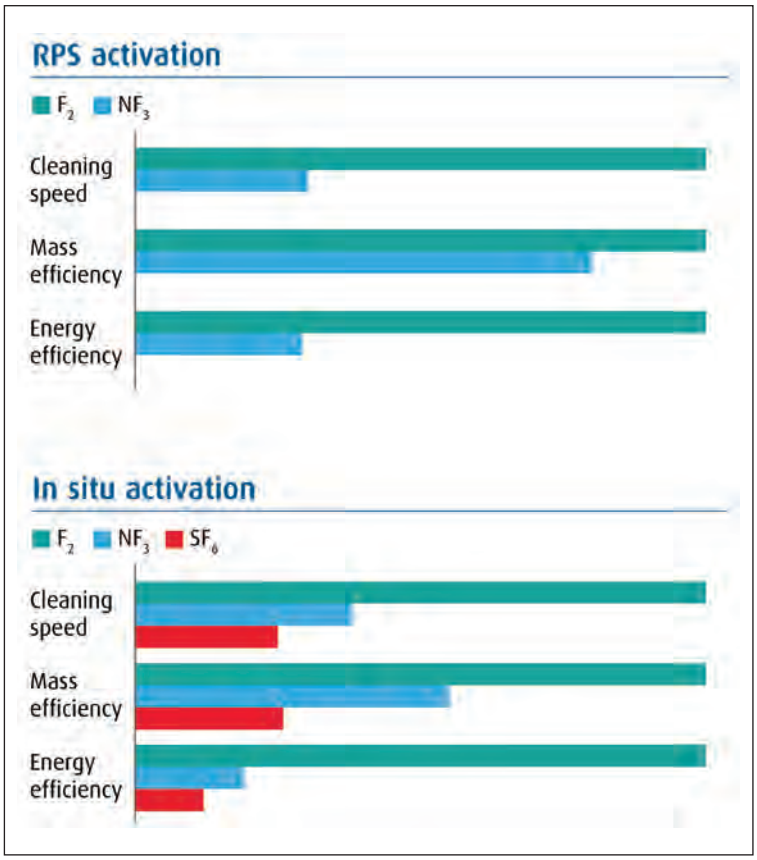

Figure 5: Summary of PECVD chamber cleaning performances

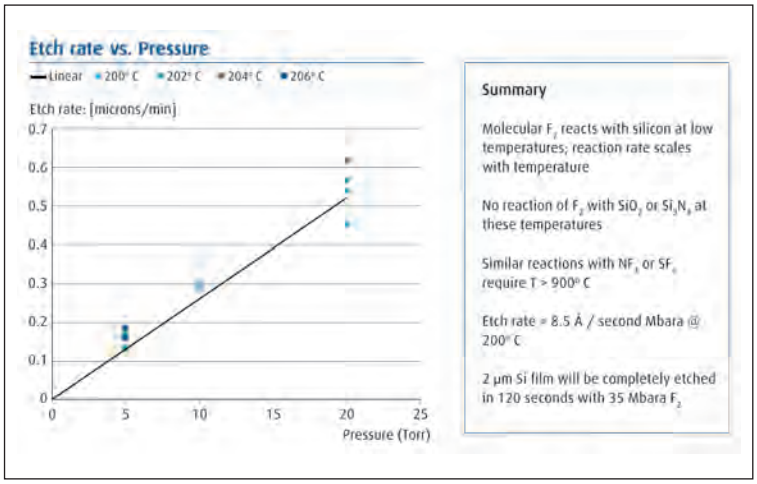

Figure 6: Molecular cleaning with F_2

Figure 5 summarizes the F_2 process benefits vs. SF_6 and NF_3 for speed, mass efficiency, and energy efficiency demonstrated for chamber cleaning. Faster cleaning, less gas used, and lower energy consumption are achieved across all of the tested PECVD tools. While the other chamber cleaning methods discussed above rely on first converting F-gases to F radicals, there exists an alternate cleaning method unique to F_2 for silicon films. The responsible kinetic mechanism is a direct reaction between F_2 and the silicon surface [6]. As seen in Figure 6, the cleaning rate is directly related to the amount and pressure of F_2 available. This method has been further demonstrated to be achievable under zero flow conditions, indicating a very fast and cost-effective clean [3].

On-site fluorine: The zero global warming potential choice

Beyond the significant process benefits demonstrated by using F_2 as a chamber cleaning agent, growing adoption of F_2 also alleviates serious problems associated with the use of GHGs like C_xF_y, SF_6, and NF_3. Unlike GHGs, F_2 does not absorb UV radiation and convert it to heat energy, and therefore it does not have any global warming potential (GWP) or contribute to global warming. Table 2 (see page 27) illustrates the very large GWPs associated with other chamber cleaning gases.

In 1990, C_xF_y and SF_6 gases were recognized for their potential to damage the environment and were included in the Kyoto Protocol for the reduction of GHGs. Large-scale adoption of NF_3 for chamber cleaning began just after this time. Scripps Institute scientists, tasked by the US government since the 1970s to collect atmospheric samples for monitoring of ozone-destroying compounds, analyzed their repository and found that NF_3 has been growing at a semi-exponential and unabated rate since industrial use began in the 1990s [7]. They showed that more than 10 percent of NF_3 produced ultimately escapes into the atmosphere. Recently, several national and local environmental authorities have moved to monitor the use of NF_3. The US Environmental Protection Agency has included NF_3 and other GHGs commonly used in the electronics industry as part of its reporting rule. Manufacturers are required to report not only the amount of individual GHGs used, but also to measure the gases at key steps in their processes.

While not yet regulated by means of a carbon equivalent tax, the cost of compliance is estimated at over $1 million (USD) for larger fabrication facilities [8]. Because cleaning gases constitute approximately two-thirds of the GHGs used in a typical semiconductor fab, converting PECVD chamber cleaning to fluorine will allow some mid-tier manufacturers to decrease their total GHG usage below the reporting threshold, while the largest manufacturers will be able to significantly reduce their compliance burden.

Clean Gas	Atmospheric Lifetime	Global Warming Potential
CF_4	50,000 years	6,500 GWP_{100}
C_2F_6	10,000 years	9,200 GWP_{100}
C_3F_8	2,600 years	7,000 GWP_{100}
SF_6	3,200 years	23,900 GWP_{100}
NF_3	740 years	17,200 GWP_{100}
F_2	0 years	0 GWP_{100}

Table 2: Global warming potentials of CVD chamber cleaning gases

Summary

Manufacturers in the semiconductor, display, and photovoltaic industries have safely and reliably chosen on-site F_2 for their CVD chamber cleaning requirements. Initially adopted for its cost and process enhancement benefits, F_2 is now proving to be an easy choice for manufacturers who also want an environmentally sustainable alternative.

For the past 20 years, Linde has been the leader in providing on-site fluorine generation for the electronics industry and other markets. With over 30 installations, Linde continues to support its customers' choice for faster, more efficient cleaning processes with zero global warming potential. Linde partners with manufacturers and OEMs for the extension of these benefits to additional applications.

DR. PAUL STOCKMAN joined Linde in 1996. He currently is Head of Market Development, Linde Electronics, where he guides Linde's strategy to anticipate the needs of its customers in the semiconductor, display, solar and LED markets. During his career with Linde, Dr. Stockman has held roles in electronic materials product, purification and analytical development; equipment development; as well as Technology and Commercialisation Manager for Linde's on-site fluorine equipment. Dr. Stockman has been granted 5 U.S. patents and holds a Ph.D. in Chemical Physics from the California Institute of Technology.

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Visit: **www.linde.com/electronics** for more information

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REDUCE GOLD USAGE

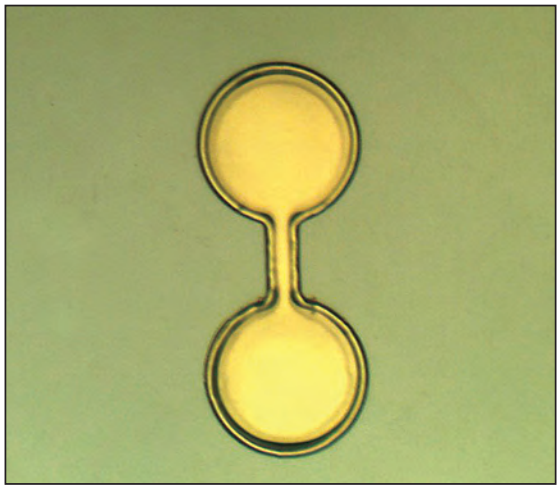
Nothing surpasses gold's inherent semiconductor performance benefits. But ClassOne Technology explains how its electroplating system can keep performance high at a fraction of the cost.

GOLD, despite its high cost, has long been an essential element in semiconductor processing because it is a highly efficient and reliable electrical conductor that also resists oxidation and corrosion. These qualities make gold ideal for connectors, switches and relay contacts in a vast array of applications, which is why in 2015 the electronics industry used more than 290 tons of this precious metal.[1] However, a newer generation of electroplating tools is starting to reduce that usage in certain sectors.

Addressing the problems of PVD, CVD and wet bench deposition

In semiconductor processing, gold is often deposited by physical vapor deposition (PVD) and chemical vapor deposition (CVD) methods. While those techniques sufficed for a time, they also brought certain significant problems such as material wastage, slow deposition rates and downtime for necessary equipment cleanings. Some have tried to use wet benches for gold plating, but with limited success due to the high non-uniformity inherent in that approach. Also, manually operated wet benches were prone to undesirable levels of variation and the risk of human exposure to open baths of toxic chemistry.

Gold plating by the Solstice S8 system



Many semiconductor applications require gold layers ranging in thickness from 3 to 35 microns

However, a newer generation of electroplating systems, exemplified by the Solstice family from ClassOne Technology, is designed to overcome those limitations. The systems provide fast, waste-free, cost-efficient, and production-oriented solutions with uniformities in the 1 percent range.

Eliminating gold loss, reducing gold expenditure

For gold deposition, one fundamental challenge with PVD and CVD was that those techniques did not coat just the wafer, they also coated the entire inner surface of the deposition chamber — in this case, with a very costly material. Theoretically, the 'oversprayed' gold could be recaptured and reclaimed. But in practice, cleaning and reclaiming processes have proved to be very difficult, time-consuming, potentially dangerous (perhaps requiring the use of hazardous chemicals such aqua regia) and ultimately inefficient. Consequently, a great deal of the oversprayed gold

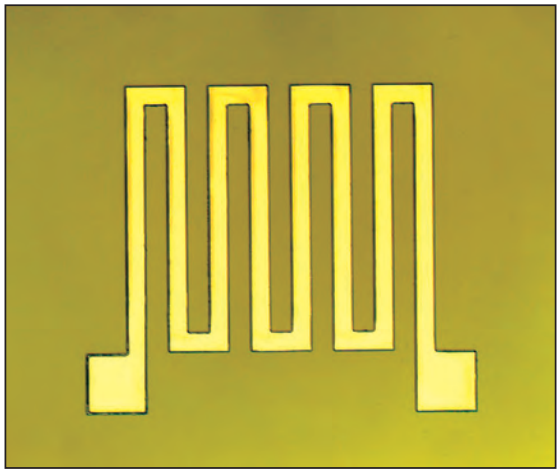
was permanently lost, which significantly increases the total cost of ownership of the process.

By contrast, new electroplating systems only deposit gold onto the wafer, specifically where it is needed. There is no 'overspray' or waste of gold. Also, there is no equipment downtime for chamber cleanings and no need for reclamation efforts. The new electroplating process is cleaner and simpler; it is also more precise and efficient. It reduces costs substantially by cutting gold usage and eliminating waste. The amount of gold needed is further reduced by the fact that electroplating is a self-purifying process, so it requires only four nines of purity in the electrolyte solution instead of the six nines required in evaporation pellets or sputtering targets.

Faster deposition, more streamlined processing

In addition to the gold loss problem, PVD and CVD processes have also been limited by relatively slow deposition rates — typically between 10 and 30 nm/min. This had been acceptable for creating relatively thin layers; however, as applications began to require thicker gold layers, the long deposition process times became increasingly problematic. Today, many emerging markets such as lasers, LEDs, RF and MEMS have requirements for gold layers as thick as 3 to 35 microns, so manufacturers are actively seeking faster deposition solutions.

New Solstice electroplating systems provide deposition rates in the order of 150 to 300 nm/min, or roughly 10 times faster than previous deposition methods. In addition, the new tools are specifically designed for ≤200mm wafer processing and are thus strategically positioned to serve the needs of many emerging markets that use smaller substrates.



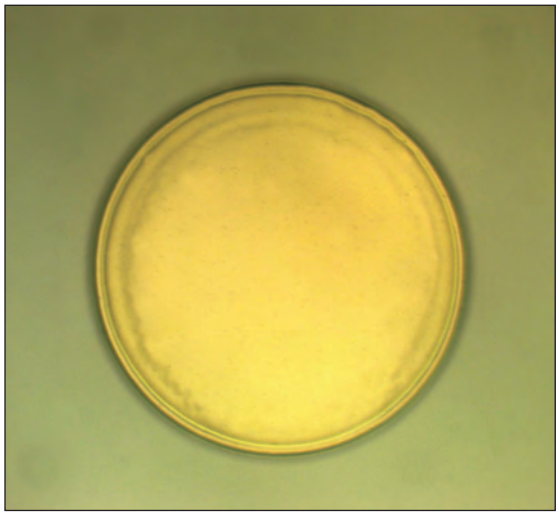
The Solstice S8 can electroplate device features, reducing the amount of pure gold needed by up to 10 times

A view inside ClassOne Technology's Solstice S8 electroplating system showing the tool's eight processing chambers

New electroplating tools further reduce cycle times because no vacuum is required, so processing can start immediately. There is no pump-down wait time before processing can begin. Also, one wafer can be run at a time if desired, without incurring any overhead penalty. The resultant savings in time and increased throughput can add a further level of cost efficiency.

Innovative layering technique can reduce gold usage substantially

Because of its unique 8-chamber design the Solstice S8 electroplating system enables it to replace a solid gold layer with a multi-metal stack, and use much less gold than would otherwise be required.
For example, a feature that previously required a 5μm layer of solid gold can be replaced with a 'sandwich' of 0.25μm Au, 1μm Ni, 2.5μm Cu, and another 1μm Ni – all topped with 0.25μm Au – to achieve equivalent functionality while reducing gold usage by a factor of ten. The multi-chamber equipment design enables it to deposit the Au / Ni / Cu / Ni / Au layers all in a single cycle; no additional process steps or time are



Gold contact points made of an electroplated 'stack' using Au, Ni and Cu instead of pure gold

required to gain significant cost savings.

The magnitude of potential gold savings can be estimated by extending the example above: Assume that a fab is running 1,500 wafers per week through a metal lift-off process where 5 μm of gold is deposited over 50 percent of a 150 mm wafer area. Further assume that all oversprayed gold is recovered and that the price of gold is $1200 per troy ounce with no additional processing fees for the purity.

Under those conditions, using a solid gold layer, the user's annual gold cost would be approximately $2,150,000. However, with the same operational assumptions, if the Solstice's Au / Ni / Cu / Ni / Au 'sandwich' technique were used, the total deposited metal costs (Au + Ni + Cu) would be reduced to just over $108,000 per year — yielding an annual savings of over $2,042,000. Thus, the gold cost reduction in the first year alone would more than pay back the cost of the electroplating tool! And if gold were to rise in price, the payback would be reached even more quickly.

Substantially reduce costs while increasing performance

In summary, Solstice electroplating systems are able to deposit thicker gold layers more quickly and efficiently while eliminating gold waste. The process requires no downtime for cleaning vacuum chambers, and it provides increased uptime and more cost-efficient processing. Perhaps most significantly, the tool's chamber design enables innovative layering techniques that can potentially yield enough reduction in gold usage to pay back the equipment purchase cost within a year.

Reference
1. World Gold Council, (www.gold.org)

Multi-metal stack (right) can reduce gold usage by up to 10x compared with solid gold layer (left).

A side view 'cut-away' illustration showing the composition of an electroplated device feature that uses 10x less gold than a pure gold analog

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PRODUCTIVELY MANAGING EQUIPMENT RELOCATIONS

Manufacturing consolidations have led to industry-wide change. When fabs open or close, relocating valuable process tools is a key consideration. As specialist NSTAR explains, making a move productive and efficient takes a trusted partner.

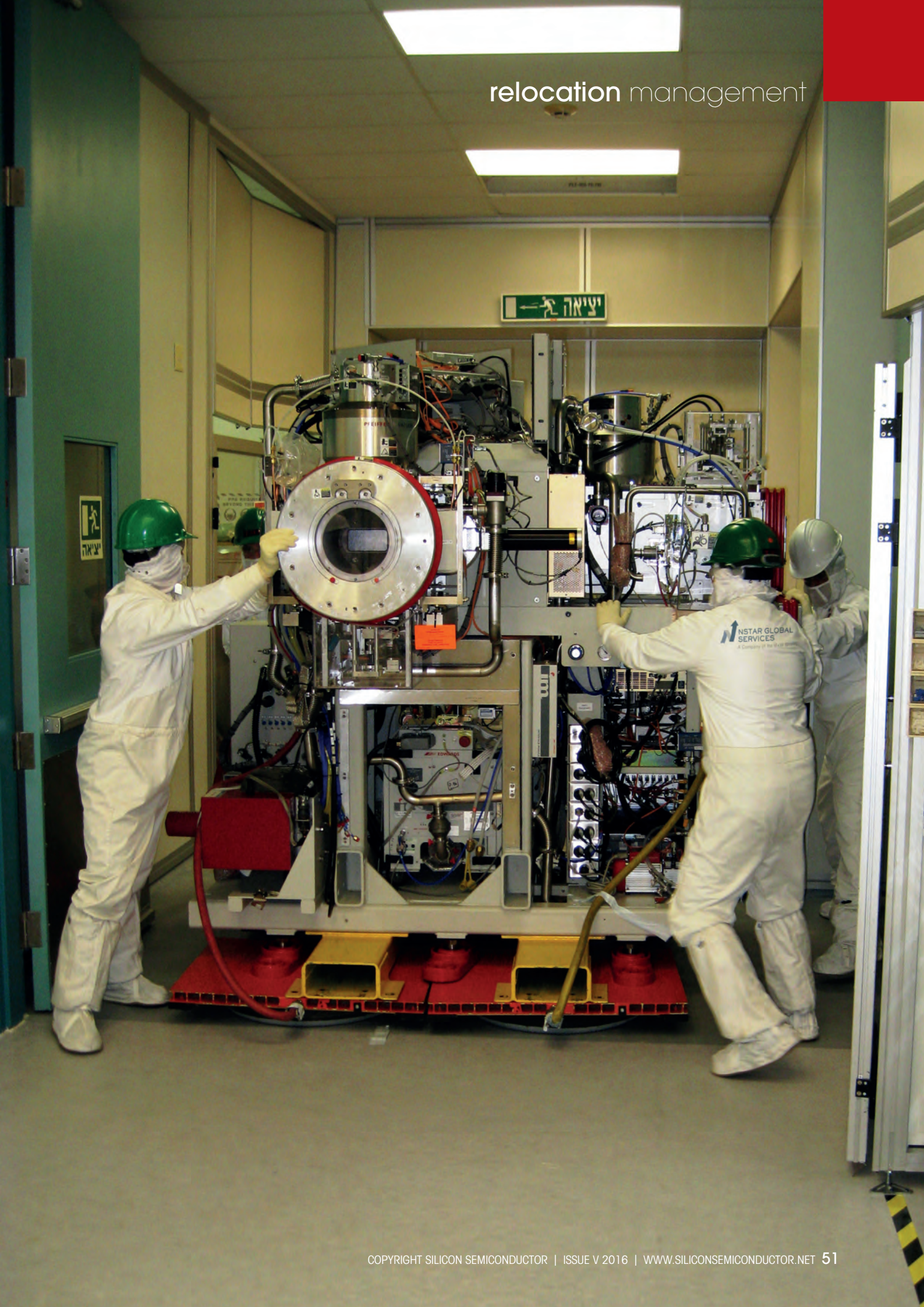
OVER THE PAST FEW YEARS, the secondary market for 200mm semiconductor manufacturing equipment has been on a roller coaster ride. First the market declined, causing as many as two hundred 200mm fabs to close, resulting in an estimated 6,000 used semiconductor tools coming onto the market. This was followed by a resurgence in added capacity driven by new applications related to mobility, sensing and the Internet of Things (IoT) as well as refurbishment of 200mm fabs to leverage legacy node silicon and alternative materials process tools to build devices that do not require the capacity of 300mm wafers. Industry consolidation has further added to the number of high quality process tools moving across regions and to different countries.

Many plant owners are outfitting 200mm and other fabs with refurbished tool sets purchased on the secondary market. Considering that a large number of these tools are located at manufacturing facilities scattered across the globe, removing process equipment from a particular factory—either to relocate the asset, resell it, or scrap the tool—can be a monumental logistical nightmare if not handled correctly. This article discusses the complexity of semiconductor equipment relocation, using two case studies to illustrate best practices.

Decontaminating, decommissioning and relocating complex process tools is a highly specialized business that requires very specific skills, and considerable expertise. There are two paramount concerns: to protect the value of the asset, and, to ensure that the decommissioning and relocation is conducted safely. A third element—time—also drives some moves when relocating assets to another facility is done because the receiving fab operator needs the tool to be brought up to full capacity as rapidly as possible.

Semiconductor chips are built in fabs and foundries that use extremely sophisticated equipment requiring a variety of toxic gases, chemicals and high electrical power. The decommissioning and relocation process is built around safety as the primary concern. The process for de-installation starts with ‘fingerprinting’ the tool so that its as-is condition is documented, recording the system functionality, the last qualification records and creating a ghost image of the tool software. Then, the system is decontaminated: chemical and physical hazards are removed, and any process gases or liquids are flushed/purged. The system is next disconnected from all utilities, all lines are capped or plugged, and any loose parts are individually labelled, wrapped and packed into shippable containers along with necessary documentation. Finally, the process tool itself is rigged, packed and crated for transport, and the site is remediated for any environmental impacts resulting from prior manufacturing operations.

At every step along the way, the de-installation process is documented; following proper safety protocols is critical. (For example, in some cases, the use of hazardous material suits and self-contained breathing apparatus are required.) The key to successful equipment relocation is meticulous planning, rigorous project management and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adherence to best known methods (BKM), all with a strong overlay of 'safety first.' Depending on the project size, teams should include a project manager, a safety manager and enough engineers/technicians to execute the project, along with any specialized equipment for loading, delivery and on-site setup if the tool is moving to a new operational location. The complexity of the project is also determined by whether the tool or tools are in a working fab—if manufacturing operations are ongoing, the decommissioning and relocation project must be designed to not impact ongoing production.

Case studies

One recent case involved decontaminating, decommissioning, disassembling, moving out/crating, shipping, uncrating and installing over 70 semiconductor process tools, and ancillary and support equipment within live production environments across the globe at different integrated device manufacturer (IDM) locations. The IDM contracted M+W Group as the general contractor and NSTAR Global Services as the project management team to handle the relocation. It began with the de-install process in Israel and concluded with installation in Singapore.

The relocation team provided technical resources who liaised with the client's tool owners to provide a concise snapshot of the tools' fingerprint prior to decommissioning (which included functionality audits, making ghost images of hard drives, and last qualification records). Following the steps previously outlined, and using BKMs, the tools were disassembled and loose parts were individually labelled, wrapped and packed into shippable containers. Each tool travelled with a complete parts inventory assembled prior to crating, with all pertinent shipping documents provided.

At the time de-installation was taking place in Israel, the team was simultaneously preparing the receiving site facility in Singapore to reduce tool downtime, enable full integration and ensure a smooth transition of the production process. The same engineers and technicians who handled the de-installation performed the reinstallation to ensure continuity of tool knowledge. Most importantly, the entire project was achieved with zero safety incidents.

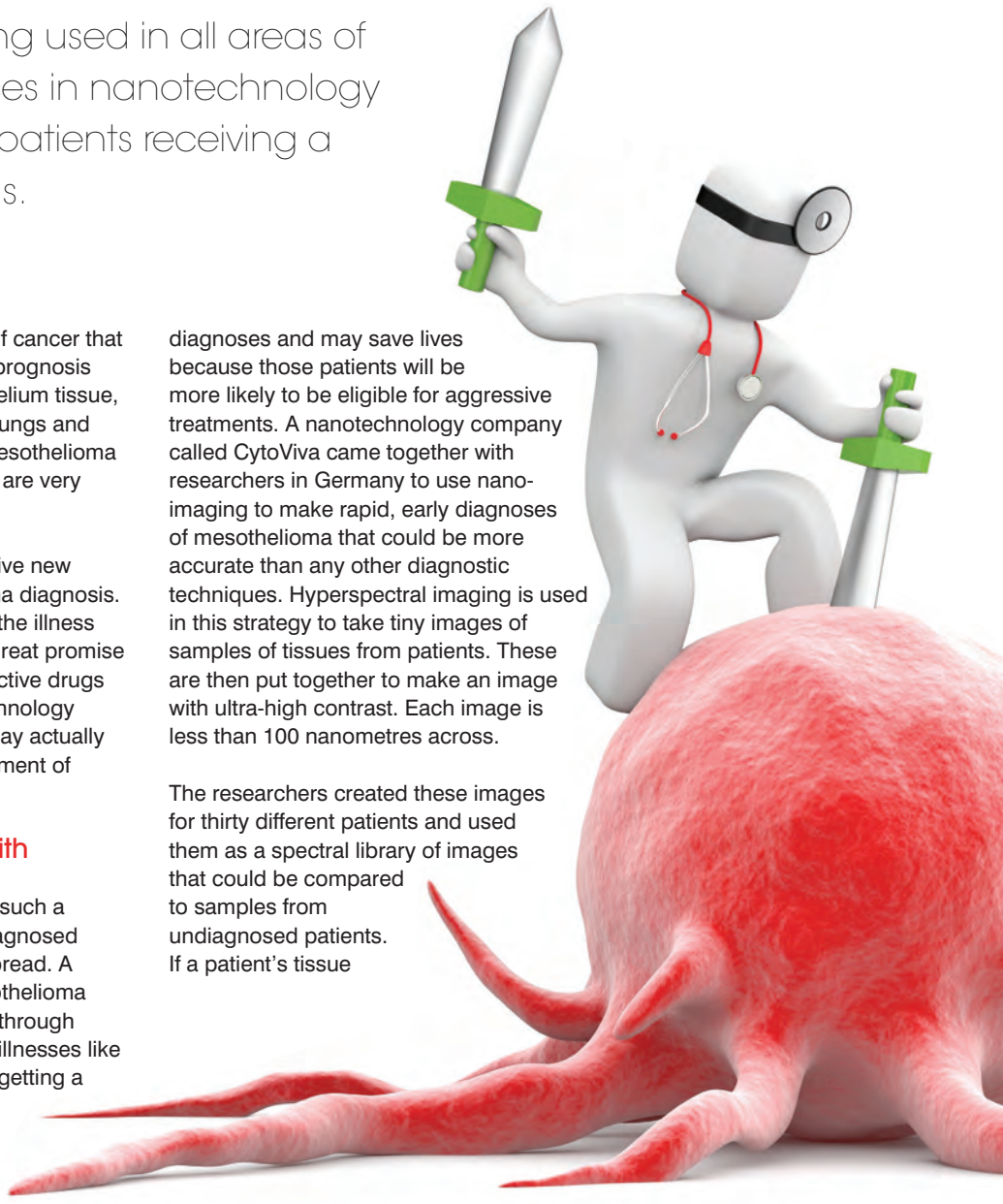
A second relocation case study involved moving tools from a deactivated facility, with tools destined for installation in multiple locations for reinstallation. One hundred semiconductor process/metrology tools required decontaminating, decommissioning and rigging-out from a facility in Taiwan that had closed and was no longer in production. This situation creates an entirely different set of challenges and site restrictions. The tool inventory had been sold to various companies and brokers with the understanding that a single general contractor (GC) would control the overall site management. The GC mandated that all documentation and discussions be conducted in Taiwanese. To facilitate these conditions, the company assigned a bilingual Asia project manager who assembled a team of Taiwanese resources comprising a safety officer, lead engineers, engineers and technicians. All team members were involved in daily meetings with the safety officer during the ongoing tool removal, and site walks were conducted three times a day. Throughout the project, safety protocols were strongly emphasized. Even under drastically different conditions, the project was successfully completed without incident.

Conclusion

As illustrated in this article, managing the logistics of semiconductor equipment relocation is an extremely complex process, with many and varied challenges that differ from one situation to another—all depending on tool locations, conditions at both originating and receiving sites, government restrictions, etc. Relocating semiconductor equipment requires a specialized skill set, and should not be undertaken in an ad hoc manner. Rather, for optimal outcome in semiconductor, flat-panel display and solar manufacturing industries it is best to contract with a company specializing in equipment decommissioning, decontamination and relocation services such as NSTAR Global Services (M+W Group).

Nanotechnology could be the silver bullet in war on cancer

Nanotechnology is being used in all areas of medicine. New advances in nanotechnology may give new hope to patients receiving a mesothelioma diagnosis.



MESOTHELIOMA is an aggressive kind of cancer that is most often deadly and has a negative prognosis when diagnosed. It begins in the mesothelium tissue, in most cases in the tissue that lines the lungs and chest cavity. Most cases of this kind of mesothelioma are caused by exposure to asbestos and are very difficult to treat.

New advances in nanotechnology may give new hope to patients receiving a mesothelioma diagnosis. Tiny images are being used to diagnose the illness earlier, while nanoparticles are showing great promise in being able to target the delivery of effective drugs to tumours. On the other side of nanotechnology developments, some of these particles may actually be harmful and contribute to the development of mesothelioma.

Making an earlier diagnosis with nano images

One of the reasons that mesothelioma is such a deadly type of cancer is that it is often diagnosed in the later stages, when it has already spread. A major reason for this is the fact that mesothelioma is difficult to diagnose. Many patients go through several misdiagnoses for more common illnesses like pneumonia or long cancer, before finally getting a diagnosis of mesothelioma. Any strategy that can be employed to make a more accurate diagnosis will lead to earlier diagnoses and may save lives because those patients will be more likely to be eligible for aggressive treatments. A nanotechnology company called CytoViva came together with researchers in Germany to use nano-imaging to make rapid, early diagnoses of mesothelioma that could be more accurate than any other diagnostic techniques. Hyperspectral imaging is used in this strategy to take tiny images of samples of tissues from patients. These are then put together to make an image with ultra-high contrast. Each image is less than 100 nanometres across.

The researchers created these images for thirty different patients and used them as a spectral library of images that could be compared to samples from undiagnosed patients. If a patient's tissue

sample is a match for one in the library, it would mean a diagnosis of mesothelioma or another specific type of cancer. The researchers tested this technique using samples of tissues that had already been diagnosed and ran them through the spectral library. The result was quick and accurate diagnoses.

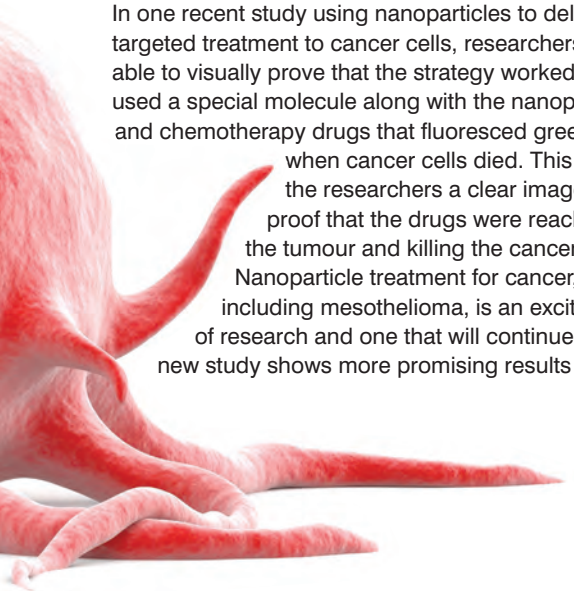
Nanotechnology particles to deliver treatment

An early, accurate diagnosis is a great start in using nanotechnology to beat this insidious disease, but better treatments are needed too. Nanotechnology may be able to deliver better and more effective treatments with fewer side effects. The research is early, but promising, and in an Australia, at least one patient seems to have been cured of mesothelioma using a nanotechnology technique.

The researchers used nanoparticles containing micro RNA. The nanoparticles were then injected into the body and were directed right to the tumours through the use of targeted antibodies. These acted like guides to get the particles to the tumour while ignoring other tissues. Once at the site of the tumour, the particles could release the micro RNA into cancer cells. There, these small molecules inserted new genes to stop the growth of the cancer cells.

This nanoparticle treatment strategy is being tested with different types of cancers and different medicines. Anything can be packed into the particle, and with the guidance of antibodies, directed at specific cancer cells. For instance, chemotherapy medications could be placed in the particles and delivered directly to the cancer cells. Currently these drugs are administered to the entire body and are not very specific. They target any living cells that grow and divide rapidly, which means that they cause a lot of uncomfortable side effects. By targeting cancer cells only, those side effects could be avoided.

In one recent study using nanoparticles to deliver targeted treatment to cancer cells, researchers were able to visually prove that the strategy worked. They used a special molecule along with the nanoparticles and chemotherapy drugs that fluoresced green when cancer cells died. This gave the researchers a clear image and proof that the drugs were reaching the tumour and killing the cancer cells. Nanoparticle treatment for cancer, including mesothelioma, is an exciting line of research and one that will continue. Each new study shows more promising results and it may not be long before this becomes a treatment method that can be used on a majority of cancer patients, many of whom had little hope of survival.



Ongoing nanotechnology research

With the promise of nanotechnology to treat and possibly cure difficult cancers like mesothelioma, many research institutes are investing in further research. These include the Institute of Bioengineering and Nanotechnology in Singapore where researchers are using nano-sized biochips to test how effective drugs are on cancer cells and to deliver individualized treatments to patients.

At the University of Pennsylvania, the main goal of the Penn Centre for Orphan Disease Research and Therapy is to develop and test nanoparticles for the targeted delivery of drugs. The Centre recently received a $10 million gift to work toward the goal of making these treatments work. New York University's Langone Medical Centre is working with a high-tech piece of equipment called a NanoString Technologies nCounter Analysis System. It will help researchers investigate cancer and how to treat it at the molecular level using nanotechnology.

Some nanotechnology may contribute to mesothelioma

Nanotechnology holds great promise for treating diseases like mesothelioma, but some of these tiny particles may also cause harm. Nanotubes, according to research, may cause damage when inhaled, damage similar to that caused by mesothelioma-causing asbestos fibres. Studies have shown that these long, thin tubes resemble asbestos fibres and act like asbestos fibres.

Nanotubes were discovered a couple of decades ago and they have many properties that make them a kind of wonder mat erial. They are light like plastic, but even stronger than steel. These nanotubes have been used in research for batteries and electronics, engineering structures, and medicine. The study that compared nanotubes to asbestos used mice and found that the particles caused damage similar to that seen with asbestos fibres. Currently, it is not likely that these nanotubes will often become airborne as asbestos does, so it is not a great concern for most people.

Mesothelioma is a difficult cancer. It comes with little hope of surviving, largely because it is aggressive and because it gets diagnosed in later stages. Nanotechnology could address both of these issues. While more research is needed, these technological advances could help make mesothelioma diagnoses more accurate and help kill the cancer cells in tumours.

WET BEATS DRY IN 3D BACKSIDE PROCESS STUDY

With 3D integrated circuit wafer stacking entering mainstream HVM, backside processing has become a more critical step for device manufacturers. A study commissioned by Veeco Instruments points to clear advantages of wet etch processing. By Mark Andrews, technical contributor, Silicon Semiconductor.

Right: Veeco's silicon etch system is configured with Profile Match Technology for adaptive process control

FOR 3D-IC strategies to succeed, critical manufacturing processes need to maintain productivity and efficiency without extending costs and complexity to the point where negatives outweigh positives. A recent study commissioned by Veeco Instruments points to clear advantages for wet etch processes worthy of consideration by manufacturers looking for ways to optimize performance while reducing factory floor space and overall costs.

Careful and highly precise backside processing is an area of 3D-IC production that manufacturers pay particular attention to since success (or defects) have a multiplying effect. Backside processing is so important since through-silicon vias (TSVs) finished during these and subsequent steps are hands-down favorites for creating interconnects. TSVs also provide the greatest number of interconnection points compared to other strategies and can be produced with mature, cost-effective technologies.

While there are various points along the production process where TSVs can be made (first, middle or last,) the so-called 'via-middle' position has emerged as the most favored for etching vias into silicon. This point is somewhere between the contact and BEOL layers; approaches may differ from one manufacturer to another. (See Figure 1) In via-middle processing, the wafer has been bonded to a carrier and has gone through an initial grinding to thin the bulk of the silicon wafer.

Process tool manufacturers have focused on the steps that actually reveal the vias as a point of differentiation since the two major approaches are quite different and choices at this point represent options to reduce costs and complexity while improving results.

The figures and details documented in the study referenced in this article were produced by SavanSys Solutions LLC in cooperation with Veeco Instruments. SavanSys is a group of respected and specialized semiconductor industry supply chain cost modeling analysts that use the company's patented software and extensive process flow library to create activity-based cost models for assembly and/or fabrication plant operations.

Veeco's WaferEtch System enables uniform etching on multiple process levels for semiconductor and advanced packaging manufacturers

Two primary approaches to TSV reveal

After mechanically grinding silicon to remove the bulk of unneeded material, additional thinning is required to safely reveal the vias. This takes place to eliminate surface roughness and any defective silicon that may have been released during grinding. The final etch and surface conditioning can be done with a combination of chemical-mechanical planarization (CMP) and plasma dry etching, or wet chemical etching. One approach that is not typically used is simple CMP as a solo step due to the potential for contamination if copper particles come into contact with the silicon wafer backside.

CMP or dry-etch processes utilize costly slurries and involve cleaning steps to remove slurry particles and other contaminants not used in wet etch. They also include expensive plasma equipment and etching gases with much higher consumable and maintenance costs. Plasma etch processes also require a separate wet cleaning following intermediary steps. The SavanSys researchers found that Veeco's wet etch equipment and processes could replace four tools commonly used in the dry etch process of record (POR) including the CMP, plasma etch, cleaning and silicon thickness measurement tools. The key to making the wet etch approach most economical is eliminating the CMP step in the overall sequence. They found that Veeco's two-step wet process (all performed inside one advanced WaferEtch® tool,) accomplishes this in a simpler, more cost-effective manner.

Accelerating production/cutting costs

How can the wet etch approach to TSV reveal involve fewer steps and yield better results while it cuts costs? Essentially, the tool and processes were built from the ground up to do all these things along with delivering greater flexibility. Veeco Vice President of Marketing for its Precision Surface Processing BU, Scott Kroeger, explained the genesis of their wet etch approach.

"We were focused on the fact that the industry needs a lower cost silicon etch-to-reveal process in order to help the industry scale. The current competitive solution involves multiple tools, so the Capex associated with that is significantly higher than a single tool solution like Veeco's. Also, we were focused on delivering excellent surface (condition) and uniformity with lower consumables cost, which is also critical to enabling the silicon etch process. One other very important criteria in the design approach was to build a system that could sense incoming wafer profiles and adjust the etch process automatically to compensate without operator intervention. This takes complexity out of the process recipe tuning and puts the system virtually into autopilot," he remarked.

The first step in Veeco's wet processes relies on a high-rate silicon etch to contour and smooth the

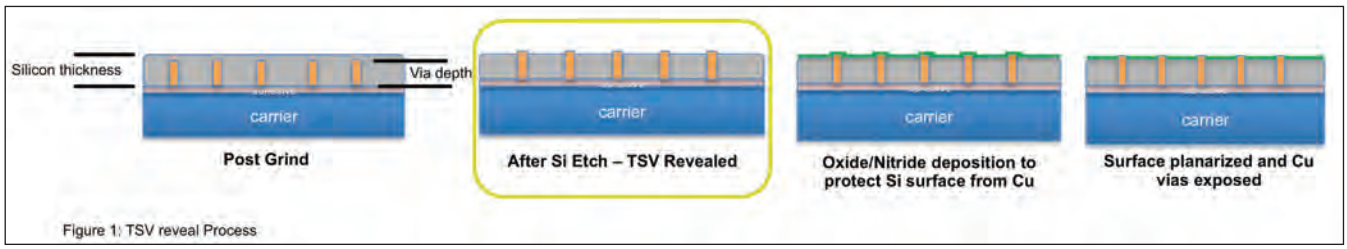


Figure 1: Veeco TSV reveal process

silicon surface to within ~2μm of the TSVs. This step eliminates grind marks from previous processing and compensates for non-uniformities in the silicon wafer. Next, the chemistry is changed to SACHEM Reveal Etch to precisely uncover the vias since this etchant is selective to silicon and does not etch the oxide liner covering the TSVs. Etching is controlled by integrated measurement of the silicon wafer before and after using the company's Profile Match Technology™ (PMT). (See Figure 2)

It should be noted that PMT adds utility beyond establishing and controlling etch rate. The incoming silicon thickness is measured and the program determines the etch profile based on TSV depth data and the reveal height requested by the manufacturer. This ability to precisely and automatically control thickness requirements enables compensation for radial variations for a more uniform reveal height, so it also reduces the amount of reveal needed in many cases. Lower reveal heights translate into lower passivation deposition, and typically, less final CMP to expose the copper surface.

Veeco's Chief Technical Officer for Precision Surface Processing, Laura Mauer, explained that the result of these key, primary wet etch process steps is a smoother wafer with fewer irregularities and a more precise approach to finished thicknesses. Mauer noted that Veeco's new approach does not incorporate TMAH (tetramethyl ammonium hydroxide), an etchant that has been used by other companies and research groups. Veeco replaced TMAH with SACHEM Reveal Etch™.

"TMAH is considered toxic, especially in the high concentrations that are needed for silicon etching. We eliminated it when we invented our approach. Veeco utilizes SACHEM Reveal Etch, which is about 5 times less hazardous than TMAH. The chemistry is one part of the differences in processes. The other is that Veeco's process uses a two-step etch sequence. First, a fast etch smooths the surface followed by the second step using the SACHEM etch to selectively thin the silicon and safely reveal the TSVs," she said.

Another important benefit of Veeco's wet etch compared to a dry etch is the final product: reduced

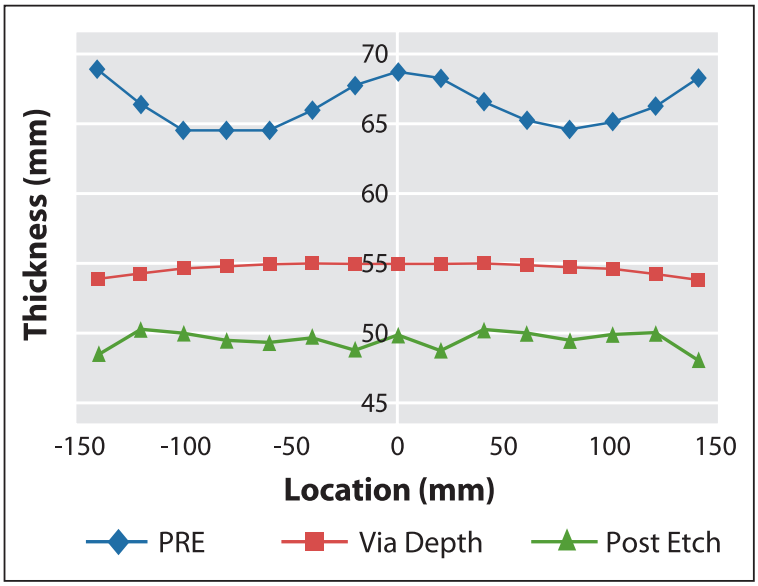


Figure 2: Profile Match Technology chart

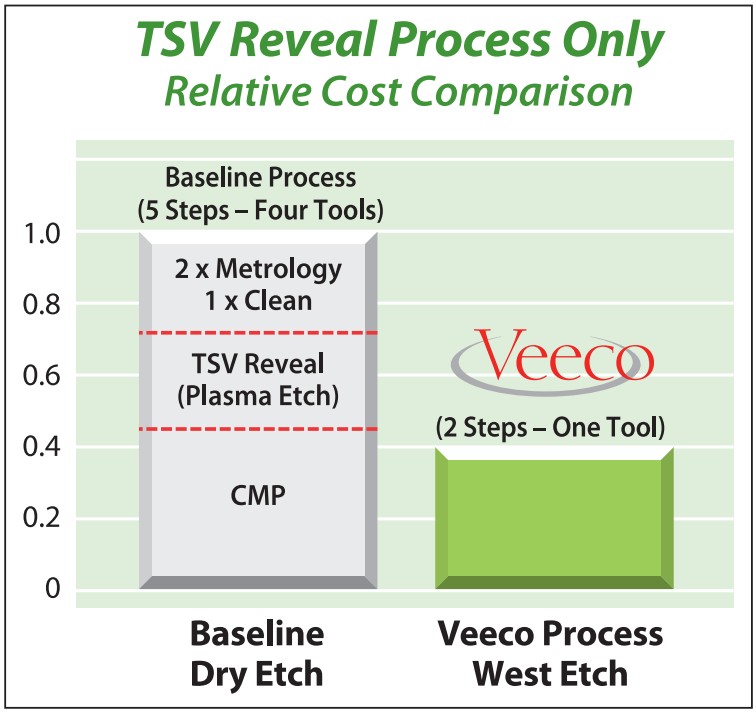


Figure 3: Direct TSV Reveal Process Step Comparison

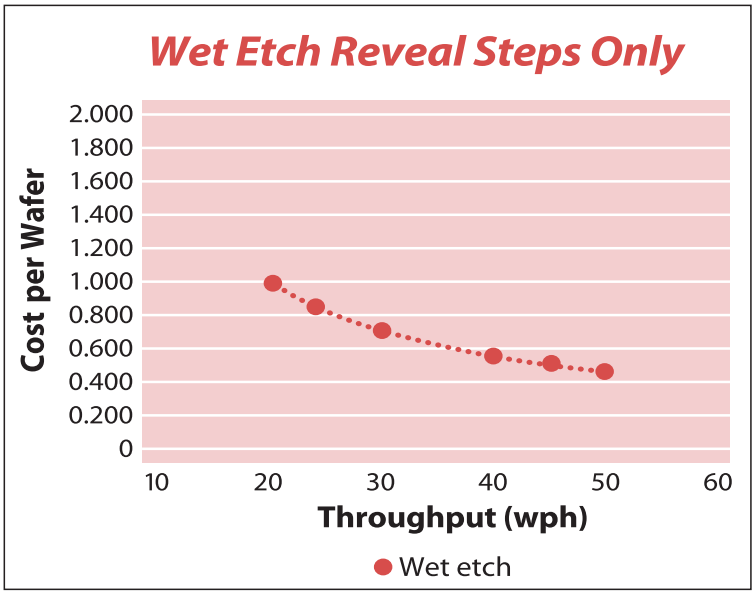


Figure 4a: Wet etch rate sensitivity analysis

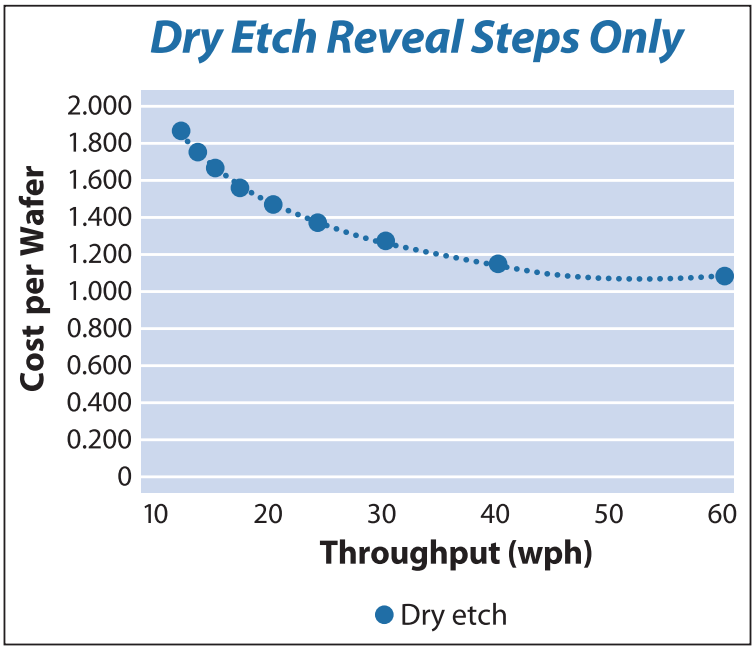


Figure 4b: Dry etch rate sensitivity analysis

surface roughness along with precisely controlled TSV reveal. While post-processing surface roughness can be 4nm or higher with dry etch, Mauer indicated that Veeco's wet etch pushes the benchmark below 4nm.

Cost modeling

Researchers utilized activity-based cost modeling to understand key cost centers of the TSV reveal process with both etching methods. This is a bottoms-up approach that involves breaking down a process flow into individual activities with the costs associated with each item factored into determining how dry vs. wet etch compare on an equal footing. For comparison sake, the TSV reveal process using dry etch begins with bonding to a carrier wafer. The process moves through a series of grinding and CMP steps occurring before and after dry etch, and includes chemical vapor deposition (CVD) passivation once the vias are revealed, along with a few metrology steps. The wet etch reveal process also begins with bonding to a carrier wafer and then proceeds through two major liquid-based process steps within one machine.

Figure 3 shows the cost comparison between the standard four-tool process of record versus Veeco's wet etch process. It is understood that this percentage is heavily dependent on design parameters, type of assembly, the number of redistribution layers (RDLs), etc. However, even with many variables it is clear that TSV-related processes are costly – about 11 percent of the total. Since every factory is somewhat different these numbers may vary; however, the comparison provides insight about relative cost structures and equipment needs as well as materials costs. Yields were assumed to be equal while any potential defect reductions obtained would add to the cost benefits. Determining the baseline is based upon the dry etch POR.

Strikingly, we can see that the two-step wet etch reveal approach delivers the same serviceability as the five-step dry etch baseline processes, yet wet etch costs less than half as much. Secondly, this type of comparison easily identifies where cost is coming from within each incremental step and not just the overall costs. Within the baseline dry etch POR, the plasma etch stage contributes high capital cost while the CMP step contributes high material cost. In the wet etch approach, most of the cost is associated with equipment (roughly 80 percent), which is not surprising since one tool essentially replaces four tools required for TSV reveal in the current POR that includes CMP, dry etch, clean and metrology. The charts in Figure 4a and 4b demonstrate how TSV reveal step costs change as the etch rate changes.

Comparing baseline cost drivers for both etch approaches provides important insights. Cost of ownership is critical to ensuring that an investment like TSV reveal is contributing to a manufacturer's competitiveness and not holding it back. Veeco's Scott Kroeger said that besides reducing the number of tools a factory needs to maintain, his company's approach also delivers better performance and increases throughput, reducing capital costs as well as consumable expenses. The Veeco approach also has long term applicability to a wide range of current and future device form factors.

"The TSV reveal configuration of our WaferEtch tool is well suited for other silicon etch process applications beyond 3D-IC. One main driver for wafer thinning is to reduce the thickness of semiconductor packages such as fan-out wafer level packaging for use in consumer electronic applications, MEMS devices and image sensors.

"There is a growing need for ultra-thin wafers (below 120μm) and we believe that wet etching can achieve

the best results in terms of uniformity and reducing surface roughness. Also, we find that after mechanical grinding and polishing steps, there is subsurface damage in the wafers that causes significant stress and presents a potential for yield loss. We have demonstrated that our wet etch process can remove most of the sub-surface damage and strengthen the wafers," he added.

Better control, smaller footprint, lower costs

The SavanSys analysis of Veeco's wet etch approach to wafer thinning and TSV reveal shows that wet etch can outperform various dry etch processes while reducing the complexity of these critical steps. Since TSV reveal can amount to 11 percent of an interposer-based process like those employed in building 3D-IC devices, controlling costs here has a multiplier effect and direct impact on a manufacturer's bottom line. By choosing an advanced wet etch tool like the Veeco WaferEtch solution, manufacturers can reduce the number of tools they have to maintain as well as the volume of costly consumables while achieving superior performance. Manufacturers can also extend their capabilities into additional wafer thinning operations that are expected to take a larger role in supporting next-generation device designs.

Veeco

Type of Company: Public

Traded as NASDAQ: VECO

Industry: LED, Data Storage, Semiconductors, Power Electronics, Wireless, Optical, MEMS

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Founded: 1989
Website: **www.veeco.com**

Acoustic screening
reveals component defects

Plastic encapsulated microcircuits (PEMs) are mainstays of consumer, defence and commercial electronic products. Tom Adams, consultant at Sonoscan, explains how to safeguard your bottom line with optimized acoustic screening.

IMAGINE a typical plastic-encapsulated microcircuit (PEM) component. Inside this particular PEM lies an area of electronic mold compound that is separated from the die paddle by a gap. This very thin gap may be called a delamination, suggesting that the two materials were once bonded but later separated; or it may be a 'non-bond,' suggesting that the two materials were never bonded. One side of the gap borders the die attach, but the gap does not extend under the die.

Regardless of its specific defect, this PEM poses a risk to any system in which it is installed. If the die must dissipate significant amounts of heat, the chief risk is that the gap will expand laterally under the die as a result of thermal cycling. There it will reflect heat being dissipated from the die back into the die. In time it may cause the die to overheat and fail electrically.

Figure 1: Automated acoustic micro imaging tools (here the Sonoscan DH2400) use carefully defined standards to make good accept/reject decisions on large numbers of components.

If the PEM is to be used in a low- or medium-priced consumer product, such failure may not be of critical concern. But if the PEM is to be used in a higher-level product (automotive, medical, military, aerospace, and some commercial products), such an internal gap-type defect is of considerable concern and should be found before the PEM is mounted on a board. The PEM itself may be inexpensive, but if it is going into a critical application it should be screened acoustically for internal structural defects before use. Undiscovered defects can cost the manufacturer time, money and even its priceless brand reputation.

The most effective non-destructive means of finding gap-type defects is an acoustic micro imaging tool such as a Sonoscan C-SAM system. Laboratory, semi-automated and automated versions (Figure 1) all use a scanning transducer that pulses very high frequency or ultra-high frequency (ultrasound) into the PEM or other sample thousands of times per second. A pulse that encounters a gap-type defect is virtually 100 percent reflected by interface between the solid material and the air in the gap, even if the gap is as thin as 10 nm.

There are two widely used modes of acoustic imaging for screening PEMs:

- **Reflection mode imaging.** A pulse striking a well-bonded interface is partly reflected to the transducer and partly transmitted across the interface. A "white" pixel in the acoustic image is made by a pulse striking a gap-type interface; a "gray" pixel is made by a pulse striking a well-bonded interface between solids. Pixel colors are

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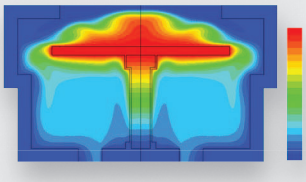

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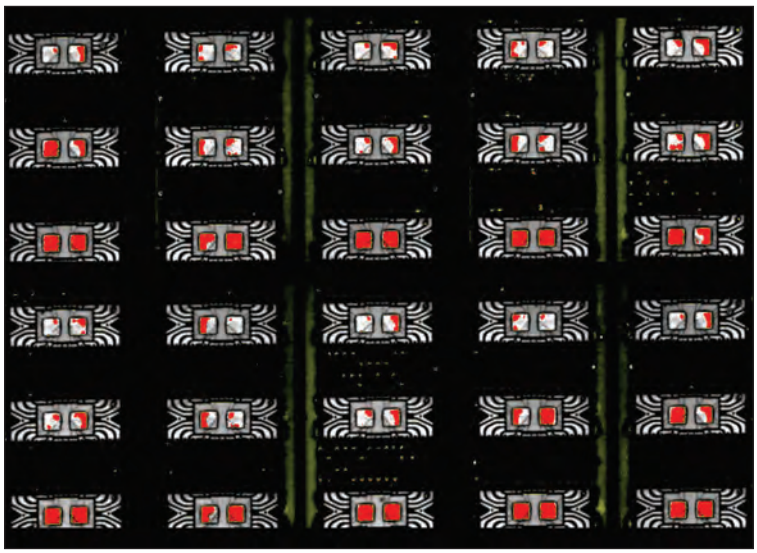

Figure 2: Acoustic image of JEDEC-style tray holding small PEMs. The numerous red features are disbonds of the mold compound from the die face - a defect very likely to break a wire bond.

sometimes altered for viewing.

- **Thru-SCAN imaging.** The echoes are pulsed into the sample, but the reflections are ignored by the transducer. Pulses that exit the bottom of the sample are recorded by a separate sensor. In a THRU-Scan acoustic image, exiting pulses are typically gray, while locations where the pulse was blocked by a gap above are black because no ultrasound was detected.

Either reflection-mode or Thru-SCAN can be used in screening parts. Where it is useful to see a defect in detail and to know the approximate depth of a defect or feature, reflection mode is employed. If the goal is simply to identify a defect at any depth, Thru-SCAN is used.

Reflection mode was used in Figure 2, which shows a portion of a JEDEC-style tray of small PEMs. In these images, red indicates internal gap-type defects. Here the defects are delaminations between the die face and the mold compound. These are particularly risky defects because they can shear off wire bonds on the chip. In this image there are probably no acceptable components.

Whichever imaging mode is used, the acoustic data and images will identify the gap-type defects in all of the components in the lot, whether the lot consists of a handful of components or tens of thousands. Imaging can also reveal some non-gap defects, such as a die that is tilted or rotated from its intended position.

Clear definitions of acceptable and non-acceptable structural anomalies should be made before screening is performed in order to determine which components to scrap and which to use in production. The overall goal is to achieve the highest product reliability without scrapping components with internal defects that are probably harmless. It is easy enough to look at an acoustic image and examine a bright white feature that indicates a gap on the die paddle or in the die attach. But how do you accurately evaluate the risk this gap presents? The results of acoustic imaging are easier to interpret if they can be compared to an existing standard.

Several industry standards are available that can be used for comparison. One is Application of Scanning Acoustic Microscopy to Plastic Encapsulated Devices, Basic Specification No. 25200 of the ESCC (European Space Components Coordination). This standard provides guidelines for determining reject of components having defects of specific sizes. For voids in the die attach material of plastic packages, this standard would reject a component where more than 50 percent of the die attach area is occupied by voids. It would also reject components where a single void occupies 15 percent or more of the die attach area, or a void in a corner than occupies 10 percent or more of the die attach area. Finally, it would reject any plastic encapsulated component where 70 percent or more of any one quadrant is occupied by voids. These are straightforward values that are measured and reported automatically by C-SAM tools.

But for a specific lot of a plastic encapsulated components, these guidelines may not be a perfect match. There are simply too many attributes that can vary from one component type to another. IPC/JEDEC J-STD-020 E, Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices, lists more than 20 critical attributes. If even one of these attributes is changed in the redesign of a component, the component may need to be requalified for moisture sensitivity. The critical attributes include items such as die thickness, die passivation, wafer fabrication process, die attach process, and lead frame finish.

J-STD-20 is an industry standard, but was not designed for predicting overall reliability. It measures the ability of a given lot of plastic encapsulated parts to survive exposure to atmospheric humidity during assembly. A component's moisture sensitivity level is related to overall reliability, but generally does not accurately predict that reliability. It is not uncommon for engineers arranging for the acoustic inspection of one or more lots of components at one of Sonoscan's applications laboratories to mention that they would like to use J-STD-20. It may be an appropriate choice, or lab personnel may suggest a standard more directly related to reliability. If the customer is concerned about die attach defects, a good choice may be MIL-STD-883 Method 2030, Ultrasonic Inspection of Die Attach, or PEM-INST-001: Instructions for Plastic Encapsulated Microcircuit

> Since each component has its own profile of attributes, finding an industry standard that is, without modification, a satisfactory match for a given component can be difficult

(PEM) Selection, Screening, and Qualification. The customer's goal typically is to screen out those components whose internal structural defects are very likely to cause defects - multiple long delaminations on the top side of many of the lead fingers, for example, or voids that occupy 70 percent of the die attach. The more critical the application, the less risky will be the defects that can be accepted. Since each component has its own profile of attributes, finding an industry standard that is, without modification, a satisfactory match for a given component can be difficult. Often a standard needs to be altered to fit well with a particular component; even J-STD-20 is used, with appropriate modifications. The odds of successful acoustic screening can be improved if the customer acquires more information about the component to be screened and its application.

Customers can acquire this information by performing some form of life test on the component in question. Depending on the particular hazards the component will face in service, the user might employ thermal stress testing, mechanical shock testing, radiation testing, or another test type. Putting the results of testing together with an industry standard should bring the user closer to achieving optimal results from acoustic screening. Life testing might reveal, for example, that thermal stress causes small delaminations between the die attach and the die, but that additional thermal stress does not greatly enlarge these delaminations.

Figure 3 is the acoustic image of a PEM before and after 1000 cycles of thermal testing. Before testing, there were delaminations on several of the lead fingers where the wires are bonded. After 1000 cycles, these delaminations have hardly changed, but the mold compound is now delaminated from essentially all of the area around the die. The testing has identified two anomalies that should be sought during acoustic screening.

Additional insight is available from Sonoscan's test lab personnel, who have imaged thousands of different plastic encapsulated microcircuits, and who can help with modification of standards. The lab references about a dozen military and industrial standards for screening PEMs, but these are often just starting points. Many companies that use the lab have developed and maintain their own standards. Standards can be modified in any way that will benefit a particular application. If, for example, there is a hot spot on the die, instructions can be written to reject a component having any heat-blocking anomaly at the same x-y coordinates.

Occasionally an acoustic imaging mode other than reflection or THRU-Scan modes is used for specific purposes. If a component is likely to have structural defects at multiple depths (a TO-220, for example), an imaging mode can be used that scans multiple depths. There is no reduction in scan speed, and each depth produces its own acoustic images.

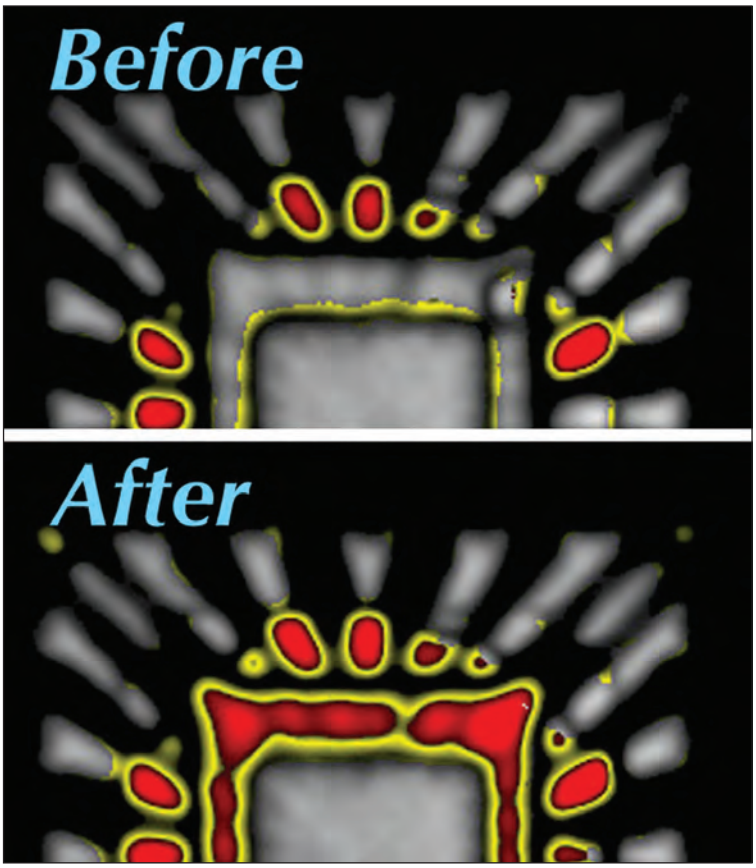

Figure 3: A PEM imaged acoustically before and after 1,000 thermal stress cycles, which had little impact on existing voids but which the die paddle to delaminate from the mold compound.

ELASTOMER SEALS: PURITY OR PLASMA RESISTANCE? CAN YOU HAVE BOTH?

Reducing cost in semiconductor manufacturing is a constant way of life and reducing cost of consumables (CoC) is just one of many ways in which the industry can become more competitive and hence, more profitable. The seal type or material is an integral part of this cost equation. Knut Beekmann, Market Manager for Semicon and Dr Murat Gulcur, Senior Scientist at Precision Polymer Engineering (PPE) explain.

IN SEMICONDUCTOR MANUFACTURING, particle contamination throughout the whole process flow is a significant threat to yield and hence profitability. It's also not just a matter of limiting the total number of particles but, particle size can also be a critical factor. Key manufacturing technologies include vacuum processes such as dry etch and deposition, all of which require elastomer seals to maintain the vacuum integrity. Seals in critical locations, meaning in direct contact with the process and in relatively close proximity to the substrate being processed, are often exposed to extremely aggressive chemistries and variable temperatures.

The net effect is always some kind of physical degradation of the seal over time, the most obvious being erosion. The seal needs to be compatible with the maintenance period of the tool and should not be the limiting factor in determining mechanical intervention or labour intensive additional down time. Furthermore, the seal should not contribute to yield loss through whatever erosion by-products may be formed.

Reducing cost in semiconductor manufacturing is a constant way of life and reducing cost of consumables (CoC) is just one of many ways in which the industry can become more competitive and hence, more profitable. The seal type or material is an integral part of this cost equation.

Background

The choice of seal materials available to end users can be bewildering. Without the luxury of having test chambers or fab production equipment dedicated to testing a multitude of seal materials in the various applications, the choice becomes a potentially risky one, which involves making a change and running live product using a new seal.

The effort must therefore be rewarded with a cost saving that is commensurate with the risk or resource required to carry out such a test. Such a saving can be achieved either through an extension of the uptime cycle, a reduction in the part cost or, a combination of the two. In order to greatly alleviate the risk of incorrect seal choice, potentially leading to scrapped product or wasted test resource, a comprehensive study has been carried out to benchmark seal materials from the leading elastomer O-ring suppliers. The creation and maintenance of such a database serves to greatly offset the risk associated with

changing a seal material in order to reduce CoC and increase profitability or competitiveness.

Methodology

End users often run processes that are tuned to individual needs. It is also normal practice for manufacturers to keep such detailed process information confidential. To test every seal material in every process would be an impractical task. There are however, common chemistries used in plasma etch and deposition and this study was designed to test the various different elastomer materials in the more aggressive chemistries and plasma conditions. The process chemistries chosen are commonly used for etching of silicon, metals, compound semiconductors, dielectrics, resist ashing and particularly aggressive deposition chamber etch. Various different plasma modes were also employed, reflecting a variety of different process requirements. This included direct parallel plate, high density remote inductively coupled plasma (ICP) and sources specifically designed to create high radical and in particular, high fluorine radical content.

In all cases, elastomer materials were placed on the substrate holder on a carrier and subjected to the various process chemistries and plasma sources for fixed periods of time. The substrate holder was not biased to more closely represent the case where a seal would sit within a groove or retaining feature and as a result, would not normally be subject to significant ion bombardment. Materials were evaluated for their relative erosion rates or, mass loss and observation of surface particle formation. TGA spectra were also carried out in order to determine the nature of the material compound and in particular whether the material was purely organic and filler free, contained organic filler or, contained inorganic filler. The process chemistries chosen were:

- O2 in a direct parallel plate plasma system
- O2 in a remote ICP system
- Cl2, BCl3, HBr in a remote ICP system
- SF6, O2 in a remote ICP system
- SF6 in a low volume ICP optimized high radical plasma system

Figure 2: Oxford Instruments PlasmaPro ICP high radical etch system

Figure 1: Oxford Instruments PlasmaPro ICP etch system

The fillers used in the compounding play an important role in the plasma resistance of the elastomers. Most organic polymers have higher etch rates than the fillers. In order to achieve optimum, etch resistance, organic polymers are usually compounded with various types of fillers. The filler particles shield the organic backbone of the elastomer from erosion and therefore improve the plasma resistance of the elastomer material.

The filler particles which are dispersed and trapped within the polymer matrix however; can become free after the polymer matrix is etched away. These free particles on the elastomeric seal can cause contamination and therefore reduce product yields in chemically aggressive processes. In order to minimize the risk of particle contamination and decrease erosion rates, some advanced filler systems can be used in the plasma

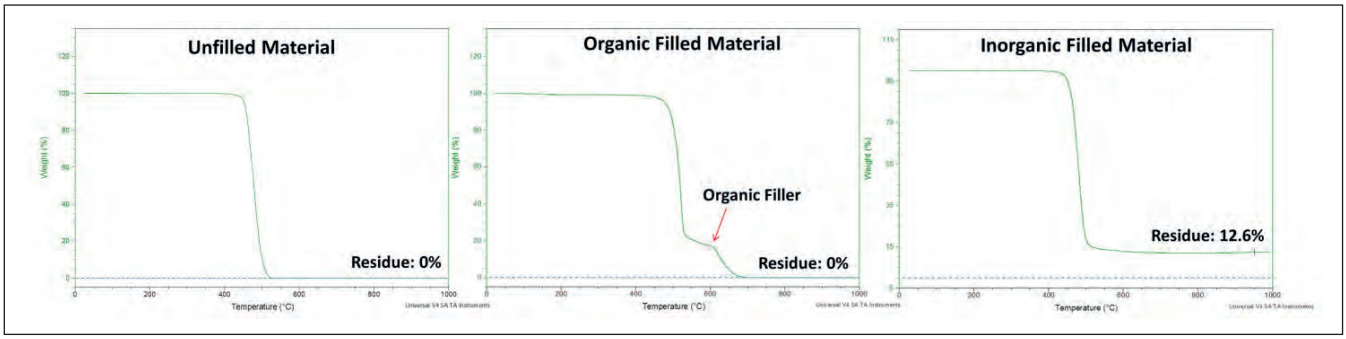

Figure 3. Thermogravimetric analysis (TGA) curves of A filler-free, B organic and C inorganic filled elastomer materials

resistant elastomeric material formulation. Minerals, metal oxides and synthetic fillers are some examples of advanced filler systems. In general, the fillers can be classified in two groups as organic and inorganic fillers. Inorganic fillers provide better erosion resistance when compared with organic fillers because of their rigid crystal structure and relative chemical stability. The chance of contamination however, is generally lower when organic fillers or no fillers are used in the elastomer formulation, with the disadvantage that erosion rates are considerably higher than their inorganic filled counterparts.

Results

The Thermogravimetric Analysis (TGA) curves in Figure 3 show the differences between the elastomer formulations with different filler types. A pure elastomer formulation with no fillers decomposes completely at around 500°C leaving no residue (Figure 3A). Similarly, a formulation prepared using an organic filler also fully decomposes at around 600°C without leaving any residue. In this case, the decomposition of organic filler can be observed in the TGA by a characteristic shoulder at slightly higher temperature than the polymer degradation (Figure 3B). A residue is observed in the inorganic filled elastomer even at high temperature after the organics in the formulation are fully decomposed (Figure 3C). The amount of remaining residue corresponds to the amount of filler used in the formulation. As mentioned above, the chance of particle formation and hence contamination, by using an unfilled or organic filled elastomer is lower than that from a traditional inorganic filled material but the etch rates of inorganics are lower than the organic filled or the unfilled polymers.

This paradox can be resolved by using an advanced inorganic filler system which also significantly minimizes the risk of contamination. The use of lower amounts of filler with maximized surface area is an ideal solution. A filler system with very high surface area has very small particles, ideally in the nanometer size range and they need to be well dispersed. In Figure 4, the plasma erosion rates of several different

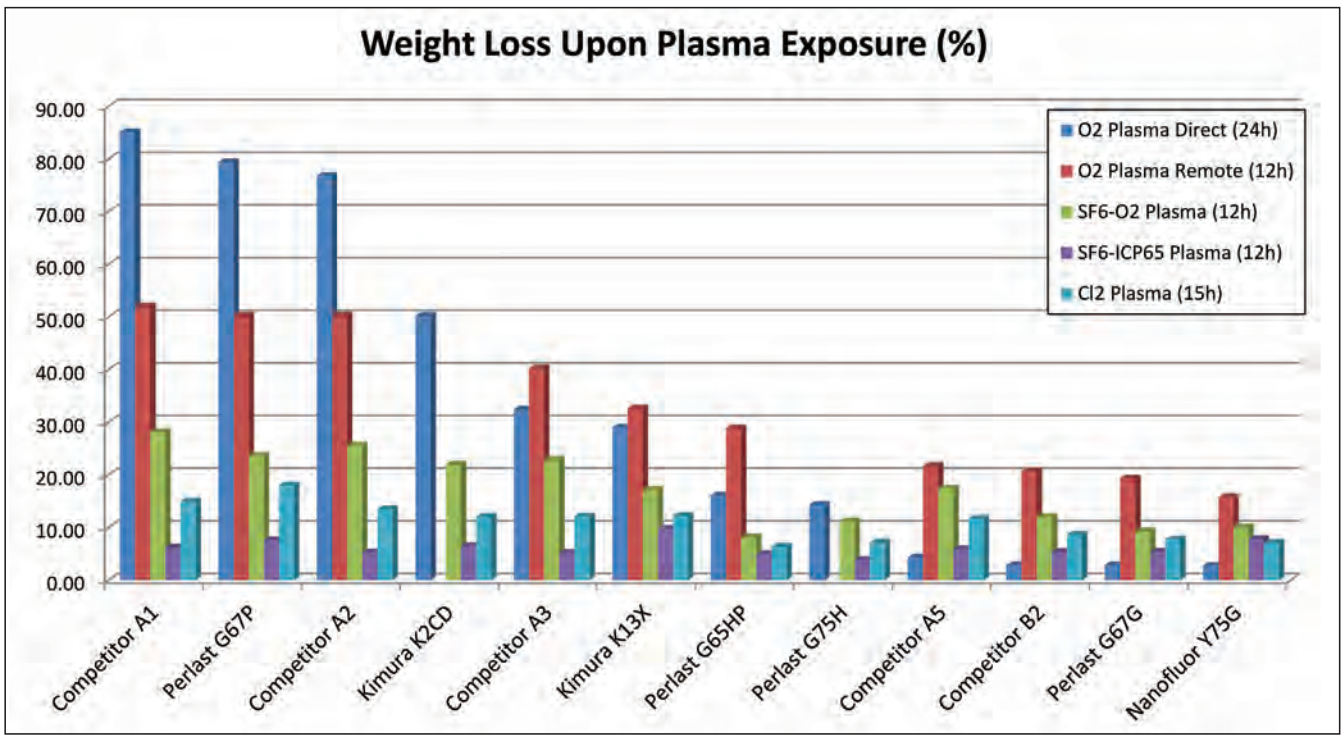

Figure 4 - Summary of the weight loss of various competitor, current and development PPE grades upon exposure to O2 (Direct and remote), SF6/O2, Cl2 (BCl3 / HBr) and high radical SF6 plasmas.

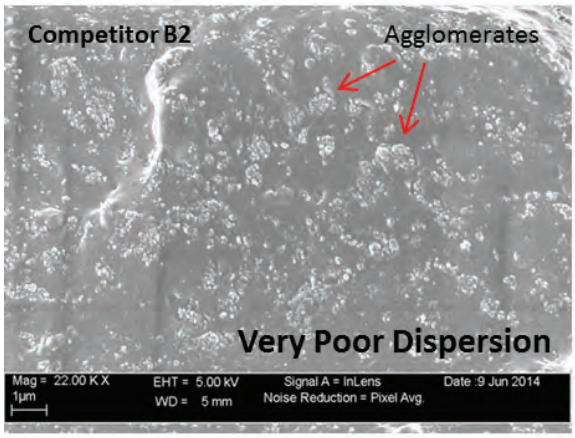

Figure 5a

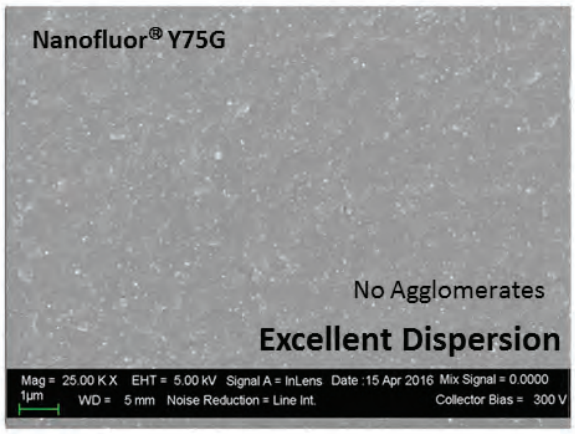

Figure 5b

fluoroelastomers are graphically presented. Perlast® G67G and Nanofluor® Y75G have been found to provide very good plasma resistance in a variety of chemistries. These grades have been uniquely compounded with relatively low levels of an advanced, non-metal oxide, nano-filler system which has an average particle size of 25-40 nm.

The dispersion of nano-fillers[1] in the elastomer formulation is another very important factor for determining the plasma etch resistance and potential for particle contamination upon plasma exposure. Nano-fillers must be perfectly dispersed in the polymer matrix to achieve maximum plasma etch resistance and minimum chance of contamination of the wafer or substrate being processed.

Nanoparticles have very high surface energy and very large surface area. In order to diminish this energy, they naturally prefer to form agglomerates or clumps which consist of several or up to several hundreds of individual nanoparticles.[2] These agglomerates must be broken into single nanoparticles when compounding and dispersed uniformly in the polymer matrix. If this is not achieved, these agglomerates will behave as macro sized particles and can be released as micron sized defects upon plasma erosion. This phenomenon can be seen in the cross-sectional SEM image of an unused sample, Figure 5A, which is a very good example of poor filler dispersion. As can be seen in Figure 5B, Nanofluor® Y75G however, exhibits excellent Nano filler dispersion and therefore provides significantly reduced chance of contamination or, generation of killer defects.

Providing a smooth surface after plasma erosion is also very important for critical sealing applications. Excellent dispersion results in a smooth surface even after plasma exposure. Poor dispersion causes a rough and uneven surface as a result of inconsistent etch rates on the surface (Figure 5). The TGA analyses of grade B2, Perlast® G67G and Nanofluor® Y75G in Figure 7 shows that the amount of nano-filler used in grade B2 is 20-35 percent higher than in either G67G or Y75G respectively. This therefore leads to a higher risk of particle contamination from grade B2.

Summary

During aggressive vacuum wafer processing, elastomer seals

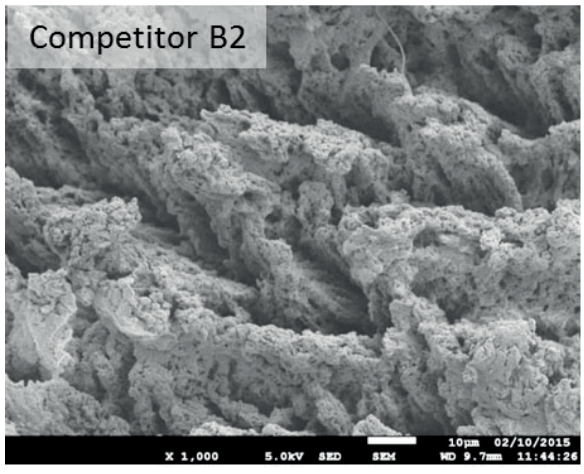

Figure 6a

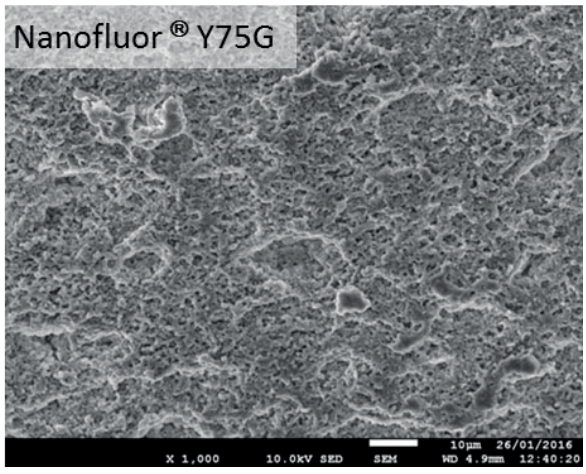

Figure 6b

in key tool locations will be subject to wear during normal operation and will expose the wafer to the degradation by products of the elastomer material and also to any compounded materials contained within the elastomer. As evidenced by the erosion rates, there is inevitably a compromise between using seal materials that are completely free from any filler and organic fillers and those that use inorganic filler systems although some overlap between materials can be seen.

The best solution is generally to use inorganic materials which have well dispersed nano-fillers in the compound, which therefore offer optimized erosion and hence seal lifetime and greatly reduced chance of yield limiting particle contamination.

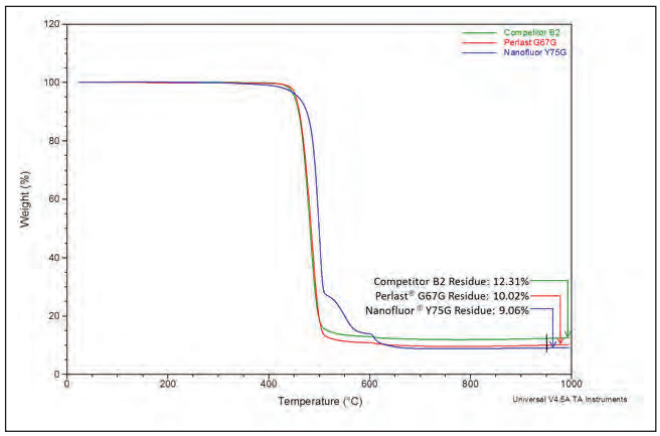

Figure 7 - TGA curves of Nanofluor® Y75G, Perlast® G67G and Grade B2.

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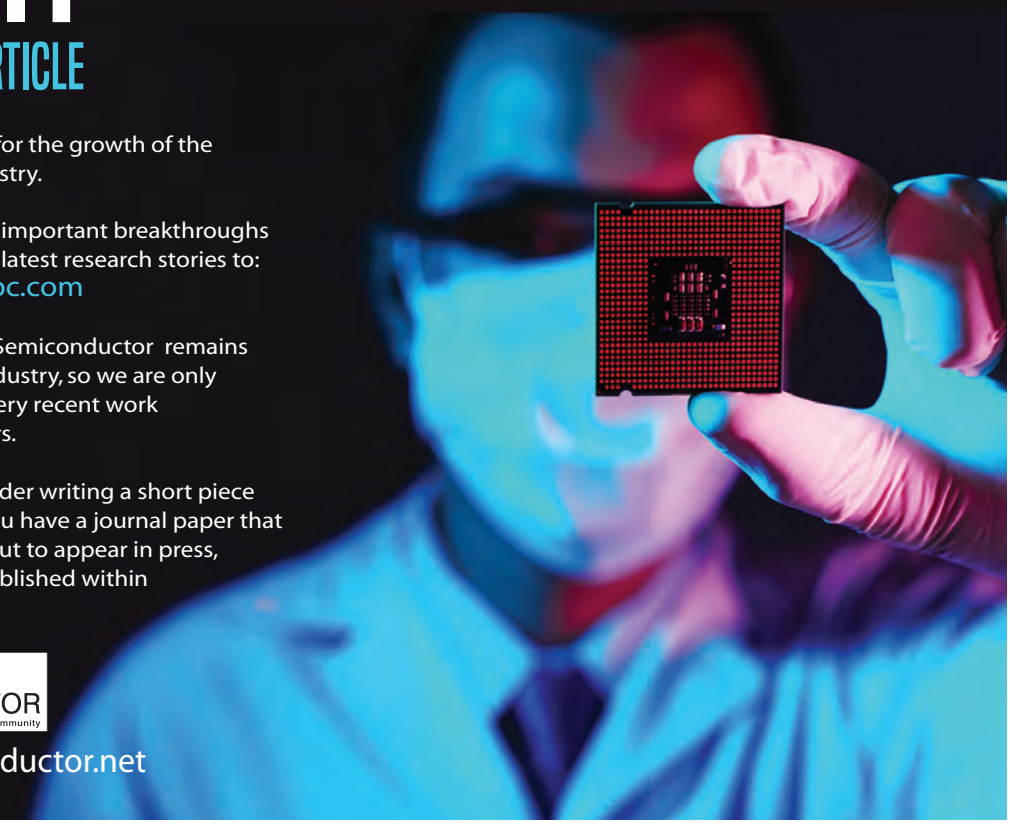
1- Mark, J. E.; Erman, B.; Eirich, F.R. (Eds.) (2013) The Science and Technology of Rubber (4th Ed); Elsevier Inc., Oxford, UK. ISBN: 978-0-12-394584-6

2- Walter, D. (2013) Primary Particles – Agglomerates – Aggregates, in Nanomaterials (ed Deutsche Forschungsgemeinschaft (DFG)), Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, Germ



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Researchers seek elusive pellicle solution

Readying extreme ultraviolet lithography (EUVL) for high volume manufacturing has presented many challenges along the road to creating next-generation semiconductors. Imec researchers believe they are a step closer in delivering a much needed pellicle solution.

WITHIN A FEW YEARS, the lithographic community needs a suitable pellicle to protect photomasks during extreme ultraviolet (EUV) exposures in high-volume manufacturing. While developing a new technology involves many vexing challenges, some seemingly innocuous aspects have far-reaching implications. Developing a pellicle to protect photomasks is very challenging since EUV light is absorbed by most materials. Whatever pellicle is chosen must be greater than 90% transmissive at EUV's 13.5nm exposure wavelength. Materials that work for other lithographic processes do not work well in EUV. Thermal, chemical and mechanical requirements complicate pellicle development.

Emily Gallagher, principal engineer at imec, and her team are screening many candidate materials from both imec and partner organizations to assess suitability. In this article Gallagher explains the imec approach to pellicle development, and highlights carbon nanotubes as one of the promising solutions.

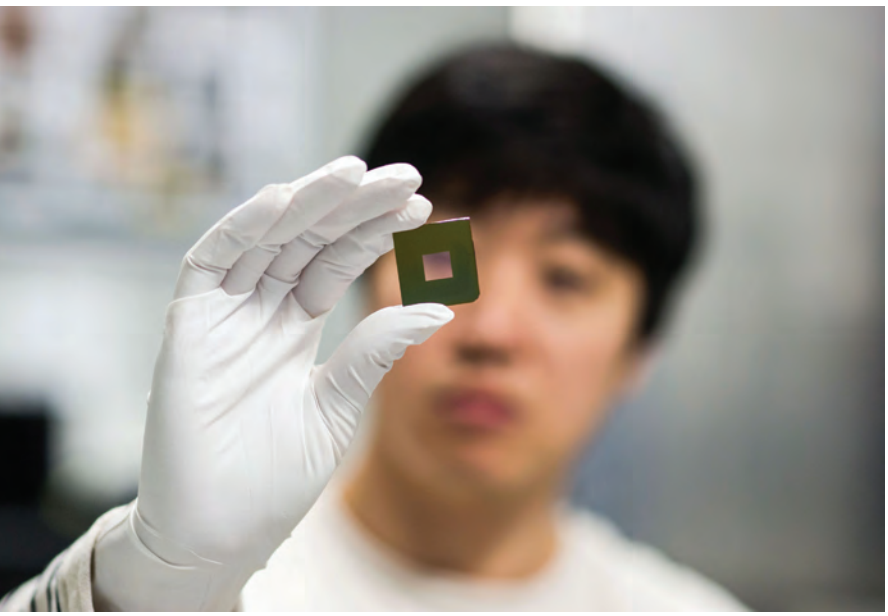
Why a pellicle?

Employing a pellicle is common practice in deep ultraviolet (DUV) lithography utilizing 193nm and

Imec researchers discussing a pellicle sample in development for use in extreme ultraviolet lithography.

248nm wavelength exposures. The pellicle membrane protects the photomask from contamination. But the different exposure wavelength in EUV complicates pellicle choices.

"(The pellicle) is mounted a few millimeters above the surface of the photomask so that particles that land on it will be too far out of focus to print. For DUV, thin film pellicles can be fabricated from low-cost fluoropolymers. They are inexpensive and transmit over 99 percent of the light, ensuring that the imaging impact is minimized," Gallagher explained. "But extreme ultraviolet lithography (EUVL) is a different story. The 13.5nm EUV light is absorbed strongly



Jae Uk Lee from imec's pellicle membrane development team, handling a EUVL pellicle sample.

by most materials, including fluoropolymers. Also, the pump-down sequences in the EUVL vacuum system and the high intensity of the EUV light source complicate the development of a suitable pellicle solution."

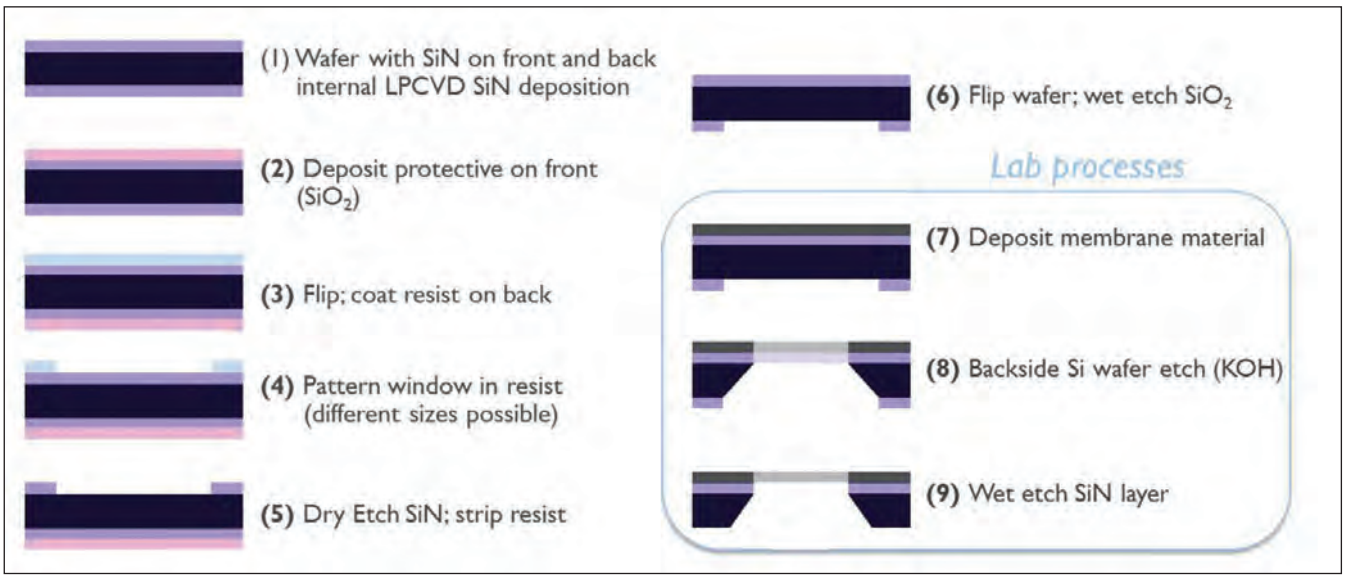
Gallagher added that the industry initially planned to introduce EUVL into manufacturing without any pellicle. The idea was to make the photomask handling and exposure vacuum chamber particle-free, eliminating the need for a protective membrane. However, after defectivity assessments, the chip industry is convinced that a pellicle solution is mandatory for high-volume EUV exposure tools. The pellicle is currently considered a major area for EUVL development.

"While considerable progress has been made in improving the EUV source power, resist sensitivity and mask blank defects – areas that are also considered major challenges – a suitable pellicle for high power exposure (greater than 250 W) has not yet been found. That's why we initiated a project for pellicle membrane development as part of imec's Advanced Lithography Program. Our goal is to have a solution ready within two or three years from now, the time when the IC industry will need a pellicle for their high-volume EUV lithography tools," she said.

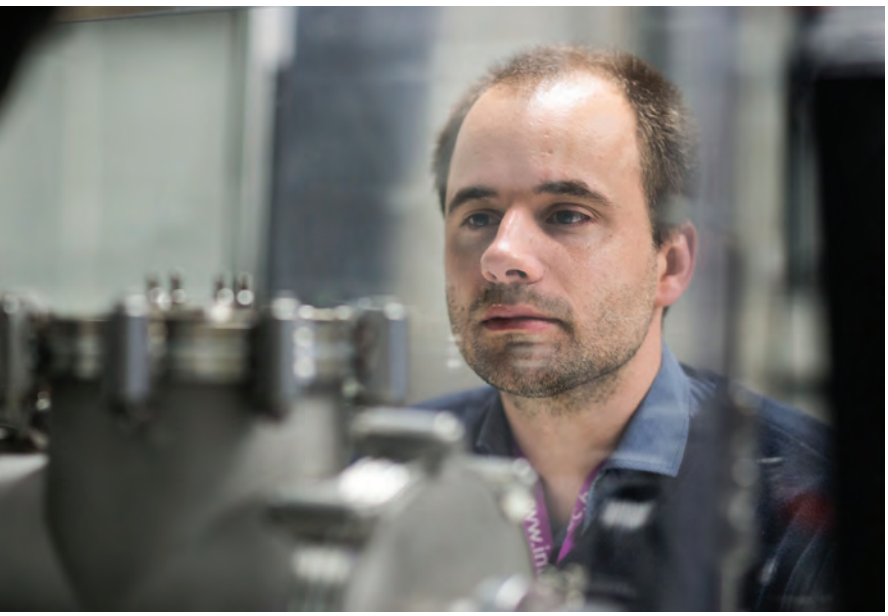
Optical, mechanical, chemical and thermal challenges

One of the most important requirements for the EUV pellicle is related to the transmission of EUV light. Gallagher noted that during EUV exposure, single-pass transmission (including light passing through the pellicle) must be at least 90 percent in order to ensure the productivity of the EUVL tool at a targeted source power of 250 W. Too low of a transmission would reduce the effective exposure power, hence the productivity of the tool (measured as wafers exposed per hour,) would be negatively impacted.

Finding a material with sufficient transmission qualities is very challenging since EUV light is absorbed by almost all materials. The pellicle also needs to be mechanically stable, which is difficult to achieve for membranes that are thin enough to meet light transmission requirements. In practice, thin pellicle membranes are mounted on a frame and fixed to the photomask. During use in the EUVL scanner vacuum chamber pellicles are subjected to handling and periodic pump-down/vent cycles, which enhance the risk for bulging and finally breaking membranes. Pellicle lifetime could also be affected by the presence of hydrogen radicals in the scanner since highly



Imec's SiN membrane platform for fabricating thin pellicle solutions.



Johannes Vanpaemel from imec's pellicle membrane development team photographed at the experimental bulge tester.

reactive hydrogen is used to keep the chamber sidewalls and optics clean, but it could also react with the pellicle material. Thermal considerations also complicate pellicle choices.

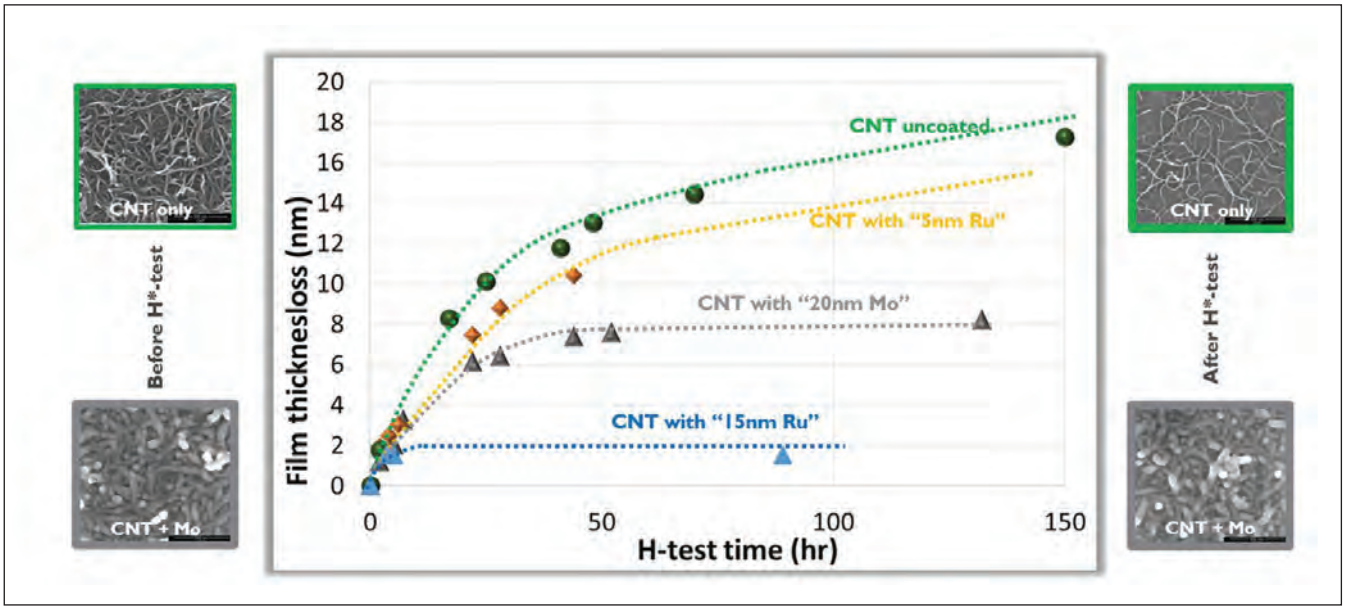
"We need to (also) take account of some thermal considerations. Some of the light that is not transmitted is absorbed, heating the membrane considerably. However, heat transfer options through evaporation or convection are minimal for a material in vacuum; heat conduction is very limited for a thin membrane. The only way to transfer heat is radiation. For some materials, additional emissivity layers will be needed to enhance radiation and decrease the peak temperature of the pellicle. These capping layers can also serve to protect the pellicle from hydrogen etching if selected appropriately," Gallagher said.

Imec's approach to pellicle development

To meet transmission requirements, it is logical to start with low absorption materials. This translates into selecting a material with a low EUV absorption coefficient k. Both silicon (Si) and carbon (C) fulfill this requirement.

"After choosing the right material, we can reduce the absorption even further by thinning and by reducing the density of the material. The latter can be done by either inducing voids (e.g. by etching into a continuous film), or by depositing a material that is inherently porous, like carbon nanomaterials," Gallagher explained. EUV pellicles have been in development for more than a decade. Reasonable options have already been proposed, but they all have their issues. Either the pellicle development is too immature (as is the case with graphene), or the pellicle membranes break at higher source powers (as is the case with poly-silicon or silicon nitride-based pellicles). A key element of imec's strategy is developing alternative solutions. "Building on existing solutions brings no additional value to our partners," Gallagher observed. One of many potential pellicle materials tested by imec are carbon nanotubes (CNTs). Carbon nanomaterials, like CNT films, can have an extremely low density, so the transmission is likely to be high.

"We also expect them to add to the membrane's mechanical strength. Another nice thing about carbon



Results from the hydrogen tests with coated and uncoated CNTs. Coated CNT demonstrate a flat response after exposure to H radicals as required.

nanotubes is that their properties are tunable. This means that issues with the material can possibly be solved by careful engineering," she said.

Carbon nanotube pellicles can be fabricated using imec's 300mm process flow and can be scaled for larger wafer sizes. The pellicle process starts with a silicon wafer. Deposition, patterning and strip processes are deployed to create a flexible platform for membrane development. Silicon nitride (SiN) can serve several functions. It can either be thinned and used as a part of the final membrane stack, or it can be etched away so it is not part of the final membrane. The 300mm platform is compatible with scaling-up membrane sizes, targeting 10 x 10cm^2 and even larger, which is important for developing 450 mm silicon wafer technologies. CNTs process ed on this membrane platform successfully passed several tests that have been established at imec to evaluate potential pellicle solutions.

"The transmission of a stack of three to four layers of nanotubes (~50nm thick) was measured to be higher than 95%. The CNT-based pellicle was also subjected to mechanical testing. At imec, we built an experimental bulge tester that (can) apply a differential pressure across the membrane to test the point at which the pellicle bursts. This burst pressure is then compared to identical SiN membranes without additional layers. The measurements clearly show an improved durability when CNTs are added to the membrane.

"We also looked at the impact of hydrogen (H), which is particularly worrisome since hydrogen is known for etching carbon. The results from our hydrogen tester indeed showed that CNT films loose thickness after long exposure to hydrogen radicals. Fortunately, we can solve this issue by coating or encapsulating the CNTs with a suitable material that has minimal impact on EUV transmission, such as ruthenium or molybdenum," she explained.

Advancing EUVL pellicle development

Besides developing and evaluating its own pellicle solutions, imec is also screening pellicle materials developed by partners and other external suppliers. Gallagher said that EUVL pellicle development is a very complicated and challenging activity.

"Carbon nanotube pellicles can be fabricated using imec's 300 mm process flow and can be scaled for larger wafer sizes. The pellicle process starts with a silicon wafer. Deposition, patterning and strip processes are deployed to create a flexible platform for membrane development. Silicon nitride (SiN) can serve several functions. It can either be thinned and used as a part of the final membrane stack, or it can be etched away so it is not part of the final membrane"

To accelerate development, imec believes it is important to have many companies exploring multiple paths in parallel, and to engage the EUVL community. For this reason, imec has made its testing processes available for partners including its in-house capabilities for optical, mechanical, chemical and thermal testing. This puts imec in a unique position.

"If we need a solution within two to three years, we must exploit this infrastructure to the maximum. With our carbon nanotube-based pellicle, we have a promising path forward, but we remain open to alternatives since enabling an industry solution constitutes a success for imec and for our partners," she concluded.

- "Collaboration is the centerpiece to push the limits of lithography", vision by Greg McIntyre in imec's 2015 annual overview.

EMILY GALLAGHER has been a principal engineer at imec since 2014. Her work currently focuses on pellicle membrane development, EUV imaging and photomasks. Prior to this position, she was a senior technical staff member at IBM leading the extreme ultraviolet lithography (EUVL) mask development effort there. She grew up in Montreal, Canada, studied physics in the US, earning her PhD from Dartmouth College with a thesis on free electron lasers. She has authored over 70 technical papers, written two book chapters on photomasks and holds 18 patents.

Wafer defects can't hide from Park Systems

Atomic Force Microscopy (AFM) leader Park Systems has simplified 300mm silicon wafer defect review by automating the process of obtaining high-resolution 3D images, making it faster and simpler than ever before.

SEMICONDUCTOR MANUFACTURERS have options for defect review once inspection tools have identified potential flaws on bare silicon wafers. While conventional AFM provides data-rich 3D images, the process is slow compared to 2D, SEM-based techniques. A new AFM process developed by Park Systems changes that equation like none other.

Park Systems (Suwon, Korea and Santa Clara, California, USA) is one of the leading pioneers of atomic force microscopy (AFM) for semiconductor manufacturers and researchers. The company's founder (Sang-Il Park, PhD) led early efforts to commercialize the technology after being an integral part of AFM's development team at Stanford University in the 1980s.

Park Systems made the extreme, high-resolution 3D imagery of AFM commercially practical, going on to develop products and software for surface roughness measurement in hard disk media that became an industry standard (the Park HDM series product family). Park's AFMs are also 'non-contact' review tools, which eliminates the possibility of tool tips accidentally touching surfaces and possibly damaging wafers under review.

While quality, data-rich images have been a hallmark of Park's AFMs from the beginning, this extreme quality came at the price of speed and simplicity. The company subsequently automated AFM scanning for disk media and has now brought a similar approach to reviewing defects of interest (DOI) on silicon wafers up to 300mm. Its hardware and software also support extreme ultraviolet (EUV) reticle photo masks, a critical step in creating future 450mm silicon wafers.

Finding silicon wafer DOIs is challenging. All bare silicon wafers have a unique crystalline structure that is prone to small defects (Figure 1)that may be one nanometer or smaller. Manufacturers determine threshold sizes of interest along with shape and

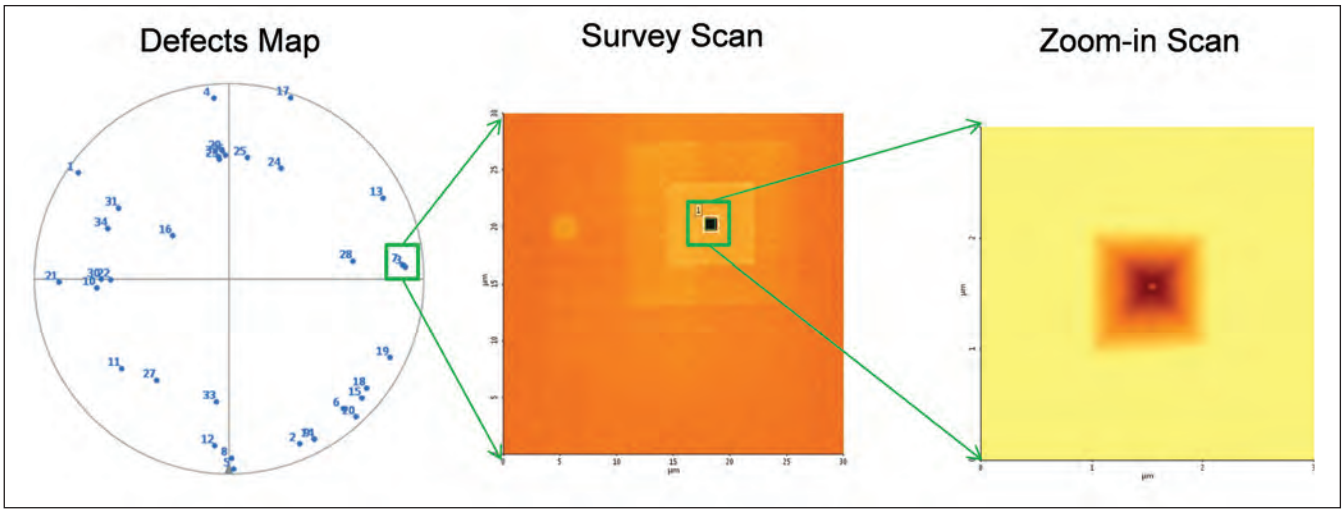


Figure 1: After coordinate mapping, ADR AFM will automatically perform a survey scan, zoom-in, processing, analysis and classification of each defect.

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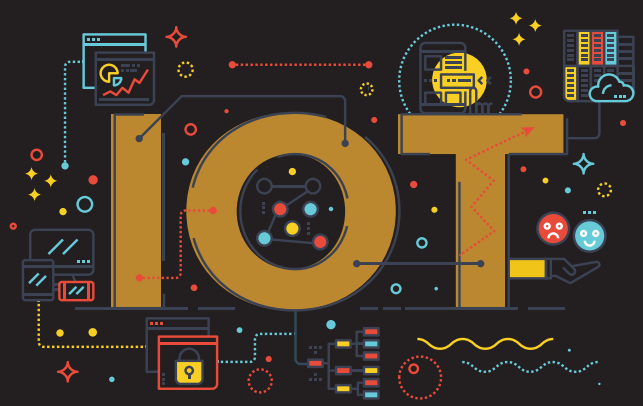

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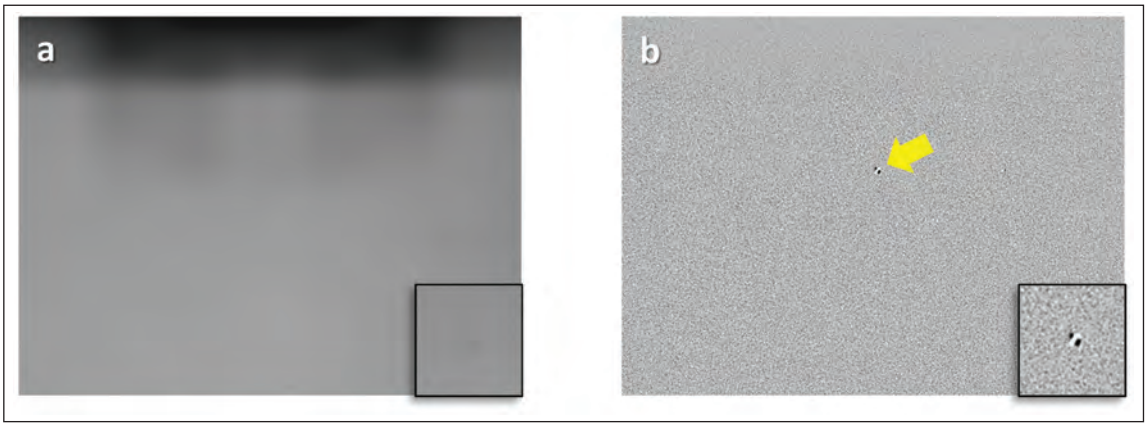


Figure 2: Images collected via (a) standard vs. (b) enhanced vision of a bare silicon wafer with one small defect. The insets show magnified views. The small defect is easily observable in enhanced vision.

depth characteristics that need attention. But while thresholds vary by manufacturer, it is clear that shrinking device geometries will impact whether defects once considered too tiny for concern could present problems for next-generation devices. There are a variety of laser light scattering techniques and process tools for inspecting wafers quickly, scanning hundreds or even thousands per hour. But inspection is just the beginning. A follow-up review by scanning electron microscope (SEM) or AFM takes inspection coordinates and zeros in on each location to image the defects. While SEM review is relatively quick, it cannot reveal much detail beyond a 2D image: a defect's 'X' and 'Y' dimensions. AFM goes much farther, creating X, Y and Z 3D images along with detailed topographic maps that further help identify and characterize an imaged DOI. AFM reveals defect details that SEM can routinely miss.

Park's AFM defect review is highly accurate, which is a key ingredient for success in an industry that measures in microns and nanometers. The accuracy of their AFMs is so great that the company holds a roughly 90 percent share of the market for hard disk drive defect review systems.

"Whether the defect is on a silicon wafer or the surface of hard drive media, the key is how accurately the review device locates it and delivers the information needed for proper defect classification. SEM may give

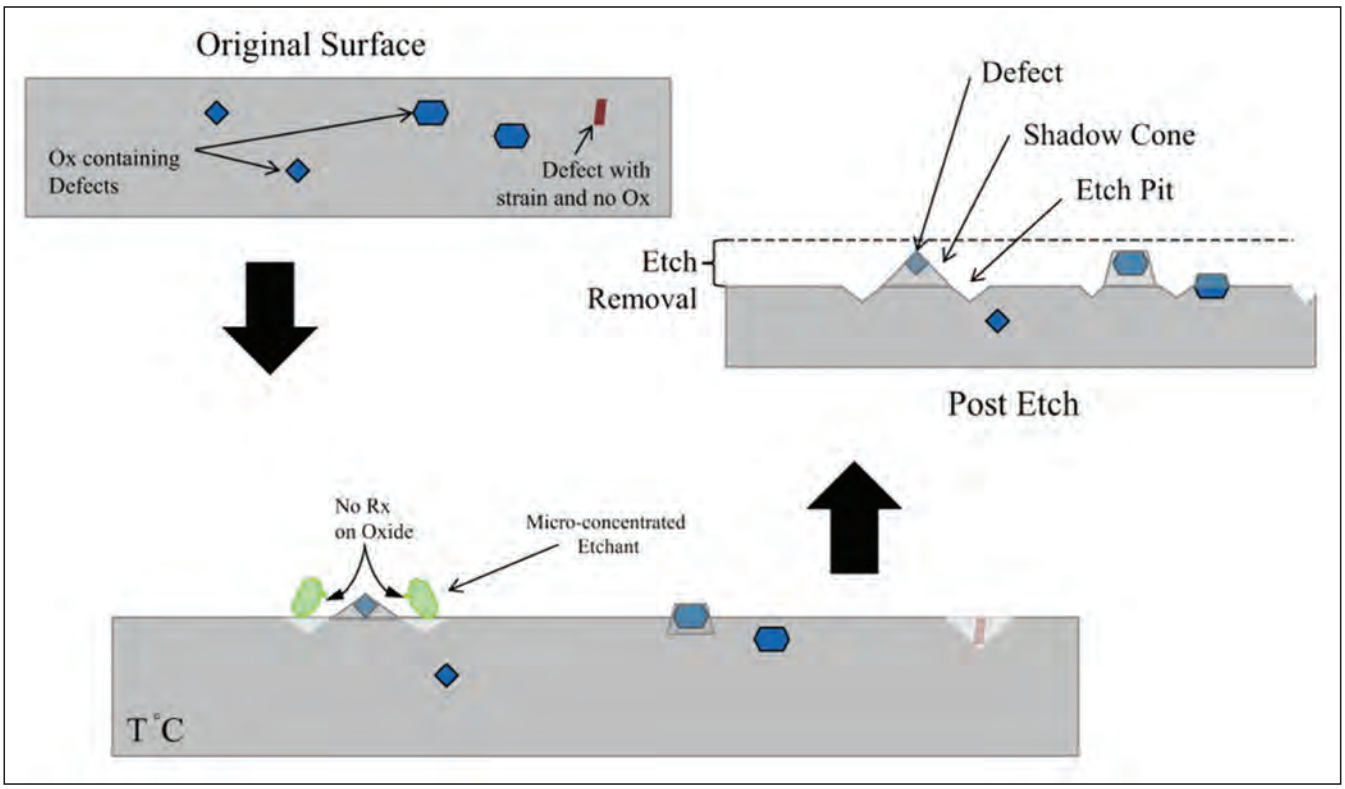
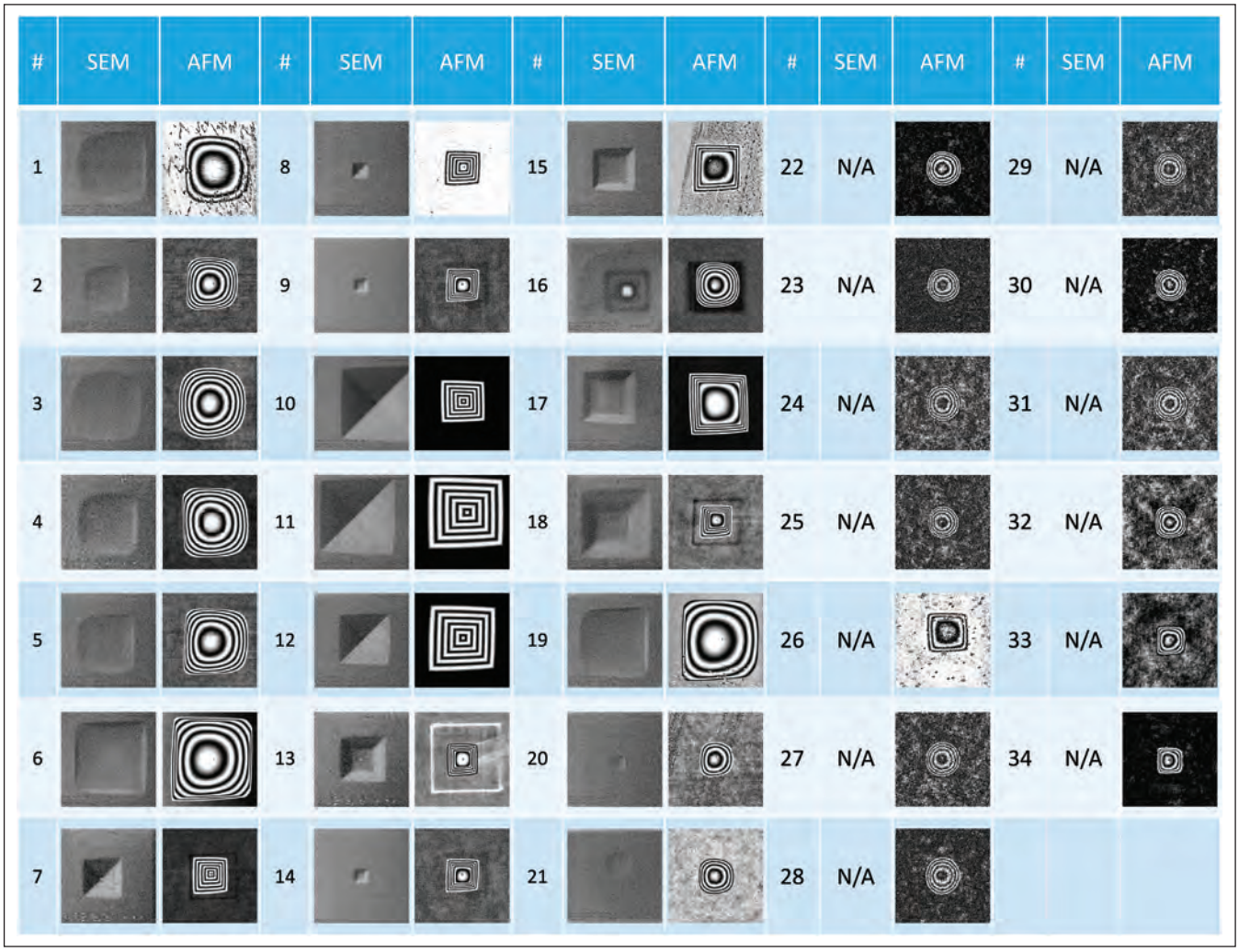


Figure 3: Schematic of the process used to decorate crystal imperfections for defect inspection.



a quick image, but it lacks the information that can be provided by AFM (see figure 4).

"As a reference tool, AFM is the 'go-to' technology. Other AFMs can be a challenge to operate, so Park Systems addresses the problem with ADR: automatic defect review. We automated defect review and simplified it, so any technician can start the review process, and then simply walk away to do other tasks while the ADR AFM is operating," said Ardavan Zandiatashbar, PhD, Park's senior applications scientist.

While different manufacturers have varying approaches to how they handle silicon wafer defects, all likely agree that better data about a particular defect determines whether it is serious enough to affect lithographic processing, or whether defects are so great in number and size that a wafer should be rejected outright.

"We started with hard drive media defect review. Manufacturers needed to know the source of defects for failure analysis purposes. While SEM can give a quick image, its image can't easily tell you if a defect is a pit or a bump or how tall or how deep it is. This is where AFM comes in; it helps you to identify and classify defects accurately and completely. We do what others cannot do," Zandiatashbar said.

Wafer defects in Park's study typically fall into eight basic categories—additional categories in different wafer surface reviews are possible. Some defects can't be classified at the inspection stage and may not fit into a typical category even after AFM review. But through AFM, the manufacturer will definitely know a defect's size and depth; they can apply their own standards to determine what actions should be taken.

"Many manufacturers want to use AFM routinely, but locating the defects and linking the AFM to inspection tools were critical issues previously. Results from conventional AFMs depend on the skill of the operator. We eliminated those issues by automating the process. Now, instead of reviewing just a few defects per day through laborious efforts and changing

Figure 4: Defect review results with ADR AFM vs. SEM are shown. ADR AFM was able to locate and image all defects; SEM did not find defects 22 to 34. AFM and SEM images are rotated 180 degrees with respect to each other.

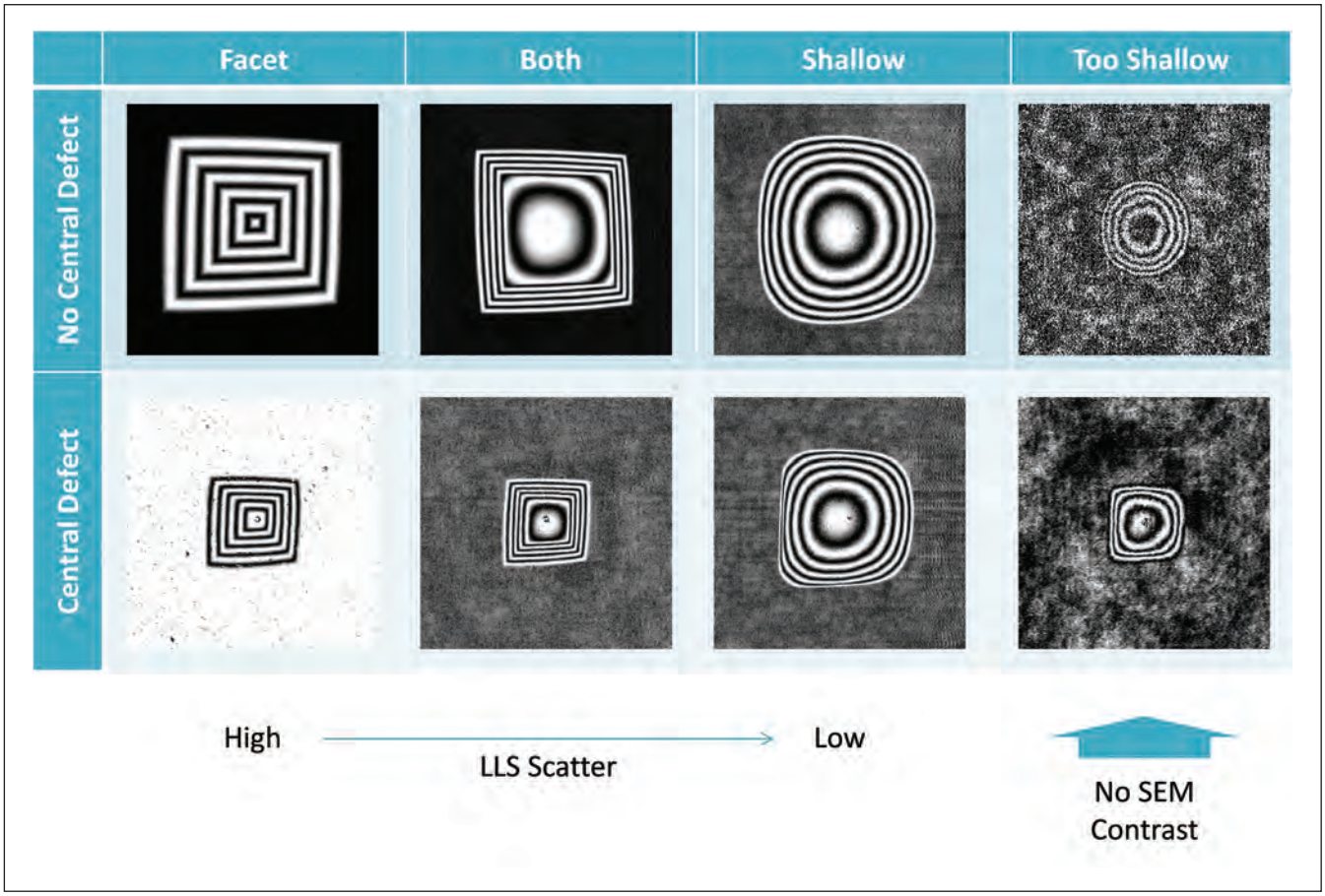


Figure 5: Defect classification based on the AFM data.

numerous tool tips, Park's ADR AFM can image and fully characterize between four and 10 defects per hour. A technician can start ADR and let it run 24/7. Manual AFM review proceeds only as quickly as a skilled operator can function," he added. "Park's ADR AFM is a turn-key solution."

In addition to automating the review process, Park's non-contact approach to AFM does not alter the wafer's surface in any way, meaning every wafer reviewed can go onto further processing as needed. SEM-based review processes have another issue beyond quality of data. Their electron beams also have the potential to 'burn' scan areas (see figure 6). This effect is typically more critical for photo-resist layers, but any disruption of a wafer's surface area can affect yield or other important factors.

The differences in results obtained using Park Systems ADR AFM compared to SEM-based results are dramatic. In a test conducted by Park, a wafer containing surface defects was reviewed using both SEM and AFM-based techniques. The ADR AFM utilized was from Park's NX-WAFER family of products. 34 defects identified at the inspection stage were candidates for review. The first 21 defects were imaged by SEM, which delivered aerial, 2D views without sufficient information about the depth or out-of-plane dimensions. The remaining 13 defects were not found by SEM despite identification during a laser light scattering (LLS) inspection (see figure 4).

Park's ADR AFM was able to find all 34 defects. The SEM had found defects down to a certain size threshold; those imaged by ADR AFM were typically

The differences in results obtained using Park Systems ADR AFM compared to SEM-based results are dramatic. In a test conducted by Park, a wafer containing surface defects was reviewed using both SEM and AFM-based techniques. The ADR AFM utilized was from Park's NX-WAFER family of products. 34 defects identified at the inspection stage were candidates for review.

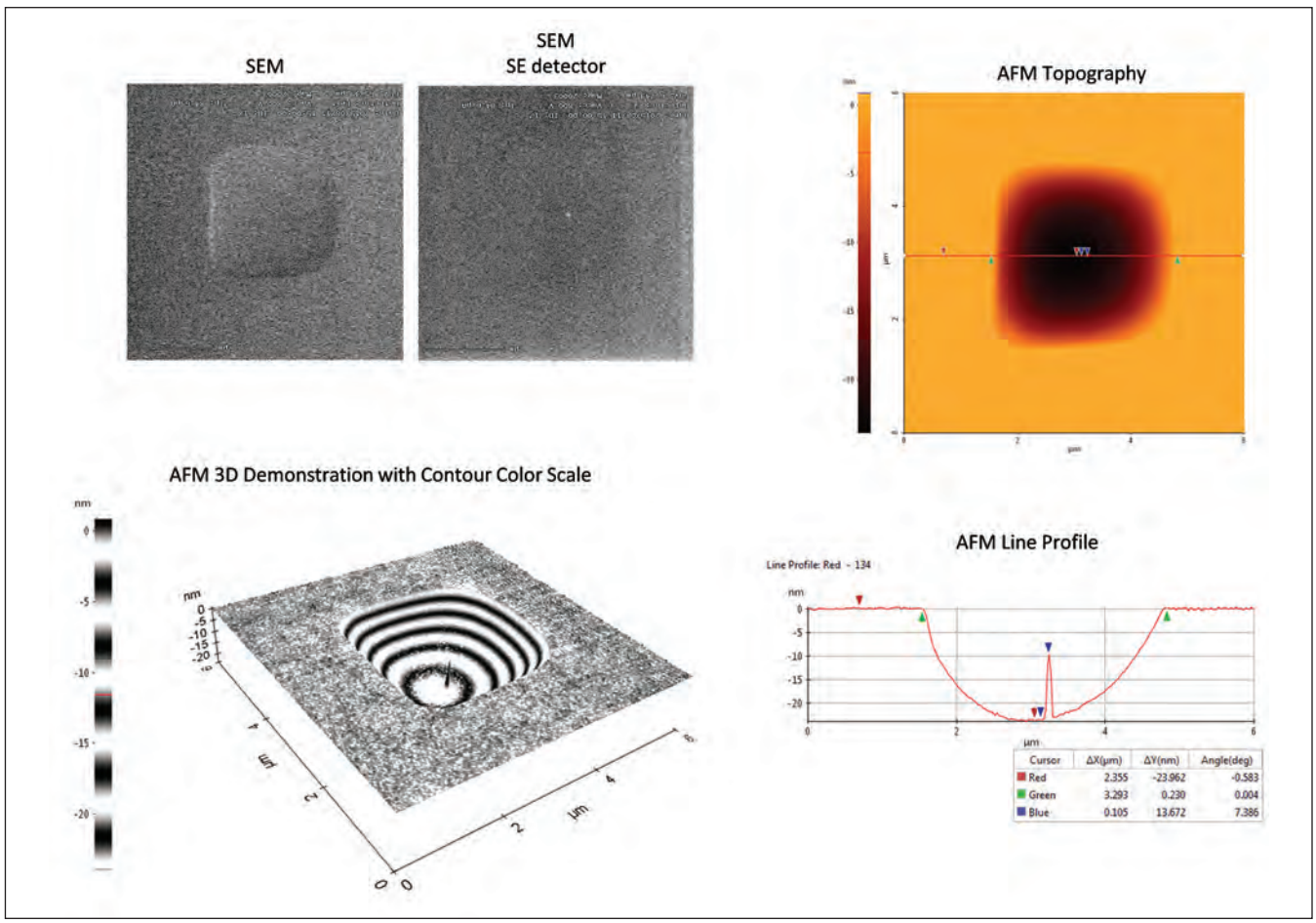


Figure 6: Comparison of data collected by SEM vs. ADR AFM. SEM shows a 2D, aerial view, while ADR AFM includes 3D data, thereby enabling a line profile, 3D construct and contoured colour scale.

smaller or shallower than defects that the SEM could identify. The SEM also had issues identifying defects that had less edge sharpness, whereas the AFM in its automated scanning mode found everything (see figure 6) .

"From the customer perspective, locating the defects of interest during the review process and determining size and depth can be critical. While SEM-based techniques can locate larger defects, it does not find them all and in fact missed 13 of 34 in this case. The lack of 3D information and SEM's inability to image the shallow and small defects matters to manufacturers. With Park's automatic defect review manufactures can have high quality 3D data of DOIs more quickly using a turn-key solution that any technician can operate," said Zandiatashbar. Automatic defect review from Park Systems maximizes productivity by up to 1,000 percent as reported by customers. But what satisfies customers most is the unprecedented level of accuracy including 3D imagery and detailed topographic information of even the smallest defects. With ever-shrinking semiconductor device geometries reaching beyond 14nm, defects critically impact microelectronic device performance. Park's approach to automating 3D imaging is revolutionary because it makes the benefits of AFM practical for leading device manufacturers and researchers pushing future product generation boundaries.

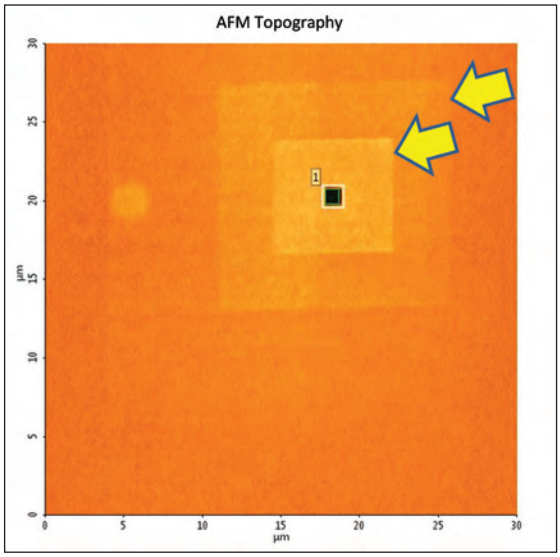


Figure 7: AFM image of a facet defect with several SEM burn-marks is shown; burns are marked by arrows.

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Pure-play foundry market surges in 2016 to reach $50 billion

THE PURE-PLAY foundry market is forecast to play an increasingly stronger role in the worldwide IC market during the next five years, according to IC Insights' new 2017 McClean Report, which becomes available later this month. The 20th anniversary edition of The McClean Report forecasts that the 2016-2021 pure-play IC foundry market will increase by a compound annual growth rate (CAGR) of 7.6 percent; growing from $50.0 billion in 2016 to $72.1 billion in 2021.

IC foundries have two main customers – fabless IC companies (e.g., Qualcomm, Nvidia, Xilinx, AMD, etc.) and IDMs (e.g., ON, ST, TI, Toshiba, etc.). The success of fabless IC companies as well as the movement to more outsourcing by existing IDMs has fueled strong growth in IC foundry sales since 1998. Moreover, an increasing number of mid-size companies are ditching their fabs in favor of the fabless business model. A few examples include Fujitsu, IDT, LSI Corp. (now part of Avago), Avago (now Broadcom Ltd.), and AMD, which have all become fabless IC suppliers over the past few years.

In 2016, the "Big 4" pure-play foundries (i.e., TSMC, GlobalFoundries, UMC, and SMIC) held an imposing 85 percent share of the total worldwide pure-play IC foundry market. As shown, TSMC held a 59 percent market share in 2016, the same as in 2015, and its sales increased by $2.9 billion last year, more than double the $1.4 billion increase it logged in 2015. GlobalFoundries, UMC, and SMIC's combined share was 26 percent in 2016, the same as in 2015.

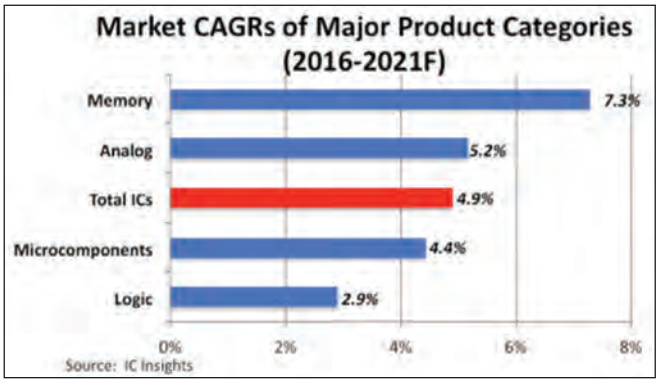
The three top-10 pure-play foundry companies that displayed the highest growth rates in 2016 were X Fab (54 percent), which specializes in analog, mixed-signal, and high-voltage devices and acquired pure-play foundry Altis in 3Q16 to move into the top 10 for the first time, China-based SMIC (31 percent), and analog and mixed-signal specialist foundry TowerJazz (30 percent). In contrast to X-Fab's 2016 growth spurt, TowerJazz and SMIC have been on a very strong growth curve over the past few years. TowerJazz went from $505 million in sales in 2013 to $1,249 million in 2016 (a 35 percent CAGR) while SMIC more than doubled its revenue from 2011 ($1,220 million) to 2016 ($2,921 million) and registered a 19 percent CAGR over this five-year timeperiod.

Seven of the top 10 pure-play foundries are based in the Asia-Pacific region. Europe-headquartered specialty foundry X-Fab, Israel-based TowerJazz, and U.S.-headquartered GlobalFoundries are the only non-Asia-Pacific companies in the top 10 group.

Memory market poised for strong growth through 2021

SALES of memory ICs are expected to show the strongest growth rate among major integrated circuit market categories during the next five years, according to IC Insights' new 2017 McClean Report, which becomes available this month. The 20th anniversary edition of The McClean Report forecasts that revenues for memory products including DRAMs and NAND flash ICs will increase by a compound annual growth rate (CAGR) of 7.3 percent to $109.9 billion in 2021 from $77.3 billion in 2016.

The 2017 McClean Report separates the total IC market into four major product categories: analog, logic, memory, and micro components. The table shows the forecasted 2016-2021 CAGRs of the four major IC product categories compared to the projected total IC market annual growth rate of 4.9percent during the five-year period. As shown, the memory IC category is forecast to show the strongest growth rate through 2021 while the weakest increase is expected to occur in the logic category, which includes general-purpose logic, ASICs, field-programmable logic, display drivers, and application-specific standard products. The strong memory CAGR is driven by surging low-power memory requirements for DRAM and NAND flash in portable wireless devices like smartphones and by growing demand for solid-state drives (SSD) used in big-data storage applications and increasingly in notebook computers. Moreover, year-over-year DRAM bit volume growth is expected to increase throughout the forecast to support virtualization, graphics, and other complex, real-time workload applications.



Analog ICs, the second-fastest growing segment, are a necessity within both very advanced and low-budget systems. Power management analog devices are critical for helping extend battery life in portable and wireless systems and have demonstrated strong market growth in recent years. In 2017, the signal conversion market is forecast to be the fastest growing analog IC category, and the second-fastest growing IC product category overall, trailing only the market growth of 32-bit MCUs.

Total micro component sales have cooled significantly. Fortunately, marginal gains in the cellphone MPU market and strong gains in the 32-bit MCU market have helped offset weakness of standard PC and tablet microprocessor sales.

Infrared, near infrared and raman spectroscopy

Bruker Optics manufactures and distributes research, analytical and process analysis instruments based on infrared (IR), near-infrared (NIR), FT-Raman and dispersive Raman Spectroscopy. These products are utilized in industry, government and academia for a wide range of applications and solutions

Q What have been the highlights of 2016 for your company?

A Bruker is the leading supplier of infrared based silicon quality control systems for impurity quantification. Compared to other e.g. wet chemical approaches the FTIR technique has many advantages such as its non-destructiveness, high sensitivity, short measurement time and specificity. Due to the new investment cycle we have seen increased interest in these solutions in 2016.

The CryoSAS is the most complete and easy-to-use FTIR Silicon analyzer on the market, allowing for high sensitivity quantification of C, O, B, P, As, Al and other impurities down to the low ppba and even ppta level. In 2016 we successfully implemented improvements such as e.g. new data evaluation algorithms to even increase the CryoSAS user benefit.

The most important highlight in 2016 was the introduction of the new SiBrickScan (SBS) for high sensitivity Oxygen analysis along the axis of complete square or cylindrical Si ingots. SBS provides valuable and early answers on Si quality and crystallization process without the need to prepare wafers or test samples.

Q Where do you see the next big opportunities coming from either technologically or geographically?

A We see an increased demand for ultra-high purity Silicon in certain electronics applications. Bruker can support this with low temperature photoluminescence systems providing detection limits less than 1ppta for residual dopants such as B or P.

Q Are you working on anything "new" for 2017?

A Of course we are always developing new products: e.g. currently we explore the option to make the SBS available for even larger ingots. Furthermore, the purity analysis of Trichlorosilane via low temperature photoluminescence of epitactic layers is a potentially hot topic for the Si industry which we plan to have a closer look at.

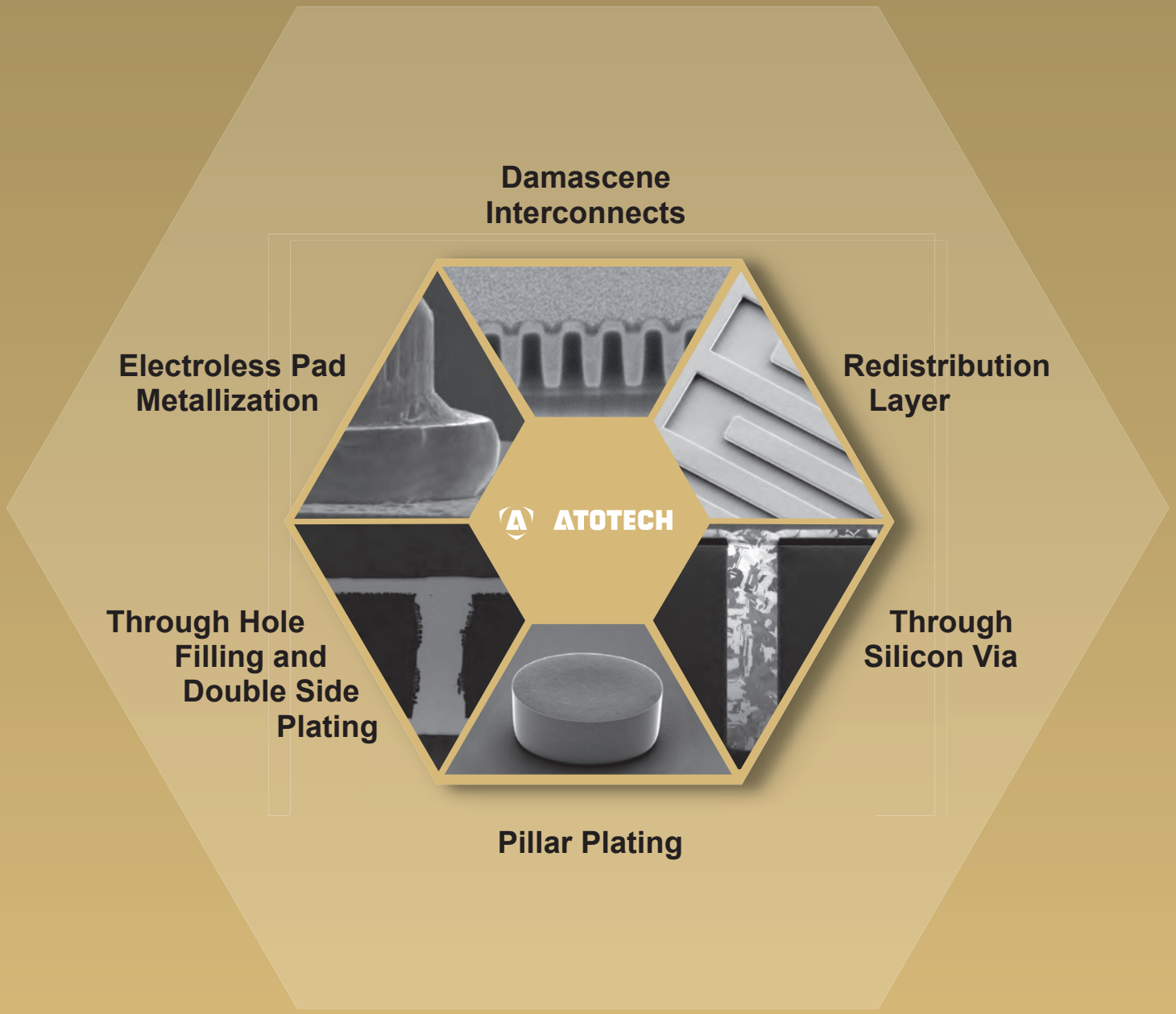
Q What, if any, major changes do you see for the supply chain in the next five years?

A In particular due to photovoltaics growth, the worldwide Silicon demand will continuously grow implying increasing Si prices and even possible shortage. Regions such as mid-east or India will play a more important role.

Q What part will your company plays in these changes?

A We will further support Silicon industry with up-to-date equipment to prove material quality and make sure that our services are available in all relevant regions of the world.

Our Semiconductor Portfolio at a Glance



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ALD SUPPLEMENT

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IN ASSOCIATION WITH EpiValence
Building Chemical Bonds

Exploring the benefits and challenges of ALD/ALE

DEVELOPING next-generation semiconductor technologies as geometries continue to shrink challenges process designers and manufacturers across the supply chain. Atomic layer deposition (ALD) and atomic layer etch (ALE) offer unique benefits, namely the ability to deposit metal alloys in layers a single atom thick. Or etch away materials with extreme precision. But there are trade-offs such as slower throughput and higher costs running counter to the needs of high volume manufacturers. *Silicon Semiconductor* is beginning a two-part series of articles exploring the benefits and challenges of ALD/ALE through companies that offer novel solutions for eliminating impurities and speeding process times.

A new approach to growing GaN crystals

MOCVD is utilized to grow gallium nitride (GaN) crystalline structures on a variety of substrates. But manufacturers face challenges including the fact that MOCVD reactors typically employ ammonia to obtain the nitrogen needed for processing, and the fact that the 1000-degree temperatures a reactor must achieve makes growing GaN structures with MOCVD expensive and costly to scale. Nano-Master (Austin, Texas, USA) offers a solution to speed crystal growth while mitigating other concerns.

Speeding backside SiC etch

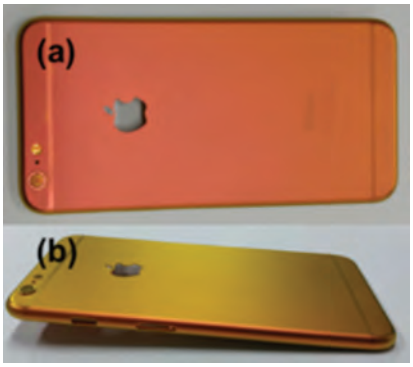
GaN on silicon carbide (SiC) devices are entering the mainstream in greater numbers. Their power density, ruggedness and ability to reduce circuit size makes GaN on SiC ideal for power electronics transistors, switches and related components. Advanced device designs that require etched vias are challenging with SiC given the fact that silicon carbide hardness is second only to diamond. Oxford Instruments (UK) offers new insight into the processes and techniques it offers to speed SiC etching.

NCD enables ALD decorative coatings

MANY PEOPLE want to make consumer products including valuable electronic devices more unique, outstanding, or have characteristics that add value. Atomic layer deposition (ALD) can meet these requirements, providing goods with higher quality and more functions – characteristics that were previously impossible to achieve without utilizing polymer-based coatings or other industrial applications that (while functional) did not contribute positively to a device's appearance, or added cost and production time. ALD can make a surface anti-tarnishing and anti-wear. Even antibiotic properties can be added as well as more conspicuous colours by taking advantage of thin film interference phenomena. NCD has demonstrated several precise colour coatings on various samples with multi laminating metal oxide thin films prepared by atomic layer deposition. The company's unique approach to ALD makes it possible to employ what was a time consuming and costly process in more high volume manufacturing settings.

In creating its sample products, NCD utilized Essential Macleod software to estimate various colour coating results. It was determined that the fullest visible range of colours could be obtained by controlling the thicknesses of metal oxides and corresponding light interferences and reflections. The company utilized various structures of five nano-laminated thin films of Al2O3 and TiO2. Evaluated colours created with ALD corresponded well with the simulated colour spectrum results shown by the software.

In another case, several parts of a watch band that were coated at a low growth temperature of 100°C using Lucida series ALD show different bright, warm, metallic and mirror-like colours including purple, blue, green, yellow, orange and red—a rainbow of colours. The back cover of a smart phone deposited by ALD shows the decorative red colour with incident angles at 0° and gold-colour sample with an incident



angle of 90°. An interesting aspect of using ALD to colorize metallic finishes is the fact that the relative thickness of the layers can be varied, thus yielding different colours that can be perceived at different angles of view created when light waves pass through or reflect from various depositions.

ALD technology is a great method to augment various consumer or commercial products by adding anti-tarnishing, anti-wear and anti-bacterial effects as well as tailored decorative coatings; this can be accomplished even on very complicated figures like 3D objects at low temperatures.

Films can be created without particles and pinholes. ALD decorative coatings have huge potential markets including automotive applications, electronics, jewellery, medical devices, sporting goods, watches and other advanced products.

Even though there are many advantages and potential applications of ALD decorative coatings, the technology has not been well industrialized until now because of its low productivity and relatively high production cost. However, NCD has developed the highest throughput and the largest-area ALD technology with its Lucida GS and GD Series. By using its new technology, NCD is able to provide remarkable ALD solutions for creating decorative and functional mass production solutions that can make products more outstanding, different and functional.

A faster etch for RF devices

As GaN-on-SiC RF devices reach market, Oxford Instruments has delivered a new via etch process to ease fabrication, reports Rebecca Pool.

For the RF industry, smooth and fast SiC backside via etching is crucial to high performance devices.

JUST LAST MONTH, Oxford Instruments revealed its latest SiC via etch process to be added to the PlasmaPro100 Polaris etch system.

Already designed to deliver fast etch rates on GaN, sapphire, SiC wafers and more, the single-wafer etch system now promises a faster, smooth via etch through SiC at a time when the wide bandgap material is proving crucial to the development of GaN-on-SiC RF devices.

"The system was released a couple of years ago, but this SiC via process is new," says Mark Dineen, Optoelectronics Product Manager at Oxford Instruments Plasma Technology.

"We saw a market need for this, developed it and believe now is the time to release it," he adds. "GaN-on-SiC is definitely a growing market and we want to be part of that."

But the road to the smooth SiC via hasn't been straightforward. SiC backside via etching is crucial to form a contact with electrodes during the fabrication of GaN-on-SiC transistors. However, SiC is a tough material to etch and researchers worldwide have grappled with how best to handle a substrate with a hardness close to that of diamond. Oxford Instruments now believes it has the answer.

New steps

As part of the latest etch process, SiC is mounted onto a sapphire carrier using wax, ready to plasma-etch the via some 100 μm through the wafer. As Dineen highlights, this wafer thickness demands a fast, aggressive etch, and as such, process engineers at Oxford Instruments have opted for a 1.2 μm per minute etch rate. "We need smooth sidewalls in the via, and if we went faster, we would produce jagged

features within the via which leads to localised heating and reduces device lifetime," he says. "But any slower, then throughput is just too slow and the [system] cost of ownership is too high."

A key issue that many researchers have encountered while optimising SiC substrate via etch processes is the formation of so-called pillars in the via hole, which impede metallisation. These unusual structures form on the end of micro-pipes – hollow tubes that are created during SiC growth – and are exposed after the relatively thick SiC wafer is chemically thinned to around 100 μm for the via etch.

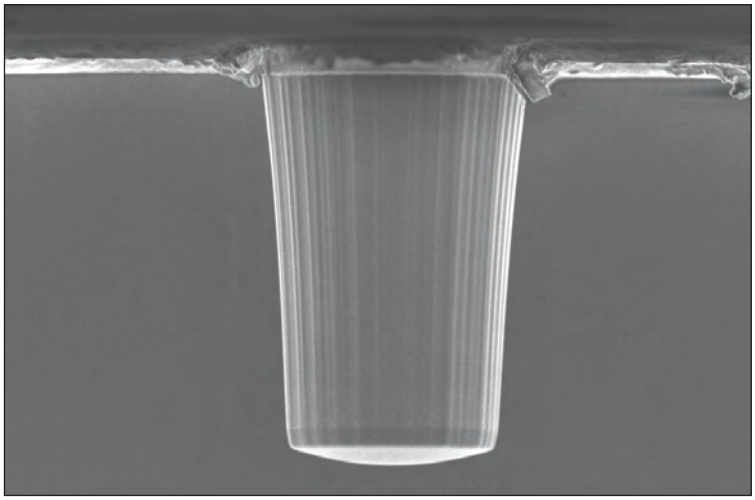
Myriad researchers have experimented with pre-etch clean and etch processes to avoid pillar formation. But according to Dineen, Oxford Instruments has countered this problem by introducing a 30 second etch to the process. It smoothly removes the top layer and accompanying defects to produce a clean surface prior to the main SiC via etch.

So, with defects removed, the relatively fast, aggressive plasma-etch swiftly produces a smooth, slightly sloped via, ready for post-etch metallisation. However, this process also generates heat around the wafer and sapphire carrier, spelling bad news for the all-important wax attachments that have an upper temperature limit of 150°C.

To maintain wax integrity, the wafer is electrostatically clamped to a lower electrode, which contains liquid cooling channels to transfer heat away through the electrode. As Dineen highlights, electrostatic clamping is widely used in the silicon industry, but during this SiC via etch process, a non-conducting sapphire substrate is being handled that will adhere to the clamp at the end of the etch. Given this, the company transferred a technology to the system that was developed as part of its past GaN-on-sapphire LED research.

"We had developed an electrostatic clamp that could efficiently clamp bare sapphire as part of our patterned sapphire substrate process," explains Dineen. "Thanks to the control method we developed, here we have excellent cooling in our system and the wafers are handled very smoothly."

While the company capitalises on lessons learned from LED process development, does it also expect the up and coming GaN-on-SiC RF device market to provide the same potential for growth? Dineen points to the likes of Wolfspeed, Panasonic and Fujitsu, all developing GaN-on-SiC RF devices, and also highlights how China-based manufacturers are now penetrating the market. Yet, an LED-type boom isn't expected. As Dineen puts it: "We do see a lot of growth in this market, but I don't think we will see anything quite as big as the LED market."



Oxford Instrument's latest via etch process promises a via with smooth, slightly sloping sidewalls for high performance devices.

"This is an interesting market, it's growing and SiC also has potential in power applications," he adds. "This all ties in with our expertise around III-V materials in these niche production markets."

And what about rival GaN-on-silicon devices? For example, this time last year, MACOM celebrated shipping more than one million GaN-on-silicon RF devices while claiming a 100 W transistor with comparable performance at a cheaper cost. And more recently, imec has launched a GaN-on-silicon research programme to produce 8 inch wafers.

"Processing costs will be a barrier for GaN-on-SiC devices but its performance is driving demand," he says. "If you measure GaN-on-SiC device quality versus cost, it is a strong choice compared to GaN-on-silicon. GaN-on-silicon will have a place for sure, although there are limitations on performance."

Still, Oxford Instrument's PlasmaPro100 Polaris etch system can handle wafer sizes up to 8 inches. And as Dineen concludes: "I'm not sure whether or not SiC wafers will reach that diameter, but GaN-on-silicon wafers are getting there, so we can etch a GaN recess into these wafers if needed."

THE ATTRACTIVE ATTRIBUTES OF ATOMIC LAYER DEPOSITION

Ammonia-free atomic layer deposition can yield tremendously smooth layers of GaN with incredibly high levels of uniformity.

BY RICHARD STEVENSON

THE USE of MOCVD to grow GaN films lies at the heart of the production of numerous commercial devices. This growth technology is used to form the LEDs that backlight countless screens and illuminate homes, offices and public spaces; it is used to manufacture blue and green lasers employed for reading discs and projecting images; and it is used to produce HEMTs for RF and power electronics that are deployed in radar, wireless communication and power supplies.

Given this wide-ranging, tremendous success, GaN growth by MOCVD clearly has its merits. But there are also undesirable aspects of this process that creates a film of GaN through the interaction of a gallium-based precursor with ammonia at highly elevated temperatures.

Some of the drawbacks are associated with the hardware that is used. MOCVD reactors designed for GaN growth must be capable of growth temperatures in excess of 1000 °C, which makes them expensive to build and run. These tools are also challenging to scale, so significant investment is required when developing reactors to accommodate larger wafers. Another major downside is the use of ammonia as the nitrogen source. This caustic, extremely hazardous gas has to be handled with great care, with abatement systems needed downstream to deal with any ammonia that has not been consumed in the growth process.

There are also weaknesses associated with GaN films grown by MOCVD. The stoichiometry of the compound is imperfect, the films are not flat on an atomic scale, and the material is plagued with

Precursors for the Nanomaster NLD-4000 are housed in a dedicated glove box.

hydrogen. This latter weakness can lead to variations in etch rates, and it can hamper device performance. For example, if hydrogen diffuses to the gate of a GaN transistor, it can shift the threshold voltage. It is possible to address all of these weaknesses associated with the growth of films of GaN by a novel, ammonia-free form of atomic layer deposition (ALD) pioneered by Nano-Master of Austin, Texas. The NLD-4000 tool made by this company retails for around $250,000, compared to $1 million or more for an MOCVD reactor, and it is straightforward to scale growth from 2-inch substrates to those of 450 mm in diameter.

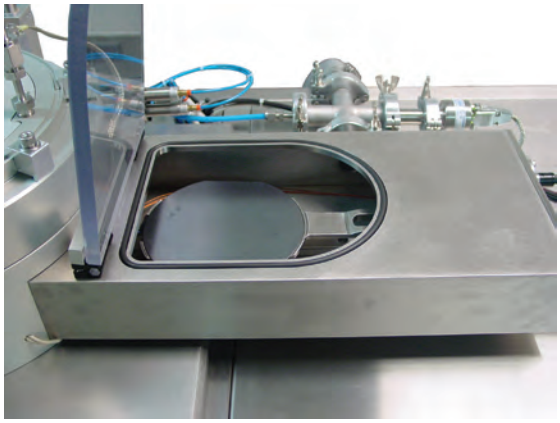
While the conventional form of ALD involves the repeated cycling of one precursor and then another to create a film one atomic layer at a time, the process pioneered by Nano-Master has a key difference: in this case, the plasma-formed nitrogen source is applied continuously, cutting cycle times in half.

Tracing the tool

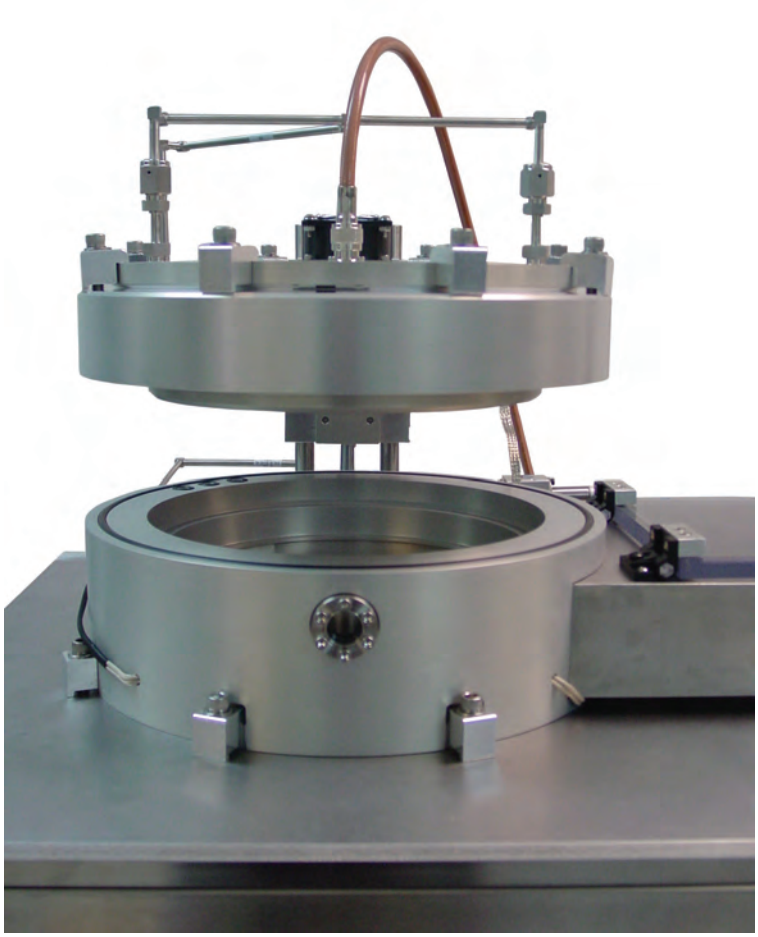
The approach employed in the ammonia-free ALD tool produced by Nano-Master has its roots in the work undertaken by company president and CEO Birol Kuyel. When working at AT&T in the 1980s, he investigated the growth of SiN by plasma-enhanced CVD.

"I found out that there is no way to get the uniformity and stoichiometry simultaneously using ammonia chemistry," says Kuyel. But when he turned to pre-activated nitrogen, they could independently control the stoichiometry and physical characteristics of SiN. "We were successful, had very low levels of hydrogen, and we filed a patent on that," explains Kuyel.

The next milestone came about ten years ago, when a professor at the University of Arkansas approached Kuyel, who by now was CEO at Nano-Master. The academic wanted a conventional MOCVD tool for GaN growth, but could not afford one, so Kuyel suggested a plasma-enhanced variant with N_2 rather than NH_3. This switch lowered the growth temperature to around 600 °C, which allowed the use of lower-cost, simpler hardware, and eliminated NH_3 abatement.



To prevent oxidation, wafers can be placed in load-lock after growth, where they are flushed with nitrogen and cooled.

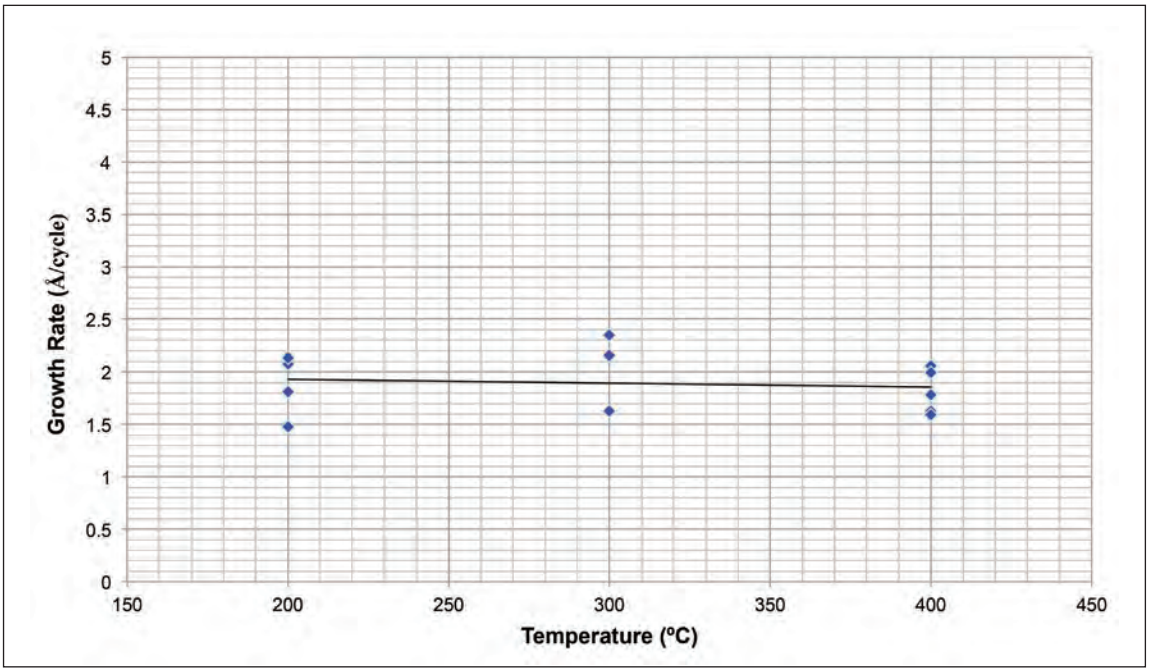


Use of a planar inductively couple plasma leads to very fast pump-down times, thanks to a very small gap between the substrate and the pump chamber.

Plasma-enhanced MOCVD proved a great success. "They were saying that they were getting the world's best gallium nitride," explains Kuyel. So pleasing were these results to these academics that they were unwilling to share the details of their success with Nano-Master. What Kuyel does know, however, is that the growth involved plasma-activated N_2, and the GaN films had low levels of hydrogen.

The success led Kuyel and his colleagues to wonder what might be possible by applying a nitrogen-plasma process to ALD. But they did not have the finances to pursue this idea until early 2015 when they won an order for this novel growth tool. Thanks to the accumulated knowledge from manufacturing other growth systems, they were successful at the first attempt, getting the reactor out of the door before the end of 2015.

To prevent the plasma from damaging the GaN film, the tool features separate chambers for the plasma and for ALD. The nitrogen plasma is formed above the chamber and introduced through a showerhead that "kills" the plasma to inject activated nitrogen. "To do nitrogen chemistry, you don't need nitrogen ions – you need natural nitrogen, but in an activated state," says Kuyel. Using pulses of gallium precursors in

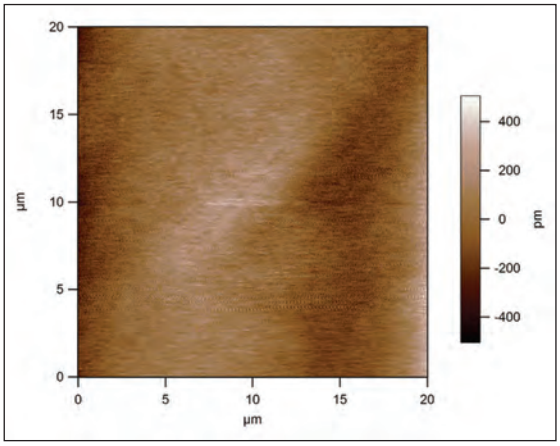


The growth rate is governed by the number of cycles, and has little dependence on temperature.

bursts with a duration of typically 20 µs to 60 µs and growth temperatures of between 200 °C and 400 °C, the tool is capable of producing films with a thickness independent of temperature, pulse width and cycle time. "We were able to grow a number of [atomic] layers based only on the number of cycles we used," says Kuyel. Another strength of the Nano-Master ALD tool is its very fast pump-down time to a typical growth pressure of 0.2-0.3 Torr. This stems from the use of a planar inductively coupled plasma system, rather than one based on a cylinder or a coil. By selecting this system architecture, the gap between the substrate and the pump chamber can be just a few centimetres.

Fantastically flat films

The tool is capable of producing some incredibly impressive results. For example, film thickness over a 6-inch substrate varies by less than 1 Å. "All those points [that are measured] have the same number of atoms," argues Kuyel. "MOCVD will depend on the flow patterns, reactivity concentrations and so on. This doesn't." When films of GaN are grown on silicon they form a very strong bond with the substrate. "We did not even have to do special preparation of the silicon surface," remarks Kuyel.The Achilles' heel of GaN growth with the Nano-Master ALD tool is the slow growth rate. Although it is faster than that of many ALD processes, thanks to pulsing of just the gallium source, growth rates are at best a few Angström per second. This effectively rules out the growth of thick films in a single-wafer processing chamber for chip production.



Films of GaN that are deposited by ammonia-free ALD have a tremendous degree of flatness.

As the take-up of this tool is still in it infancy, it is not yet clear where it will find its greatest use. One option, says Kuyel, is to build a composite system with an ALD chamber and an MOCVD chamber and a transfer between them under high vacuum. He believes that such an approach could be used for making blue lasers, which would benefit from the high-quality foundation that results from ALD.

Another possible use of the Nano-Master ALD system is the production of mirrors. Using a gallium-tri-chloride source, it is possible to grow films with a surface roughness on the pico-metre scale. "This is better than mirror finishes that you obtain for optical elements," claims Kuyel. "That's why I'm thinking that making mirrors from multi-layer dielectrics would be possible."

The plans for the future involve raising awareness of the tool and driving up its sales. Kuyel wants to build dual-chamber systems, which could either be: a pair of ALD chambers; a combined ALD and MOCVD multi-chamber cluster tool; or multi-wafer batch processing tools. There is also the opportunity of using the tools to deposit oxides, such as HfO_2, that could aid development of next-generation logic. So there is clearly much promise for this novel ALD tool.

EpiValence: R&D strategy

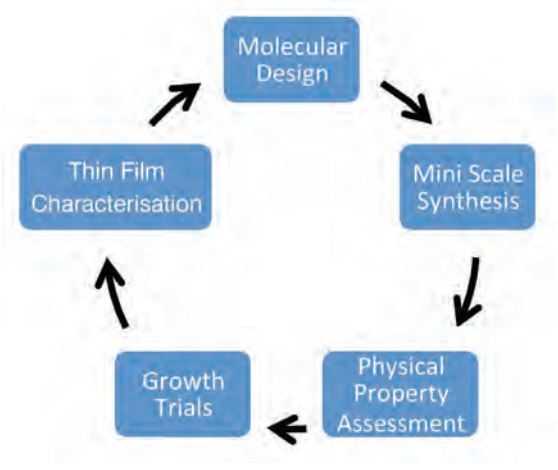
EpiValence believes a robust research and development pipeline is critical to meet current and future customer needs.

UNDERSTANDING market demands and working with partners to deliver compounds suitable to enable next generation applications is performed as widely as possible to ensure the EpiValence product portfolio evolves appropriately. Collaboration helps identify the molecule characteristics that are desired and then the EpiValence R&D team work in the laboratory to experimentally produce potential candidates that can be tested and evaluated. Further detail of this process is described below along with the subsequent steps that are necessary to introduce a new product in a controlled fashion at the scale demanded to service customer processes as they take up new technology.

EpiValence is a specialised chemical manufacturer with dedicated laboratories designed to handle highly sensitive materials in a safe, controlled fashion such that ultra-high quality products can be made and delivered to end users. With fumehoods equipped with bespoke Schlenk line technologies and high integrity glove boxes, strict inert atmosphere protocols can be applied to minimise contamination and ensure impurity levels are very low (typically 4N-6N grade products are available). As an SME operating in the North East of UK EpiValence relies on its expert team of chemists whose combined involvement in the precursor industry spans in excess of 40 years. Both Production and Research personnel pay the utmost attention to detail using quality procedures that are ISO9001 compliant.

The main objective in developing a new precursor offering is to enhance the performance of end user devices fabricated using the chemical. This can be achieved by either increasing an existing molecules purity or by creating a new molecule (or combination of molecules) that can be used in a modified process to optimise the specific deposition quality. For example by increasing precursor stability a higher deposition temperature could be employed to access a different phase of the target film or by decreasing stability the ability to deposit on thermally sensitive substrates can be accessed. In all cases managing the synthesis and design changes needed must consider numerous production challenges to ensure the highest potential compound is investigated.

The process employed at EpiValence is an iterative one as shown on figure above and involves many evaluation steps to assess the samples prepared

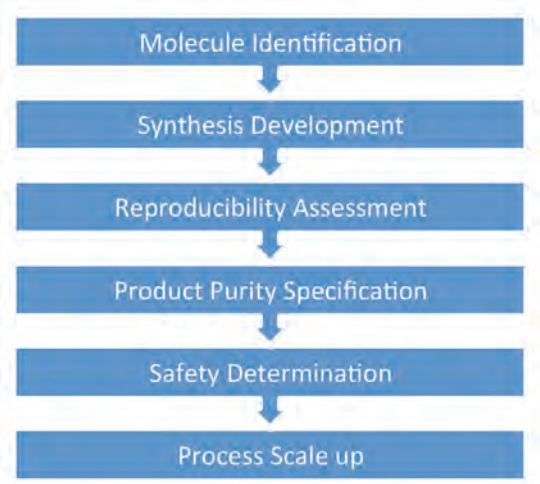


experimentally. The physical assessment is performed to identify firstly the chemical properties of the compound (ie stability, reactivity, volatility) and secondly the purity with respect to organic and trace metals. For all vapour phase delivery processes there are three areas to consider namely a) conversion of source chemical to vapour b) transport of this vapour to the deposition chamber c) use of vapour to deposit target film. The physical properties listed above indicate if a) and b) can be achieved and provide key information for c).

The suitability of a precursor to a specific deposition technology is highly dependent on that technology with different levels of importance allocated to each criteria involved. For example in ALD, a surface driven deposition technique, high thermal stability and high reactivity are key. In CVD, a thermally driven technique, the gas phase reactivity should be low and thermal stability must be managed between strict parameters.

The main techniques employed to evaluate samples are Thermogravimetric analysis (TGA), Nuclear magnetic resonance (NMR) for physical properties and organic purity and Inductively coupled plasma mass spectrometry (ICP-MS) for metallic purity. TGA provides stability and volatility information to demonstrate its transport properties and potential for use in the deposition process whilst NMR confirms the structure of the molecule. Both also highlight organic impurities such as solvent or unreacted raw materials to inform the chemists of the effectiveness of the synthesis/purification processes employed to isolate

the sample. Having successfully isolated high purity material, EpiValence partners perform growth trials to assess the quality of deposition that can be achieved and highlight the performance improvements gained. Feedback from the growth team is used to modify the molecule design and/or synthesis method to generate further samples and the cycle is repeated to maximise performance and identify the best candidate for the end user.



On identification of the molecule, the EpiValence team proceed to transition the synthesis to a production environment by increasing scale and establishing repeatability criteria such that a complete product specification can be generated and offered to customers in the volumes needed for their processes. As illustrated in the flow chart to the right, quality and safety issues are addressed throughout this task, thus reliability can be ensured for all new precursors generated immediately on product launch.

EpiValence is currently working on a number of exciting projects to expand its product range to enhance choice and improve performance in end user processes. These include higher purity precursors for specialised applications, increased volume production for molecules that are rolling out into new areas and speculative research into new chemistry to enable deposition of novel materials from new precursor combinations under conditions suited to flexible electronics as well as conventional coatings.

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Improve deposition and process control with minimal metrology overhead

Run-to-Run control can significantly improve process performance, but often at considerable time and cost. Taking a higher level view that applies novel methodologies can increase performance and savings with minimal metrology burdens says Joerg Reichelt, Yulei Sun – Rudolph Technologies, Inc. Tilo Bormann, Andreas Gondorf – Vishay Siliconix Itzehoe GmbH.

SEMICONDUCTOR manufacturing is arguably the most sophisticated and unforgiving volume production technology ever developed [1]. It consists of a complex series of hundreds of unit process steps. The technology continues to evolve; it becomes more complex as device sizes and associated manufacturing tolerances shrink, which is aggravated by increasing layer and mask quantities as well as introducing new materials and process steps when manufacturers seek to accommodate a greater mix of products at higher volumes and efficiencies. R2R process control is a strategy that seeks to optimize process performance by tuning the operating parameters for the next cycle based upon previous cycle result measurements.

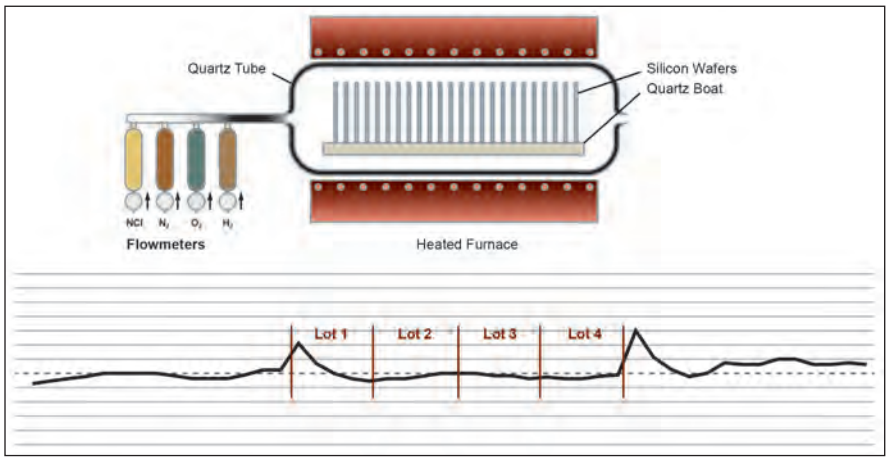

Figure 1: Wafer-to-wafer thickness variation is a relatively well-behaved function of position within the furnace carrier that can be approximated by a piecewise linear function.

Traditionally, R2R controllers for semiconductor manufacturing are process-centric[2], meaning the R2R controllers are designed to solve the local control problems at a single step in the manufacturing process without aiming at the bigger picture of a series of steps. For example, in a furnace deposition and CMP process flow, the majority of the post-CMP wafer-to-wafer thickness variation usually comes from variation in the pre-CMP thickness of wafers as they complete the deposition process in the furnace. The deposition process is complex, with many parameters available to adjust performance that also need to be controlled.

A process-centric design philosophy will implement a multi-input-multi-output (MIMO) furnace controller [3] to minimize the wafer-to-wafer thickness variation locally before it can propagate downstream to the CMP process. An additional CMP control strategy would be designed to compensate for the post-CMP wafer thickness variation introduced by the CMP tool drift. The complexity of the deposition process makes R2R control difficult. Adjusting the operating parameters requires the execution of complex experiments that consume significant time and resources. In addition, deposition furnaces are different from most other types of process equipment in that they are designed to process multiple lots of wafers loaded into a single carrier in each run. In contrast, the CMP process operates on one wafer at a time. The performance of a CMP tool on a given product wafer usually drifts relatively slowly over time, so control strategies typically operate at the lot level, adjusting polishing time for

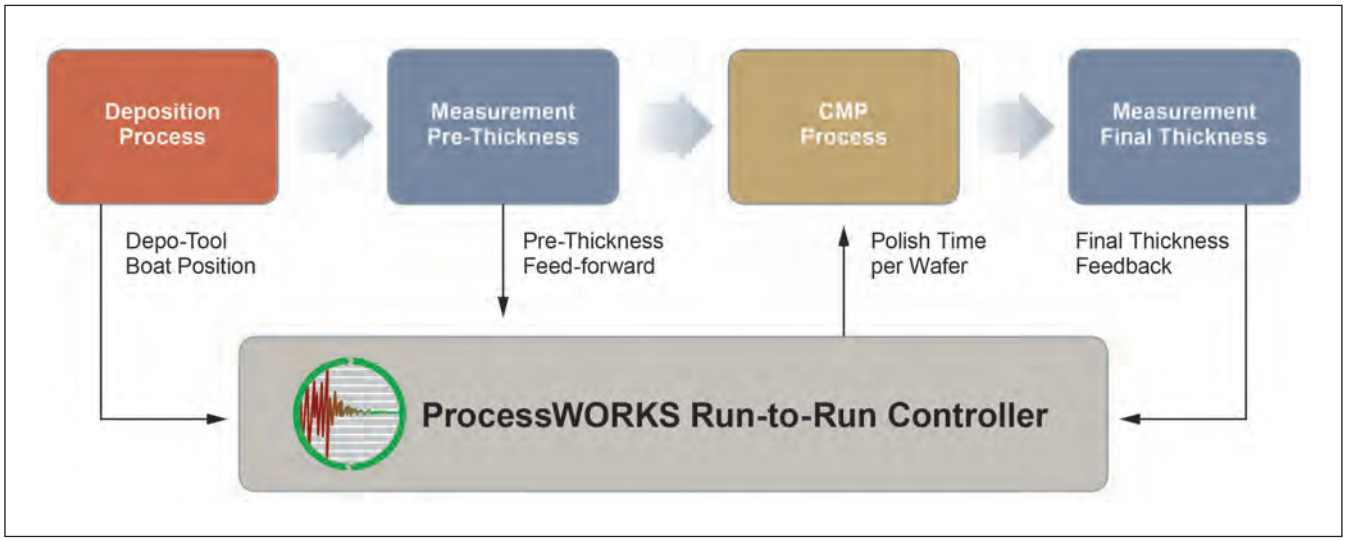

Figure 2: The multistep R2R controller uses inputs fed forward and backward from sampled pre- and post-CMP measurements to calculate polish times for each wafer.

a subsequent lot based upon measured thickness of the previous lot. Lot level R2R control is a well-developed and widely accepted practice for CMP. It is possible to adjust polishing times for each individual wafer, but this requires thickness measurements of each wafer after deposition. The measurement overhead for such wafer-level control introduces prohibitive time and cost overhead.

Multistep R2R control

To address the issue of thickness variability without introducing unacceptable metrology overhead we have developed a multistep R2R control strategy using Rudolph Technologies' ProcessWORKS software. Essentially, this approach postpones compensation for post furnace wafer-to-wafer thickness variation until the CMP step, providing control for both steps.

The strategy is based on our observation that most wafer-to-wafer, post-furnace thickness variation is a relatively well-behaved function of the wafer's location in the furnace carrier that can be approximated by a piecewise linear function (Figure 1). Thus it is possible to interpolate the likely thickness of each wafer based on sampled measurements of a few wafers in each lot, yielding a significant reduction in the overall metrology burden when compared to a conventional wafer-level control strategy. In this case we sampled 5 wafers in locations spread evenly through each lot. Likely thicknesses for unmeasured wafers were interpolated based on these sample measurements; CMP polishing times for each wafer were calculated based on the measured and interpolated thickness values. Post-CMP measurements of the thickness of the same 5 wafers were used to monitor and control CMP performance at the lot level. All calculations were handled automatically by the ProcessWORKS software.

Results

Implementation of the multistep R2R controller using ProcessWORKS is relatively straightforward; no programing is required. The operator defines the equation to calculate the output parameter, in this case polishing time, and configures the system interface with metrology and process equipment and factory control software. In our case, integration took three weeks and the controller was deployed in the factory five weeks after an initial requirements gathering meeting.

Figure 3 compares SPC charts before and one month after the controller was

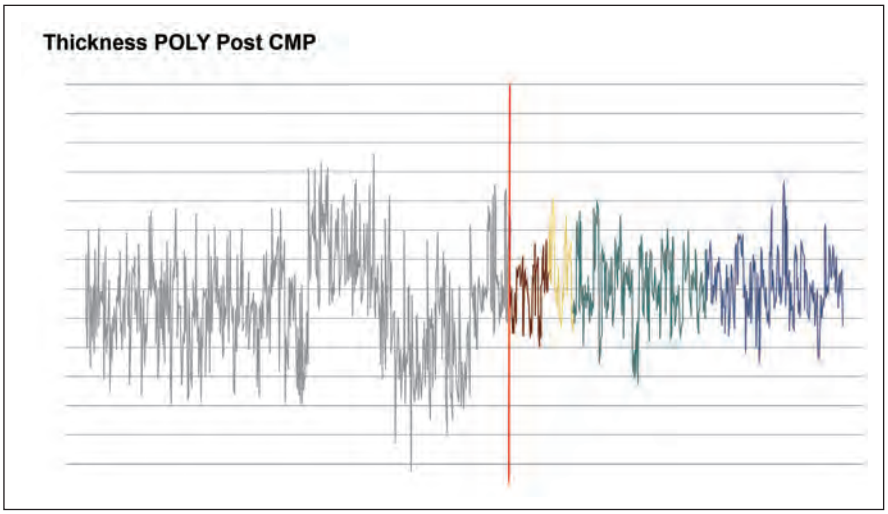

Figure 3: Post CMP wafer thickness measurements are illustrated before and one month after the multistep R2R controller was brought into production. These results demonstrate a 72 percent improvement in Cpk. The colors on the right side of the plot represent different CMP tools.

brought into production, showing a 72 percent improvement in Cpk for post CMP wafer thickness and the elimination of all out-of-limit excursions. The colors on the right side of the plot, after controller implementation, represent different CMP tools and make apparent the consistency of the improvements across all tools.

After implementation of the controller, observations that the post-CMP thickness was also dependent on which furnace was used to process the wafer at the deposition step led to additional modifications in the R2R controller to include a correction for the furnace in polishing time calculations, yielding an additional 39 percent improvement in Cpk.

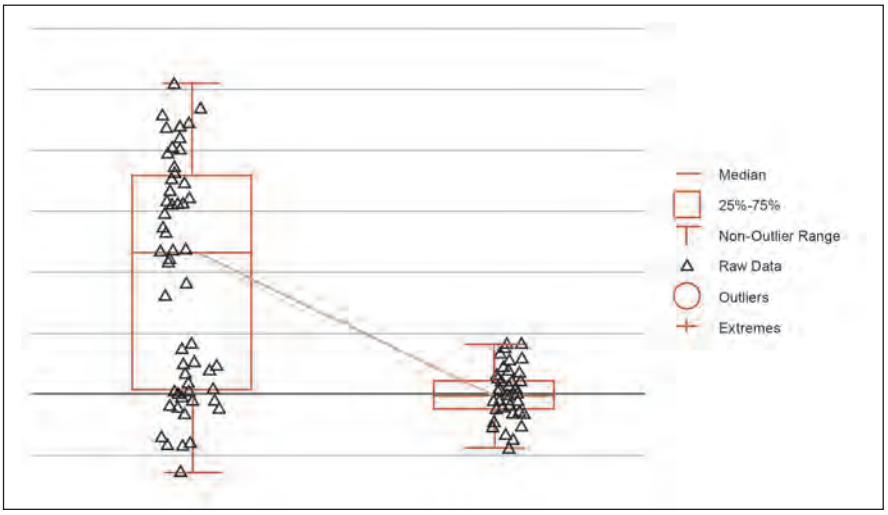

Figure 4: A box plot of pre- and post-controller wafer thickness variation.

In addition to process performance gains, the multistep R2R controller saved an hour per day by eliminating the need for a daily tool monitoring run, reduced operator/engineering time for manual adjustments and extended preventive maintenance cycles.

Conclusion

We have described the use of a multistep R2R process control strategy to reduce post CMP wafer-to-wafer thickness variability. It has successfully reduced the combined variability of the deposition and CMP processes without adding an unacceptable metrology burden. We were able to integrate the controller with the Vishay factory systems in three weeks, which allowed us to deploy the CMP controller within five weeks of the initial requirement gathering meeting. Since the deployment of this wafer-level CMP controller in production, the Cpk of the CMP process has increased by 72 percent with zero spec limit violations.

The post-CMP wafer-to-wafer thickness variation has been reduced by 70 percent. We subsequently discovered that the post-CMP thickness is also dependent on which furnace was used to process the wafer at the deposition step and additional modifications to the R2R controller now use different values for different furnaces when calculating the polish times, improving Cpk by another 39 percent. Additional benefits of the controller included the elimination of nonproductive daily tool monitoring runs, reduction of engineering/operator time for manual adjustments and the extension of preventive maintenance cycles.

Rudolph Technologies and Vishay. Figures can be downloaded at: **https://rudolphtechnologies.sharefile.com/d-s469e110d6184e288**

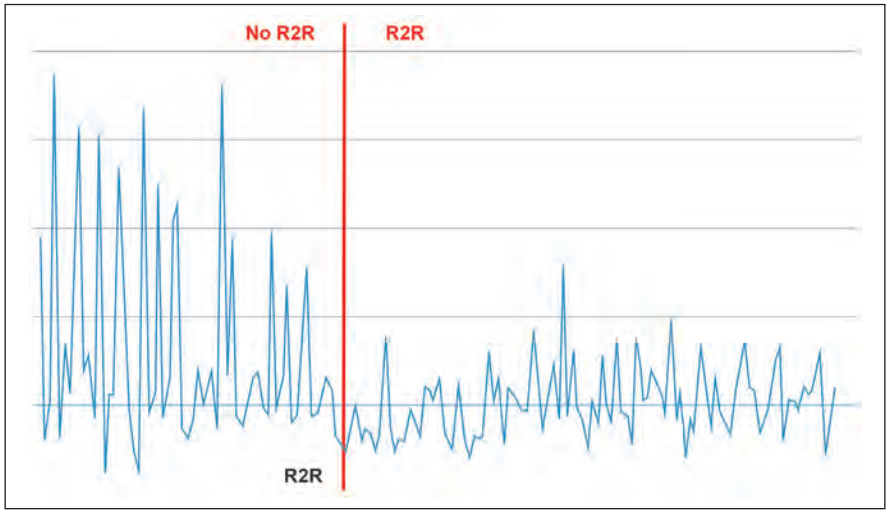

Figure 5: Improvements in wafer-to-wafer thickness control significantly increased the performance of the downstream etch process.

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