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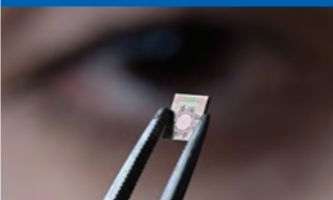
Extending the era of Moore's Law

Wireless communications



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editor'sview

By Name, Title

Payday is here for IoT pioneers

SOME industry insiders say that semiconductor manufacturers need only keep the IoT in their sights to realise growth. That is a panacea; a fairy tale. Somewhere beyond such extremes lies the truth and a path to healthy growth.

The reality of the IoT market is much like any business proposition: investment returns are not guaranteed; payday is here for some / others may lose. The only guarantee is that those who do not get in the game will never win it. The IoT is already big business for many. Last year IoT products were roughly (USD) $10 billion of a $355 billion global semiconductor market. Payday is here for IoT pioneers. But the deals are not over. This emerging market has many opportunities.

In reality, IoT hype should really mention its long-term potential: trillions of chips in everything from sensors to actuators to gateways to the cloud. This type of growth will redefine semiconductor manufacturing in the years to come.

That's right: years to come. Why years? This belief is built on the fact that sustainable markets do not materialise overnight – they never have; it is especially true of huge markets with the potential to touch everything from appliances to automobiles. Today's best estimates are merely guesstimates. Researchers at IHS Global recently offered some facts to off-set the hyperbole: every one of the top 20 global microcontroller unit makers has an IoT strategy—not most, but every one of them. While some chip makers like Broadcom exited IoT, others are doubling down. Intel, after announcing 12K lay-offs last year, said it was confident in IoT and expanded their commitment.

Samsung introduced new IoT cloud chips as its Note 7 was failing; ARM is bullish. Qualcomm is developing whole families of IoT devices even as smartphones flatten. At the Mobile World Congress—the world's largest cellular event—IoT dominated to the point that Ovum TMT Intelligence said the MWC is transforming into an internet tech event. All of this and more for an 'emerging' market.

Now is the time to plan and strategize. Now is the time to adapt and develop new products. Now is the time to partner with IoT security experts, gateway developers, and standards groups. Now is the time to begin the marathon. While the Big Money in IoT may be farther down the road, one fact is certain: those who show little interest today will likely see no profits tomorrow.

Publishing Editor Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Technical Contributor Mark Andrews
Sales Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
USA Representatives Tom Brun Brun Media E: tbrun@brunmedia.com +001 724 539-2404
Janice Jenkins E: jjenkins@brunmedia.com +001 724-929-3550
Amy Rogers arogers@brunmedia.com +001 678-714-6775
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214
Circulation Director Jan Smoothy jan.smoothy@angelbc.com +44 (0)1923 690200
Chief Operating Officer Stephen Whitehurst stephen.whitehurst@angelbc.com +44 (0)2476 718970

Directors Bill Dunlop Uprichard – CEO, Stephen Whitehurst – COO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal, Jason Holloway.

Published by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. T: +44 (0)1923 690200 F: +44 (0)1923 690201 E: ask@angelbc.com

Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 F: +44 (0)2476 718 971 E: info@angelbc.com

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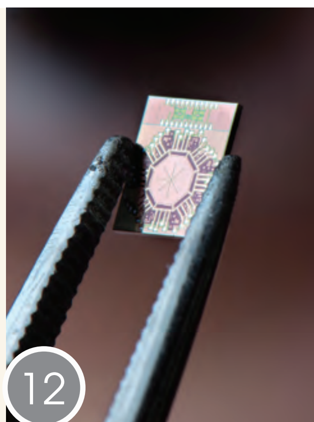

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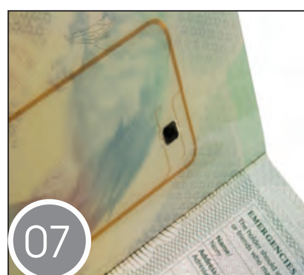

Intel $7 billion investment in next-generation semiconductor factory

INTEL CORPORATION has announced plans to invest more than $7 billion to complete Fab 42, which is expected to be the most advanced semiconductor factory in the world. The high-volume factory is in Chandler, Ariz., and is targeted to use the 7 nanometre (nm) manufacturing process. It will produce microprocessors to power data centres and hundreds of millions of smart and connected devices worldwide. The announcement was made by U.S. President Donald Trump and Intel CEO Brian Krzanich at the White House.

The completion of Fab 42 in 3 to 4 years will directly create approximately 3,000 high-tech, high-wage Intel jobs for process engineers, equipment technicians, and facilities-support engineers and technicians who will work at the site. Combined with the indirect impact on businesses that will help support the factory's operations, Fab 42 is expected to create more than 10,000 total long-term jobs in Arizona.

"Intel's business continues to grow and investment in manufacturing capacity and R&D ensures that the pace of Moore's law continues to march on, fueling technology innovations the world loves and depends on," said Krzanich. "This factory will help the U.S. maintain its position as the global leader in the semiconductor industry."

"Intel is a global manufacturing and technology company, yet we think of ourselves as a leading American innovation enterprise," Krzanich added. "America has a unique combination of talent, a vibrant business environment and access to global markets, which has enabled U.S. companies like Intel to foster economic growth and innovation. Our factories support jobs — high-wage, high-tech manufacturing jobs that are the economic engines of the states where they are located."

Intel is America's largest high-technology capital expenditure investor ($5.1 billion in the U.S. 2015) and its third largest investor in global R&D ($12.1 billion in 20151). The majority of Intel's manufacturing and R&D is in the United States. As a result, Intel employs more than 50,000 people in the United States, while directly supporting almost half a million other U.S. jobs across a range of industries, including semiconductor tooling, software, logistics, channels, OEMs and other manufacturers that incorporate our products into theirs.

The 7 nm semiconductor manufacturing process targeted for Fab 42 will be the most advanced semiconductor process technology used in the world and represents the future of Moore's Law.

In 1968 Intel co-founder Gordon Moore predicted that computing power will become significantly more capable and yet cost less year after year. Making a leading-edge computer chip is the most complex manufacturing process in the world, engineering magic that turns sand into semiconductors, the foundation of the knowledge economy.

The chips made on the 7 nm process will power the most sophisticated computers, data centres, sensors and other high-tech devices, and enable things like artificial intelligence, more advanced cars and transportation services, breakthroughs in medical research and treatment, and more.

Pure-play foundry market surges in 2016 to reach $50 billion

THE PURE-PLAY FOUNDRY market is forecast to play an increasingly stronger role in the worldwide IC market during the next five years, according to IC Insights' new 2017 McClean Report. The 20th anniversary edition of The McClean Report forecasts that the 2016-2021 pure-play IC foundry market will increase by a compound annual growth rate (CAGR) of 7.6 percent; growing from $50.0 billion in 2016 to $72.1 billion in 2021.

IC foundries have two main customers—fabless IC companies (e.g., Qualcomm, Nvidia, Xilinx, AMD, etc.) and IDMs (e.g., ON, ST, TI, Toshiba, etc.). The success of fabless IC companies as well as the movement to more outsourcing by existing IDMs has fueled strong growth in IC foundry sales since 1998. Moreover, an increasing number of mid-size companies are ditching their fabs in favor of the fabless business model. A few examples include Fujitsu, IDT, LSI Corp. (now part of Avago), Avago (now Broadcom Ltd.), and AMD, which have all become fabless IC suppliers over the past few years.
In 2016, the "Big 4" pure-play foundries (i.e., TSMC, GlobalFoundries, UMC, and SMIC) held an imposing 85 percent share of the total worldwide pure-play IC foundry market. As shown, TSMC held a 59 percent market share in 2016, the same as in 2015, and its sales increased by $2.9 billion last year, more than double the $1.4 billion increase it logged in 2015. GlobalFoundries, UMC, and SMIC's combined share was 26 percent in 2016, the same as in 2015. The three top-10 pure-play foundry companies that displayed the highest growth rates in 2016 were X Fab (54 percent), which specializes in analog, mixed-signal, and high-voltage devices and acquired pure-play foundry Altis in 3Q16 to move into the top 10 for the first time, China-based SMIC (31 percent), and analog and mixed-signal specialist foundry TowerJazz (30 percent). In contrast to X-Fab's 2016 growth spurt, TowerJazz and SMIC have been on a very strong growth curve over the past few years. TowerJazz went from $505 million in sales in 2013 to $1,249 million in 2016 (a 35 percent CAGR) while SMIC more than doubled its revenue from 2011 ($1,220 million) to 2016 ($2,921 million) and registered a 19 percent CAGR over this five-year time period.

NXP identifies top three global trends in electronic passports

NXP SEMICONDUCTORS N.V., has identified three distinct trends in electronic passports (ePassports or biometric passports): increasing functionality, stronger security and the emergence of "virtual mobile identity."

Out of 900 million passports issued, 730 are ePassports, which now represent the majority of passports in circulation. According to the International Civil Aviation Organization (ICAO), the United Nations agency that oversees international air travel and defines ePassport standards, 120 states claim that they are currently issuing ePassports. The infrastructure supporting ePassports has expanded as well. Today, over 5,000 automated border crossings (ABC) gates are operating worldwide, supporting more than 20 million ABC transactions daily.

Trend #1: Increasing functionality

ePassport functionality is continuously evolving. ICAO first introduced BAC (Basic Access Control), then EAC (Extended Access Control) and today is currently migrating to SAC (Supplemental Access Control) protocols. All ePassports use the same data format, known as the Local Data Structure (LDS), to store and "seal" data to protect it from tampering. The data that is embedded in the chip remains the same for the whole lifespan of the document and can't be modified.

A new format called LDS2, which is a backwards-compatible extension to previous generations of electronic passports and not far away from publication, will change that. It enables the digital storage of travel data such as electronic visas and travel stamps directly on the chip, and allows the complete passport booklet to be available in digital format.

In addition, the read-and-write capacity allows new biometric data to be added. Countries will have more choice in national policy, and give people the option of submitting biometrics if they want to participate in a trusted-traveller program. Introducing the concept of passport applications opens up opportunities to efficiently automate the processing of passengers and their documents. This frees up time at borders so officials can attend to more high-value activities, and increase return on investment in the border-clearance infrastructure.

NXP's long-standing expertise in supporting ePassport solutions around the world has led to a huge existing infrastructure enabling easier integration of international traveller programs.

Currently, NXP ships SAC solutions globally in high volume, and NXP is fully involved in the definition and standardization of ePassport LDS2 and has developed a solution that successfully passed initial ICAO compliance tests performed by the ICAO NTWG.

Trend #2: Stronger security

The European refugee crisis, the rise in international terrorism and the increase in criminal activity spiked the demand for stolen and forged passports. This development advances the distribution of ePassports on a global scale. Countries that already issue ePassports are looking to increase the security further.

As a result, the future will see more data being transferred from the physical pages of an ePassport, to the secure and tamper-resistant Integrated Circuit (IC). The IC is designed to resist attempts to steal, modify or misuse the data, and ceases to work properly if physically tampered with.

In reality, the chip in the electronic passport has more capacity and functional flexibility than just supporting the ICAO 9303 protocols, which offers untapped opportunities to implement electronic forensic security features. It provides functionality that may be used on an international and/or national level, depending on feature implementation and international cooperation.

Customer-specific functionality implemented in the chip can introduce additional security and efficiency in the process of border management and can elevate document security and fraud prevention to an unprecedented level.

NXP's SmartMX secure microcontroller family with its world-class security features make up the core component for secure identity programs. SmartMX products contain the IntegralSecurity architecture with more than 100 security mechanisms representing a true benchmark in security and are currently ready to support custom-specific electronic forensic features.

Trend #3: ePassport complemented by "virtual mobile identity"

Answering the demand for leaner administration and stronger security, the ePassport is evolving from "just" being a travel document to being a government-issued root credential for other applications, including a "virtual mobile identity." In the future, the single, secure digital ID in combination with technology such as NFC, will allow ePassport owners to identify themselves, to interact with and authenticate applications via NFC-enabled mobile smartphones or wearable formats.

ICAO is using the 9303 NTWG (New Technology Work Group) to work on potential future policies and standards for a "virtual mobile identity."

NXP is an NFC co-inventor, and its SmartMX product family is the preferred choice for the secure element of NFC-enabled smartphones. NXP is also involved in ISO and ICAO standardization activities for "virtual mobile identities."

The combination of technology know-how and expertise in eGovernment solutions is a valid reason to trust NXP as a partner for mobile-based government solutions.

Remote patient monitoring revenues to reach €32.4 billion in 2021

REVENUES for remote patient monitoring (RPM) solutions reached € 7.5 billion in 2016, according to a new study released by Berg Insight. This includes revenues from medical monitoring devices, mHealth connectivity solutions, care delivery platforms and mHealth care programs. RPM revenues are expected to grow at a CAGR of 33.8 percent between 2016 and 2021, reaching €32.4 billion at the end of the forecast period. Savings attributable to payers and care providers will by far exceed this amount as connected care solutions can allow better health outcomes to be achieved more cost efficiently. The new care models enabled by these technologies are often consistent with patients' preferences of living healthier, active and independent lives.

The healthcare industry is advancing towards an age where connected healthcare solutions will be part of standard care practices. "All health related devices that can be connected will be connected and patient data management therefore becomes increasingly important", says Anders Frick, Senior Analyst at Berg Insight. He describes how the line between medical devices and health gadgets becomes blurred and traditional as well as startup companies try to position themselves as important players in the ecosystem for mHealth data.

National PHR systems, device manufacturing companies, independent app producers and tech giants such as Google, Apple and Microsoft are some of the stakeholders. Another major trend is the consumerization of medical-grade mHealth devices and apps. During 2016 hundreds of thousands of consumers have connected medical monitoring devices via their smartphones to cloud platforms. This marks a substantial shift that will open up new opportunities in the remote patient monitoring market in the coming years. "Payers and healthcare providers will have opportunities to take advantage of this trend, as consumers that already have started to use connected medical devices more easily can be onboarded onto new mHealth care programs", concludes Mr Frick.

The new mHealth study from Berg Insight also investigates the connected AED market. An automated external defibrillator (AED) is a portable electronic device that automatically diagnoses and corrects life-threatening heart problems in a patient. Yearly shipments of AEDs are around 500,000 units globally. Several vendors recently started to offer AEDs featuring built-in connectivity whereas others are only in the planning stage to add connectivity. Berg Insight estimates that about 10 percent of all AEDs sold this year will be connected, a percentage that will increase to 50 percent by 2021.

Ultratech receives repeat multiple system order

ULTRATECH, a supplier of lithography, laser processing and inspection systems used to manufacture semiconductor devices and high-brightness LEDs (HBLEDs), as well as atomic layer deposition (ALD) systems, today announced that it has received a repeat, multiple-system order from a leading semiconductor manufacturer for its advanced packaging AP300 lithography systems.

The AP300 systems will be utilized for high-volume, leading-edge, fan-out wafer-level packaging (FOWLP) applications used to manufacture state-of-the-art application processors. Ultratech will begin shipping the AP300 systems in the first two quarters of this year to the customer's facility in Asia.

Ultratech General Manager and Vice President of Lithography Products Rezwan Lateef stated, "Ultratech has maintained its leadership position in the advanced packaging market segment by consistently delivering superior on-wafer results, cost-of-ownership and reliability performance for high-volume manufacturing (HVM) environments.

Fan-out technologies continue to be the optimal solution for the highly-demanding mobile and wireless markets by offering improved performance in a reduced form factor. The AP300 is ideally suited to address this market with HVM -proven extendibility well below 2 microns.

This substantial repeat order again confirms our technology leadership and the value proposition of Ultratech's AP300 systems over full-field 1X scanners and reduction steppers. We are pleased to expand our photolithography-tool-of-record position at this valued customer. We look forward to working with them to meet their volume production and technology roadmaps."

Toshiba starts construction of fab 6 and memory R&D centre in Japan

Toshiba Corporation has announced that it has started construction of a new state-of-the-art semiconductor fabrication facility, Fab 6, and a new R&D centre, the Memory R&D Center, at Yokkaichi Operations in Mie prefecture, Japan, the company's main memory production base.

Fab 6 will be dedicated to production of BiCS FLASH, Toshiba's innovative 3D Flash memory1. Like Fab 5, construction will take place in two phases, allowing the pace of investment to be optimized against market trends, with completion of Phase 1 scheduled for summer 2018.

Toshiba will determine installed capacity and output targets and schedules by closely monitoring the market.

Toshiba will also construct a Memory R&D Centre adjacent to the new fab, with completion targeting December 2017. The facility will advance development of BiCS FLASH and new memories.

Toshiba is determined to enhance its competitiveness in the memory business by timely expansion of BiCS FLASH production in line with market trends, and to retain leadership in innovation in the memory business.

Note: [1] A structure that stacks Flash memory cells on a silicon substrate. It realizes significant density improvements over planar NAND Flash memory, where cells are formed on the substrate.
*BiCS FLASH is a trademark of Toshiba Corporation

Amkor Technology to acquire NANIUM

AMKOR TECHNOLOGY and NANIUM S.A. have announced that they have entered into a definitive agreement for Amkor to acquire NANIUM, a world class provider of wafer-level fan-out (WLFO) semiconductor packaging solutions.

The acquisition of NANIUM will strengthen Amkor's position in the fast growing market of wafer-level packaging for smartphones, tablets and other applications. NANIUM has developed a high-yielding, reliable WLFO technology, and has successfully ramped that technology to high volume production. NANIUM has shipped nearly one billion WLFO packages to date utilizing a state-of-the-art 300mm Wafer-Level Packaging (WLP) production line.

"This strategic acquisition will enhance Amkor's position as one of the leading providers of WLP and WLFO packaging solutions," said Steve Kelley, Amkor's president and chief executive officer. "Building on NANIUM's proven technologies, we can expand the manufacturing scale and broaden the customer base for this technology."

"The Amkor transaction is a great fit for us and provides NANIUM and its employees with a strong platform for future growth," said Armando Tavares, President of NANIUM's Executive Board. "Amkor's technology leadership, substantial resources and global presence coupled with NANIUM's best-in-class WLFO packaging solutions will accelerate global acceptance and growth of this technology worldwide."

Rudolph receives multi-system order for advanced memory ramp

RUDOLPH TECHNOLOGIES has announced that a leading memory manufacturer in Asia has placed orders totalling over $8 million USD for process control equipment to support the ramp of their latest high-performance stacked memory devices.

The equipment spans front- and back-end applications. It includes MetaPULSE metrology systems for plating and etch control and NSX 330 systems for two- and three-dimensional (2D/3D) inspection and metrology throughout the back-end process. The systems are scheduled to ship in the first quarter of this year. "Controlling the etch process is critical for high-performance memory stacks at advanced nodes," said Mike Goodrich, vice president and general manager of Rudolph's Process Control Group. "Rudolph's MetaPULSE system is widely used to measure opaque materials, like metals, for critical processes at sub-20nm nodes. We are happy to see its capabilities now applied to new process steps for controlling hard mask etch and plating, which are challenged by increased memory density.

With the MetaPULSE G system, our customer was able to obtain the critical on-product metrology required to achieve high device yields, while at the same time, reducing process-related costs by eliminating monitor wafers."

NXP and Mobis India deploy DRM chips and receivers designed in India

NXP SEMICONDUCTORS, one of the world's largest suppliers of automotive semiconductors and Hyundai Mobis, have announced the successful completion of field trials of MOBIS DRM receivers and NXP chips designed in India.

The chips and DRM receivers are now deployed in DRM-fitted car infotainment receivers in a newly launched vehicle in India by a leading carmaker.

DRM is an innovative digital radio standard that has been deployed in emerging markets such as India. DRM provides FM-comparable, or better audio quality on the AM radio band. Since AM radio covers more than 98 percent of the population in India, and only 37 percent of listeners can currently receive the FM signal, DRM significantly improves radio coverage and quality. This technology is affordable and provides additional data services such as traffic updates, natural disaster warnings and news.

The development and deployment, showcased at a DRM Round Table

conference on January 31, was made possible by a regional collaboration between All India Radio, NXP Semiconductors, Hyundai Mobis, and the DRM Consortium. At the event, the NXP's SATURN + HERO Chipset demo and DRM receiver fitted vehicle generated huge interest and was experienced by Hon'ble Union Minister of Information and Broadcasting, Mr. Venkaiah Naidu, and delegates from the public, government and the automotive and consumer industries.

Bob Paul Raj, head of multimedia division, Mobis Technical Center India, said, "Mobis India is a believer in Make in India and has been working with NXP on the design of this world-class radio entertainment system with DRM functions. The two firms have cooperated on comprehensive field trials from design stage to final product to ensure the solution meets the requirements of the Indian market.

Hyundai Mobis' demonstration of live DRM reception in a car at a DRM round table ahead of the BES event in New Delhi confirmed the company's leadership image by innovating ahead of the curve and offering the latest technological solutions to its consumers. The work and tests which have been carried out highlight that DRM in India is a reality and that the auto industry is at the forefront of the Indian digital radio roll-out."

Ashok Chandak, senior director, NXP Semiconductors South Asia Pacific, commented, "It is incredibly exciting to have participated in this DRM rollout in India. With this launch, NXP is one of the world's first semiconductor companies to demonstrate digital audio across all three global standards from the same car radio co-processor — a real milestone for NXP.

Cypress enhance security for IoT applications

CYPRESS SEMICONDUCTOR has introduced 64 Mb and 128 Mb densities to its family of NOR Flash memories with a Quad Serial Peripheral Interface (Quad SPI). The new FL-L NOR Flash devices provide the utmost reliability and security for high-performance embedded systems that store critical data and operate at extended temperatures. The FL-L devices also offer low power consumption and AEC-Q100 automotive-grade qualification with high read bandwidth and fast program time at an extended temperature range. Using small, uniform 4 KB physical memory sectors allows the devices to optimally store program code and parametric data. The devices are ideal for high-performance applications, such as Advanced Driver Assistance Systems (ADAS), automotive instrument clusters and infotainment systems, industrial control and smart factory equipment, networking equipment, IoT applications, video game consoles and set-top boxes.

"Our FL-L Quad SPI NOR Flash family offers the highest reliability and enhanced security, along with the bandwidth and small form factor that high-performance applications require," said Rainer Hoehler, Vice President of the Flash Business Unit at Cypress. "Expanding this family fits in with our strategy to offer high-performance memories that combine with Cypress' MCU, analog and connectivity solutions to offer complete embedded system-level solutions for our fast-growing target markets."

High-performance system designs require high read bandwidth for program execution, small, low-pin-count packages, and fast program and erase times. Cypress' 128 Mb and 256 Mb FL-L Quad SPI NOR Flash devices are each capable of 133-MHz Single Data Rate (SDR) and 66-MHz Double Data Rate (DDR) for bandwidth of 67 Mbps, and the 64 Mb devices leverage a 54-MHz DDR mode to deliver read bandwidth of 54 Mbps, enabling fast program execution for high-performance systems. The memories provide low standby current and a deep-power-down mode that extends battery life for battery powered applications. The family offers AEC-Q100 automotive qualification and supports an extended temperature range of -40°C to +125°C. The 128 Mb and 256 Mb devices can increase customers' manufacturing throughput with a fast 0.30-ms program time per 256 bytes, and they offer a 50-ms erase time that enables new data to be written quickly. The devices are available in industry-standard packages including the USON (4mm x 4mm) package that saves board space and simplifies layout.

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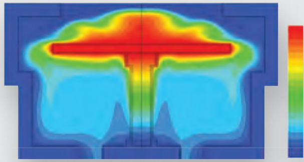

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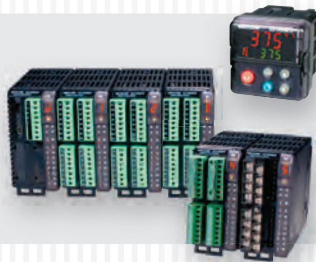

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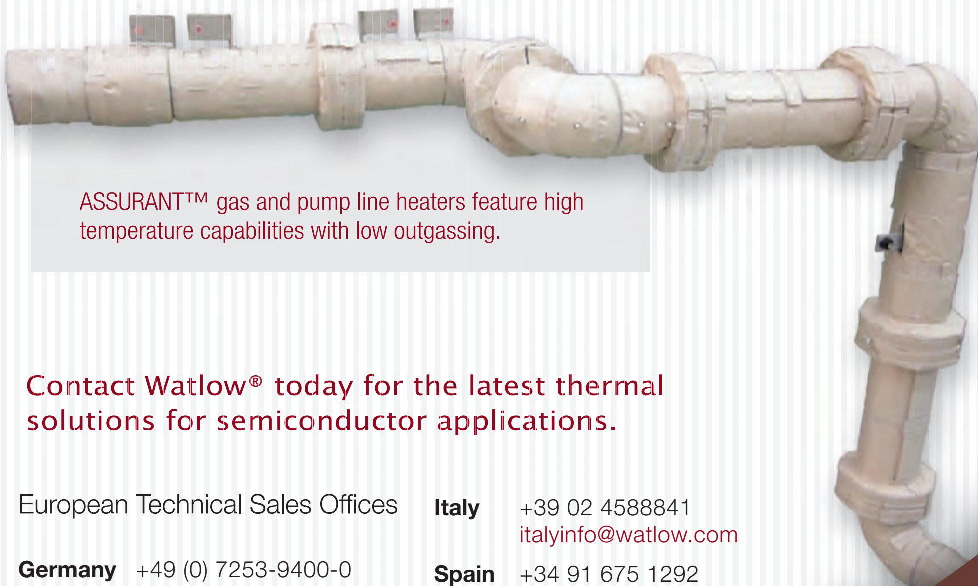

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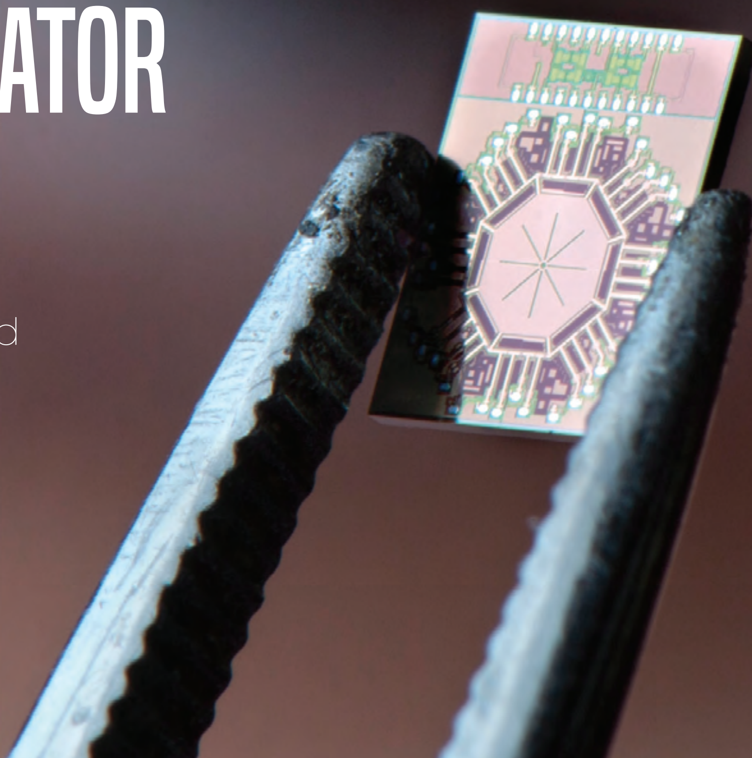
UCI ENGINEERS DEVELOP POWERFUL MILLIMETRE-WAVE SIGNAL GENERATOR

Device could revolutionise scanning, spectroscopy and wireless communication



YOUR DOCTOR waves a hand-held scanner over your body and gets detailed, high-resolution images of your internal organs and tissues. Using the same device, the physician then sends gigabytes of data instantly to a remote server and just as rapidly receives information to make a diagnosis.

Tiny though it is, the Heydari lab's radiator chip boasts the highest power and efficiency of any device in its class, according to its creators. Steve Zylius / UCI Integrated circuit researchers at the University of California, Irvine have created a silicon microchip-based component that could make these and many other actions possible.

Known as a "radiator," the tiny gadget emits millimetre-wave signals in the G band (110 to 300 gigahertz). Waves of this frequency easily penetrate solid surfaces and provide extremely sharp resolution, enabling new, more effective methods of biomedical and security scanning and imaging. The chips also can perform a key role in point-to-point wireless communication.

The UCI engineers who created the technology said that tests in their lab have shown it to have the highest power and efficiency ever recorded in such a radiating element while exhibiting the lowest noise (interference from other sources of radiation).
UCI professor of electrical engineering & computer science Payam Heydari, lead investigator on the project, will present information about the development at IEEE International Solid-State Circuits Conference in San Francisco.

"We're very excited about the successful design of this radiator because it represents a complete breakthrough," said Heydari, a 2017 IEEE Fellow. "We're offering an entirely new kind of physics, a new kind of device really. Our power and efficiency is an

order of magnitude greater than other designs." Through a process of trial and error, he and members of his UCI lab invented a tool that performs three crucial functions, he said. It combines power from multiple amplifiers; it modulates that signal to a desired frequency setting; and it radiates it out in waves that are used to see, sense or communicate. "By making a single device that provides a multitude of operations, we've gotten rid of all the interstage, highly inefficient systems found in other radiators, and as a result, we can achieve higher power output," Heydari said.

One of his lab's graduate students, Peyman Nazari, designed the device as an octagonal semiconductor chip with a unique cavity structure that allows for the emission of circularly polarized radiation. Most transmitters now generate linearly polarized signals, which can get "lost" when antennas and receivers are out of alignment. Emissions from one of the UCI radiators, if you could see them, would appear as tiny spinning tornados. Beams of this shape are particularly effective at penetrating solid objects and providing detailed pictures of what's inside.

Heydari said his group's invention will be particularly beneficial in biomedical applications, as it will give doctors a way to differentiate tumour masses from healthy tissue. It could also be used in genomic research, equipping scientists with an instrument that can be so precisely tuned as to enable the excitation, or lighting up, of individual proteins.

But the new radiator can do a lot more than facilitate scanning and imaging. According to Heydari, it could be the key that unlocks millimetre-wave transmission as part of the fifth-generation wireless standard now in development. In addition, the tiny yet powerful chips can be embedded virtually anywhere. The internet of things will rely heavily on machines, buildings and other infrastructure being equipped with sensors and antennae. Driverless vehicles will only be possible if cars and trucks can detect each other.

"By using this millimetre-wave technology, cars all of a sudden become super-smart processing systems," Heydari said. "Vehicles will be able to communicate with one another, and radar capabilities will be enhanced, greatly improving blind spot detection and collision avoidance."

His lab's radiator work is sponsored by the Samsung Advanced Institute of Technology's Global Research Outreach Program.

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Nanowire "Inks" enable paper-based printable electronics

Highly conductive films make functional circuits without adding high heat

BY SUSPENDING tiny metal nanoparticles in liquids, Duke University scientists are brewing up conductive ink-jet printer "inks" to print inexpensive, customizable circuit patterns on just about any surface.

Printed electronics, which are already being used on a wide scale in devices such as the anti-theft radio frequency identification (RFID) tags you might find on the back of new DVDs, currently have one major drawback: for the circuits to work, they first have to be heated to melt all the nanoparticles together into a single conductive wire, making it impossible to print circuits on inexpensive plastics or paper.

A new study by Duke researchers shows that tweaking the shape of the nanoparticles in the ink might just eliminate the need for heat.

By comparing the conductivity of films made from different shapes of silver nanostructures, the researchers found that electrons zip through films made of silver nanowires much easier than films made from other shapes, like nanospheres or microflakes. In fact, electrons flowed so easily through the nanowire films that they could function in printed circuits without the need to melt them all together.

"The nanowires had a 4,000 times higher conductivity than the more commonly used silver nanoparticles that you would find in printed antennas for RFID tags," said Benjamin Wiley, assistant professor of chemistry at Duke. "So if you use nanowires, then you don't have to heat the printed circuits up to such high temperature and you can use cheaper plastics or paper."

"There is really nothing else I can think of besides these silver nanowires that you can just print and it's simply conductive, without any post-processing," Wiley added.

These types of printed electronics could have applications far beyond smart packaging; researchers envision using the technology to make solar cells, printed displays, LEDS, touchscreens, amplifiers, batteries and even some implantable bio-electronic devices. The results appeared online Dec. 16 in ACS Applied Materials and Interfaces.

Silver has become a go-to material for making printed electronics, Wiley said, and a number of studies have recently appeared measuring the conductivity of films with different shapes of silver nanostructures. However, experimental variations make direct comparisons between the shapes difficult, and few reports have linked the conductivity of the films to the total mass of silver used, an important factor when working with a costly material.

"We wanted to eliminate any extra materials from the inks and simply hone in on the amount of silver in the films and the contacts between the nanostructures as the only source of variability," said Ian Stewart, a recent graduate student in Wiley's lab and first author on the ACS paper.

Stewart used known recipes to cook up silver nanostructures with different shapes, including nanoparticles, microflakes, and short and long nanowires, and mixed these nanostructures with distilled water to make simple "inks." He then invented a quick and easy way to make thin films using equipment available in just about any lab -- glass slides and double-sided tape.

"We used a hole punch to cut out wells from double-sided tape and stuck these to glass slides," Stewart said. By adding a precise volume of ink into each tape "well" and then heating the wells -- either to relatively low temperature to simply evaporate the water or to higher temperatures to begin melting the structures together -- he created a variety of films to test. The team say they weren't surprised that the long nanowire films had the highest conductivity. Electrons usually flow easily through individual nanostructures but get stuck when they have to jump from one

structure to the next, Wiley explained, and long nanowires greatly reduce the number of times the electrons have to make this “jump”.

But they were surprised at just how drastic the change was. “The resistivity of the long silver nanowire films is several orders of magnitude lower than silver nanoparticles and only 10 times greater than pure silver,” Stewart said.

The team is now experimenting with using aerosol jets to print silver nanowire inks in usable circuits. Wiley says they also want to explore whether silver-coated copper nanowires, which are significantly cheaper to produce than pure silver nanowires, will give the same effect. This research was supported by funding from the National Science Foundation (ECCS-1344745 and DMR-1253534) and a GAANN Fellowship through the Duke Chemistry Department.

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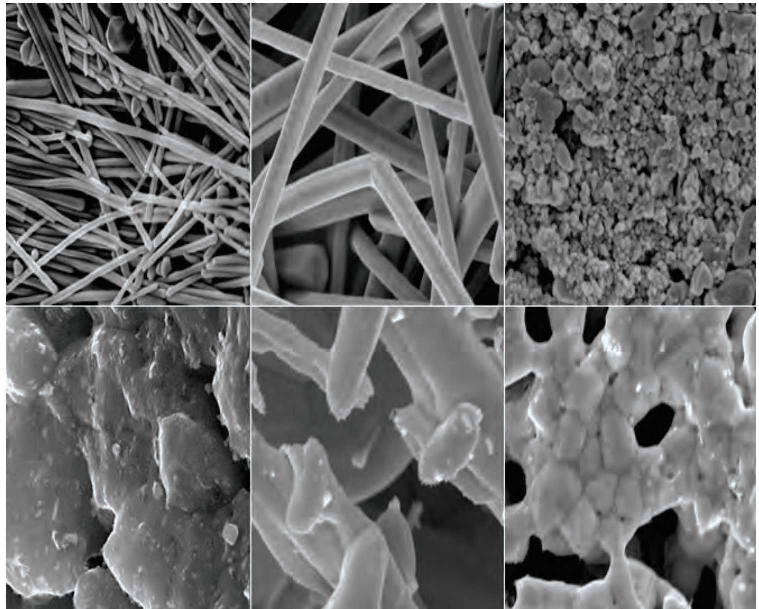

Reference

“The Effect of Morphology on the Electrical Resistivity of Silver Nanostructure Films,” Ian E. Stewart, Myung Jun Kim, and Benjamin J. Wiley. ACS Applied Materials and Interfaces, Dec. 16, 2016 (online). DOI: 10.1021/acsami.6b12289

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WET BATCHSPRAY POWER DEVICE MANUFACTURING

As history tells us, before a solution can be found, a problem must first arise that needs to be solved. The history of Siconnex began when a power device manufacturer was faced with this challenge and since then many new applications and solutions have been enabled throughout the semiconductor industry, including power, LED, analog/ mixed signal, MEMS, and many more.

Optimization of a standard power process: Al(Si) – freckle or Ti/TiN etch and resist strip

One of the most common processes within the power industry is Al etch followed by barrier or freckle etch and resist strip. This process sequence opened up the door to success for Siconnex at a European customer's site 12 years ago. The main issue faced by the customer was that this process sequence requires a large number of different wet benches full of chemicals, which at that time were mainly manually operated. This procedure involved wasting huge amounts of cleanroom space, exhaust gas, chemicals, and operator time. In addition, the result was barely sufficient in terms of particles and uniformity.

In standard production conditions, nobody wants to change an existing process or system. It's good to maintain a healthy scepticism when it comes to amending processes, but the possibility for improvement will eventually be exhausted. In this case, it was the sheer number of factors which were far from the optimum level that led to the decision being made to change the process.

At this stage, Siconnex introduced the Siconnex BATCHSPRAY technology. The system used was equipped with three chemical tanks and the option of using ozone in the process. With the Siconnex BATCHSPRAY solution, all the chemicals, water, ozone, and other gases are channelled to a process chamber, where they are sprayed onto a rotating batch or batches of wafers.

This principle enhances chemical exchange significantly. Furthermore, drying can also be performed inline in the process chamber.
With this solution, the customer combined the whole process sequence into one system with a 2.2 m^2 footprint and on a dry in–dry out basis.

As a further benefit, uniformity dropped to below 2 percent as a result of the high chemical exchange. This was achieved for "within wafer," "wafer to wafer," and even "batch to batch" uniformity thanks to the in-situ, automated end point detection system.

Throughput saw a significant improvement too once the whole sequence was processed without interruption and intermediate drying. With operators not having to carry the wafers from one wet bench to another, the throughput was more than doubled.
One of the most important benefits was the use of ozone, which made it possible to replace the solvent chemical entirely. This is a huge benefit in terms of cost, since only O_2 is needed to generate O_3.

Additionally, this is an advantage for the operators. Since most solvents are hazardous chemicals and replacing them with what is basically air leads to a much better working environment.

"The use of ozone made it possible to replace the solvent chemical entirely." When all the benefits of this optimized process technology are summarized together, the real cost-saving potential is revealed:

- Combination of four processes:
- Al etch
- Freckle etch
- Ti/TiN etch
- Resist strip

(up to five processes are possible in total)

- Simultaneous processing of 50 wafers
- Average process: 45 min
- Average throughput: 67 wph
- Uniformity: <2 percent
- No solvent required
- Dry-to-dry process

Taking all of this into account, the typical time for return on investment (ROI) is close to one year, depending on the existing process.

This process with the Siconnex BATCHSPRAY technology has been implemented at 16 plants around the world and continues to be in high demand among existing and new customers alike even after 12 years.

State-of-the-art technology, processing of SiC, and GaN for high-end technology

One of the changing factors within the power device industry is the wafer material used. For high frequency, high power, high temperature, or low leakage current, compound semiconductor substrates are used to ensure that the increasing requirements are met. The two materials most commonly in use at the moment are SiC and GaN.

For these materials, Siconnex has developed, and is still developing, processes so as to put itself in a position to provide state-of-the-art equipment. The focus of these investigations is to provide cleaning technologies for new materials, as well as the possibility to perform uniform etching.

300 mm Semiconductor Manufacturing

Although the current power market is focused predominantly on 200 mm or below, Siconnex is already one step ahead, providing its BATCHSPRAY platform–fully automated and ready for full integration in state-of-the-art 300 mm fabrication plants–for all semiconductor sectors.

In this case, two BATCHSPRAY process chambers share one robot. Each chamber is able to process 25 wafers with a diameter of 300 mm simultaneously. The results for 300 mm wafers are the same as or even better than the results achieved for 200 mm,

meaning that uniformity values below 2 percent are standard. The Siconnex BATCHSPRAY system is the method of choice for high-volume, low-cost production.

Future challenges

Siconnex is looking forward as technology progresses, seeing every challenge as a possibility to provide the ideal solution. A future step within the power sector is going to be keeping an eye on the evolution of emerging materials like AIN, diamond or Ga_2O_3 and developing the solutions the industry needs.

Besides the power sector, Siconnex also provides solutions for markets such as LED, MEMS, analog/mixed signal, and many more. Our goal is to replace wet benches with the Siconnex BATCHSPRAY technology to help our customers save resources and money, while also achieving better process results. For this reason, Siconnex is constantly looking into new applications within existing and new markets. In the Siconnex laboratory, new processes are developed and existing processes continually optimized.

The Siconnex equipment development team works closely with the process team to guarantee that the rising demands placed on Siconnex systems are fulfilled and that our systems are at the cutting edge of technology.

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“Besides the power sector, Siconnex also provides solutions for markets such as LED, MEMS, analog/mixed signal, and many more. Our goal is to replace wet benches with the Siconnex BATCHSPRAY technology to help our customers save resources and money, while also achieving better process results”

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PLASMA DICING

Strength in numbers

The demand for smaller electronic products including burgeoning IoT applications has led to new focus on die size and wafer singulation. Richard Barnett, Etch Product Manager at SPTS Technologies explains how the benefits of plasma dicing grow as die continue to shrink.

WITH THE ever-constant evolution of new technologies for mobile applications now extending to even smaller "wearables", the need to make device packages even smaller, thinner, faster and power efficient shows no signs of abating. We, the consumer, are fuelling this with our expectations; that mobile and wearable devices survive lifestyle activities; that medical/automotive/smart-home sensors function for as long as is needed, etc.

One parameter above all others coming to the fore as a consequence of device shrink and performance expectations is die strength, which is something that plasma dicing has the capability to improve significantly.

Conventional blade and laser dicing will still be a cost-effective method to singulate die in some cases; however, there are a growing number of applications where plasma dicing can offer economic and die quality benefits when compared to conventional techniques. In some cases, namely for smaller and thinner die, plasma dicing enables singulation which is virtually impossible with the other methods. Plasma dicing before grind (DBG) has been used in selected applications for a number of years, but plasma dicing after grind (DAG) is at the early stages of adoption for volume production. The trend toward thinner, smaller die, along with the in-service reliability demands, distinguishes plasma dicing as an increasingly attractive alternative.[1]

Silicon plasma dicing uses Deep Reactive Ion Etch (DRIE) technology, more typically referred to as the "Bosch" process. This is a well-established production technology, used in silicon MEMS micromachining and via etching in 3D packaging. DRIE is now adding dicing technology in the "back-end" of semiconductor processing to its portfolio of production applications. Like any other dry step in the device process flow, integration is key, and these challenges are the only gate to the use of plasma as a singulation method. These considerations are not only related to wafer layout and preparation, but also accommodating the standard back-end frames and tape combinations. The objective is that the process flow not be disrupted to the point where it becomes a hindrance to the adoption of a technology that offers so many potential benefits.

Benefits of plasma dicing

No Damage = Stronger Die / Higher Yield

In mechanical dicing, (especially for small die or thin wafers when using high feed speeds), the risk of chipping at the edge of the die is an issue. In laser dicing heat damage has to be accounted for, which becomes a more significant threat for smaller/thinner die. As a chemical process, plasma dicing eliminates all of the damage caused by the other mechanical methods, e.g. crack initiation, thermal damage, edge chipping, and vibrations. Plasma can also remove the need for fluids used to cool blades and remove debris. The Bosch process, which is made up of alternating etch and passivation steps, creates characteristic "scallops" on the sidewalls of the die (see Fig 1), with each scallop representing a single etch-passivation cycle. They are generally $<3\mu m$ in depth and as they are the result of a chemical etch do not cause crack initiation nor act as stress raisers. In plasma dicing the wafers are held electrostatically on a chuck with active cooling to maintain a low wafer and tape temperature, which are important for maintaining tape integrity for the subsequent expansion and pick-and-place steps. Plasma dicing is also attractive for fragile devices

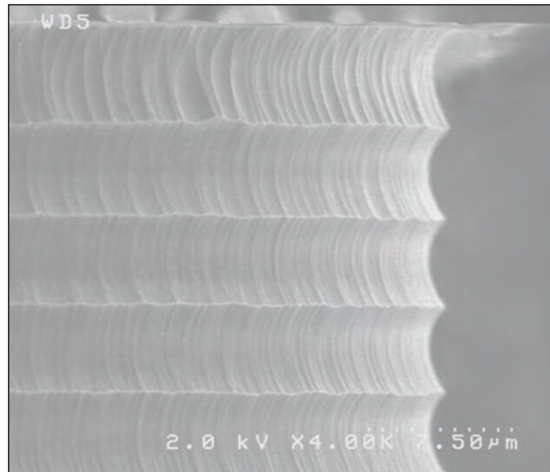

Fig 1 Characteristic DRIE scallops cause no crack initiation

such as MEMS, with movable structures and thin membranes, as there are no physical forces to vibrate the wafer and damage the devices.

Increased die counts

When using a conventional dicing method, the lane width is determined not just by the width of the saw blade or laser spot, but also by the placement and accuracy for test pads and damage limitation. Considering plasma, lanes are not restricted in the same way and can be made much narrower, freeing up valuable silicon real estate for more die per wafer. For smaller die, like RFID chips (at~$0.04mm^2$), this saved real-estate can give a potential increase of 80% more die per wafer. With plasma dicing eliminating the risk of crack initiation at the die edge, any "crack stop areas" can be eliminated from the die layout freeing up yet more space for active die. (There still needs to be a motivation by the user to move test structures out

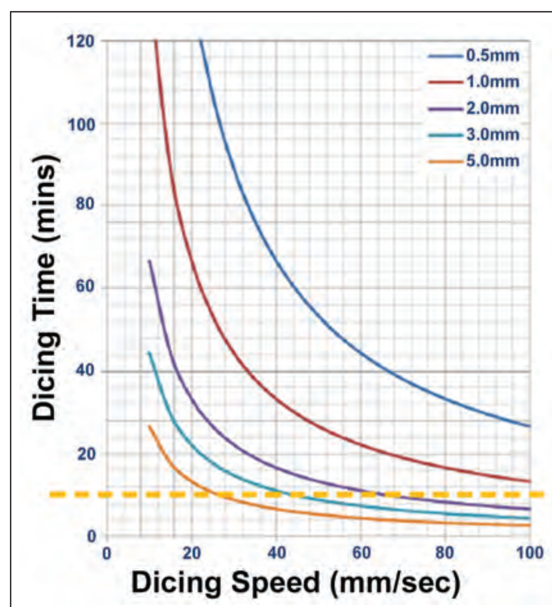

Fig 2: Curves showing how blade and laser increase cycle time as die size reduces. Plasma dicing (orange dashed line) has constant dicing "rate" regardless of die size.

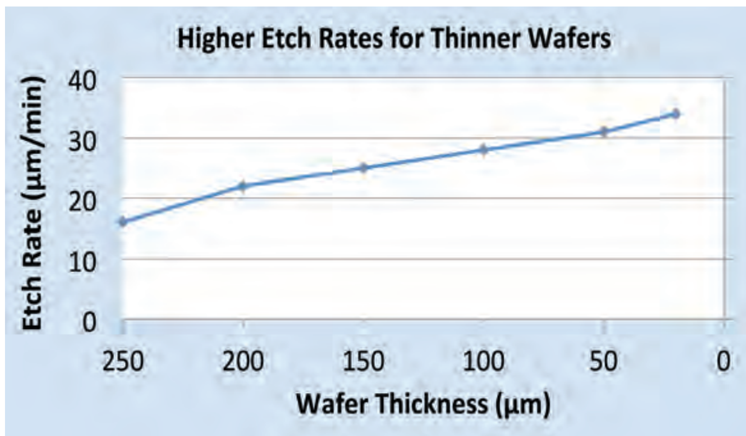

Fig 3 Effect of wafer thickness on silicon etch rate

from lanes to achieve full realisation of benefits.) As well as reducing lane width, plasma dicing can also increase die per wafer because the wafer layout is not constrained by the need to have orthogonal dicing paths. Plasma dicing gives device designers much greater flexibility with regard to fundamental die shape and size, removing guard rings and positioning test groups to make best use of the available wafer area.

Increased throughputs for smaller, thinner die

As die sizes shrink, allowing more die to be patterned onto wafers, the number of dicing lanes increases. For serial methods such as laser or saw, the consequence is a significantly reduced throughput as the number of cutting passes grows as the die size reduces (see Fig 2). Plasma dicing is a parallel process, with all dicing lanes etched simultaneously. The throughput of plasma dicing is largely governed by the wafer thickness, or aspect ratio of the etch, and not by the number of dicing lanes or die per wafer.

Also, with the industry generally driven toward thinner die, mechanical sawing and laser dicing become more difficult. Further decreases in throughput occur as feed speeds are reduced to prevent damaging these fragile devices. Conversely for plasma dicing, thinner wafers are quicker to etch through because there is less silicon to remove, and etch rates are higher for thinner wafers (see Fig 3). Both these factors increase throughput, while still improving the physical integrity of the die.

Due to the front-end genesis of the plasma approach, cluster platforms are available capable of carrying multiple modules thereby giving an easy scaling from pilot to volume production.

Consistency = Increased throughput

Plasma dicing is a repeatable technique which will process wafer-after-wafer in exactly the same manner, unlike blade dicing that requires regular blade dressing (reducing throughput) to maintain a consistent blade shape and performance. Consistency reduces the need for inspection and further cements the yield and quality advantage for the plasma dicer.

Integration considerations

Designing in plasma dicing from the outset of a device lifecycle is the easiest way to realise all of the benefits that the technique can provide. However, in this article we present novel approaches which have already proven that plasma dicing can be immediately adopted into existing process flows.

The most common integration challenge facing plasma dicing is the potential range of materials that can be encountered in the dicing lane. Currently, plasma dicing is a silicon etch activity and as previously mentioned uses the Bosch process to achieve this in a process module designed as a silicon etcher. This means that any metals or dielectrics in the dicing lane cannot be etched without causing compromise to the substrate. To complete die singulation additional steps are required. Metal is the worst case scenario. Metal in the lanes can be “designed out” for new device layouts, but for existing products it may be necessary to remove the metal layers earlier in the process flow.

Alternatively, lasers or mechanical saws can be used to “pre-define” the dicing lanes. Using this method is more typically valid for larger die which will be less affected by the obvious throughput impediments of the definition step. Other methods for defining the dicing lane include standard photolithography, although the additional masking step to define the dicing lanes is sometimes viewed by some as a

As die sizes shrink, allowing more die to be patterned onto wafers, the number of dicing lanes increases. For serial methods such as laser or saw, the consequence is a significantly reduced throughput as the number of cutting passes grows as the die size reduces

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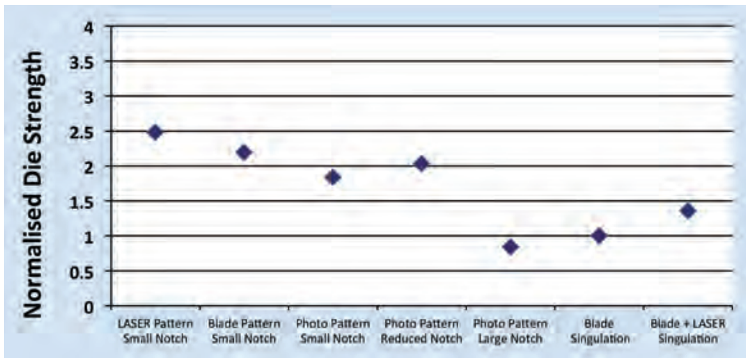

Fig 4 Effect of dicing method on die strength

hindrance to adoption. More easily adopted is the approach of using existing layers that are extended to allow for erosion of this material during plasma etching. This latter method can be described as maskless.

Test pads are a crucial part of back-end flow, and test probes need a certain size for testing. In conventional dicing schemes, the pads are often located in the relative large dicing streets and simply removed away by the dicing method. When plasma dicing is introduced, allowing the designer to reduce the lane widths, it leaves the question of where to put the test pads. Utilising the additional real estate from reducing the lane widths and combining with the flexibility of die shape/positioning it is fairly straightforward to move test pads elsewhere on wafer, or even adopt an "on-die" test pad scheme.

Tape choice is important. With proper process control most can be used, but some will behave better than others. The choice will depend on the subsequent steps e.g. if you have a backside metal, the DRIE will not etch this. As part of backside metal separation the metal must stick to the tape during pick and place, while the adhesive is able to release the die for easier picking. There are a variety of materials used for tapes and adhesives and when checking suitability for plasma dicing, the user must concentrate on the film material and the adhesive strength parameter. Both of these will give some early warning of potential problems during plasma dicing. Tape properties due to exposure to the plasma also need to be considered. Most tapes are non-conductive and will become positively charged during the plasma processing, which deflects negative ions within the plasma towards the silicon sidewall, creating a "notch" at the bottom of the etch feature near the tape. The same effect is observed in etching MEMS devices from silicon-on-insulator (SOI) wafers where the oxide becomes charged once exposed. Patented methods to combat this "notching" developed for the MEMS industry have now proved useful to optimise plasma dicing to a tape.

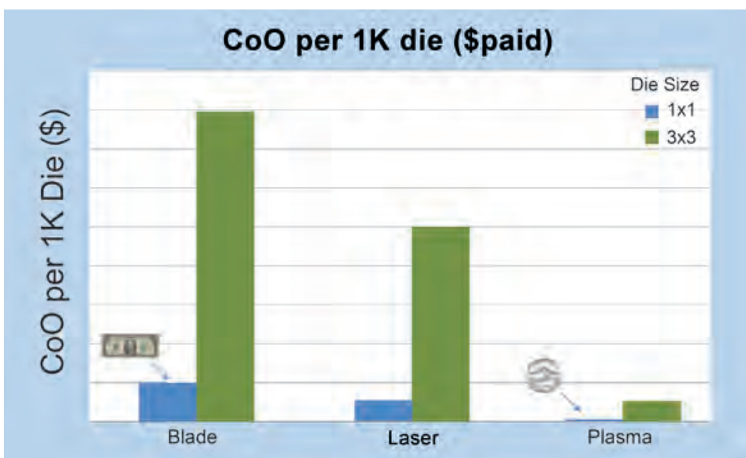

Fig 5: Cost of ownership comparison for blade vs. laser vs. plasma dicing for two different die sizes, (incorporating the possibility of a thinner wafer and narrower dicing lanes for plasma dicing.)

Die strength comparison

Recent work [2] has shown that plasma dicing typically doubles the strength of resulting die, even if integration with the existing process flow determines that the dicing lanes must be pre-defined by a blade or laser. Even with these combination methods, significant strength/yield increase can still be achieved. However, Fig 4 also emphasises the importance of plasma processing control, illustrating how plasma dicing, even defined by photolithography, can in fact reduce die strength if the process control is poor and a large notch is allowed to form at the tape interface. Plasma dicing can offer significant advantages over other dicing methods, but without good process control these benefits can be negated by undesirable damage to the die.

Plasma dicing eliminates all physical damage phenomena as seen with conventional methods. For plasma it is also important that notching at the Si-to-tape interface mentioned above is also tightly controlled. Two patented technologies, already well-established and proven in SOI MEMS manufacturing, can be employed to prevent damage to the silicon and the tape during plasma dicing. First, a proprietary end-pointing technology [3] can accurately monitor the progress of the etch front and manage a change in recipe conditions when the tape is exposed. Patented "bias pulsing" [4] can then be used during the final stage of die singulation to control the final stages of the etch, preventing any lateral under-etching of the die, or "notching." Fig 4 shows how the strength of plasma diced die with "small" or optimized "reduced" notching is typically twice that of a blade or blade/laser approach. However, plasma dicing with no control of the notching will severely compromise die strength.

Cost of ownership comparison

In some cases, where the die size is not particularly small, the relative throughput of laser dicing could appeal to prospective users, especially when the capital cost of a laser dicing system is generally less than a plasma etch system. However, careful consideration must be given to the ongoing cost of ownership when selecting the right solution for an application, as well as the trends in die size and

wafer thickness. When all the benefits of plasma are realised, combining all of the topics previously discussed, this reveals a major cost advantage over conventional methods.

In the Fig 5, we have compared the cost of singulating 1,000 die for two die sizes, 1 mm x1 mm and 3 mm x 3 mm. For the conventional methods a 100 μm thick wafer is used with 80 μm dicing lanes. For plasma dicing, the wafer is thinned to 50 μm with lanes reduced to 10 μm. When coupled with yield gains and ability to eliminate crack stop areas, it is easy to see that the plasma approach significantly reduces the cost contribution of the singulation step. For the 1 mm x 1 mm die, the blade singulation cost per 1000 die is 20 x that of the plasma dicing approach.

Dice after grind for 300 mm wafers

Plasma dicing after grind is typically carried out on thinned, ground wafers mounted on tape frames. Until recently DRIE sources were only available for processing silicon wafers up to, and including 300 mm in diameter. A 200 mm/8" wafer, on a standard tape frames with an external diameter of 296 mm, could therefore be accommodated within an existing 300 mm-compatible silicon etch plasma source. This enabled plasma dicing of taped 200 mm wafers to be demonstrated relatively easily, notwithstanding the other issues associated with etching to a tape, discussed above.

A 300 mm/12" wafer, however, requires a frame with an exterior diameter of 400 mm, which was too large to be handled and processed in existing 300 mm DRIE equipment, so a new system was developed taking on board all of the learning achieved on the original 200 mm DAG platform and process module. In 2016, SPTS released a new silicon etch source with a larger plasma chamber and automated wafer handling for this larger substrate size.

Summary

Despite many integration challenges, plasma dicing offers considerable benefits for die singulation, providing opportunities to achieve increased throughput and die count per silicon area as well as flexibility for die layout and design. Perhaps most important of all, plasma dicing provides improved die quality and strength. As such, plasma dicing is well positioned to become the benchmark technology for fabs seeking to increase die strength, throughputs and yields for small or thinned and fragile die on 150 mm, 200 mm or 300 mm wafers.

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Further reading

[1] Thin Wafer Processing and Dicing Equipment Market report, Yole Développement, May 2016

[2] R. Barnett, D. Thomas, O. Ansell, J, Carpenter, W. Worster, G. Ragunathan "Improving Device Yields and Throughput using Plasma Dicing" presented at IWLPC2015

[3] US Patent No 9,159,599 – "Apparatus for chemically etching a workpiece"

[4] US Patent No: 6,187,685 - "Method and apparatus for etching a substrate"

Hydrogen in Electronics:

Growing applications and consumption

Hydrogen will play an increasing role in semiconductor manufacturing due to its wide serviceability and importance in extreme ultraviolet (EUV) lithography. Linde Electronics' head of market development, Dr. Paul Stockman, explains why ensuring a safe and reliable source of hydrogen will be critical for next-generation device manufacturers.

COLORLESS, odorless, and even burning with an invisible flame, hydrogen is nevertheless omnipresent in the semiconductor fab and an increasingly important material for chip manufacturing. Leading-edge wafers consume more than their own weight of this ultra-light gas during processing and the long-anticipated adoption of EUV (extreme ultra-violet) lithography will drive demand even further.

This article reviews the properties of hydrogen that make it essential for leading-edge semiconductor manufacturing, details the specific processes that require hydrogen including the coming high-demand EUV application, and reviews the different supply options available.

Important properties of hydrogen

Composed of the lightest element, molecular hydrogen (H_2) has some extreme properties that give rise to its usefulness and hazards.

Chemical reducer: Molecular hydrogen is useful for the direct substitution of hydrogen atoms for other elements, as well as influencing the pathways of key chemical reactions.

Heat transfer: Hydrogen is able to convectively remove heat faster than any molecule other than helium.

Light mass: Hydrogen is one of the smallest molecular compounds of any gas or liquid fluid and can therefore "fit" in places that other molecules cannot, including in the porous voids of some solid materials. Its light mass also makes it relatively inexpensive to transport on a volume basis, but conversely expensive to transport on a mass basis. Compared to air, hydrogen is nearly 15 times lighter and quickly rises and diffuses.

Kinetic isotope effect: Chemical reaction rates change when one stable isotope of an atom is changed for another. Often this is a slight effect, but because hydrogen's (mass = 1 amu) stable isotope deuterium (mass = 2 amu) is twice as heavy, this effect can be significant.

Low boiling point: Hydrogen boils at a very low 20.7 K (-423.2°F or -252.9°C), second only to helium. It therefore takes a lot of energy to liquefy hydrogen, a consideration in its transport and purification.

Flammable and explosive limits: Hydrogen's most hazardous properties are its wide range for flammability (ability to burn with an ignition source) and explosivity (ability to explode or to cause a shock wave) in air. Hydrogen forms flammable mixtures between 4 and 75% concentration in air, and explosive mixtures between 18 and 59% in air. Fortunately, the buoyancy of hydrogen relative to air means small leaks of hydrogen usually diffuse rapidly below these limits.

Existing process applications

Hydrogen has been adopted as a material in processes throughout the fab. Its unique chemical properties continue to expand its usefulness. These applications typically use flows of 100s to 1,000s of sccm (standard cubic centimetre per minute):

Epitaxy: Hydrogen is used as a reducing agent during the epitaxial growth of crystalline thin-films. This is often used to make a starting silicon surface for semiconductor manufacturing by reacting newly cut and polished silicon wafers with trichlorosilane ($SiHCl_3$) in an epi-house or end-user fab. The hydrogen reduces the gas-phase chlorine atoms, and the HCl product is removed from the reactor as a gas. Leading-edge channel materials like strained silicon, silicon-germanium, and germanium are also grown using hydrogen-mediated epitaxy.

Deposition: Hydrogen can also be incorporated directly into thin-films to disrupt crystal lattices to make them less crystalline, more amorphous. This is often used with silicon thin-films, which need to be made more electrically insulating.

Plasma etch: Hydrogen and hydrogen-containing plasmas are used to directly react with the surface of the wafer in order to clean or remove unwanted thin films, especially for removing unwanted fluorocarbon deposits on silicon oxides.

Anneal: Silicon wafers are heated to temperatures over 1000°C, often at elevated pressure, in order to repair their crystal structures. Hydrogen assists by transferring heat uniformly over the surface of the wafer, and also by penetrating into the crystal lattice to react with atomic impurities.

Passivation: Hydrogen is used to react and remove native oxides on silicon surfaces and to mediate the reconstruction of silicon-silicon bonds in the final layers of the crystal.

Ion implantation: With more precision than bulk annealing and passivation, protons produced from hydrogen gas can be implanted to specific depths and concentrations in a thin film using ion implanters. Not only can hydrogen atoms be inserted to modify a thin film, but in higher doses and implantation energies, it can be used to cleave slivers of silicon and sapphire wafers.

Carrier gas: Hydrogen is used as a carrier gas to entrain (entrap) and transport less volatile chemicals—ordinarily liquids at atmospheric pressure and room temperature—into the reaction chamber. The hydrogen is heated and bubbled through the liquid chemicals. Because the mass of hydrogen is very light compared to entrained chemical vapor, specialized mass flow controllers can then be used to sense, measure, and precisely control the amount of chemical vapor dispensed.

Deuterium defense against hot-carrier injection: Hydrogen bonds to silicon at thin-film interfaces are susceptible to breakage by hot carrier injection, which are electrons and holes caused by short-wavelength radiation like x-rays and gamma rays. In semiconductor structures, deuterium-passivated thin-films have different bond strengths, and a much lower probability of cleavage due to hot carriers.

This is particularly important for chips in critical applications and those in environments with high levels of short-wavelength radiation, like spacecraft. Like regular hydrogen annealing and passivation, deuterium is reacted with wafers in a pressurized furnace at high temperatures.

Material stabilization: The addition of hydrogen extends the shelf life of important electronic materials like diborane (B_2H_6) and digermane (Ge_2H_6), which otherwise slowly decompose. The slightly stronger bonds in deuterated stannane (SnD_4) allow it enough stability in a deuterium balance to be useful; the normal isotope version of stannane (SnH_4) decomposes too quickly to have commercial applications.

Package	Volume [m^3]
Cylinder	7
Compressed gas trailer	10,000
Liquid trailer	40,000

Application for EUV

Extreme ultraviolet (EUV) lithography is the much-anticipated new application expected to simplify the process patterning complexity for critical dimensions in leading-edge devices. While it has taken a long time for this technology to come close to commercialization, top-tier manufacturers are coalescing their predictions for volume manufacturing adoption in the 2018-2020 window. Whereas other hydrogen-consuming applications have a usage rate of 100s of sccm, EUV will require much larger flows of 100s of slm (standard liters per minute), or roughly 100 to 1000x more per individual tool.

Deep ultraviolet (DUV) lithography, the current workhorse of the patterning tools, uses an electrical discharge in neon or krypton mixed with halogen gases like fluorine to produce UV light at 193 nm and 248 nm; EUV light production is much more complicated. Tin metal is heated above its melting point of 232°C, and small droplets of tin (~25 μm diameter) are rapidly (50,000 droplets per second) produced. These droplets are first vaporized and then excited with high-power CO_2 lasers. The excited tin atoms emit EUV light at 13.5 nm, which is more than 14 times shorter than the DUV tools.

The light is emitted in all directions and is collected and collimated (aligned) by an array of mirrors. The light is then passed to the primary lithography tool for focusing and image transfer before illuminating the photoresist on the wafer. All materials heavily absorb EUV light. Absorption losses are minimized by using multi-layer reflective optics instead of the transmissive lenses used in DUV lithography, and the entire light source and patterning systems are housed in vacuum chambers. These highly complex tools are expected to cost end users around $100 million USD each, and when fully adopted, a leading-edge fab could require 20 or more of these tools.

Scattered tin debris from the vaporization of droplets is a major potential source of contamination of both the collector and focusing optics. Unmitigated, the lifetimes of these expensive components would be unacceptable. Hydrogen gas is used to shroud the tin excitation region, and tin vapor and aberrant droplets are reacted to form stannane (SnH_4), which is then removed from that section of the housing by means of the vacuum line. Higher flows of hydrogen can be used in periodic plasma-based cleaning to remove tin that deposits on the collector optics.

Demand and supply

Even before the adoption of EUV technology, leading-edge logic and foundry processes have begun consuming several normal cubic meters (1000 liters) of hydrogen per wafer processed. This usage trend is expected to continue increasing in the 10 nm and 7 nm nodes commercialized before widespread EUV use. Consequently, major fabs now use hundreds of Nm^3 per hour. EUV, when fully extended to all of the critical layers, will roughly double the amount of hydrogen used in these fabs. In a related application, the largest LED fabs also use hundreds of Nm^3 of hydrogen per hour, primarily as a carrier gas and diluent for the gallium, arsine, and phosphorus precursors used to make the light-emitting devices.

Supply of hydrogen to electronics customers has historically been driven by regional source types, engineering and transportation codes, and by end user preferences and process qualification. However, steep demand curves are causing users to consider new supply schemes for access to larger volumes, greater supply chain security, and lessening of local fab logistics.

Over 60 million metric tons of hydrogen are produced globally, almost exclusively from hydrocarbon feedstocks: natural gas, oil, and coal. Most of this is used as a chemical intermediate to make ammonia, methanol, and transportation fuels. Electronics manufacturing consumes much less than 1% of global hydrogen production.

Hydrogen is supplied in the following modes:

Cylinders: In smaller volumes, hydrogen is supplied in standard-sized gas cylinders, which hold about 7 m^3 of gas pressurized at approximately 175 bar (250 cu ft at 2,500 psi). The largest fabs now consume this amount in less than one minute. Individual cylinders can be manifolded together to create larger packs of cylinders, which are typically mounted into metal pallets for easier handling. These packs can even be arrayed into full truck trailers of connected cylinders. Despite the increased volume, there is a limitation on the level of mass flow that can be safely achieved from this configuration.

Supply of hydrogen to electronics customers has historically been driven by regional source types, engineering and transportation codes, and by end user preferences and process qualification. However, steep demand curves are causing users to consider new supply schemes for access to larger volumes, greater supply chain security, and lessening of local fab logistics

Compressed gaseous hydrogen (CGH) trailers: To improve on both mass distribution and packaging/handling costs, specialized trailers with much larger, pressurizable vessels are used. These CGH (compressed gaseous hydrogen) trailers can hold 10,000 Nm^3 at pressures similar to smaller packages, yet are the distribution equivalent to over 1,400 individual cylinders. Just as importantly, fewer, larger vessels are faster to fill, and easier to maintain quality to the very high standards required by the semiconductor industry. Fewer components and

Compressed gaseous hydrogen (CGH_2)

Economical transport for short to medium distances

Liquid hydrogen (LH_2)

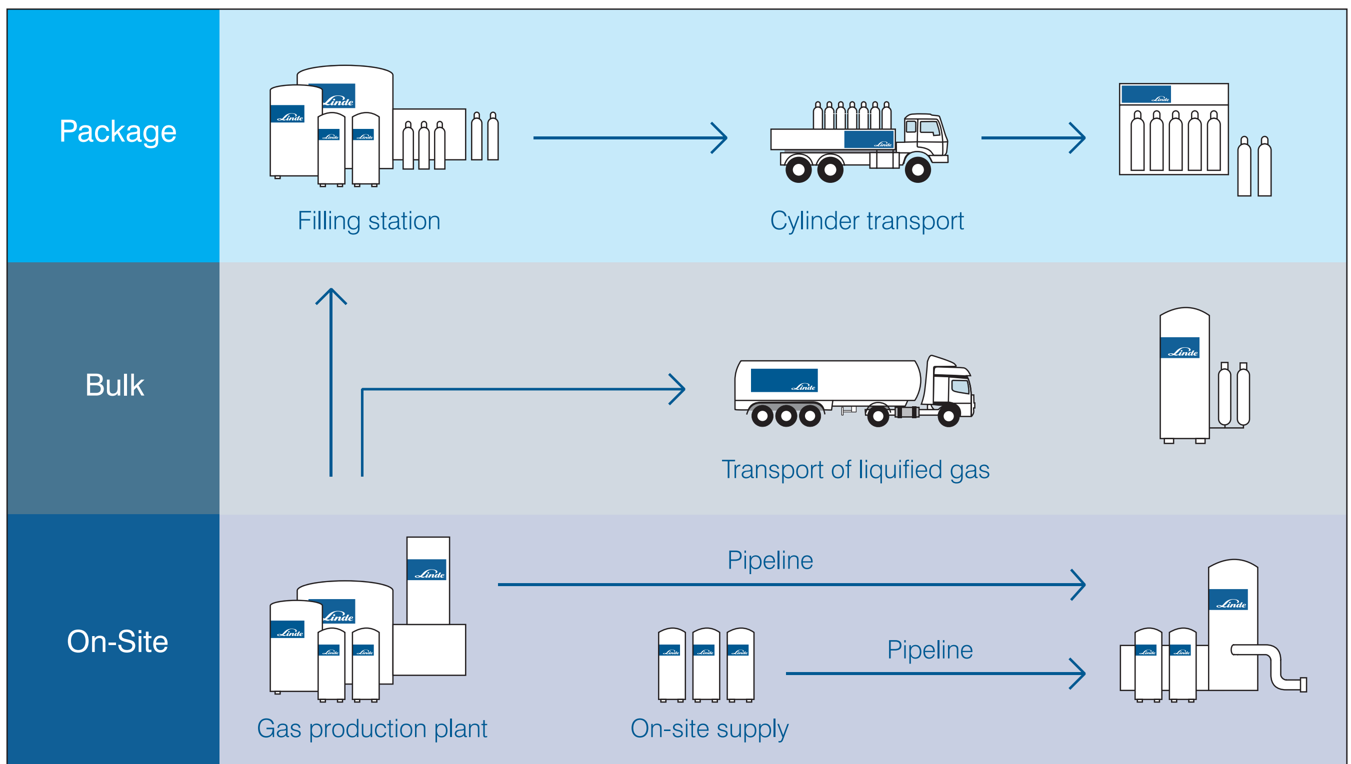
Economical transport for medium to long distances

(only in U.S. and Europe)

On-site production

Production through steam reforming or electrolysis

No hydrogen transport costs



human interactions also reduce safety risks.

Liquified hydrogen transport: In North America and much of Europe, liquefied hydrogen transport is allowed. This further increases the amount of hydrogen per truck to 40,000 Nm^3 gas, or the equivalent of around 6,000 cylinders. In addition to increasing the volume, liquefication of hydrogen is also an added purification step. By cooling the material down to the boiling point of 21 K (-252°C), most impurities are solidified and can be reduced in concentration by absorption.

These benefits come with a trade-off, however. Liquefying hydrogen to the very low required temperatures consumes a lot of energy, and mandates additional safety protocols. Moreover, there are fewer liquid hydrogen production sources versus gaseous facilities, and transportation distances and supply logistics can be substantially increased. It is important to note that liquid hydrogen transport is not allowed in the primary semiconductor producing countries of Asia (China, Japan, Singapore, South Korea, and Taiwan), and therefore not a consideration for users in that region.

On-site hydrogen production: A solution that is becoming appropriate for some fabs is on-site hydrogen production. All major fabs already have either direct on-site production of gaseous nitrogen, or are supplied via pipeline by local plants. On-site hydrogen production has similar considerations of footprint, redundancy, and back-up. On-site hydrogen technologies suitable for semiconductor processes are either electrolysis of water or so-called "shifting" or "cracking" of hydrocarbon feedstocks. Electrolysis is relatively expensive at volume because of the energy needed to break water molecule bonds even though achieving purity in the feedstock water is relatively simple. More economical are hydrocarbon feedstocks like natural gas, LPG (liquefied petroleum gas – mostly propane and butane), and methanol. Choices for the exact plant technology depend upon the local feedstocks available and the customer quality profile requirements.

Regardless of whether the hydrogen is supplied in gaseous or liquefied containers or made on-site, semiconductor hydrogen supply schemes incorporate on-site, and often additional point-of-use, purification using various technologies: adsorption, gettering, and application of the unique property of hydrogen to diffuse through palladium metal membranes, which are impervious to most other molecules. In addition, hydrogen purity is monitored at several points in the distribution by multiple types of detectors. Deuterium, an isotope of hydrogen, increasingly is being used as chips are put into critical applications, and device dimensions are reduced to the atomic scale where one misplaced atom can result in chip failure. Because it is used in smaller amounts and is a very high cost material, deuterium is only packaged in individual cylinders.

Deuterium is produced by electrolysis of heavy water (D_2O), which is then further dried and purified before being compressed and packaged. Heavy water is produced primarily as a reaction moderator of certain uranium-based nuclear reactors. For higher flow applications, it can be feasible to recover deuterium from the waste stream and reprocess it off-site.

Safety

As with all chemical supplies, safety is paramount. With hydrogen, the main safety risk is associated with its wide range of flammability and explosivity. Throughout production and packaging, multiple types of redundant protocols are used to ensure that no oxidizers are contacted or incorporated into the hydrogen and plant designs minimize the risk for leaks.

Specialized clothing resistant to fire and static is worn in some hydrogen producing and using environments. Materials of construction and component qualification are also important to guard against a phenomenon known as hydrogen embrittlement, where at elevated temperatures and/or pressures, hydrogen can permeate and weaken certain metals and alloys. Finally, liquefied hydrogen introduces the additional risk associated with cryogenic materials and the need to use insulating vessels and personal protection.

Conclusion

Semiconductor manufacturing has long used hydrogen in an essential and expanding portfolio of applications. The supply of hydrogen is already a bulk material scheme, with source, transport, and logistic considerations. The adoption of EUV at leading-edge fabs in the next few years will accelerate the pace of hydrogen consumption, and drive the consideration of new supply schemes. End users should evaluate hydrogen supply options for future fabs as part of their advanced planning to ensure that their quality, supply, and process integrity requirements will be met.

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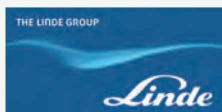

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Extending the era of Moore's Law through lower-cost patterning

Researchers at the University of California at Berkeley and Axcelis Technologies have taken a different approach to extending the Moore's Law era of solid-state transistor evolution. By using their techniques, it may be possible to forestall introducing extreme ultraviolet (EUV) lithography or simplify the multi-pattern processes that are typically used to produce today's most powerful ICs. By Peng Zheng[A], Leonard Rubin[B], Tsu-Jae King LiuA and Mark Andrews

INTEGRATED CIRCUITS (ICs) at the heart of today's most advanced computers, smartphones and myriad other devices depend upon solid-state transistors that have reliably gotten smaller and less expensive since the mid-1960s. Intel Co-Founder Gordon Moore's principles (Moore's Law) have predicted the evolution of transistor technology for more than 50 years. But miniaturizing device structures to pack more transistors into smaller spaces can only continue to a certain practical limit, which most manufacturers agree is fast approaching [1].

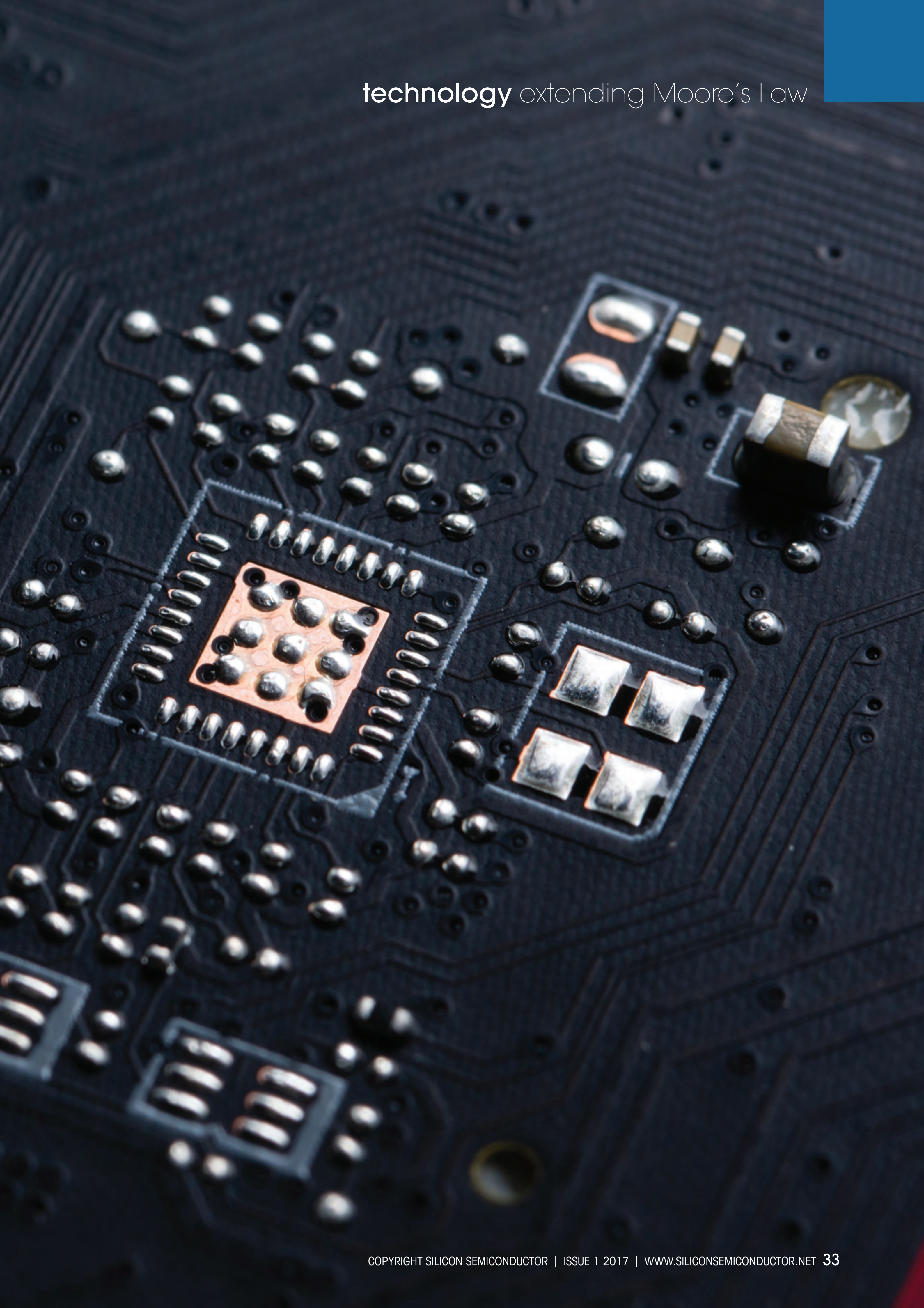
To achieve regular cost reductions through smaller geometries and increased transistor density semiconductor manufacturers have developed novel techniques that extend the limits of 193nm photolithography. As the minimum feature size of an IC has been scaled to well below the wavelength of UV light, the semiconductor industry has faced a growing challenge to increase transistor density at ever lower costs [1]. To pattern features with a resolution and pitch beyond photolithographic limits, more restrictive design rules [2] and "multiple patterning" techniques have been adopted in high-volume IC manufacturing.

But while multiple pattern approaches along with FinFETs, fully-depleted silicon-on-insulator (FDSoI), 3D ICs and chip stacking designs have enabled better performance in smaller form factors, these approaches have also typically elevated costs or extended processing time, or both. But even if cost-neutral, no multi-patterning technique can rewrite physical laws that will eventually end CMOS device miniaturization.

Self-aligned double-patterning (SADP) is a multiple patterning approach that was first demonstrated to be advantageous for forming sub-lithographic fins in a FinFET fabrication process [3] and more generally for increasing feature density [4], which has since been used for the manufacture of non-volatile memory chips (beginning at the 34 nm node in 2008 for Micron's 32 Gb flash memory product [5]) and more recently for leading-edge microprocessors (Intel's 14 nm FinFET process [6]).

It is anticipated that iterative double-patterning ("quadruple patterning") will be needed to achieve ever higher transistor density [1]. Also, as the feature density of the lowermost interconnect layers increases, more IC layers will need to be patterned using SADP or other double-patterning techniques. As a result, patterning-related costs will escalate [7] and could bring the era of Moore's Law to an end.

Major silicon IC manufacturers have considered other



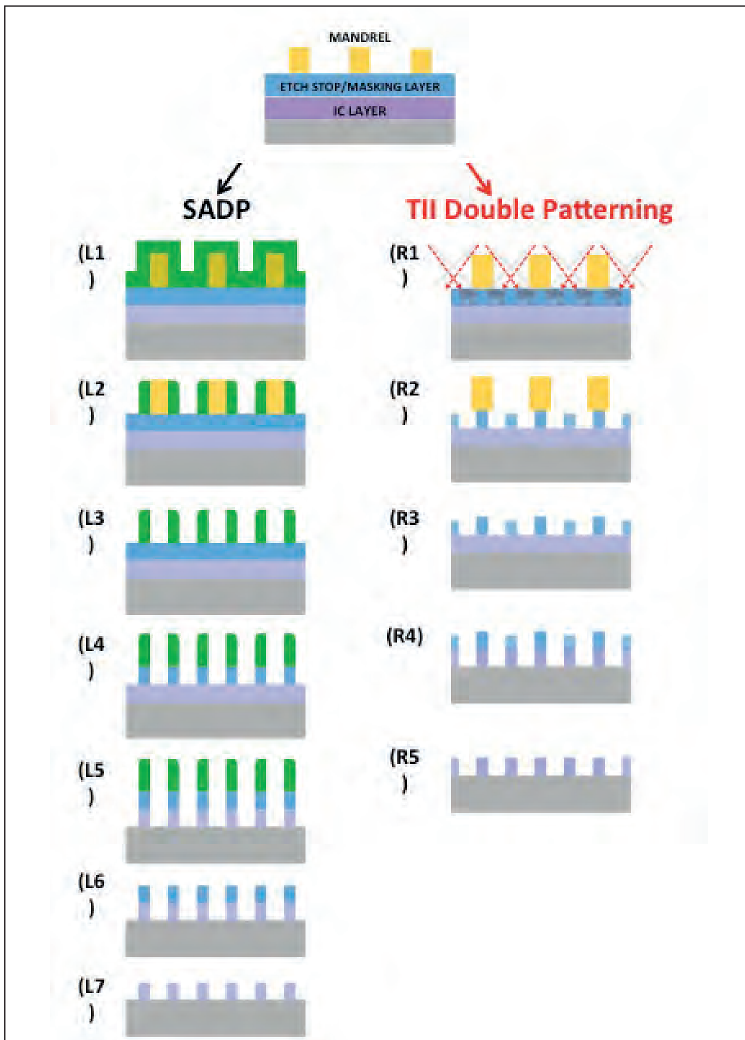


Figure 1. Schematic cross-sections illustrating the self-aligned double-patterning (SADP) and tilted ion implantation (TII) double-patterning methods. TII utilizes fewer process steps yet achieves high quality.

approaches to continue Moore's Law device evolution including extreme ultraviolet (EUV) lithography, which most believe will be required below the 7nm node.

But EUV adds still more costs and complexity to processes that are already the most complex ever seen in modern high volume manufacturing (HVM). According to ASML (Veldhoven, Netherlands,) each EUV process tool will cost upwards of (euro) 100 million. EUV photolithographic tools are about the size of a large transit bus; operational electricity is significantly more than what is used by industry-standard 193nm photolithography tools.

To address this growing challenge, Berkeley researchers proposed and demonstrated a double-patterning method that utilizes tilted ion implantation (TII) to achieve sub-lithographic features and pitches, down to below 10nm half-pitch [8-10]. The basic concepts are:

1. To use ion implantation to alter the etch rate of a thin masking layer;
2. To perform the implantation at a tilted angle since it has been demonstrated that this will achieve sub-lithographic implanted regions that are self-aligned to pre-existing photoresist or hard-mask features over the masking layer on the surface of the IC layer to be patterned.

The process sequences for SADP and TII double-patterning methods are compared side-by-side in Figure 1.

Both the SADP and TII techniques start with a patterned mandrel layer on top of an etch-stop layer or thin masking layer. SADP utilizes these steps as shown in Figure 1:
(L1) A relatively thin hard-mask layer is conformally deposited;
(L2) An anisotropic etch process is used to form hard-mask "spacers" along the sidewalls of the mandrel features;
(L3) The mandrel layer is selectively removed and the

Due to various significant issues that EUV has been facing it's not quite clear when EUV will become HVM ready. The primary driver for TII is to achieve a low-cost, sub-lithographic patterning technique with conventional CMOS processes that are already HVM ready. Compared to self-aligned double patterning, TII double patterning can reduce the processing cost and increase throughput by approximately 50% and 35%, respectively.

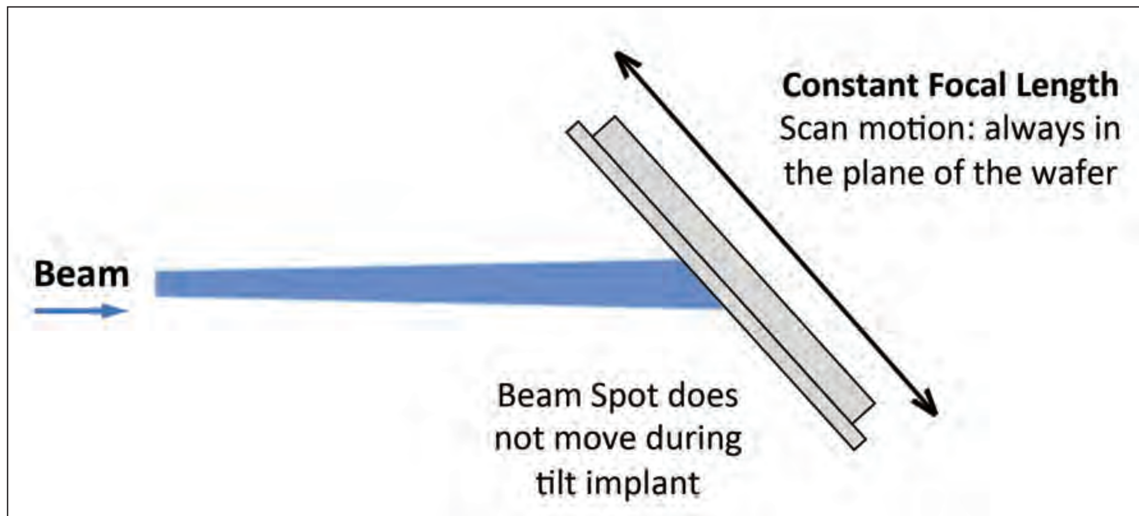


Figure 2. An illustration of tilted ion implantation (TII). An Axcelis Purion implanter was utilized to perform TII in the UC Berkeley study. Implantation is usually performed in a high-vacuum environment. Implanters can precisely control the tilt angle, ion acceleration energy and dose. TII is a contamination-free, highly precise IC manufacturing technique.

wafer is then cleaned;
(L4-L5) A multi-step etch process is used to transfer the hard-mask pattern to the IC layer;
(L6-L7) The spacers and the etch-stop layer are selectively removed.

TII double patterning utilizes these steps:
(R1) Ion implantation is performed at positive tilt angle as shown in Figure 2 and also at negative tilt angle to selectively damage regions of the mask layer, leaving the central region between the mandrel features undamaged due to the shadowing effect;
(R2) Portions of the damaged mask layer are etched away more rapidly than the undamaged portions;
(R3) The mandrel layer is selectively removed;
(R4) An etch process is used to transfer the pattern of the mask layer to the IC layer;
(R5) The mask layer is selectively removed.
The new TII double patterning approach essentially inserts an ion implantation process step between lithography and etch process steps, and can be used in conjunction with SADP to achieve quadruple patterning. It should be noted that ion implantation is a relatively simple process step as compared to deposition and etch process steps, so that the TII double patterning approach is more cost-effective.

Table I compares the number of steps and costs for TII double-patterning against those for SADP using arbitrary units (a.u.) to depict standard costs across

Table I. Cost Comparison of Double Patterning Approaches

Self-aligned Double Patterning			TII Double Patterning		
Process Steps		Cost	Process Steps		Cost
Process	Description	(a.u./wafer)	Process	Description	(a.u./wafer)
PECVD	Etch stop layer	1.5	LPCVD	Mask layer	2
CVD	Mandrel layer	2	CVD	Mandrel layer	2
Photolithography	Patterning	30	Photolithography	Patterning	30
Dry etch	Mandrel etch	10	Dry etch	Mandrel etch	10
ALD	Spacer deposition	3	Ion implantation	Double implants	1.7
Dry etch	Spacer etch	16	Wet etch	Selective mask etch	1
-	Mandrel pull	-	Dry etch	Mandrel removal	16
Wet clean	Clean	1	-	Pattern transfer	-
Dry etch	Pattern transfer	16	Wet etch	Mask removal	1
	Pattern transfer	-	-	-	-
Wet etch	Spacer removal	1	-	-	-
Wet etch	Etch stopper strip	1			
	Total:	**81.5**		**Total:**	**63.7**

each processing step. Clearly the TII approach requires fewer steps, which provides more than a 20% reduction in double-patterning costs.

It should be noted that the photoresist layer itself could be used as the mandrel layer in a TII double-patterning process [9] to achieve further cost savings. This is in contrast to SADP, for which the mandrel layer must be able to withstand high process temperature (greater than 150°C) associated with the hard-mask deposition process.

Summary

By eliminating the deposition, etch, and clean process steps associated with the mandrel layer, the cost of TII double-patterning can be approximately 50% the cost of utilizing SADP techniques. With TII patterning, the researchers experimentally demonstrated feature sizes of 9 nm, which indicates an approximate 20 nm pitch is achievable.

The Taiwan Semiconductor Manufacturing Company said in its latest 7 nm technology paper[11] presented at the 2016 IEEE International Electron Device Meeting (IEDM), that the smallest metal pitch is 40 nm. Hence, TII is expected to be a very intriguing new candidate for the 5nm technology node and beyond.

TII double-patterning presents a technological pathway for the semiconductor industry to extend the era of Moore's Law without additional costs or process steps. A number of semiconductor companies have expressed interest in developing the TII technique for high volume manufacturing (HVM) and the researchers are pursuing those queries.

The research team welcomes industry collaboration to further develop different aspects of TII techniques.

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Researcher Affiliations:
A) Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, 94720 USA
B) Axcelis Technologies, 108 Cherry Hill Drive, Beverly, Massachusetts 01915 USA

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Automating cleaning processes for quality and volume

Cleaning process repeatability is often critical to uniform product quality and can enable higher volume production throughput explains JST Manufacturing.

THE CONSISTENT PURITY of materials used to fabricate components of electronic devices can have a critical impact on their performance. For example, producing semiconductor-grade silicon used for electronic chips involves upstream cleaning of polysilicon chunks to a purity of has high as 11N, which translates to 99.999999999 percent. For photovoltaic applications such as solar cells, the silicon purity levels are not quite as high (5N) but critical to producing efficient photoeffect.

These and many other types of products used by the MEMs, biotech, LED panel and other micro-and nano-technologies that depend on uniformity that is provided by the repeatability of automated cleaning systems. The cleaning process usually incorporates cleaning agents such as chemicals, an appropriate rinse bath, and a method of drying the material.

Chemicals may also need to be heated and or product agitated to provide optimal cleaning results. An accurate means of measuring and dispensing cleaning agents safely and also safely transporting the products and materials being cleaned are required.

Manually operating a cleaning process calls for at least some worker intervention to precisely perform the above activities using a production system such as a wet processing bench. Because some cleaning processes require etching with harsh chemicals, worker safety is also a concern.

"Companies that choose to automate a cleaning process usually do so for one or both of two reasons", says Louise Bertagnolli, president of JST Manufacturing (Boise ID). JST designs and manufactures a variety of manual and automated cleaning equipment, including proprietary systems that include all of the features and transfer devices required for a complete turnkey cleaning process. "The first reason is repeatability, the ability to precisely repeat a cleaning process, including the exacting measurement and dispensing of the cleaning agents and rinsing solutions as well as providing the systems and tools necessary to clean and transport the items being cleaned from one bath to another," Bertagnolli explains. "This ensures that all materials or products will be uniform in purity, and a 'plus' benefit of worker safety is also provided."

The second reason some companies automate the cleaning process is to enable greater throughput for high-volume production. If the process takes place in a cleanroom, then the entire system including motors and robotics must be appropriate for that environment.

"There is also another class of semi-automatic equipment that enables automated process control, a built-in transfer system and other features on a relatively small footprint," Bertagnolli adds. "This type of system is an economical solution to lower-volume cleaning of such products as nuclear sensors, crystals, and polysilicon."

Ensuring successful automation

Customizing cleaning systems can provide high dividends, yet it is also a complicated undertaking and requires engineers and technicians who understand the individual needs of customers.

JST works with automation partners such as Bosch Rexroth (Charlotte, NC) to develop comprehensive wet-bench cleaning stations using linear motion and electric drive and control technology.

In a recent project the two firms worked together to create an automated system for cleaning silicon

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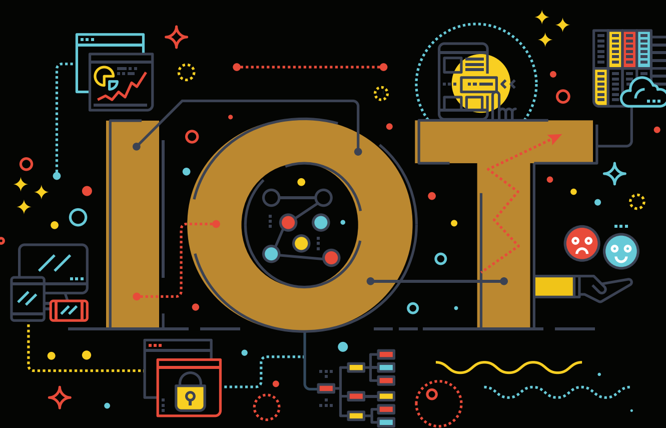

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chunks to the extreme purity of 11N to meet requirements for the manufacture of semiconductor chips. The project entailed building a cleaning line 138 ft. in length and incorporating multiple gantry robots.

"The throughput volume requirement for these chunks was four tons for every 22-hour shift," Bertagnolli explains, "so we had to develop a basket system to transport the material throughout the application. The process included etch-cleaning and vacuum drying that volume, which was difficult because the chucks all had a variety of uneven surfaces."

To provide for such a long cleaning system, JST engineered and built it in two units. In the 24-ft-long unit, baskets of chunks are manually loaded through an auto-door. Then two-axis robots cycle the baskets through five acid etch baths and two rinse baths arranged in a single row down the length of the second unit.

Throughout the silicon cleaning process, protecting the components against contamination and pitting is critical. Yet, one on the unusual aspects of this cleaning system is that the first unit of the line employs overhead gantry, or Cartesian robots, which are not often used in semiconductor process systems to avoid generating particles over the product.

However, after extensive particle testing in cleanroom conditions, the system proved to generate far fewer particles than the specifications allowed.
Proprietary seals keep the linear motion rolling strips clean and prevent the chemical etch from pitting the linear modules. The system incorporated other features to ensure the system met Class 10 cleanroom standards or better.

JST and Bosch Rexroth also partnered on a "sister" project that involved the cleaning of silicon "seed rods" that grow the polysilicon ingots from which the chucks are made.

The seed rod cleaning tool also utilizes a gantry robot to move the ingot-carrying cylindrical carriages through a sequence of etch baths. One of the keys to that solution is a custom designed fixture that rotates the rods in order to have them etched evenly.

"This rotational fixture also enables the rods to be cleaned to a very high purity," Bertagnolli notes. "We use a variety of rotational cleaning fixtures quite often, but also incorporate other designs and techniques as well – whatever will be most effective in getting the job done efficiently."

Bertagnolli advises that not every project is fully customized from the ground up. Quite often standard automation platforms can be customized according to length and height and number of baths. Cleaning process designers can consult with automation suppliers to determining where to put the transfer system and what automation modules will fit best in the space available,

The semi-automated system

Many processors with lower volume throughput requirements might consider semi-automated cleaning systems, which can provide the advantage of repeatability as well as other production advantages and added safety. This type of cleaning system is appropriate for MEMs, LEDs and silicon applications. It is compact, software controlled and usually easy to service.

JST manufactures a standard compact semi-automated wet bench called the Tigress, a two axis, front-to-back compact system that is used by smaller semiconductor companies.

A dual version of this semi-automatic system is also available. It is popular among semiconductor manufacturers who use it for cleaning, stripping, and etching of semiconductor substrates who use cleaning acids and bases or solids to remove photoresists.

"These semi-automated cleaning systems are ideal for companies that are cleaning MEMs and smaller semiconductors. They are a very cost-effective means of automation," Bertagnolli says.

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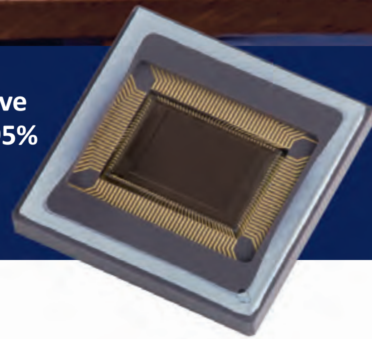

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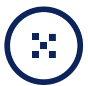

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Wafer defects can't hide from Park Systems

Atomic Force Microscopy (AFM) leader Park Systems has simplified 300mm silicon wafer defect review by automating the process of obtaining high-resolution 3D images, making it faster and simpler than ever before.

SEMICONDUCTOR MANUFACTURERS have options for defect review once inspection tools have identified potential flaws on bare silicon wafers. While conventional AFM provides data-rich 3D images, the process is slow compared to 2D, SEM-based techniques. A new AFM process developed by Park Systems changes that equation like none other.

Park Systems (Suwon, Korea and Santa Clara, California, USA) is one of the leading pioneers of atomic force microscopy (AFM) for semiconductor manufacturers and researchers. The company's founder (Sang-Il Park, PhD) led early efforts to commercialize the technology after being an integral part of AFM's development team at Stanford University in the 1980s.

Park Systems made the extreme, high-resolution 3D imagery of AFM commercially practical, going on to develop products and software for surface roughness measurement in hard disk media that became an industry standard (the Park HDM series product family). Park's AFMs are also 'non-contact' review tools, which eliminates the possibility of tool tips accidentally touching surfaces and possibly damaging wafers under review.

While quality, data-rich images have been a hallmark of Park's AFMs from the beginning, this extreme quality came at the price of speed and simplicity. The company subsequently automated AFM scanning for disk media and has now brought a similar approach to reviewing defects of interest (DOI) on silicon wafers up to 300mm. Its hardware and software also support extreme ultraviolet (EUV) reticle photo masks, a critical step in creating future 450mm silicon wafers.

Finding silicon wafer DOIs is challenging. All bare silicon wafers have a unique crystalline structure that is prone to small defects (Figure 1)that may be one nanometer or smaller. Manufacturers determine threshold sizes of interest along with shape and

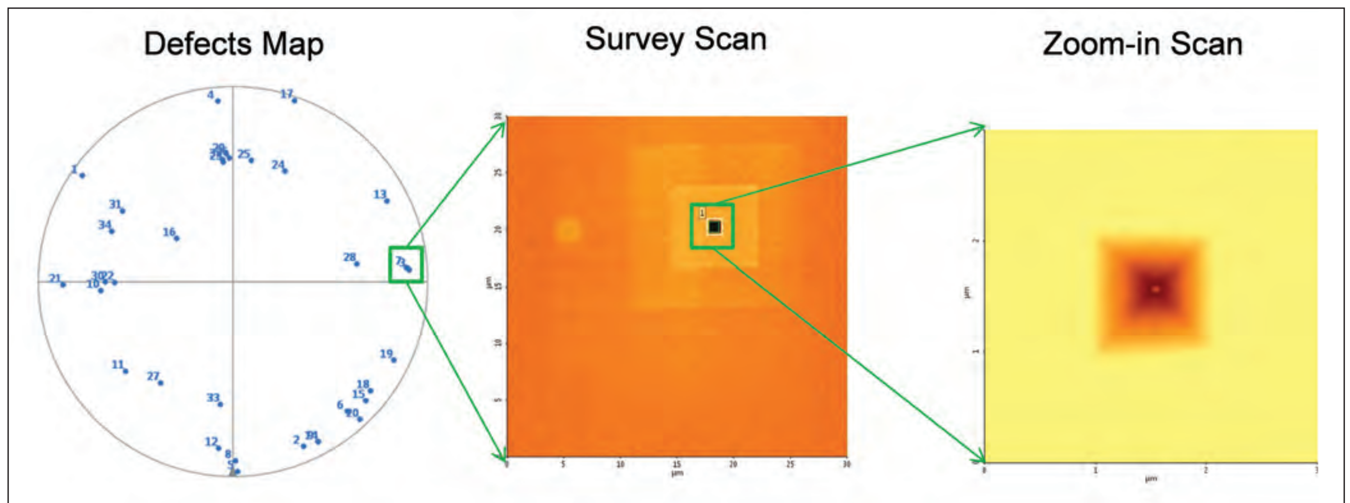

Figure 1: After coordinate mapping, ADR AFM will automatically perform a survey scan, zoom-in, processing, analysis and classification of each defect.

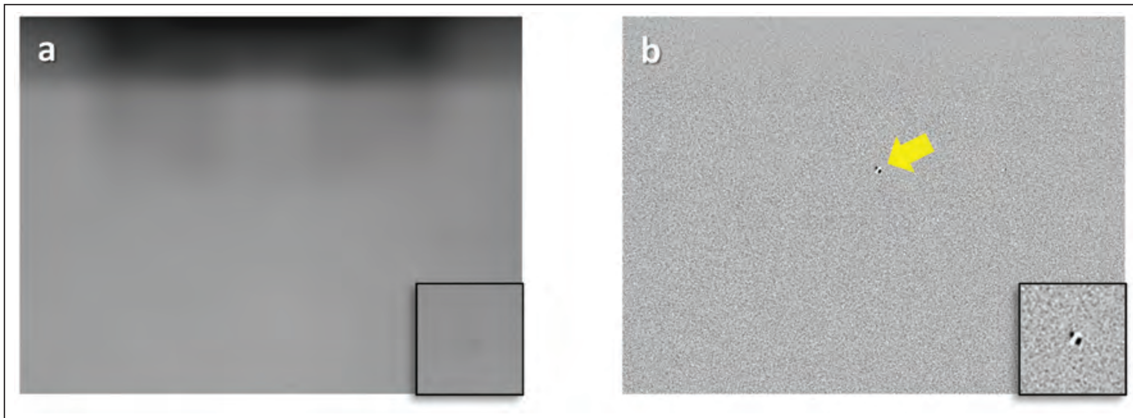

Figure 2: Images collected via (a) standard vs. (b) enhanced vision of a bare silicon wafer with one small defect. The insets show magnified views. The small defect is easily observable in enhanced vision.

depth characteristics that need attention. But while thresholds vary by manufacturer, it is clear that shrinking device geometries will impact whether defects once considered too tiny for concern could present problems for next-generation devices. There are a variety of laser light scattering techniques and process tools for inspecting wafers quickly, scanning hundreds or even thousands per hour. But inspection is just the beginning. A follow-up review by scanning electron microscope (SEM) or AFM takes inspection coordinates and zeros in on each location to image the defects. While SEM review is relatively quick, it cannot reveal much detail beyond a 2D image: a defect's 'X' and 'Y' dimensions. AFM goes much farther, creating X, Y and Z 3D images along with detailed topographic maps that further help identify and characterize an imaged DOI. AFM reveals defect details that SEM can routinely miss.

Park's AFM defect review is highly accurate, which is a key ingredient for success in an industry that measures in microns and nanometers. The accuracy of their AFMs is so great that the company holds a roughly 90 percent share of the market for hard disk drive defect review systems.

"Whether the defect is on a silicon wafer or the surface of hard drive media, the key is how accurately the review device locates it and delivers the information needed for proper defect classification. SEM may give

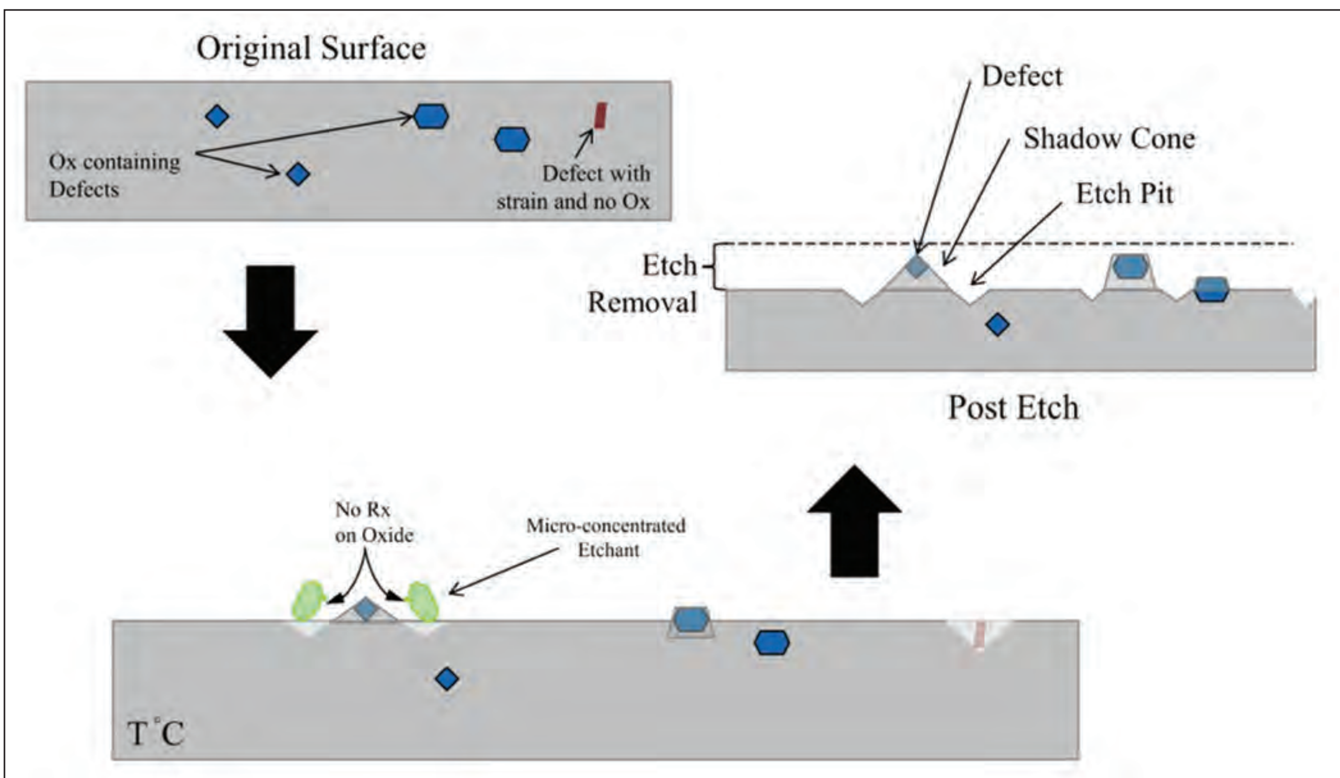

Figure 3: Schematic of the process used to decorate crystal imperfections for defect inspection.

#	SEM	AFM	#	SEM	AFM	#	SEM	AFM	#	SEM	AFM	#	SEM	AFM
1			8			15			22	N/A		29	N/A	
2			9			16			23	N/A		30	N/A	
3			10			17			24	N/A		31	N/A	
4			11			18			25	N/A		32	N/A	
5			12			19			26	N/A		33	N/A	
6			13			20			27	N/A		34	N/A	
7			14			21			28	N/A				

Figure 4: Defect review results with ADR AFM vs. SEM are shown. ADR AFM was able to locate and image all defects; SEM did not find defects 22 to 34. AFM and SEM images are rotated 180 degrees with respect to each other.

a quick image, but it lacks the information that can be provided by AFM (see figure 4).

"As a reference tool, AFM is the 'go-to' technology. Other AFMs can be a challenge to operate, so Park Systems addresses the problem with ADR: automatic defect review. We automated defect review and simplified it, so any technician can start the review process, and then simply walk away to do other tasks while the ADR AFM is operating," said Ardavan Zandiatashbar, PhD, Park's senior applications scientist.

While different manufacturers have varying approaches to how they handle silicon wafer defects, all likely agree that better data about a particular defect determines whether it is serious enough to affect lithographic processing, or whether defects are so great in number and size that a wafer should be rejected outright.

"We started with hard drive media defect review. Manufacturers needed to know the source of defects for failure analysis purposes. While SEM can give a quick image, its image can't easily tell you if a defect is a pit or a bump or how tall or how deep it is. This is where AFM comes in; it helps you to identify and classify defects accurately and completely. We do what others cannot do," Zandiatashbar said.

Wafer defects in Park's study typically fall into eight basic categories—additional categories in different wafer surface reviews are possible. Some defects can't be classified at the inspection stage and may not fit into a typical category even after AFM review. But through AFM, the manufacturer will definitely know a defect's size and depth; they can apply their own standards to determine what actions should be taken.

"Many manufacturers want to use AFM routinely, but locating the defects and linking the AFM to inspection tools were critical issues previously. Results from conventional AFMs depend on the skill of the operator. We eliminated those issues by automating the process. Now, instead of reviewing just a few defects per day through laborious efforts and changing

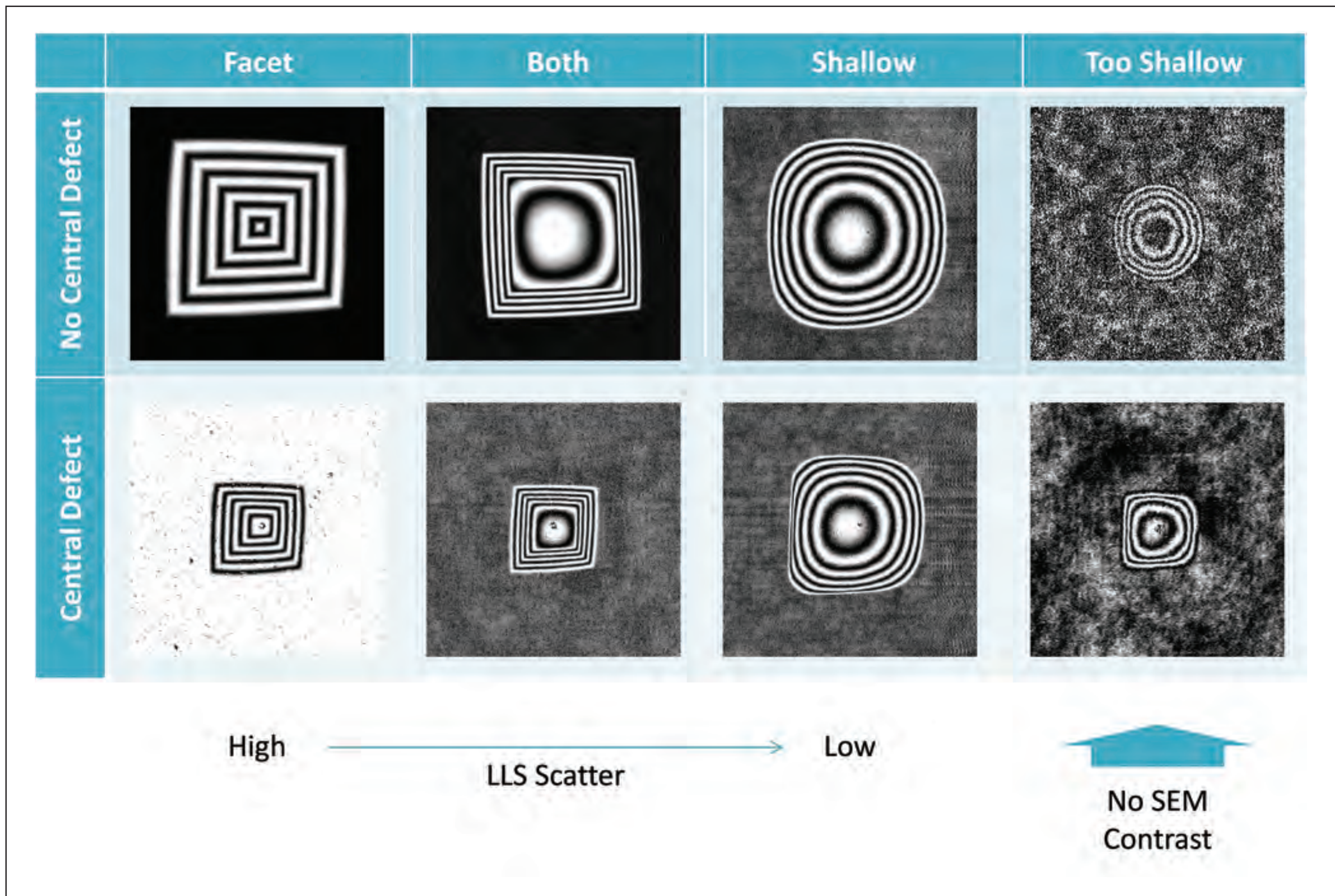

Figure 5: Defect classification based on the AFM data.

numerous tool tips, Park's ADR AFM can image and fully characterize between four and 10 defects per hour. A technician can start ADR and let it run 24/7. Manual AFM review proceeds only as quickly as a skilled operator can function," he added. "Park's ADR AFM is a turn-key solution."

In addition to automating the review process, Park's non-contact approach to AFM does not alter the wafer's surface in any way, meaning every wafer reviewed can go onto further processing as needed. SEM-based review processes have another issue beyond quality of data. Their electron beams also have the potential to 'burn' scan areas (see figure 6). This effect is typically more critical for photo-resist layers, but any disruption of a wafer's surface area can affect yield or other important factors.

The differences in results obtained using Park Systems ADR AFM compared to SEM-based results are dramatic. In a test conducted by Park, a wafer containing surface defects was reviewed using both SEM and AFM-based techniques. The ADR AFM utilized was from Park's NX-WAFER family of products. 34 defects identified at the inspection stage were candidates for review. The first 21 defects were imaged by SEM, which delivered aerial, 2D views without sufficient information about the depth or out-of-plane dimensions. The remaining 13 defects were not found by SEM despite identification during a laser light scattering (LLS) inspection (see figure 4).

Park's ADR AFM was able to find all 34 defects. The SEM had found defects down to a certain size threshold; those imaged by ADR AFM were typically

The differences in results obtained using Park Systems ADR AFM compared to SEM-based results are dramatic. In a test conducted by Park, a wafer containing surface defects was reviewed using both SEM and AFM-based techniques. The ADR AFM utilized was from Park's NX-WAFER family of products. 34 defects identified at the inspection stage were candidates for review.

Figure 6: Comparison of data collected by SEM vs. ADR AFM. SEM shows a 2D, aerial view, while ADR AFM includes 3D data, thereby enabling a line profile, 3D construct and contoured colour scale.

smaller or shallower than defects that the SEM could identify. The SEM also had issues identifying defects that had less edge sharpness, whereas the AFM in its automated scanning mode found everything (see figure 6) .

"From the customer perspective, locating the defects of interest during the review process and determining size and depth can be critical. While SEM-based techniques can locate larger defects, it does not find them all and in fact missed 13 of 34 in this case. The lack of 3D information and SEM's inability to image the shallow and small defects matters to manufacturers. With Park's automatic defect review manufactures can have high quality 3D data of DOIs more quickly using a turn-key solution that any technician can operate," said Zandiatashbar. Automatic defect review from Park Systems maximizes productivity by up to 1,000 percent as reported by customers. But what satisfies customers most is the unprecedented level of accuracy including 3D imagery and detailed topographic information of even the smallest defects. With ever-shrinking semiconductor device geometries reaching beyond 14nm, defects critically impact microelectronic device performance. Park's approach to automating 3D imaging is revolutionary because it makes the benefits of AFM practical for leading device manufacturers and researchers pushing future product generation boundaries.

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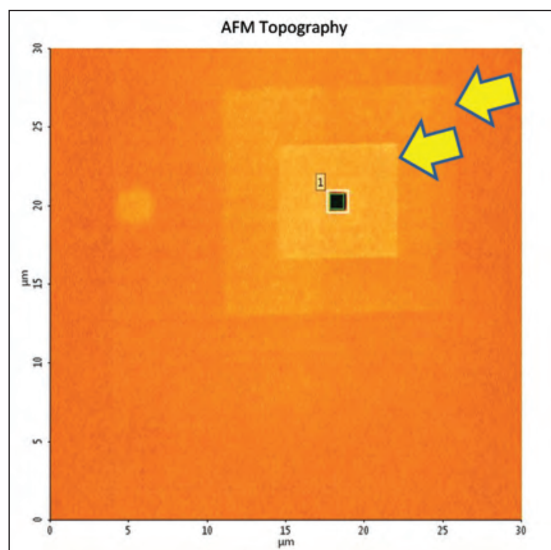

Figure 7: AFM image of a facet defect with several SEM burn-marks is shown; burns are marked by arrows.

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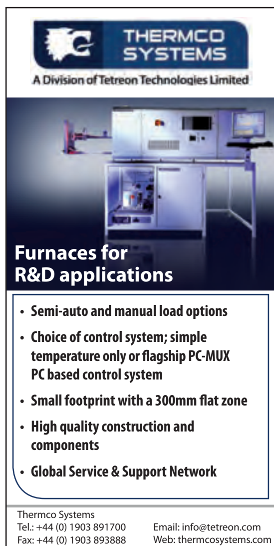

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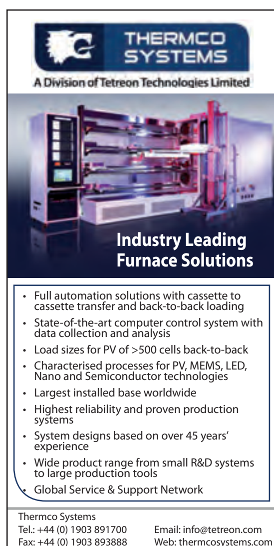

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