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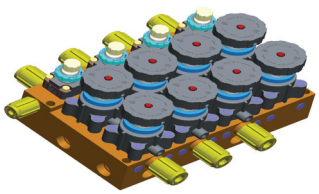
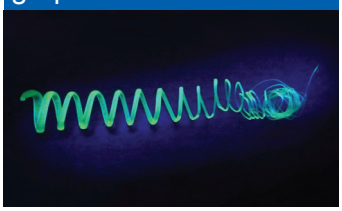
Designing lab equipment

Optimizing cost of ownership



New wafer dicing approach

An alternative to graphene



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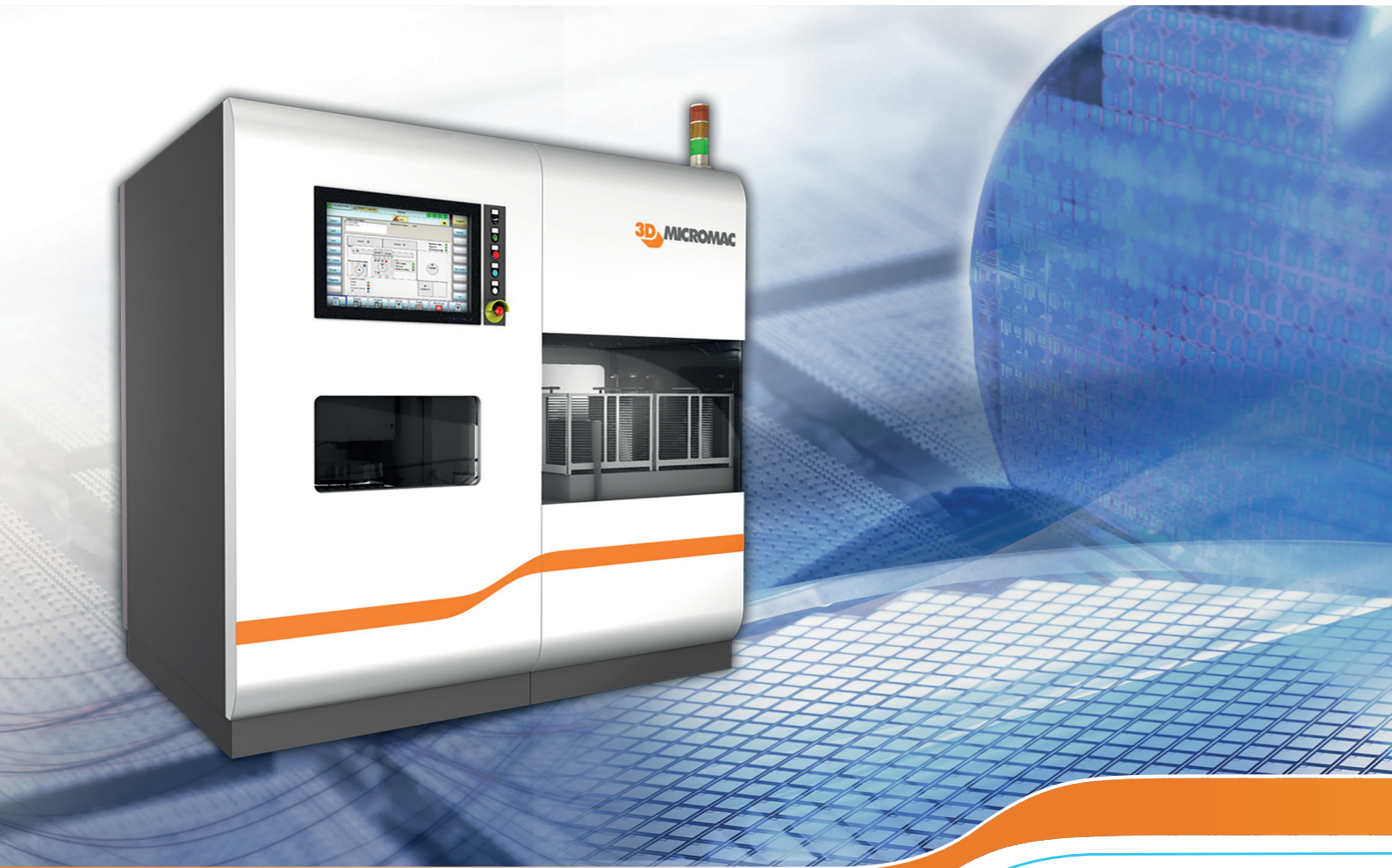

3D MICROMAC

editor's view

By Mark Andrews, Technical Editor

The highs and lows of a rebounding market

WHILE semiconductor trade groups celebrate surging 1Q sales the industry can't seem to avoid looking for some gray around the edges of a sunny day. Major semiconductor trade associations have had little but praise for 2017 as 1Q figures pointed to surging sales – good news after two years of backsliding.

The Semiconductor Industry Association (SIA) was among the first to announce notably higher revenues in 1Q 2017, rising to over 18 percent growth compared to 2016; 1Q marked the first time since 2010 that revenue grew so strongly.

And there was more good news. The SEMI organization noted that North American equipment manufacturers posted $2.03 billion in March billings, 2.6 percent higher than final February 2017 figures, and a whopping 69.2 percent higher than in March last year. It was the strongest start in 16 years! Trade group optimism seemed contagious. Intel announced that it will increase Capex spending by 20 percent to $12 billion, a level it expects will continue into 2018 as it ramps its 3D NAND and 3DXP memory programs. While Intel was bullish, Taiwan Semiconductor Manufacturing Company (TSMC) took a slightly more guarded view, forecasting an inventory correction in smartphones to continue through 2017's first half. But TSMC also increased its growth forecast to 7 percent thanks to memory demand, adding that sales may grow even more when it ramps 10 nm production later this year.

Elsewhere across industry, Apple and Qualcomm were trading claims and criticisms over royalty payments, leading some analysts to speculate that clouds were gathering. Even as Apple reported earnings of nearly (USD) $53 billion – 5 percent higher

than 2016 – some analysts pooh-poohed those results, saying the company can't recoup sales lost in China to homegrown competitors or that the 10th anniversary iPhone might grow lukewarm.

So where is 2017 headed? It is thrilling to see global chip sales grow 18 percent while equipment makers also celebrate. This points to a trend, not a fluke. Apple and Qualcomm will bury their hatchets since neither wants to kill the golden goose. Issues that could derail continuing key segment growth like IoT security and spectrum concerns or consumer wariness are fading as more companies deliver solutions in this emerging market and elsewhere. We can all can think of geopolitical upsets that could derail 2017's rally. But for now, an overwhelming number of analysts see 1Q reports as celebration worthy. Let's enjoy the sunshine and concentrate on delivering quality products that consumers cannot resist. That is the best way to ensure everyone's future.

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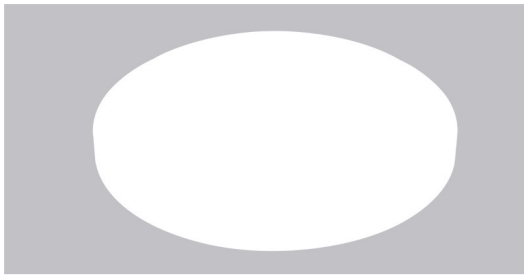

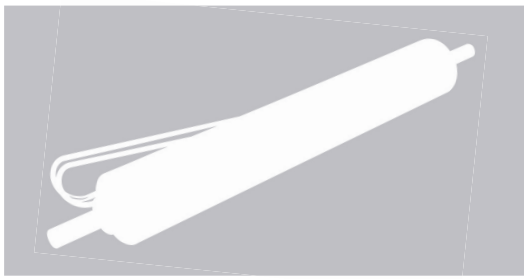

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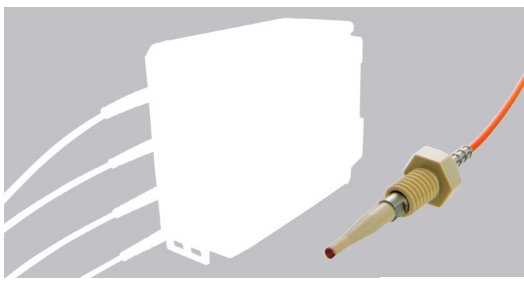

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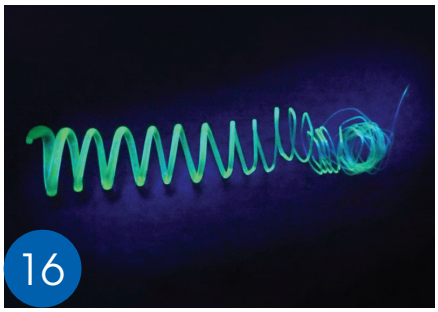
COVER STORY



Intel debuts 10 nm and 22 nm processes

INTEL used its Manufacturing Day event in San Francisco to unveil new 10 nm chips scheduled to enter production in the latter half of 2017. Intel's new processors will pack 100.8 million transistors into one square millimetre, nearly double the density of rival chip makers' 10 nm devices, Intel said.

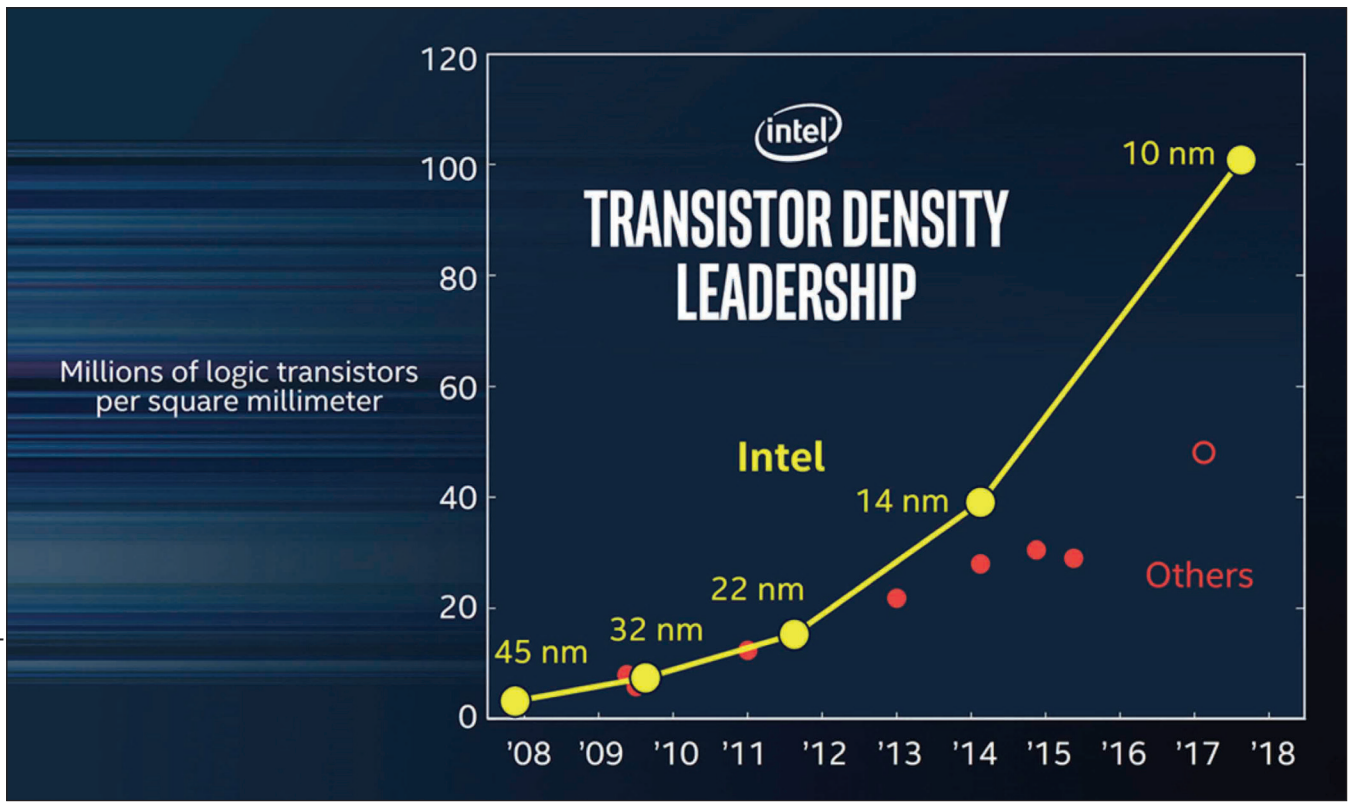
In making the 10nm announcement, Intel quelled speculation over whether its latest chips would enter production this year. Intel's road map calls for its newest devices to enter the market almost three years after it debuted its previous generation 14 nm chips.

Intel also announced it would use a different metric to gauge performance of next-generation devices, challenging peer manufacturers to utilize the same guide when discussing performance of their own semiconductor devices. The Intel metric averages density of a small and large logic cell; its 10nm chips utilize a two-input NAND cell with two active gates and a scan 'flip-flop' cell with as many as 25 active gates.

Intel representatives said their latest design will have more than 100 million transistors per square millimetre, while it believes rivals Samsung and TSMC pack about half that many transistors into the same space. Intel senior fellow and director of process architecture Mark Bohr said he believed Intel competitors previously used a similar metric in describing the capabilities of their own chips, but discontinued doing so when it appeared that performance was not increasing as fast as it had previously.

Intel's new 10 nm chips (Cannonlake devices) and subsequent generations will follow a three-year cadence. While the company previously had 18- to 24-month gaps between generations, the challenges of developing greater densities while keeping costs low and increasing performance has forced chip makers to depend on multi-pattern lithography and other enhancements that take more time than shrinking device features alone, which was the common pathway to creating faster, denser transistor cores at previous nodes. Intel forecast another three-year gap before its next new node is released; it plans to introduce performance enhancements for 10nm devices as interim steps between nodes, referring to those generations as 10+ and 10++. Intel's new 10nm chip utilises the tightest gate and metal pitches found in semiconductor manufacturing, it said, adding that this new generation marks industry's first high volume use of self-aligned quad patterning. To compensate for the rising costs of more lithographic steps, Intel said it utilizes a contact over active gate (COAG) design that helps deliver 10 percent greater transistor density. The use of a single dummy gate in its architecture rather than two provides additional scaling advantages that help reduce costs, Intel said.

The company also announced its 22 nm node FinFET low-power foundry process designed to compete for business will fully depleted silicon-on-insulator (FD-SOI) processes, such as those offered by com petitors including Globalfoundries. Intel expects to ramp its 22 nm FFL process before the end of 2017; the new devices target similar types of applications that FD-SOI now supports including mobile end user products and Internet of Things (IoT) devices. Process design kits (PDKs) are in pre-release with full 1.0 versions expected by 1 ISSUE II 2017.



Credit: Intel Corporation

Samsung to become largest semi supplier in 2Q17

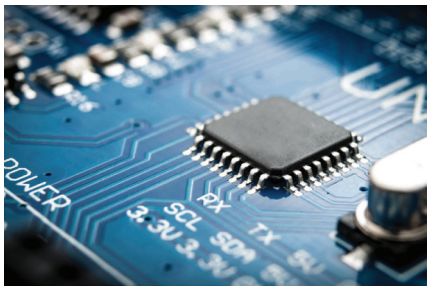
AFTER nearly a quarter of a century, the semiconductor industry could see a new #1 supplier in 2Q17. If memory market prices continue to hold or increase through 2Q17 and the balance of this year, Samsung could charge into the top spot and displace Intel, which has held the #1 ranking since 1993.

Using the mid-range sales guidance set by Intel for 2Q17, and a modest, yet typical, 2Q sales increase of 7.5 percent for Samsung, the South Korean supplier would unseat Intel as the world's leading semiconductor supplier in 2Q17.

If achieved, this would mark a milestone achievement not only for Samsung, specifically, but for all other competing semiconductor producers who have tried for years to supplant Intel as the world's largest supplier.

In 1Q16, Intel's sales were 40 percent greater than Samsung's, but in just over a year's time, that lead may be erased and Intel may find itself trailing in quarterly sales.

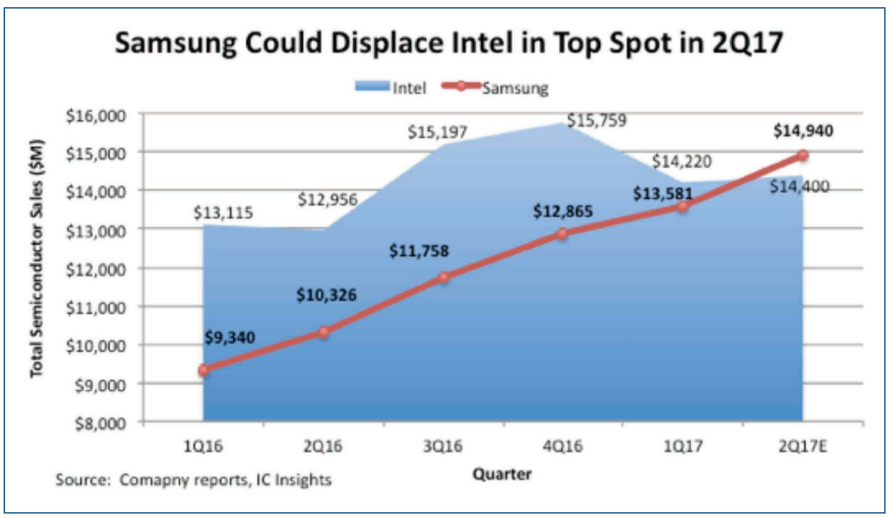
Samsung's big increase in sales has been driven by an amazing rise in DRAM and NAND flash average selling prices. IC Insights expects that the tremendous gains in DRAM and NAND flash pricing experienced through 2016 and into the first quarter of 2017 will begin to cool



in the second half of the year, but there remains solid upside potential to IC Insights' current forecast of 39 percent growth for the 2017 DRAM market and 25 percent growth in the NAND flash market.

Intel has been locked in as the world's top semiconductor manufacturer since 1993 when it introduced its x486 processor and soon thereafter, its revolutionary Pentium processor, which sent sales of personal computers soaring to new heights. Over the past 24 years, some companies have narrowed the sales gap between themselves and Intel, but never have they surpassed the MPU giant.

If memory prices don't tank in the second half of this year, it's quite possible that Samsung could displace Intel in full-year semiconductor sales results as well. Presently, both companies are headed for about $60.0 billion in 2017 semiconductor sales.



Ultratech revenue up 27 percent

ULTRATECH, a supplier of lithography, laser-processing and inspection systems for semiconductor devices and high-brightness LEDs, has announced unaudited results for the three-month period ended April 1, 2017.

For the first quarter of fiscal 2017, Ultratech net sales totaled $57.4 million, or 27 percent higher than the $45.2 million reported in the year ago quarter. This level of net sales is the highest achieved by Ultratech over the past four years, and it follows the announcement in February that process equipment company Veeco Instruments was intending to acquire Ultratech for $815 million.

On a GAAP basis, Ultratech's net income for the first quarter of fiscal 2017 was $3.0 million, or $0.11 per diluted share, as compared to net loss of $1.2 million, or $(0.04) per share, for the same quarter last year. On a non-GAAP basis, Ultratech's net income for the first quarter of fiscal 2017 was $9.7 million, or $0.35 per share, as compared to net income of $2.7 million, or $0.10 per share, for the same quarter last year.

Arthur W. Zafiropoulo, chairman and CEO, stated: "Our first quarter results illustrate our market leading technology position, combined with the strong positive leverage in our business model. Sales grew by 27 percent versus the prior year, resulting in a 250 percent increase in non-GAAP earnings per share. "Robust demand for our laser spike annealing, and advanced packaging product lines drove strong bookings momentum, generating a book-to-bill ratio of more than 1 to 1. Ultratech's portfolio of advanced products continue to meet the existing and future needs of the various industries that we serve."

NXP acquires Freescale

STRONG GROWTH in MCUs for IoT applications and suppliers jockeying for market share in this IC segment have resulted in several major acquisitions that changed the pecking order of MCU leaders in 2016, per data released in IC Insights' April Update to The McClean Report, which was released earlier this month. Figure 1 ranks the largest MCU suppliers in 2016 by dollar-sales volume.

Among the top MCU suppliers shown, NXP, Microchip, and Cypress Semiconductor moved up in the sales ranking during 2016 with strong increases in revenues, which were driven by acquisitions of IC companies that sold microcontrollers. Meanwhile, those suppliers not making significant acquisitions in microcontrollers posted low-single digit percentage increases or declines in MCU sales in 2016.

Although overall growth in microcontrollers has wobbled and stalled in the past couple years, MCUs remain at the epicentre of tremendous growth in the Internet of Things, automotive, robotics, embedded applications and other emerging systems. Major MCU suppliers have been improving their portfolios to address many of these key markets. Part of that improvement process has included merging and acquiring competitors to gain a quick foothold into these developing markets. In 2016, NXP in the Netherlands overtook Renesas Electronics in Japan as the world's largest microcontroller supplier with MCU revenues climbing 116 percent following its $11.6 billion purchase of U.S.-based Freescale Semiconductor in December 2015. Prior to its acquisition, Freescale was ranked second in MCUs and was catching up with Renesas in microcontroller sales with only $210 million separating the two companies in 2015 versus about a $1 billion gap in 2014. Renesas suffered a 19 percent drop in MCU dollar sales in 2015 (largely due to the weak yen exchange rate in that year but also because of the continued fallout from Japan's troubled economy).

In 2016, Renesas' fall in MCU sales eased, dropping 4 percent to nearly $2.5 billion, or about 16 percent of the total microcontroller market. In 2011, Renesas' MCU marketshare was 33 percent of worldwide microcontroller sales.

The Freescale acquisition moved NXP from sixth in the 2015 MCU ranking to the top spot in 2016 with a market share of 19 percent ($2.9 billion). About three-quarters of NXP's 2015 microcontroller sales were 8-bit and 16-bit MCUs used in smartcards. After Freescale's business was merged into NXP, smartcard MCUs accounted for a little over one-quarter of the company's total microcontroller sales in 2016. MCUs developed and introduced by Freescale are aimed at a wide range of embedded control applications, including significant amounts in automotive systems. NXP and Freescale both have developed extensive 32-bit MCUs with Cortex-M CPU design cores licensed from ARM in the U.K.

U.S.-based Microchip Technology climbed from fifth in the 2015 MCU ranking to third in 2016 with sales increasing 50 percent to $2.0 billion following its $3.4 billion acquisition of Atmel in 2Q16. U.S.-based Atmel was ranked ninth in MCU sales in 2015 ($808 million). Prior to buying Atmel, Microchip had been the only major MCU supplier not licensing ARM CPU technology. For about 10-years, Microchip has developed and sold 32-bit MCUs, based on a RISC-processor architecture developed by MIPS Technologies (which is now owned by Imagination Technology in the U.K., a rival of ARM).

Six months after completing the Atmel acquisition, Microchip said it would expand both its MIPS-based PIC32 MCU product line and Atmel's ARM-based SAM series. Microchip has promised to "remain core agnostic, fitting the best solution with the right customer and for the right application."

Meanwhile, Cypress in Silicon Valley moved into eighth place in the MCU ranking with sales increasing 15 percent in 2016 to about $622 million. Cypress boosted its presence in MCUs when it acquired Spansion for about $5.0 billion in stock in March 2015. Originally spun out of Advanced Micro Devices as a NOR flash memory supplier, Spansion had purchased Fujitsu Semiconductor's Microcontroller and Analog Business in 2013 for $110 million as part of its efforts to expand beyond nonvolatile storage ICs. The biggest decline in the MCU leader list was posted by Samsung, which saw its sales drop 14 percent in 2016, primarily because of weakness in the smartcard microcontroller market. Samsung sells MCUs to OEMs but also serves in-house needs for its own brands of consumer electronics, computers, and smartphones.

Nikon initiates legal actions against ASML and Carl Zeiss

NIKON CORPORATION ("Nikon") has initiated a series of legal actions in the Netherlands, Germany and Japan intended to halt infringement of its intellectual property by Dutch semiconductor lithography system manufacturer ASML Holding N.V. and its related companies ("ASML"), and by ASML's optical component supplier Carl Zeiss SMT GmbH ("Zeiss").

The basis of Nikon's claim is that ASML and Zeiss employ Nikon's patented technology in ASML's lithography systems, which are used globally to manufacture semiconductors, without Nikon's permission, thereby infringing Nikon's patents.

Nikon has met with ASML and Zeiss with the aim of reaching a resolution of these issues, but those efforts, guided by a highly experienced mediator, have failed to produce a settlement. The continued unauthorized use of Nikon's patented technology by ASML and Zeiss has given Nikon no alternative but to enforce its legal rights in the courts of law.

Nikon has initiated eleven patent infringement cases against ASML in the District Court of The Hague in the Netherlands and is filing patent infringement cases against ASML in Tokyo District Court in Japan and against Zeiss in Mannheim, Germany where the company manufactures optical components used in ASML's immersion lithography systems that are the subjects of these suits.

Per ASML's publicly reported data for 2016, 76.3 percent of its sales in the year ended December 2016, or approximately 3.5 billion, was derived from immersion lithography systems sales. Nikon believes these systems use Nikon's patented technology. The complaints seek injunctions barring ASML's and Zeiss's sale and distribution of these systems, as well as damages.

Immersion lithography technology, which Nikon pioneered in the early 2000s, has become essential in fabricating the state-of-the-art semiconductors used in smartphones, memory chips and countless other products. Today, ASML and Nikon are the only companies in the world that make and sell immersion lithography systems.

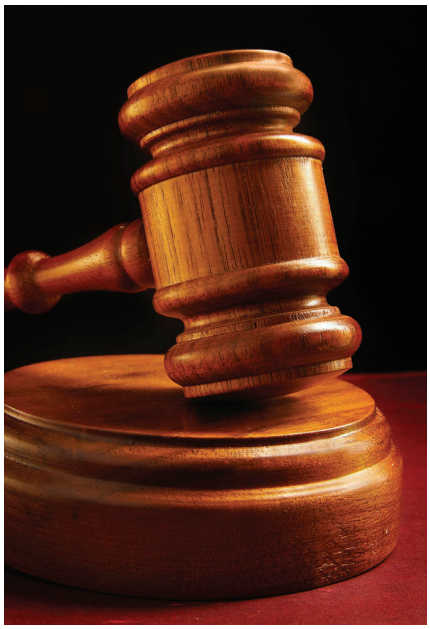
"Through substantial and sustained investment in R&D, Nikon has developed advanced lithography technologies, including immersion lithography technology, that have revolutionized the semiconductor industry," said Kazuo Ushida, President, Representative Director of Nikon. "Semiconductors are core components of the electronic devices on which consumers, companies and the global economy rely. We are proud of the role that our technology has played in advancing the global information society. "

"We firmly believe that ASML's unauthorized use of Nikon patents on our most advanced technologies, including immersion lithography technology, has enabled ASML to expand its lithography business. Respect for intellectual property is fundamental to fair and healthy competition, and is essential to promoting innovations that provide society with the most advanced products and services. That is why we have decided to commence this litigation."

Nikon has previously had to bring legal actions against ASML and Zeiss in relation to unauthorized use of its patented technology. Previous cases in the United States were settled on terms favourable to Nikon. Now, thirteen years later, Nikon intends again to pursue remedies vigorously and fully permitted by applicable law, including injunctive relief to stop ASML and Zeiss from using Nikon's intellectual property without authorization, as well as damages.

Background of Nikon/ASML/Zeiss dispute

In the 1990s, Nikon was the world's leading maker of lithography systems for semiconductor fabrication. In December 2001, Nikon filed lawsuits in the United States accusing ASML of using technology without authorization that Nikon had developed and patented. In 2004, a comprehensive settlement was reached, and Nikon entered cross-license agreements with ASML and Zeiss.



Under the agreements, older patents were licensed permanently and some patents with a later filing date were licensed for a limited period until December 31, 2009. The parties agreed in the license agreements not to sue each other for patent infringement during a non-assertion period from Jan 1, 2010 to Dec 31, 2014.

In accordance with the cross-license agreements, however, Nikon can seek damages now for ASML and Zeiss's infringement during the non-assertion period. During the non-assertion period ASML introduced products that Nikon is asserting in the litigation infringe its patents. Since the license under the cross-license agreement terminated on December 31, 2009, Nikon has attempted to negotiate with ASML and Zeiss to reach agreement on a new license agreement.

However, ASML and Zeiss have not been willing to accept terms reflecting the value of Nikon's patented technology. Nikon believes that both ASML and Zeiss are continuing their use of Nikon's patented technology without authorization, so Nikon has initiated new lawsuits against them to enforce its patents.

Austrian Innovation Award given to EV Group

From left to right, Dr. Werner Thallner, Erich Thallner, Paul Lindner, Hermann Waltl and Dr. Reinhold Mitterlehner. Source: Austrian Federal Ministry for Science, Research and Economy/ APA-Fotoservice/Schedl.

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, today announced it has received the 2017 Austrian Innovation Award, known as the "Staatspreis Innovation 2017," for the development of EVG's groundbreaking SmartNIL nanoimprint lithography technology for micro- and nano-structuring of wafers and other substrates. The highest federal accolade for innovative companies in Austria was presented by Vice Chancellor and Federal Minister Dr. Reinhold Mitterlehner on March 28 at an awards ceremony at the Hall of Sciences in Vienna.

"Receiving the Staatspreis Innovation 2017 is a huge acknowledgement for us as well as confirmation of our Triple-i philosophy of invent-innovate-implement," said Erich Thallner, who founded EVG together with his wife Aya Maria in 1980 and serves as the company's president and executive board member today. "EVG's SmartNIL technology represents a milestone for our industry and proves the innovative strength of our company once more. The great effort of all teams involved in this product and process development, as well as the vision of our company and all of its employees to always be first in exploring next-generation applications, is the basis for our success."

EVG received the Austrian Innovation Award for the project "SmartNIL process and HERCULES NIL high-volume production system for nanoimprint lithography." The functional principle of electronic, micro-mechanical or optical components and products often relies on miniscule structures being applied to their base material or substrates. Current manufacturing processes are often complex or do not provide the required precision, especially in high-volume production. Nanoimprint lithography can meet these requirements while reducing manufacturing costs by transferring extremely small structures from a stamp to a polymer material.

Thanks to the SmartNIL technology, which was specifically developed for this, uniform contact between the substrate and the re-usable imprinting stamp can be achieved even with microscopically small (sub-100-nanometre) structures. Applications include optical and semiconductor fabrication, medical device manufacturing for DNA and protein analysis, diagnostics and drug discovery, as well as water quality screening.

In total, 485 companies competed for the 37th Austrian Innovation Awards, which were organized by the Austria Wirtschaftsservice GmbH (aws) on behalf of the Ministry of Science, Research and Economy. A jury of experts chose the winner based on its assessment of the nominated companies' products, processes or services, relevant entrepreneurial data as well as the innovation's impact on the market, environment and society.

Noel Technologies expands Silicon Valley wafer fab

NOEL TECHNOLOGIES, a specialty semiconductor foundry, has expanded its wafer-fabrication facility in Silicon Valley, California, by adding square footage and installing additional equipment that boost its production capacity by 25 percent.

With additions including an i-line lithography system with 0.35-micron resolution, a top-down CD scanning electron microscope (SEM) and more plasma-enhanced chemical vapor deposition (PECVD) tools, the 20-year-old company has increased its range of foundry services for customers in the semiconductor, MEMS, bio-medical device, sensor and LED markets.

"We perform many wafer-fabrication services integral to the development of the newest micro- and nanoelectronic products," said Leon Pearce, founder and chief technical officer of Noel Technologies. "As a manufacturing partner located right in Silicon Valley, we offer chip designers a local foundry solution to shorten their R&D cycles and reduce their time to production."

Noel Technologies specialises in helping chip designers that work with advanced non-CMOS materials and non-standard process flows. The company has decades of experience and proven capabilities in developing novel process flows involving III-V compound materials, gold, silver, transparent conductive oxides and emerging materials.

All front-end wafer processing is performed in-house under the supervision of Noel Technologies' process engineering team, eliminating the need for customers to coordinate work flows among multiple suppliers. The foundry's extensive process capabilities enable short manufacturing lead times while improving device yield and performance.

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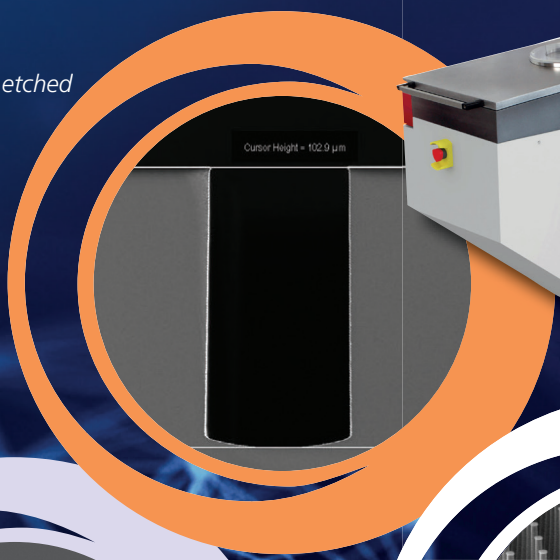
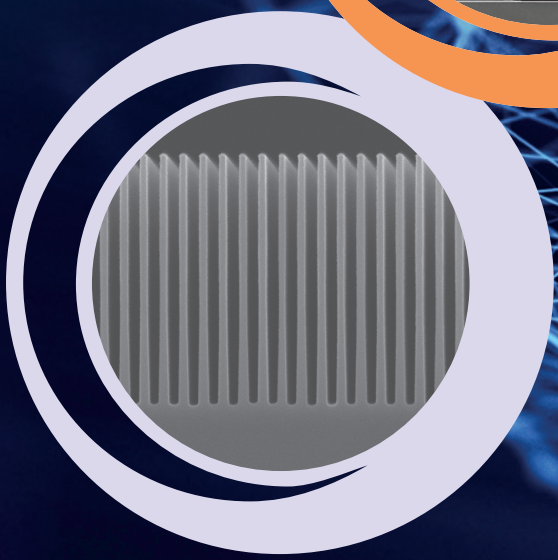
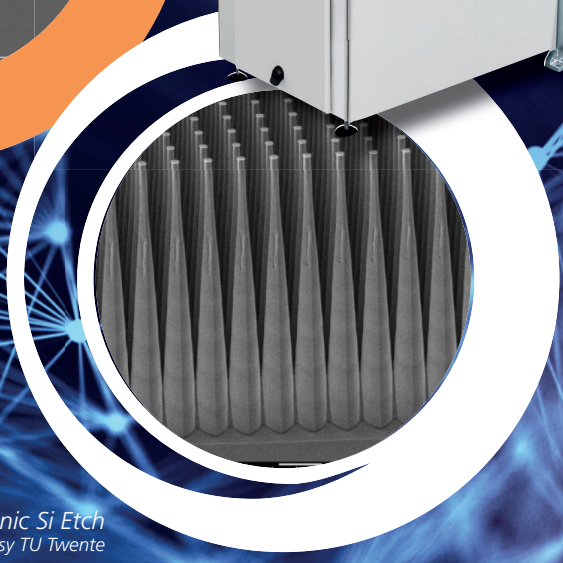




110nm wide trench, smooth sidewall 2.5µm depth (23:1 AR)



Cryogenic Si Etch
Courtesy TU Twente

www.oxford-instruments.com/Estrelas

Automated systems increase wafer lapping and polishing productivity

Logitech's new automated lapping and polishing systems for almost all substrate materials dramatically increases wafer end productivity by up to 40 percent.

THE LAPPING and polishing of wafers used to manufacture semiconductors and optical devices is a time consuming task that can risk damage to expensive custom wafers worth in excess of (USD) $5,000 each if things do not go to plan. Logitech has substantially automated the process, speeding productivity and increasing repeatability by approximately 40 percent compared to non-automated techniques.

In wafer end fabrication, lapping and polishing processes have become more predictable, but there is often the need for a significant level of user expertise, guesswork and development time in order to optimise surface finish and repeatability. This can hamper the development of new technologies, especially as a process that is optimised at the pilot stage will often need to be revisited when transitioned to full production.

The path to better process control lies within Preston's Law (see Figure 1), which provides a framework for predicting the amount of material that will be removed in a given time by lapping and polishing processes. By controlling variables using automated precision lapping and polishing systems with high levels of user control, operator variability can be minimised while process accuracy and greater repeatability can be achieved.

The Preston's Law equation states that the material removal rate (MRR) is proportional to the product of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the processing pressure/load/down-force and plate velocity. In the chemical mechanical polishing (CMP) process, polishing rates and overall accuracy are affected not only by the flow of the slurry and the characteristics of the polishing plate, but also by the mechanical action between the wafer and the plate, chemical reactions arising from slurry component molecules, and the interactions between these variables. Preston's Law can be used to accurately predict the amount of material removed from a sample and confirm stability in the process. High degrees of process stability are possible by using a stable/accurate/repeatable processing platform such as the Logitech Akribis-air, which handles up to 150mm wafers, or the PM6 Precision Lapping & Polishing system designed for wafer samples up to 100mm.

Meeting demanding wafer requirements using manual lapping and polishing tools is hard to achieve with silicon, III-V or other very hard semiconductor wafer materials because of the high level of operator skill needed to manually stage and control such operations. Setup is a time consuming process that is not conducive to the high productivity that is demanded by semiconductor research and production facilities. Cost reduction in device production is driven by volume and yield. Automated systems designed to eliminate manual steps will ultimately increase productivity in wafer fabrication processes.

Logitech's Mark Kennedy, Head of Process Technology Development, frequently works with customers in the field who appreciate the precision of an automated systematic approach to wafer lapping and polishing. "The customer used our new Logitech PM6 and reported seeing substantially higher throughput and greater control, which allowed them to achieve sample specifications that were previously unobtainable on other equipment. The features and functionality of the machine including its recipe modes, auto plate flatness and real time data collection allowed operators with basic training to achieve the same accuracy and throughput that a skilled engineer might deliver. They achieved a real boost in productivity," Kennedy said.

Silicon lapping & polishing

Every semiconductor wafer undergoes several common stages during manufacture including slicing the wafer from its crystal ingot, preparing the surface prior to fabrication and subsequent thinning of the wafer through lapping and polishing techniques.

After slicing, wafers made of silicon or III-Vs materials are lapped to remove surface scratches and flaws that occur during cutting processes. Typically performed by the wafer manufacturer, lapping removes saw marks and surface defects from the wafer and also helps relieve any internal mechanical stress that accumulated during the slicing process.

Lapping typically involves counter-rotating plates using an aluminium oxide abrasive with defined grain size distribution. During lapping, wafer flatness is improved while micro-roughness is also reduced. An edge grinding procedure may also take place. When edge grinding is needed manufacturers may also follow this step with polishing the wafer edge since doing this can greatly reduce the probability of wafer breakage further down the process line.

Chemical mechanical polishing is the final material removal step utilized in manufacturing wafers. This process allows the attainment of super-flat, mirror-like surfaces with a remaining roughness on an atomic scale. Polishing the wafer can be seen as the most crucial step in the manufacturing process since the polished wafer face is used for device fabrication; it must be as damage free as possible. Typically, CMP is achieved using a rotary or orbital motion of a chemical slurry injected in precise quantities and flow rates between the polishing plate and the wafer itself.

There are many reasons why manufacturers need stability and repeatability when it comes to wafer sample preparation. For instance, stringent quality requirements dictate that parameters such as total thickness variation (TTV), surface roughness and plate flatness must be carefully monitored. In all cases, a fundamental understanding of the process is required to ensure a quality outcome. Different types of wafer materials, slurries and polishing pads, along with polishing rate, pressure and uniformity can all impact the resulting surface. It is also important not to overburden the surface with too much slurry as this has the potential to impair detection of when the

polishing process is complete. To put this in simple terms, it is vital to accurately predict the amount of material removed from a sample in a given time. Here, Preston's Law is fundamental to successful lapping and polishing. Indeed, it is possible to analyse the Prestonian behaviour of material removal rate (MRR) to confirm that all-important process stability has been achieved.

Silicon lapping and polishing trials

Lapping and polishing trials using a typical silicon substrate deployed in semiconductor applications such as the manufacture of integrated circuits, solar and waveguide devices can be extremely revealing. In a typical silicon lapping and polishing process, a series of steps are used, each with a different slurry solution.

Firstly, a coarse lapping process is undertaken to remove material within 50 μm of the end point target. Previous experiments have shown that slurries containing Al2O3 particles measuring 20 μm provide the optimum balance between material removal speed and maintaining the integrity of the underlying silicon wafer. In a second stage, a medium/fine lapping process is conducted, during which a finer, less abrasive 9 μm Al2O3 slurry is used to remove materials to within 10 μm of the end point target. The final stage involves removing the last micrometres of material; the removal of any damage caused to the wafer during the lapping process is also undertaken using 32nm colloidal silica, such as the Logitech SF1 polishing slurry. After undergoing all three stages a typical surface roughness of Ra<1nm is achievable.

Tests to determine average silicon lapping at 50 rpm versus 100 rpm showed an average MRR of 18-22 μm/min using an automated system: the Logitech Akribis-air. This was compared to that of a standard Logitech lapping and polishing system with an MRR of 7-9 μm/min. Substantial time savings and accuracy were achieved with the automated set-up and control platform; the Akribis-air tool also provided internal clean-up facility. Collectively, all automation-derived improvements delivered a total process time savings of approximately 40 percent.

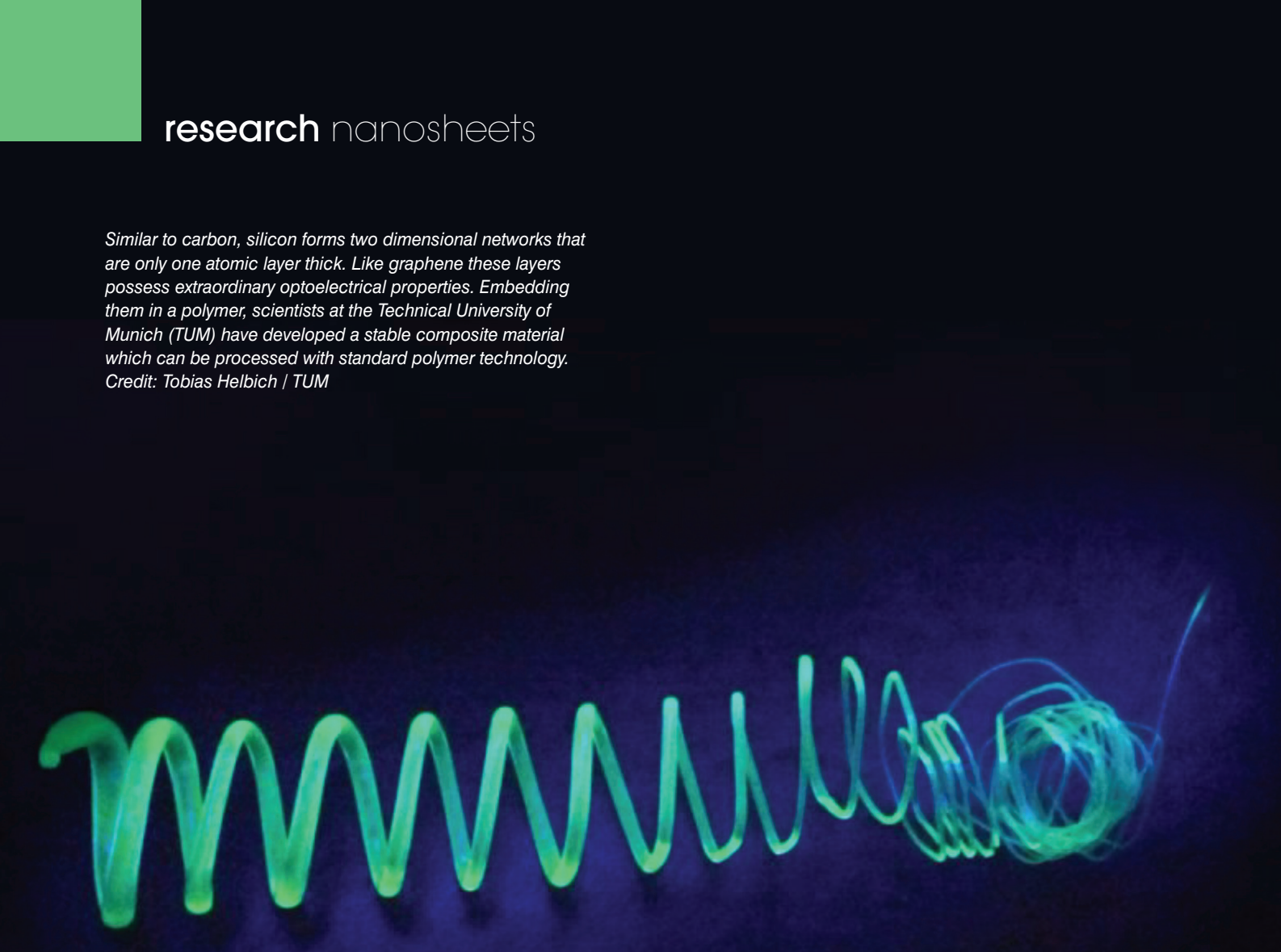
Differentiating features found in automated systems such as the Logitech Akribis-air and PM6 Precision Lapping & Polishing System are key to achieving such impressive results. Automated air jigs (available with the Akribis-air) and intelligent automated controls on both systems have positive impacts on processing that benefits not only by creating a flatter, more defect-free wafer but also in terms of substantial process time reductions. These technologies can help semiconductor and optical device manufacturers to precisely optimise their sample preparation processes.

A high degree of geometric precision, flatness and parallelism can be achieved by taking advantage of automatic wafer thickness control. Software-driven

set-up within automated systems permits faster processing times (in tandem with plate speeds of up to 100rpm) and more reliable results. There is also extensive parameter control for the processing of complex and fragile wafers; metered abrasive feed supplies for optimal processing and reduced wastage of consumables are other substantial cost saving factors. Automated system like the Logitech PM6 or the Akribis-air also provide for the export of critical data as an information base for future process refinement and documenting productivity improvements over time.

Semiconductor and optical device manufacturers demand greater process control and real-time data in their quest for improved productivity and reliable, repeatable quality. By utilizing an automated approach in wafer sample preparation such as the Logitech Akribis-air or the PM6, researchers and manufacturers alike can achieve faster throughput, more precisely prepared and polished wafers, all with dependable repeatability that also frees their most highly skilled engineers and technicians to focus on other critical endeavours.

Similar to carbon, silicon forms two dimensional networks that are only one atomic layer thick. Like graphene these layers possess extraordinary optoelectrical properties. Embedding them in a polymer, scientists at the Technical University of Munich (TUM) have developed a stable composite material which can be processed with standard polymer technology. Credit: Tobias Helbich / TUM



Polymer-coated silicon nanosheets

an alternative to graphene

Nanocomposite material with exceptional optoelectronic properties

SILICON NANOSHEETS are thin, two-dimensional layers with exceptional optoelectronic properties very similar to those of graphene. Albeit, the nanosheets are less stable. Now researchers at the Technical University of Munich (TUM) have, for the first time ever, produced a composite material combining silicon nanosheets and a polymer that is both UV-resistant and easy to process. This brings the scientists a significant step closer to industrial applications like flexible displays and photosensors.

Similar to carbon, silicon forms two dimensional networks that are only one atomic layer thick. Like graphene, for whose discovery Andre Geim and Konstantin Novoselov received the Nobel Prize in 2010, these layers possess extraordinary optoelectrical properties. Silicon nanosheets might thus find application in nanoelectronics, for example in flexible displays, field-effect transistors and photodetectors. With its ability to store lithium ions, it is also under consideration as an anode material in rechargeable lithium batteries.

"Silicon nanosheets are particularly interesting because today's information technology builds on silicon and, unlike with graphene, the basic material does not need to be exchanged," explains Tobias Helbich from the WACKER Chair for Macromolecular Chemistry at TUM. "However, the nanosheets themselves are very delicate and quickly disintegrate when exposed to UV light, which has significantly limited their application thus far."

Polymer and nanosheets – the best of both worlds in one

Now Helbich, in collaboration with Professor Bernhard Rieger, Chair of Macromolecular Chemistry, has for the first time successfully embedded the silicon nanosheets into a polymer, protecting them from decay. At the same time, the nanosheets are protected against oxidation. This is the first nanocomposite based on silicon nanosheets.

"What makes our nanocomposite special is that it combines the positive properties of both of its components," explains Tobias Helbich. "The polymer matrix absorbs light in the UV domain, stabilizes the nanosheets and gives the material the properties of the polymer, while at the same time maintaining the remarkable optoelectronic properties of the nanosheets."

Long-term goal of nanoelectronics – In leaps and bounds to industrial application

Its flexibility and durability against external influences also makes the newly developed material amenable to standard polymer technology for industrial processing.

Silicon nanosheets are particularly interesting because today's information technology builds on silicon and, unlike with graphene, the basic material does not need to be exchanged

This puts actual applications within an arm's reach. The composites are particularly well suited for application in the up and coming field of nanoelectronics. Here, "classical" electronic components like circuits and transistors are implemented on scales of less than 100 nanometers. This allows whole new technologies to be realized -- for faster computer processors, for example.

Nanoelectronic photodetector

The first successful application of the nanocomposite constructed by Helbich was only recently presented in the context of the ATUMS Graduate Program (Alberta / TUM International Graduate School for Functional Hybrid Materials): Alina Lyuleeva and Prof. Paolo Lugli from the Institute of Nanoelectronics at TU Munich, in collaboration with Helbich and Rieger, succeeded in building a photodetector based on these silicon nanosheets.

To this end, they mounted the polymer embedded silicon nanosheets onto a silicon dioxide surface coated with gold contacts. Because of its Lilliputian dimensions, this kind of nanoelectronic detector saves a lot of both space and energy.

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Transforming sub-fab service and support to lifecycle management

Edwards Vacuum President Paul Rawlings seeks to transform productivity by changing the way semiconductor manufacturers think about servicing their sub-fab equipment.

SERVICE AND SUPPORT now plays a key role in fabs to enhance process yields and reduce total cost of ownership. This has led to service models evolving away from the simple "break and fix" approach to a lifecycle management methodology, using techniques such as advanced diagnostics and predictive maintenance based on real-time monitoring of operational performance metrics. Reflecting this ever-increasing emphasis, equipment suppliers have elevated the service function to an equivalent status with other critical business functions, such as research and development and production. To support its vision of service as a customer centric enterprise that encompasses the entire product lifetime within the fab, Edwards has recently restructured its semiconductor service operation as a separate division.

Service and support for semiconductor manufacturing has evolved dramatically since the early days of the industry. For instance, our industry was among the first to put uptime requirements on equipment suppliers. To be competitive in the current environment, equipment suppliers must seek out opportunities to improve their customers' experience at all points in the product and fab lifecycle. Among the challenges we face today are: support for increasingly complicated manufacturing processes and materials; complying with increasingly stringent environmental regulations; and optimizing the use of scarce resources, such as water and energy. These are in addition to the ever-present pressure to reduce total cost of ownership and require a service model that is tailored to the varying needs at different points in the fab lifecycle. In considering this approach, it is convenient to divide the lifecycle into stages, each with its own requirements and opportunities for enhancement. The stages include: planning, installation, ramp, high-volume production, and end of life.

Planning

Engagement should begin at the earliest planning stage for a new fab or expansion of an existing facility. In this phase, it is critical that vendors explain the equipment options available to their customers and the benefits of the various choices. Important considerations include the process chemistry and vacuum demand, the evolving regulatory environment, demands of consumers for environmental responsibility, and the opportunities for lifecycle and data management.

Installation

Installation is an incredibly busy time in any new fab—when the emphasis must be on getting the equipment delivered, bolted down, hooked up and running as quickly and efficiently as possible. Given the large investment required to build a state-of-the-art fab, there is immense pressure to complete installation in the shortest possible time, and detailed knowledge of solutions that have worked in other similar applications are crucial in achieving that goal. Strong project management and the deployment of field-proven best-known-methods (BKMs) are the key to ensuring that fabs can start-up quickly and begin the critical ramp phase, proving-out tools and processes.

Ramp

The ramp phase is a race to achieve economic process yields. This invariably presents a myriad of challenges and opportunities to optimize the performance of sub-fab equipment and customize its operation to best match the process and application. Changes are inevitable, even with the best-laid plans, and it is in this situation that the deep expertise and broad experience of supplier personnel are most critical. For example, many cutting-edge deposition processes involve condensable materials that can deposit and eventually block exhaust lines unless temperature is precisely controlled along the entire exhaust pathway from the chamber exit through the vacuum pump and abatement system.

High-volume Production

High-volume production is probably where the

Figure 1: Lifecycle stages

greatest opportunity lies for tailored lifecycle management as even the slightest advantage in performance or efficiency can have a significant impact on output and the economic performance of the manufacturing process. It is here that managed maintenance—tracking the status of equipment and planning service interventions and the efficient use of on-site teams to maximize the efficiency of the fab—can have the greatest impact. It is here also that management systems (like Edwards EdCentra product), designed specifically to collect and analyze data from an entire fleet of systems installed across a facility, are essential in implementing a data-driven approach to service.

Massive and detailed data collection and analysis present many opportunities to optimize equipment performance. Each system's critical process steps can be custom tuned, before and after service, to an individualized "fingerprint" state to improve process repeatability. Predictive maintenance, which monitors critical operating parameters to determine when maintenance is required and coordinates scheduling with other process equipment, can significantly extend service intervals and reduce process downtime.

Monitoring parameters such as temperature, pressure, vibration, power consumption, and more, allows active management of equipment health and performance and can extend product lifetimes substantially. Historical usage and application data from individual systems can be used to optimize and customize the remanufacturing process for each system. Advanced diagnostics can ensure that when service is required the service engineer knows what the problem is, what to bring along to fix it and how to ensure that the repaired system will precisely replicate the performance of the system it replaces. Finally, analysis of real-time and historical data may provide an opportunity to move away from fixed price service to a more flexible and adaptive pricing approach.
On a much larger scale, aggregating data across large numbers of systems presents yet another set of opportunities. The full data set includes information acquired at every stage of the product's life cycle from original manufacture, through operation and remanufacture. Sophisticated modeling and data mining techniques can compare the performance of different products and setups in multiple situations to extract actionable information that helps service personnel to get the most from existing products and helps designers and engineers develop new products that better meet customers' needs.

End of Life

End of life management is next and is taking on a new dimension as older fabs find new life meeting the growing demand for mobile, automotive, and Internet of Things devices. This presents an opportunity to upgrade ageing electronic parts and components not typically replaced at a standard service or to take advantage of technological advances to upgrade or replace equipment with newer models that offer better performance or higher energy efficiency.
All this opportunity hides a real risk of analysis paralysis. Manufacturers must maintain their focus on meeting customer needs and delivering tangible results. Monitoring key service performance indicators, such as on-time delivery, timely installation, and speed of response for unscheduled repairs and problem solving success, can help. But the trick is to be sure that the manufacturers' indicators align with customers' priorities. Ultimately, the real opportunity lies in developing a shared view of total cost of ownership over the lifecycle of a fab. This will be the key step in implementing a fab lifecycle service model.

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Using manifold technology to optimize cost of ownership

The management of fluid systems is experiencing a drastic change on how a customer perceives the importance of the component. By Stephane Domy, Global Marketing Manager, High Purity Systems at Saint-Gobain Performance Plastics

WE HAVE MOVED from only looking at the component as a standalone item, which has its own specification and benefits for the carried fluid, to looking at the impact of a set of components, which can also be called a manifold on the installation / application. This evolution has been a driving force in the micro-e industry and prompting it to embrace the co-development of products, which is something Saint-Gobain has recognized and supported for years. It is part of our DNA.

To review what the manifold approach may bring to your installation/system, let's split the benefits provided by manifolds into three main categories: Safety, Cleanliness and Cost of ownership.

One of the direct impacts that is inherent when you manifold a set of components is that you are reducing the number of leak points. You are not simply improving the sealing efficiency of a connection; you are totally eliminating it. On average, you can expect a leak point reduction above 60 percent on some occasions it can be significantly higher than that, but that percentage relates directly to what you are manifolding. As an example, in the simple manifold illustration below we are moving from 26 connection points down to 6 (All red connection points are removed. We only keep the green ones).

Remove potential leak points (identified in red) through manifolding

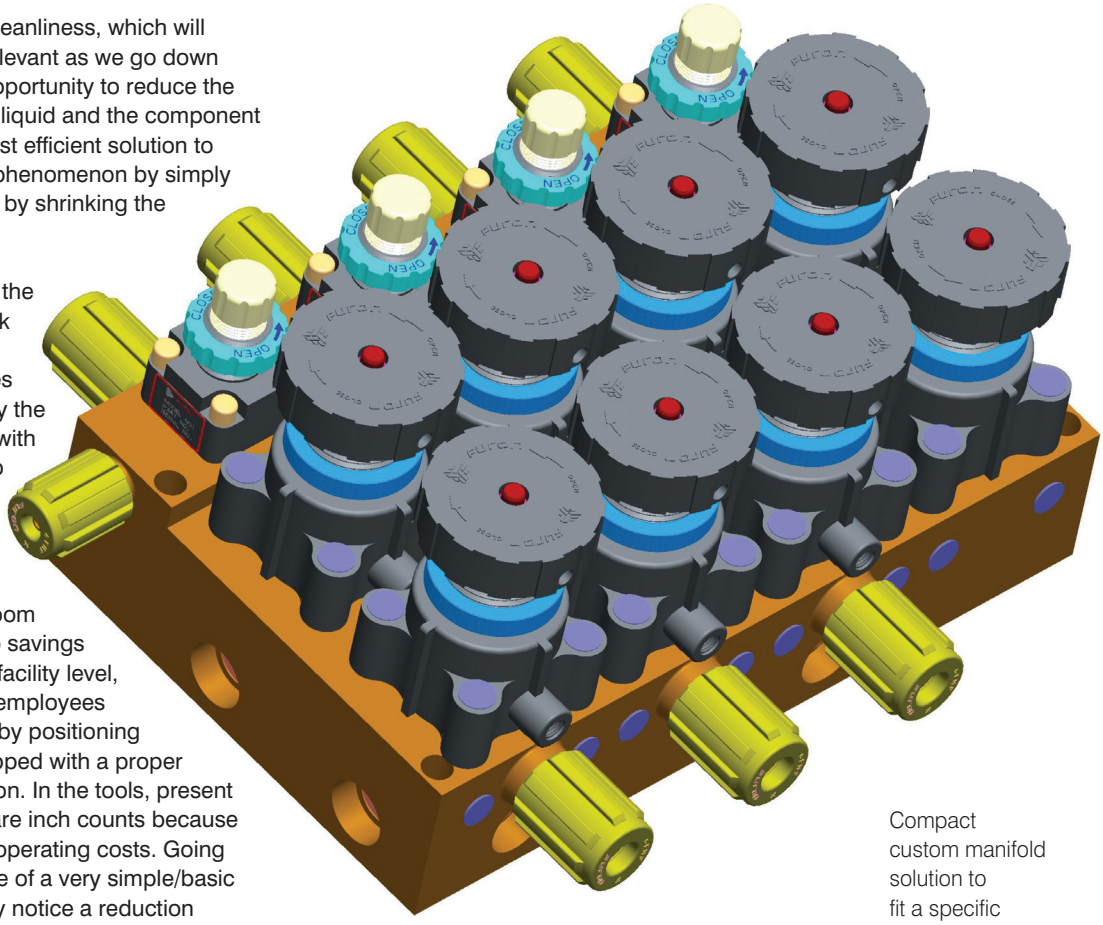
Another advantage related to safety, though less obvious than previously described, derives from the fact that when we are designing these manifolds, we (under our hat of component experts) can choose products that have the same level of performance and operating factor. Generally, this specific selection offers longer life time for components as they are installed in proper condition of use.

Following the same logic as above, but this time related to cleanliness, when we design a manifold based on a customer-specific requirement, we also ensure that from a cleanliness and SEMI standard point of view we are using components that belong to the same category. Cleanliness of a system is also directly related to the number of connections that are present in your design, as all connection points are equal to a potential entrapment point regardless of how good a fitting may be or a weld may be. So removing connection points turns your system into a cleaner system even if you are using the best connection system.

Additionally, given we are designing a custom component; we know how it will be installed (orientation), its purpose and most likely the carried liquid. Thanks to this information, we will be able to minimize entrapments zone (which is often a plague in slurry applications) as we will know how the fluid will have to flow through this given device. Based on the same logic but for a different application, we will be able to design the manifold in order to minimize potential dead volume, which is especially critical for analyzer systems.

A final comment regarding cleanliness, which will start to be more and more relevant as we go down in the printing node, is the opportunity to reduce the contact surface between the liquid and the component carrying it out, as it is the most efficient solution to limit the leaching/exchange phenomenon by simply reducing the contact surface by shrinking the component design.

As we have just seen above, the feature of being able to shrink the design of a given set of components actually provides a double advantage. Not only the one mentioned here above (with improve cleanliness) but also by allowing you to reduce your cost of ownership. If you manage to shrink down a design both at the facility level as well as in the cleanroom there is a direct translation to savings that can be achieved. At the facility level, it allows you to protect your employees as well as the manifold itself by positioning it in compact valve box equipped with a proper sensing system and ventilation. In the tools, present in the cleanroom, every square inch counts because of their high installation and operating costs. Going back to our previous example of a very simple/basic manifold, once again we may notice a reduction of over 60 percent, but this time in terms of the component's foot print.

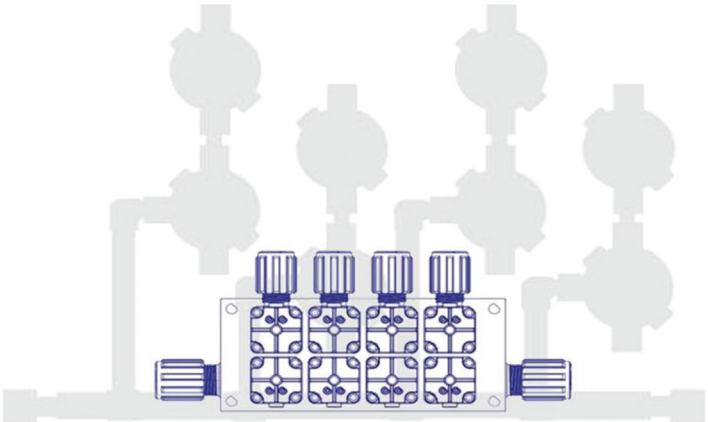


Compact custom manifold solution to fit a specific customer's needs

Manifolds also provide you significant savings if you are an end user or if you are an OEM. For the end user, this is mostly related to the maintenance/service of your installation. The first reaction that we may have is due to the fact manifolds prevent you from having discrete items, the cost impact on your maintenance may be larger. However if you look at the total cost of ownership, working with manifolds may allow you to generate significant savings. Because it's only a few components that you have to keep in stock, you are sure to always have the right parts, whereas if you are running discrete components the one that you will need to replace will always be the one you are missing.

In addition, when you are changing such a manifold it's like you are renewing the full subsystem at once and prevent to have multiple down time on components that are facing the same wearing phenomenon which may lead to potential need for replacement in a similar time frame. For the OEM, you receive a full small sub-unit that has already been assembled and tested which saves time and money related to hook up & plumbing. Also it allows you to be more nimble to address fast installations for the customer when you have a full fab install to do, using manifold design vs discrete components may save you hundreds hours of labors. The benefit to using manifold design is it enables you to get a custom answer to your unique needs. Understandably that the initial cost difference between discrete components and manifolds might be seen as a barrier to go toward this specific technology; however if you compare the cost of ownership of the two solutions inevitably you will realize that manifold systems are more economic and at the same time provides you premium benefits such as safety and cleanliness.

At Saint-Gobain we have seen numerous customers who were reluctant to make the move but once they did, they embraced this different approach by looking at the overall benefits package provided by a manifold.



How manifolding may impact a component's overall size.

New wafer dicing approach for silicon carbide devices

With the transition to new substrates like SiC, as well as thinner wafers, smaller feature sizes and larger-size substrates, wafer dicing has evolved into a critical process step that can enhance SiC device yields.

Explains Dr. Hans-Ulrich Zuehlke and Mandy Gebhardt, 3D-Micromac AG

AS A WIDE BANDGAP MATERIAL, silicon carbide (SiC) is considered a replacement material for silicon (Si)-based semiconductors in the electronics industry in certain applications due to its wide band gap, high mechanical strength, and high thermal conductivity. For example, SiC power devices can operate at higher voltages, frequencies and temperatures, as well as convert electric power at higher efficiency or lower power losses. At the same time, SiC is an extremely hard and brittle material (Mohs scale 9.2), which can create processing challenges. This is particularly true in back-end processing where wafers must be singulated into individual die prior to packaging.

Historically, wafer dicing has been treated as an after-thought in the overall semiconductor fabrication process—a necessary evil that adds little value to the overall process. However, with the transition to new substrates like SiC, as well as thinner wafers, smaller feature sizes and larger-size substrates, wafer dicing has evolved into a critical process step that can enhance SiC device yields.

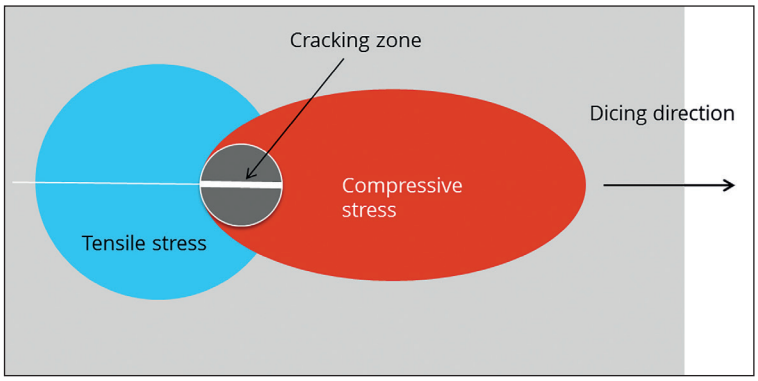


Fig. 1. Principle of TLS

Limitations of established dicing technologies

Mechanical diamond blade dicing is the traditional technique for separating SiC wafers. The wafer is mounted on a dicing tape and is cut by a diamond coated saw blade rotating at high speed. The width of the dicing street is typically in the range of 50 to 100 μm. Due to the hardness of SiC, blade sawing suffers from low feed rate and high wear of the dicing blade, resulting in higher cost. In addition, blade sawing can result in chipping and delamination at the edge of the die. As SiC wafer sizes transition from 4-inch to 6-inch diameters, the cumulated street length more than doubles and is beyond the ability of one standard saw blade to completely cut. As a result, the blade has to be changed while the wafer is in work-position, and can break during the middle of the dicing process thereby damaging the wafer.

Laser ablation is an alternative approach to mechanical wafer dicing. The laser beam is focused into the dicing street. The material is heated up by the absorbed laser energy. This leads to a significant heat affected zone and micro cracks. There can also be a thermal impact on the dicing tape, which can affect subsequent packaging processes. In addition, the ablation rate is very low and multiple passes are needed to separate the dies. The number of repetitive passes depends on wafer thickness and cutting speed. To avoid material residues on the chips, the surface of the wafer has to be coated by a protection layer. Major disadvantages of this dicing technique are low edge quality and low throughput. In stealth dicing, a short pulsed laser beam at a wavelength that transmits through the SiC wafer is focused inside of the material. It generates a layer of localized defects inside the material that serves as a starting point for wafer separation. First, the laser beam is focused into the lower part of the wafer and moves layer by layer stepwise toward the top. Because it is a cleaving process there is no material removed in the dicing street—resulting in zero kerf. Second, the final separation of the dies must be done by a separate mechanical breaking process and expansion of the dicing tape. Since the laser heats up the material inside of the wafer, there is no heat damage to the wafer surface. Defects in a pearl chain pattern with overlapped areas only occur inside of the material. In addition, the feed rate for one pass is approximately 200 mm/s, though it can be up to 300 mm/s in some applications.

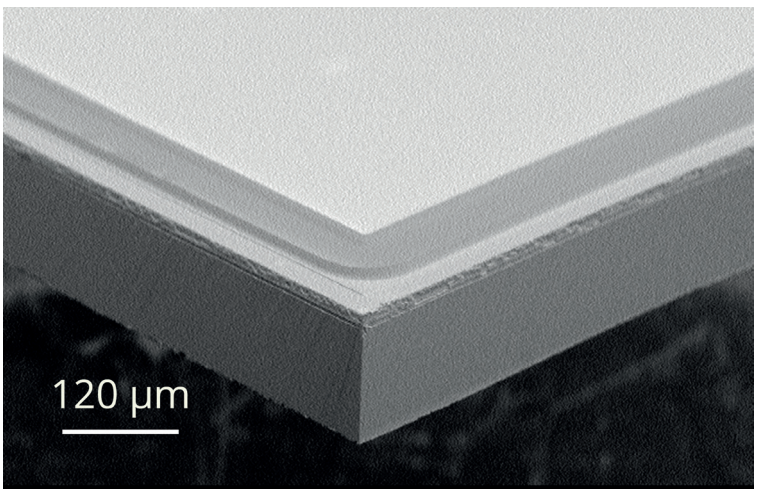


Figure 2: SiC die edge after TLS-Dicing process shows smooth edges and no micro cracks or chipping

However, depending on the thickness of the material, several passes of the laser are needed to separate the dies. This leads to damages of the chip sidewalls due to the modified layers. To focus the laser beam on a very small spot inside the wafer, a smooth and minimizing beam that scatters across a flat surface in the dicing street is needed. To avoid reflection of the laser, a metal free dicing street is required. A further disadvantage is that the required width of the open street is a function of the wafer thickness (typically, 40 percent of the wafer thickness), which means that for a standard SiC wafer with a thickness of 350 µm, a minimum dicing street width of 140 μm is necessary.

Thermal laser separation

Thermal Laser Separation (TLS-Dicing) is a fast, clean and cost-effective alternative to separating SiC wafers. A laser heats up the material and generates a zone of compressive stress, surrounded by a zone of tangential tensile stress pattern (Figure 1). A jet of extremely small amounts of deionized water spray is then applied, which creates a second cooled zone near the first zone that induces a tangential tensile stress pattern. The resulting tensile stress in the overlaying region of both stress patterns opens and guides the crack tip through the material.

TLS-Dicing is a one-pass process that separates the whole thickness of the wafer with a separation speed of up to 300 mm/s. The starting point is given by a shallow scribe that is either local or continuous at the wafer's surface. Due to the fact that TLS-Dicing is a cleaving process, it has the potential to reduce the width of the dicing street and increase the number of chips per wafer. The die edges are smooth and free of remaining stress or micro cracks and chipping zone (Figure 2). Metal structures (PCM) in the street on the front side and polyimide on the dies are acceptable. In addition, since the separation is due to the cleave as opposed to subsequent physical

TLS-Dicing is a one-pass process that separates the whole thickness of the wafer with a separation speed of up to 300 mm/s. The starting point is given by a shallow scribe that is either local or continuous at the wafer's surface. Due to the fact that TLS-Dicing is a cleaving process, it has the potential to reduce the width of the dicing street and increase the number of chips per wafer.

separation/breakage, the backside metal can be separated with no delamination or heat affects. Yield analyses on the use of the TLS-Dicing process on a typical power device wafer with full backside metallization, polyimide and metal structures in the dicing streets have shown an average yield value of more than 98 percent.

In addition, TLS-Dicing has demonstrated a significant improvement in terms of cost per wafer. A typical mechanical sawing process wears out one saw blade per wafer due to the enormous hardness of SiC, and is insufficient to completely cut a 6-inch wafer as noted earlier. To match the throughput of the TLS process, an investment in nine times more mechanical sawing tools is required. The added capital equipment cost combined with additional factors such as cost of consumables, projected tool depreciation and increased footprint result in a nearly 15X increase in overall cost per 6-inch wafer for mechanical sawing compared to the TLS-Dicing system. (Figure 3)[1]

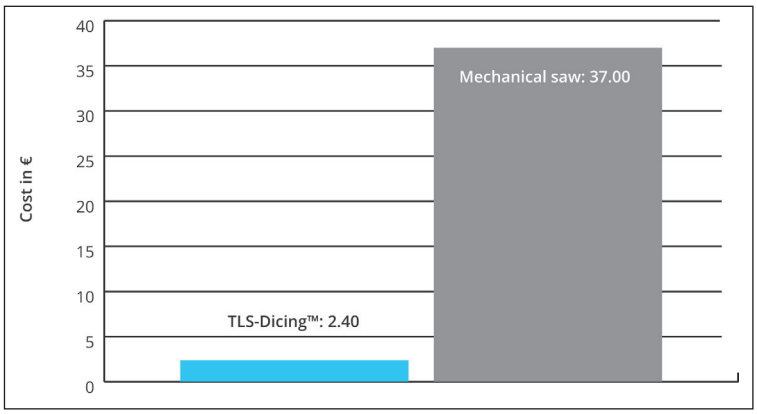


Figure 3: Throughput comparison for dicing a 6-inch wafer using TLS-Dicing and mechanical saw methods.

Conclusion

Laser dicing processes are very promising methods to separate SiC dies with high efficiency. All laser dicing technologies described in this article offer higher separation speed than mechanical blade dicing. However, in laser ablation the dicing speed depends on the wafer thickness and the edge quality is not ideal. On the other hand, stealth dicing may require several passes depending on the wafer thickness, and requires an additional breaking process to separate the dies. With stealth dicing, it is also not possible to separate wafers with metal layers on the surface.

TLS-Dicing has demonstrated unique advantages for separating SiC wafers. The cleaving is always a one-pass process, so the feed rate of up to 300 mm/s applies. It produces excellent sidewall quality with no chipping, and has a far lower cost of ownership compared to mechanical blade dicing.

The cleaving principle shows unique advantages for SiC-based products with backside metallization, such as power devices.

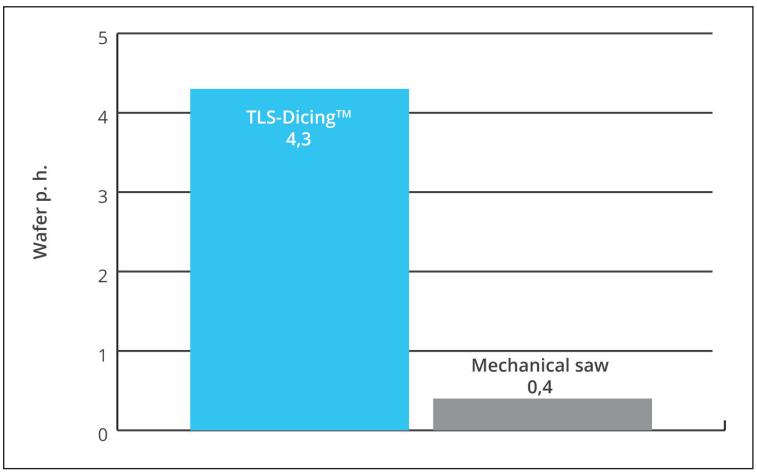


Figure 4: Cost per wafer comparison for dicing a 6-inch wafer using TLS-Dicing and mechanical saw methods.

Reference
[1] TLS-Dicing™: A Novel Laser-based Dicing Approach for Silicon Carbide Power Devices
http://3d-micromac.com/int/applications/tls-dicing

Silicon photonics
for a post-Moore era

What solutions are in the pipeline to support higher performance devices in a post-Moore era? Koji Yamada, head of the Silicon Photonics Group at the Electronics and Photonics Research Institute - a division of Japan's National Institute for Advanced Industrial Science and Technology (AIST), explores the opportunities provided by silicon photonics and discusses the next steps for this exciting PIC platform.

MOORE'S LAW expresses an empirical trend in device integration in electronic circuits, such as micro-processor chips. The device integration status is defined as the number of elemental devices -- such as transistors -- integrated on a chip, which doubles every two years. However, such exponential growth defined by Moore's law is now coming to an end, because -- ultimately -- miniaturised devices see the de Broglie wave of electrons (more details below). In other words, we are now entering the post-Moore Era. At the same time, we are seeing explosive growth in information systems, which is one of the major applications of electronic circuits, and improvements in their performance must continue. To cope with such an information explosion, various post-Moore electronic circuit technologies are now being developed under guidelines referred to as 'More Moore', 'More than Moore', and 'Beyond CMOS'. In 'More Moore', further geometrical integration is achieved by introducing novel materials and three-dimensional (3D) integration methods. 'More than Moore' is a system-on-chip (SoC) approach, where non-digital devices are implemented. 'Beyond CMOS' refers to devices based on novel principles, such as electron spins, and novel architectures suitable for these novel devices.

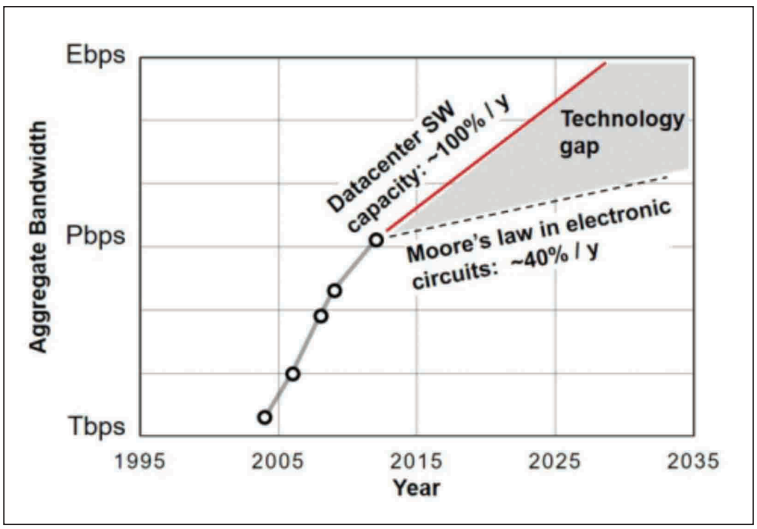


Figure 1: Trend of switching capacity in a typical large-scale datacentre.

Moore's Law in data transmission, which is an important aspect of information systems, is also facing its end. For example, as shown above, switching capacity in a typical large-scale data centre is growing at a rate of 100 to 1000 times every 10 years1, which is overwhelming Moore's Law in electronic circuits. Since electronic circuits are used for switching systems at present, such explosive growth will become unsustainable soon. In the global network system, we are also facing the end of Moore's Law. For more than 30 years, data transmission capacity per fibre has been increasing with a growth rate of 80 percent a year through various paradigm shifts in

technology, such as from TDM to WDM and multi-level modulations2. However, it has now reached the nonlinear Shannon limit.

To cope with such explosive growth in data transmission, we also need post-Moore technologies for photonics as well as for electronics - because data transmission systems consist of electronic and photonic elements. For the development of post-Moore photonics technology, the same approaches in electronics can be applied, and silicon photonics provides a platform for post-Moore photonics.

Silicon photonics as a post-Moore photonic technology

Thanks to the very strong optical confinement ability of silicon photonics technology, photonic circuits can be miniaturised considerably, and data transmission capacity per unit chip area can be increased. An example is an integrated WDM receiver chip consisting of multi-channel wavelength filters, photodiode (PD) array, and electrodes for signal output. By using silicon photonics, an arrayed-waveguide-grating (AWG) wavelength filter, which is a standard multi-channel wavelength filter, can be miniaturised to 1-mm square. Moreover, germanium PDs and through-silicon via (TSV) electronic wiring can be scattered over the whole the chip.

Therefore, as shown above, the required area of a 100-ch WDM receiver chip will be reduced to 1 cm2, which is 1/100 of the area of chips based on conventional technology. Assuming PD operation at 25 Gbps, total capacity will reach 2.5 Tbps/cm2. In parallel transmission systems, where no wavelength filter is required, total bandwidth can be increased up to 30 Tbps/cm2 3.

Spatial division multiplexing (SDM) can also be categorised as two-dimensional geometrical integration. By using silicon photonics technology to make ultra-small optical coupling structures within the area of a fibre core, highly integrated SDM modules consisting of an SDM fibre interface and optical processing circuits can be constructed4.

More than Moore: Photonics - electronics SoC

Integration with electronics is the most impactful post-Moore technology for photonic circuits. Integration with modulation drivers, transimpedance amplifiers for PDs, and various control circuits on a silicon photonics chip can significantly reduce the size of photonic-electronic integrated modules. Moreover, since electronic circuits can be placed very close to photonic devices, high-frequency performance can be significantly improved5.

Since silicon photonics is based on silicon electronics technology and the silicon platform is reliable and robust, electronic circuits can be integrated by both monolithic and hybrid approaches. Concepts of such

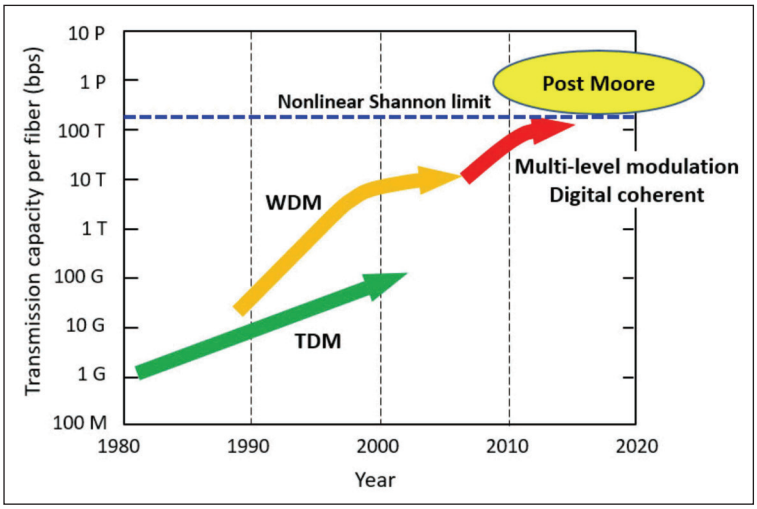


Figure 2: Trend of data transmission capacity per fibre.

photonics-electronics convergence can be seen above. The monolithic approach is very attractive from the viewpoint of ultra-high-volume production, and some short-range data transmission modules have already been commercialised6.

However, we must consider that device performance might be degraded because of narrow margins in the fabrication process for photonics-electronics convergence. For example, in monolithic photonics-electronics convergence, the dark current of germanium PDs is likely to increase. Moreover, typical CMOS electronics technology cannot provide the high-speed electronics required for high-bit-rate optical data transmission.

For improving device performance both in photonic and electronic circuits, the hybrid approach is

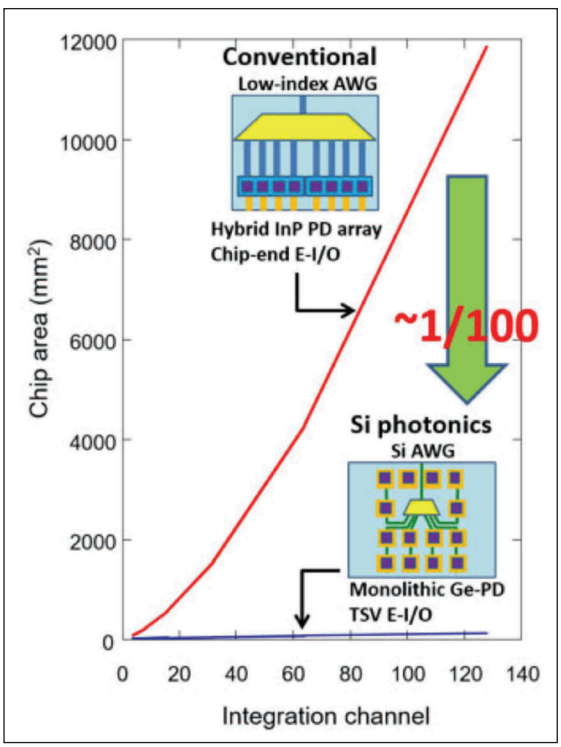


Figure 3: Estimated chip area of integrated WDM receiver sub-assembly.

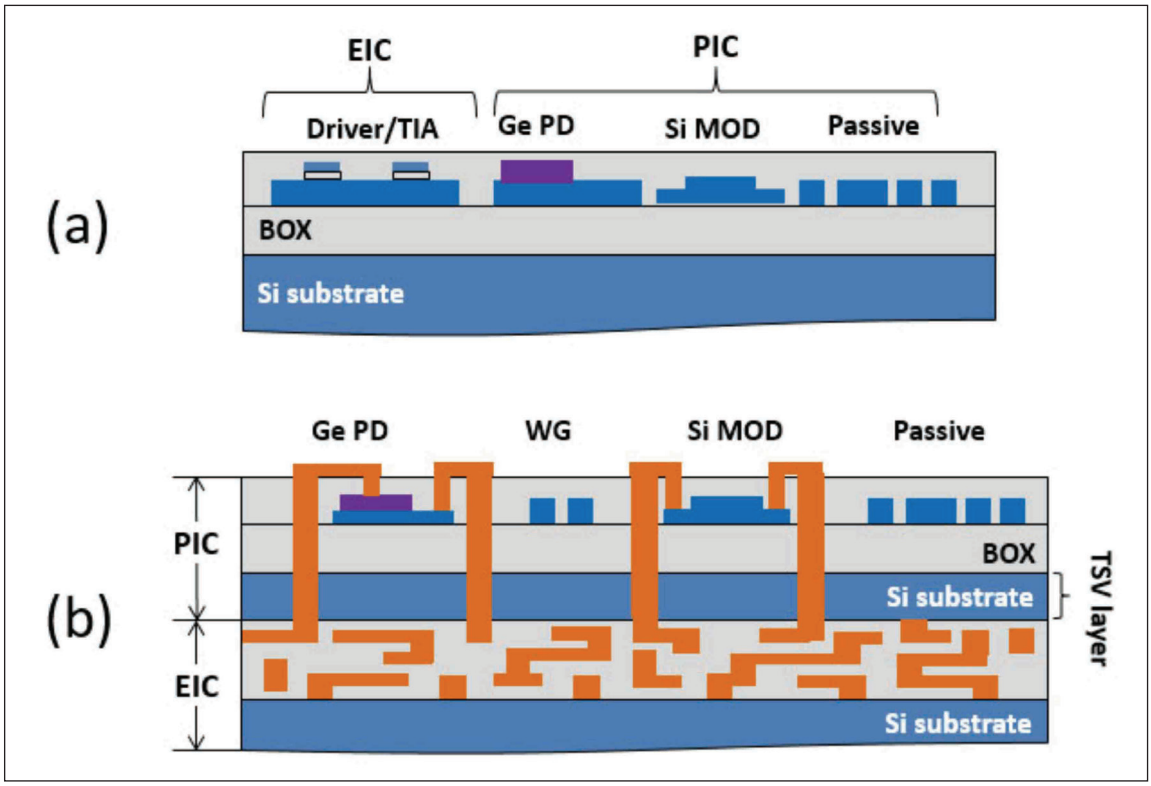


Figure 4: Photonics-Electronics convergence. (a) Monolithic and (b) TSV-based hybrid integration.

attractive. Since both types of circuits can be fabricated by their respective optimised fabrication process, high-performance photonics-electronics convergence can be achieved. Hybrid integration is performed by using various wafer-bonding/die-bonding techniques with TSV and micro-solder bump technologies7. Since hybrid integration technology is a kind of 3D integration technology, it can also contribute to geometrical integration in the More Moore approach.

Novel-principle devices and architectures: replacement of electronics with photonics

Since current optical fibre transmission systems show excellent performance, we currently have very small margins for novel-principle devices. However, if we consider data transmission systems replacing electronic circuits with photonic ones corresponds to an approach for implementing novel-principle devices and architectures. This approach can be seen

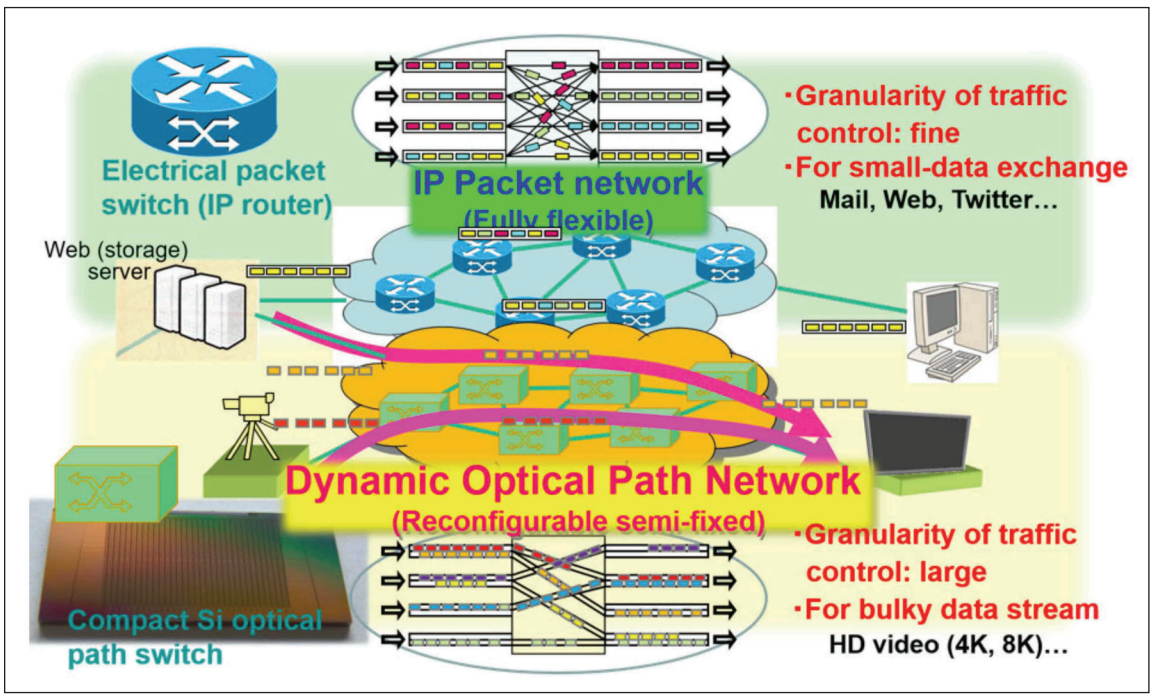


Figure 5: Dynamic optical path network.

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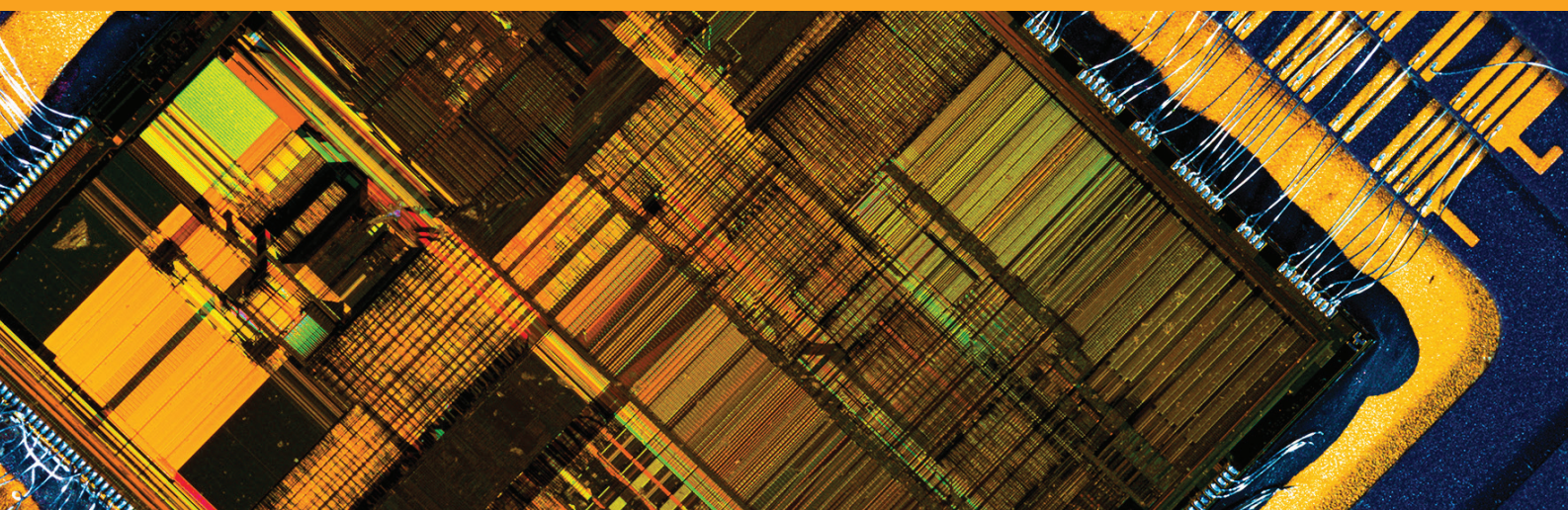

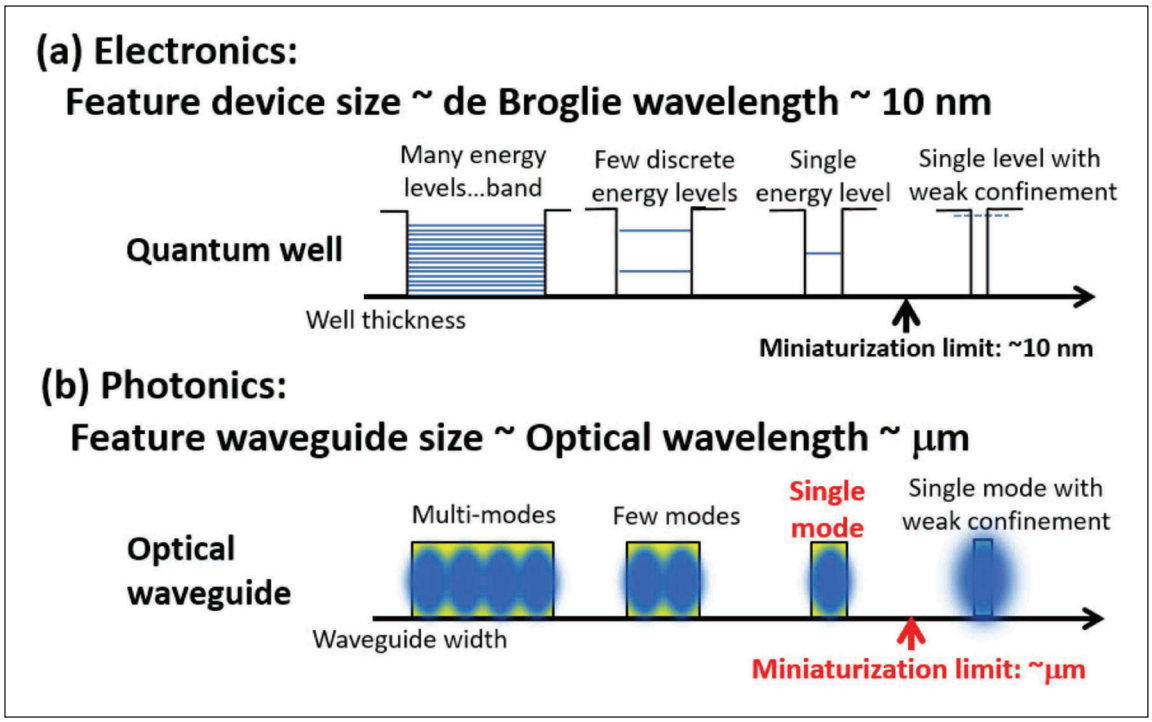

Figure 6: End of miniaturization scaling.

in the dynamic optical path network (DOPN) using large-scale optical switch matrixes8,9. Conventional switching systems are made of electronic devices, where numerous small packets are independently routed to several unspecified terminals. Thus, power consumption for the switching increases proportionally to the data traffic.

This conventional packet switching scheme, however, is not suitable for the transmission of bulky video data to specified terminals, which has been a dominant factor in the recent traffic increase. In the DOPN, as shown above, dedicated optical transmission channels are temporarily constructed by an optical switching matrix. Since packet switching is not utilised in the DOPN, the power consumption for bulky data transmission can be greatly reduced. Recently, a DPON field trial using a silicon-photonics-based optical switch matrix has been carried out8.

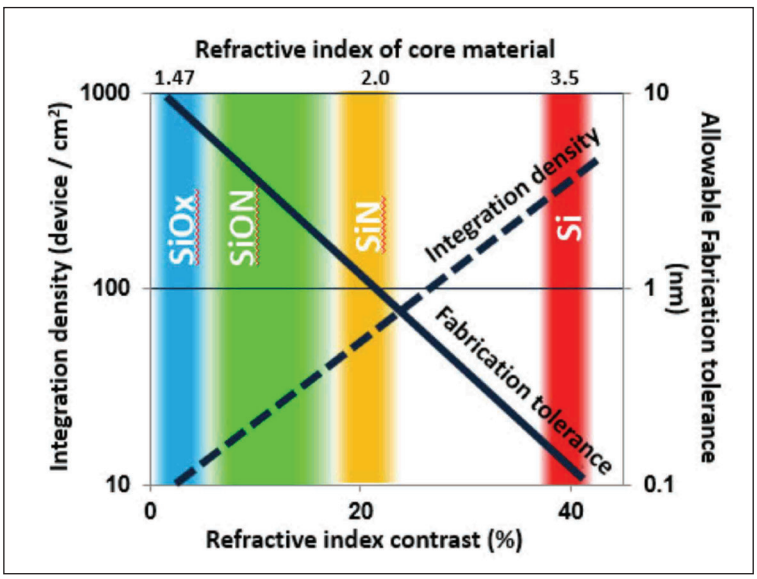

Figure 7: Integration density and fabrication tolerance in AWG wavelength filters. (200 GHz x 16 ch, neighbouring channel crosstalk < -20 dB)

Evolution of silicon photonics

As mentioned, silicon photonics technology provides immediate solutions for data transmission systems in the post-Moore era. However, to deal with the expected increase in traffic in the future, silicon photonics itself must evolve much further. This is because there are serious obstacles to further performance improvement and miniaturisation. One hurdle is the severe fabrication tolerance in silicon photonics, which is a fatal problem. Typical fabrication errors in thickness and width of Si waveguide cores are nanometres in scale. Since a silicon waveguide is very small, such errors can result in large crosstalk and strong polarisation dependence, which significantly degrade performance10.

Nonlinear effects in silicon waveguides are also serious problems in practical applications. Silicon has a large nonlinear coefficient, which is about 100 times larger than that of silica. Moreover, the optical field size in a silicon waveguide is extremely small. Thus, nonlinear effects, such as four-wave mixing and two-photon absorption, are greatly enhanced. The resulting large channel crosstalk and poor power tolerances significantly degrade device performance. Poor carrier mobility in silicon is also a serious obstacle to achieving ultra-high speed device operation of over 40 Gbps.

But what about the end of Moore's Law in silicon photonics? As discussed earlier, Moore's Law in

electronics is ending because device size has reached the wavelength of the de Broglie wave. Referring to Figure 6(a) -- for example -- as an electronic quantum well becomes thinner, the number of energy levels decreases. Eventually, the number is reduced to a single energy level, and this is the end of miniaturisation. The critical thickness is about 10 nm. Any thinner and electron confinement becomes very weak and the device will not work well.

The same analogy is applicable to optical waveguides, as shown in Figure 6(b). In other words, a single-mode waveguide, whose core size is comparable to the optical wavelength, is the end of miniaturisation. Any smaller and photon confinement becomes very weak and the device will not work well. The critical core size is about half of a micrometre for infrared transmission in the 1.55-μm telecommunications band. Since the single mode waveguide has been the most essential element in silicon photonics, Moore's Law has already ended.

Through these discussions, we cannot help but conclude that silicon photonics requires post-Moore technology, and -- we believe -- three approaches in the development of post-Moore electronics can be applied here again for the development of post-Moore silicon photonics technology.

More Moore: further geometrical integration (3D)

For 3D photonic integration, backend photonics is a promising technology. Backend photonics is a performance-assisting technology using additional waveguide systems made of various materials. The requirements for the additional waveguide systems are 1) a low-loss and compact photonics system comparable to the silicon photonics system; 2) functionalities comparable to those in the silicon photonics system; 3) low-loss interlayer coupling between the additional waveguides and silicon waveguides; and 4) the ability to fabricate the additional waveguide system without damaging the silicon photonic system underneath it. In other words, the additional waveguide systems should be constructed by using the backend fabrication technology for silicon semiconductors, which is the reason we refer to the additional waveguide systems as backend photonics.

Silicon-nitride-based materials, such as SiOx, SiON and SiN, are promising for backend photonics. The most attractive feature of these materials is that their refractive index can be largely tuned11. These materials cover a wide refractive index range, and optical waveguides using these moderate-index materials would significantly relax fabrication tolerance. The above chart shows the estimated integration density and fabrication tolerance as a function of refractive index contrast of a waveguide. Using moderate-index materials, fabrication tolerance is significantly relaxed while keeping still high integration density.

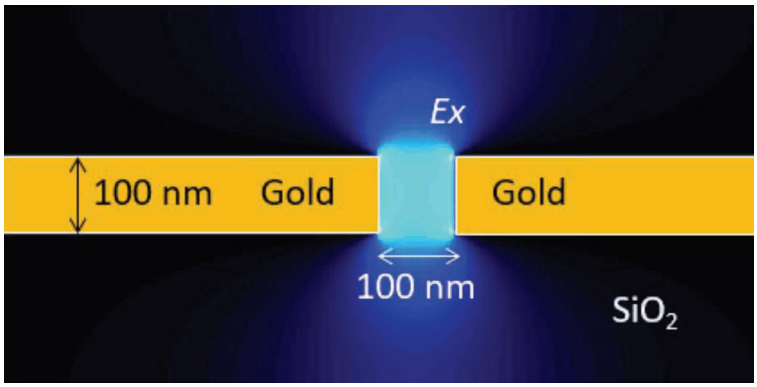

Figure 8: Structure and optical mode field of plasmon waveguide.

Table 1 shows nonlinear coefficients and thermo-optic coefficients of such materials. These coefficients are less than one-tenth of silicon's. Recently, low-loss interlayer coupling structures have been developed using inverted tapers12,13. By using PECVD technology, the deposition temperature can be reduced to less than 350 degC, which would not damage the silicon/germanium devices underneath the additional waveguide system.

This silicon-nitride-based backend photonics technology has been used to develop low-crosstalk high-resolution AWG wavelength filters and integrated them with silicon-based modulators and germanium-based PDs on a silicon photonics platform14, 15.

More than Moore: heterogeneous photonic SoC

The additional waveguide system can integrate various additional photonic functionalities on the silicon photonics platform, because it can increase the degree of freedom in device design. For example, by using silicon-nitride-based waveguides constructed on silicon waveguide systems; polarisation

Silicon-nitride-based materials, such as SiOx, SiON and SiN, are promising for backend photonics. The most attractive feature of these materials is that their refractive index can be largely tuned11. These materials cover a wide refractive index range, and optical waveguides using these moderate-index materials would significantly relax fabrication tolerance

Table 1: Nonlinear and thermo-optic coefficients of Si and backend photonics materials

	Si	SiN/SiON/ SiOx
$n_2 / n_{2(SiO2)}$	175	< 10
γ [$W^{-1}m^{-1}$]	300	< 1.4
β_{TPA} [cm/GW]	0.9	-
dn/dT [$\times 10^{-5}$/°C]	19	1~5

manipulation16, 17 and fibre-mode MUX/DEMUX18, have already been demonstrated. Because of material incompatibilities, these functionalities were constructed outside the silicon photonic chip by using bulky conventional optical components.

Novel-principle devices: restarting Moore's Law

As mentioned above, the core size of a silicon waveguide cannot be reduced to less than a half of the wavelength, and Moore's Law has already ended in silicon photonics. However, we know that radio waves, which have metres of wavelength, can be confined in a centimetre-diameter cable. Radio waves are confined as a TEM-like wave supported by surface electron density waves in metals. Here, recall that the miniaturisation limit of electron density waves is determined by the de Broglie wavelength, which is around 10 nm. Thus, we can restart Moore's Law in photonics. Roughly speaking, a photonic system based on such a metallic confinement is referred to as plasmonics.

The above schematic shows a photonic waveguide based on plasmonics on a Si photonic platform. The optical field is confined in a 100-nm-wide gap between two metallic plates. By filling this gap with electro-optic (EO) polymers and applying voltage to these metallic plates, we can change the refractive index of the EO polymer. Thus, we can construct a very compact optical phase shifter, which is a fundamental element of optical modulators.

Recently, such a plasmonic-polymer waveguide system has been used to develop Mach-Zhender interferometer optical modulators19. Since the gap is very narrow, the electric field in the gap is very strong and the modulation efficiency becomes extremely high. For example, the voltage-length product -- which is a measure of the efficiency of phase shifters -- reaches 0.006 V.cm, which is less than 1/100 of that of a typical silicon modulator. Thus, a device a few tens of micrometres long can function as a modulator with practical modulation depth, and such a small device can operate at very high frequencies of over 100 GHz. Such plasmonic devices would be a significant breakthrough in the post-Moore photonics technology.

Summary

Moore's Law in data transmission systems is nearing its end, and we need post Moore-photonics technology. In the development of post-Moore photonics technology, we can apply the same approaches that have been established in electronics, and silicon photonics can provide immediate solutions for post-Moore photonics technology.

However, we must note here that silicon photonics itself requires post-Moore technology because of the quantum limit in miniaturisation and poor material characteristics. Here again, the same approaches established in electronics are applicable to post-Moore silicon photonics with the help of backend photonics and plasmonics.

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Designing microfabrication **lab equipment** with research flexibility in mind

Optimising R&D labs usually involves vendor collaboration and planning to provide required versatility. Louise Bertagnolli, president of JST Manufacturing explains.

AS RESEARCH becomes more complex, sophisticated cleanrooms have become a virtual necessity for a wide range of cutting edge physical science, material science, and biomedical disciplines.

Due to the financial investment required for such facilities, both university and private R&D laboratories are designed and built to accommodate the needs of a wide range of researchers. This presents a challenge: few administrators have the experience to select and set up lab equipment with the versatility required to serve such a diverse group of users over decades of continually changing research.

Now a growing number of lab administrators are optimising their microfabrication equipment, both for current and future needs, by involving their vendors early in the process. This enables expert planning as well as the selection of standard equipment options that can improve safety, usability, and efficiency while cutting cost.

“Often university lab administrators have never built their own cleanroom before, so they hire an architectural firm to do the design, but are still a little lost on how to lay out the equipment for all the different potential uses,” says Louise Bertagnolli, president of JST Manufacturing. “Because universities are always pushing the boundaries of research, the equipment has to be very flexible so it can be used in ways not even conceived of yet.”

A nationwide manufacturer of manual and automated wet processing equipment, JST’s mechanical, electrical, and chemical engineers have many years of experience in industries including semiconductors, both silicon and compound, MEMS, photovoltaics, LEDs, Flat Panel Displays, and sensors.

Whether for compound semiconductor, nanotechnology, Micro-Electro-Mechanical Systems (MEMS), biophotonics, biomedical electronics, or creating solar power alternatives to traditional silicon wafer construction, much of the advanced research done in labs today requires microfabrication operations.

This typically includes wet processing equipment for metal lift-off, stripping, etching, plating/coating, cleaning, and de-bonding.

Dennis M. Schweiger, Senior Director of Infrastructure at the University of Michigan's Lurie Nanofabrication Facility (LNF), feels that the right combination of user requirements and assistance from the equipment fabricator can make a significant difference in the design, layout, and operation of a wet processing station. The LNF is a world-class facility in all areas of semiconductor device and circuit fabrication, integrated microsystems and MEMS technologies, nanotechnology, nanoelectronics, nanophotonics and nanobiotechnology. The LNF is an open use facility with hundreds of users from various UM departments, as well as many other universities and businesses.

Schweiger states, "Since we essentially rent lab space and equipment to our diverse users, it is important that we provide them with benches that suit their purposes well, from those who are processing wafers to those who may be doing very advanced research or testing on non-wafer components."

We like to give customers added flexibility by programming their equipment to do everything that the equipment is capable of doing. This enables them to dial in applications, such as chemical concentrations. They can also turn various features on or off, depending on your process requirements. Even though they may not need some of the features today, they may want to turn them on in the future, which can be both economical and powerful

According to Bertagnolli, who has guided numerous R&D lab administrators through the equipment design and selection process, the main concern is about setting up the cleanroom and procedures to serve the needs of users, but the process is not always well defined and there are many unknowns.

"When designing and laying out cleanroom equipment, it is important to talk with a vendor or consultant with the experience to help you achieve your evolving research goals," says Bertagnolli. "It is also essential that they help ensure it is correctly set up, that the proper safety, operation, and maintenance procedures are in place, and that lab managers are properly trained to carry these out."

Bertagnolli says that maintaining safety and flexible function for wet processing equipment often requires selecting the most appropriate options from a number of technologies. This may involve various chemistries, temperature controls, chemical baths/dips, ergonomic designs, as well as cleaning, filtration, ventilation, safety, and disposal technologies.

Designing modular and custom parameters

To facilitate the economical design and building of a wet processing equipment solution, many users insist on a standardized approach with customizable features that will best handle their applications parameters.

For example, JST utilizes standard products and standard methodologies to design and manufacture equipment. The equipment is modular by design, allowing for easy changing and reconfiguration should process or product requirements change.

Another powerful feature: each unit is designed with software that is capable of performing all tool functions, including those that are not required. With this, end users can create their own process, or recipes, with all sub-routines at their disposal. "We like to give customers added flexibility by programming their equipment to do everything that the equipment is capable of doing," explains Bertagnolli. "This enables them to dial in applications, such as chemical concentrations. They can also turn various features on or off, depending on your process requirements. Even though they may not need some of the features today, they may want to turn them on in the future, which can be both economical and powerful." Specifying the design parameters for many manual benches may not be as involved as those of automated systems. However, soliciting the opinion of equipment manufacturers regarding equipment design may be highly beneficial.

"Certain processes like etchings and cleanings lab managers will want to be flexible enough to accommodate a wide range of users and projects," says Bertagnolli. "We are often asked for tank construction materials that can withstand several concentrated acids, so part of design flexibility is ensuring you use the most compatible materials for the most acids."

"Another aspect to consider is properly separating, neutralizing, and disposing of all the chemistries involved after use, whether in drains or tanks for treatment or pick up," she adds.

According to Bertagnolli, having the vendor visit the user's facility can contribute to equipment design versatility that can accommodate changes in lab use over the long term.

"An eye toward optimizing working space, operating cost, or maintenance can go a long way toward creating a cleanroom that will serve the user community well now and in the future," says Bertagnolli.

Optimising LNF's Lab

The LNF's Schweiger at the University of Michigan explains that the original equipment design for the new lab areas wet processing benches was very specific, and determined by LNF staff.

"We had looked at it in terms of process flow, from start to finish, not really considering the variety, and variation, of process samples that our user community might be working with, how we'd accommodate non-standard sample sizes, or what the impact might be in total cost of ownership with respect to chemical usage," he says.

Schweiger adds that the some of the new benches had their decks reconfigured once the tools were installed. Several of the earlier benches, some of which were purchased over 20 years ago, were also modified to allow for more flexibility in meeting the process needs of the user community.

"In retrospect, our initial plan for the deck space, and processing capability of the benches, wasn't adaptable or flexible enough, and we worked with JST to implement modifications so that the bench decks were simpler, and could provide more working space," Schweiger concluded.

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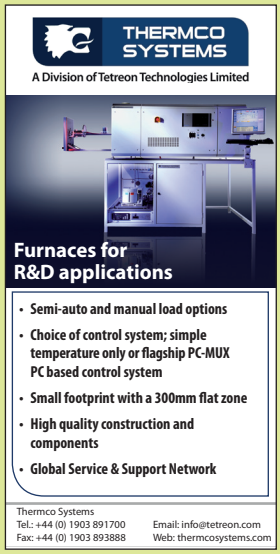

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