SiS SILICON SEMICONDUCTOR
Connecting the Silicon Semiconductor Community

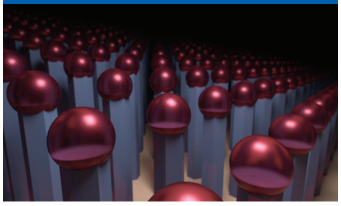
VOLUME 41 ISSUE I 2019 @siliconsemi www.siliconsemiconductor.net

A critical step in wet process cleaning

Invisible materials: on-site bulk gas supply

Realizing the promise of Industry 4.0

The holy grail of nanowire production



Comparing PTFE and PFA fluoropolymers

Dual-Layer Approach Advances WLP Performance

By Brewer Science

inside News Review, News Analysis, Features, Research Review, and much more...
Free Weekly E News round up go to: www.siliconsemiconductor.net

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION


brewer science

editor'sview

By Mark Andrews, Technical Editor

The future of chip design takes another turn

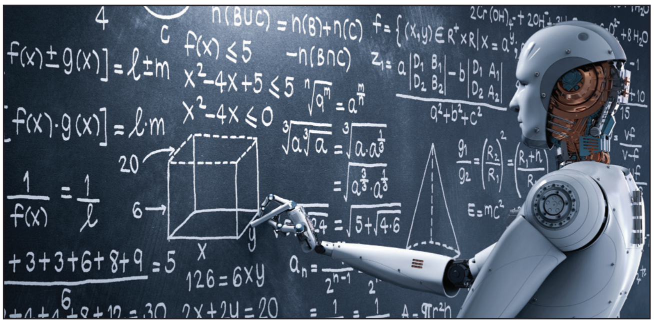
THERE was no formal announcement; no dire analysis; no obituary. But in case you haven't heard, the IoT is 'dead' as the number-one driver of IC development. The new king is AI.

Artificial intelligence (AI) enjoys the limelight amongst major chip houses, independents, and contract manufacturers according to analysts. How did this happen?

According to analyst Kurt Shuler, vice president of marketing at Arteris IP, the IoT was and is a justifiable focus of many silicon and compound semiconductor designers/developers/manufacturers. But as the IoT market has grown from 'emerging' to 'business-as-usual,' AI has demonstrated that it has real horsepower to drive future markets. In a recent study, nearly 83 percent of chip makers expect to focus on algorithm-specific ASICs, ASSPs, or SoCs by 2025. 83 percent!

While this turn of fortunes may surprise, it should be remembered that IoT-targeted chips were being designed into SoCs, MCMs and hybrid systems long before many analysts recognized a trend. Once a trend line emerged it was already peaking.

While the IoT and the IIoT will continue to see growing revenue for software and system level developers, the 'big money' will not be there for chip manufacturers. Intel, TSMC, Globalfoundries, Samsung and other tier-one players are not staking their fortunes on IoT—they expect custom chips using deep-learning algorithms will lead to explosive opportunity.



This edition of Silicon Semiconductor focuses on advanced chip design and solutions for defect elimination. The experts at Brewer Science further their discussion of materials for next generation chips targeting IC makers and display panel manufacturers. Their dual-layer approach facilitates WLP/FOWLP processes while other Brewer Science materials offer new benefits for RDL-first applications.

We also hear from Dr. Jim O'Neill, CTO at Entegris, who discusses the importance of advanced materials and filtration products that take defect elimination to the parts-per-trillion level that industry will need to achieve 7nm and smaller device geometries. Also addressing defect elimination and particle contamination are the experts at Heateflex who have studied the makeup of fluoropolymers, concluding that the reservoirs holding process chemicals may be exasperating the challenges of defect elimination.

Whether the new driver of silicon manufacturing growth is IoT devices, AI-focused ASICs, or something totally unexpected, look to Silicon Semiconductor for insights into critical supply chain issues and innovations. Hear from front-line experts at the PIC, CS and Sensor Solutions International Conference, 26-27 March in Brussels. Visit **https://sensors-international.net/** for more information.

Publisher & Editor Jackie Cannon	jackie.cannon@angelbc.com	+44 (0)1923 690205
Technical Editor Mark Andrews	mark.andrews@angelbc.com	
Sales & Marketing Manager Shehzad Munshi	shehzad.munshi@angelbc.com	+44 (0)1923 690215
USA Representatives Tom Brun Brun Media	tbrun@brunmedia.com	+001 724 539-2404
Janice Jenkins	jjenkins@brunmedia.com	+001 724-929-3550
Director of Logistics Sharon Cowley	sharon.cowley@angelbc.com	+44 (0)1923 690200
Design & Production Manager Mitch Gaynor	mitch.gaynor@angelbc.com	+44 (0)1923 690214
Circulation Director Jan Smoothy	jan.smoothy@angelbc.com	+44 (0)1923 690200
Chief Executive Officer Stephen Whitehurst	stephen.whitehurst@angelbc.com	+44 (0)2476 718970

Directors Bill Dunlop Uprichard – EC, Stephen Whitehurst – CEO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal.

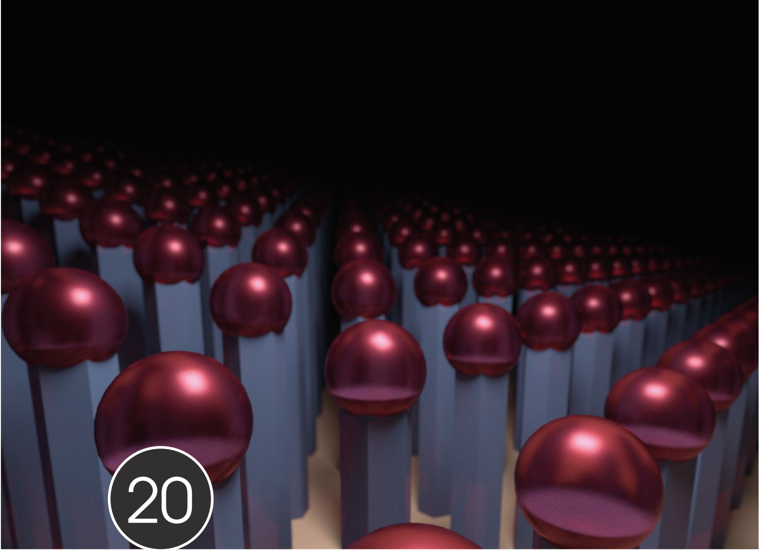
Published by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 F: +44 (0)2476 718 971 E: info@angelbc.com

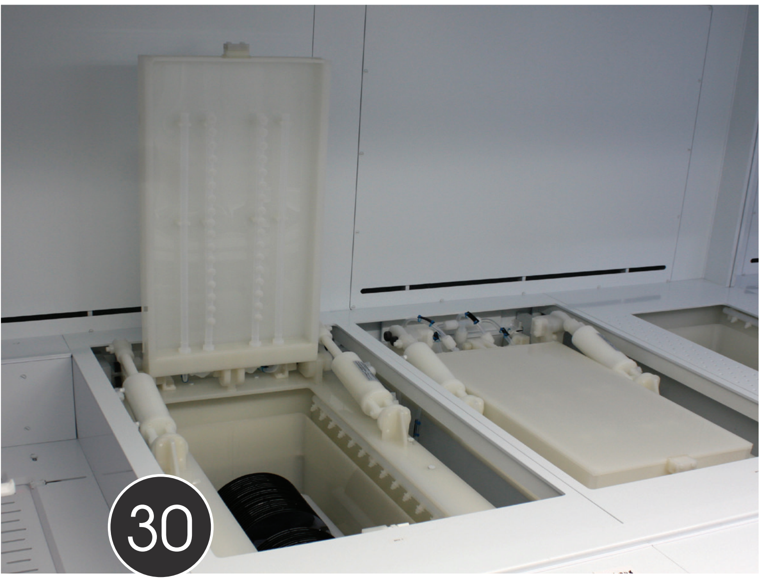
US mailing information: Silicon Semiconductor is published four times a year for a subscription of $90.00 by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts, WD17 1JA, UK. Periodicals postage paid at Rahway, NJ. POSTMASTER: send address changes to: Silicon Semiconductor, c/o Mercury International Ltd, 365 Blair Road, Avenel, NJ 07001.
Printed by: The Manson Group. © Copyright 2019. ISSN 2050-7798 (Print) ISSN 2050-7801 (Online).

VOLUME 41 ISSUE I 2019

CONTENTS

news



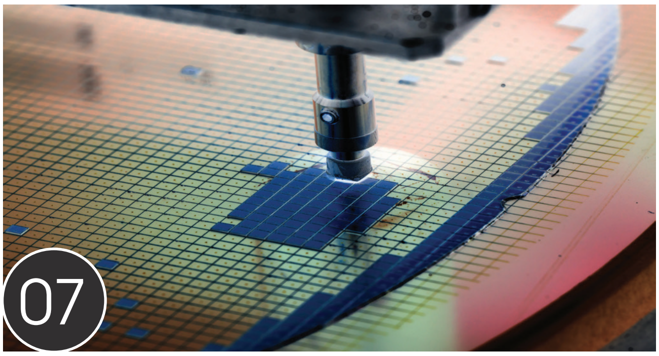


34 Entegris CTO outlines key requirements for realizing the promise of Industry 4.0

Silicon Semiconductor technical editor Mark Andrews recently spoke with Entegris CTO, Dr. James O’Neill, about the expanding role that advanced materials and defect elimination are playing as enablers of Industry 4.0, the ‘Fourth Industrial RevolutionX

40 Comparing PTFE and PFA fluoropolymers as wetted parts in advanced semiconductor manufacturing

Industry experts examining two types of fluoropolymers used to construct semiconductor process chemical containment vessels have concluded that the type of polymer utilized can affect the potential for particle contamination, a concern that grows more critical at each new device node



Critical manufacturing announces significant growth in revenue and MES orders

Critical Manufacturing, a leading developer of innovative, future-ready manufacturing execution system (MES) software, has announced 2018 end-of-year results, achieving 40% revenue growth and a remarkable 65% growth in product orders year over year. Its exceptional performance reflects the readiness of high-tech industries to adopt the huge benefits offered through Industry 4.0 (I4.0), smart factory technology.

Francisco Almada Lobo, CEO at Critical Manufacturing said, "The manufacturing landscape is undergoing significant changes and our MES is an essential element of our customers smart manufacturing strategy. The readiness of our MES for I4.0 makes it a compelling choice which is highly appealing to businesses. It is designed to provide them with a firm foundation and pathway to the huge benefits a smart factory offers in terms of greater efficiency, agility, and increased competitive edge."

The Critical Manufacturing MES has seen great success and growth in its core market segments of electronics, front and back-end semiconductor and medical device manufacturing. The recent strategic investment in the business by ASMPT, the world's largest hardware and software supplier to the electronics manufacturing industry, has further increased Critical Manufacturing's global reach and financial strength.

Almada Lobo continued, "This is a very exciting time for us. Our orders increase means we are already on track for an exceptional 2019 and now, with the investment from ASMPT, we expect our growth and results going forward to be even stronger. We have also invested in our partner network, which is increasing our representation across adjacent industries such as automotive and aerospace. In response to the huge success we experienced last year, we increased our employee count by 30% in 2018 and will continue our expansion in all areas in 2019."

Critical Manufacturing MES is designed from the ground up to be future ready and help businesses reach the full potential of I4.0. The modular system has a wide range of features to match specific customer requirements, is completely flexible and configurable to reduce total cost of ownership and has advanced I4.0 capability.

It offers a complete digital twin of a plant with 3D visualization. It provides decentralized logic to connect with the Internet of Things (IoT) and to seamlessly handle dynamic processing as associated with a smart factory.

Almada Lobo concluded, "Our MES is optimized for global, multi-site manufacturers, an area in which we have had a great deal of success during 2018. We will continue to focus and grow capabilities in our strategic markets and work with our partners to serve new business in adjacent sectors. The unique design and ultimate flexibility of our MES makes it a solid choice to increase efficiency, quality and agility in complex discrete manufacturing industries. It gives businesses the tools they need to meet changing customer demands and compete in the future."

STMicroelectronics reveals motion sensor with machine learning

STMICROELECTRONICS, a global semiconductor company serving customers across the spectrum of electronics applications, has integrated machine-learning technology into its advanced inertial sensors to improve activity-tracking performance and battery life in mobiles and wearables. STMicroelectronics Reveals Motion Sensor with Machine Learning for High-Accuracy, Battery-Friendly Activity Tracking

The LSM6DSOX iNEMO sensor contains a machine-learning core to classify motion data based on known patterns. Relieving this first stage of activity tracking from the main processor saves energy and accelerates motion-based apps such as fitness logging, wellness monitoring, personal navigation, and fall detection.

"Machine learning is already used for fast and efficient pattern recognition in social media, financial modelling, or autonomous driving," said Andrea Onetti, Analog, MEMS and Sensors Group Vice President, STMicroelectronics.

"The LSM6DSOX motion sensor integrates machine-learning capabilities to enhance activity tracking in smartphones and wearables."

Devices equipped with ST's LSM6DSOX can deliver a convenient and responsive "always-on" user experience without trading battery runtime. The sensor also has more internal memory than conventional sensors, and a state-of-the-art high-speed I3C digital interface, allowing longer periods between interactions with the main controller and shorter connection times for extra energy savings.

The sensor is easy to integrate with popular mobile platforms such as Android and iOS, simplifying use in smart devices for consumer, medical, and industrial markets.

Meyer Burger divests its wafering business to Precision Surfacing Solutions

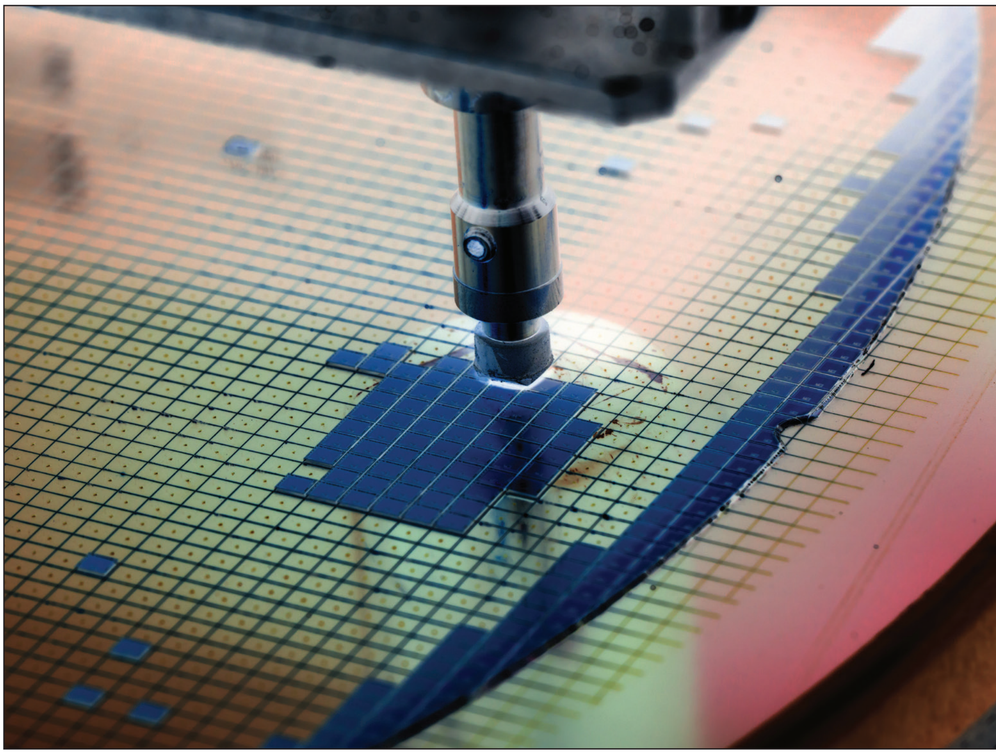
MEYER BURGER TECHNOLOGY has announced that it will sell its photovoltaic and specialised materials (e.g. semiconductor and sapphire glass industries) wafering equipment and service business to Precision Surfacing Solutions (PSS) (formerly Lapmaster Wolters Ltd), a global supplier of equipment and services for surface enhancement technology.

As part of the transaction, significant parts of Meyer Burger's current production facilities in Thun as well as around 100 employees involved in the wafering technology portfolio in Thun and the relevant service locations worldwide will also be transferred to PSS.

Completion of the contract is subject to standard closing conditions. The closing of the transaction is expected to be completed towards the end of the first quarter of 2019. The agreed purchase price is CHF 50 million in cash, which represents approximately one times net sales of the wafering equipment business.

The contract also includes an earn-out component based on certain revenue levels in 2019. Both Meyer Burger and PSS view the transaction as an important strategic milestone, which will further strengthen two global technology leaders.

PSS is a recognized industry leader in the development of technology to produce micron accuracy surface finishes. Under its Lapmaster, Peter Wolters, ELB, Micron, Aba, REFORM, Barnes and Kehren brands, PSS has a proven history of successfully developing cost effective processing solutions for the lapping, polishing, fine grinding, brush deburring, creep feed grinding, bore honing, double disc grinding, buffing through an expanding network of sales and services offices located throughout the world.



PSS is headquartered in Mt. Prospect, IL/USA, employing over 900 people across 13 manufacturing facilities on three continents.

Hans Brändle, CEO of Meyer Burger: "Although Meyer Burger grew from its roots in the wafering industry, our main focus today is on PV cell coating and module connection technologies. As the new owner of our wafering portfolio and with its presence in the semiconductor industry, PSS is ideally positioned to fully maximize the synergies with our wafering technologies. I am very pleased that with PSS as the new owner, we have found a solution that is advantageous for both parties while at the same time securing both jobs and technology know-how in Thun."

Brian Nelson, President & CEO of PSS: "The acquisition of Meyer Burger's wafering technology portfolio will further enable us to strengthen and grow our activities in our key markets. We look forward to maximizing the synergies together with a strong local team and utilizing the potential to relocate additional production activities to the manufacturing location in Thun."

PSS intends to use the know-how of Meyer Burger's local workforce and to continue product development as well as manufacturing activities in non-PV wafering applications in Thun, where it has entered into a long-term rental agreement with Meyer Burger.

Production activities for photovoltaic wafering will remain in China. PSS will further maintain global service support for all current and future wafering customers worldwide. PSS will take over around 70 employees at its Thun location and around an additional 30 globally. The Thun manufacturing location, which is owned by Meyer Burger, is now fully occupied and includes long-term leasing contracts with Precision Surfacing Solutions as well as with 3S Solar Plus AG.

Meyer Burger will further concentrate its strategic focus on the existing cell/module technologies business, especially its successful Heterojunction and SmartWire Connection Technology (SWCT), and on promising next generation cell/module technologies.

VIS to acquire GLOBALFOUNDRIES' Fab 3E in Singapore

VANGUARD INTERNATIONAL SEMICONDUCTOR CORPORATION (VIS) and GLOBALFOUNDRIES (GF) announced that VIS will acquire GF's Fab 3E in Tampines, Singapore. The transaction includes buildings, facilities, and equipment, as well as IP associated with GF's MEMS business.

GF will continue to operate the facility through the end of 2019, providing a transition period to facilitate technology transfers for VIS and existing GF customers. Fab 3E currently manages a monthly capacity of approximately 35,000 8-inch wafers. The transaction amounts to $236 million USD and the transfer of ownership is set to be completed on December 31st, 2019.

VIS and GF have already reached consensus on the transfer of Fab 3E's employees and customers. Both companies believe that employees are the most important assets of a company, so their interests should be put as the first priority during the transition; while ensuring no disruption to customers whose products are in production at the fab. Under this premise, VIS will extend employment offers to all employees currently working at Fab 3E, as well as continuously provide existing customers at Fab 3E with its foundry service, including MEMS customers.

"I appreciate the support of GF's board and management team for this transaction, giving VIS an opportunity to continue expanding its capacity and reinforce momentum for future growth," said Mr. Leuh Fang, Chairman of VIS. "Since its foundation, VIS has already had three separate experiences of successfully transforming a DRAM fab into a foundry fab. We believe this transaction is a win-win for both VIS and GF; and to VIS, it is also a decision that benefits all of our customers, employees, and shareholders.

VIS will uphold its philosophy and principles to continue satisfying customers' demands in capacity and technology, sustaining profitability and growth, and rewarding our shareholders." "This transaction is part of our strategy to streamline our global manufacturing footprint and increase our focus in Singapore on technologies where we have clear differentiation such as RF, embedded memory and advanced analog features," said GF CEO Tom Caulfield. "Consolidating our 200mm operations in Singapore into one campus will also help reduce our operating costs by leveraging the scale of our gigafab facility in Woodlands. VIS is the right partner to leverage the Fab 3E asset going forward."

VIS's capacity has been fully utilized since 2018, and it is in the interests of its customers that VIS expands capacity to meet growing demands. The new fab is expected to contribute more than 400,000 8-inch wafers per year. This acquisition demonstrates the determination and commitment of VIS to accelerate capacity expansion.

Pfeiffer Vacuum introduces turbopumps for HV and UVH applications

PFEIFFER VACUUM has introduced the extremely high compression HiPace 700 H turbopump which is ideal for pumping light gases. With a compression ratio ≥ 2 . 107 for hydrogen, the pump is suitable for generating high and ultrahigh vacuum. Due to the high compression ratio, a low residual gas spectrum is created in the chamber, making it desirable for mass spectrometry applications.

An advanced rotor design gives the HiPace 700 H turbopump an exceptionally high critical backing pressure capability of 22 mbar. This allows the pumps to reach ultrahigh vacuum, even when operating with high backing pressures that occur when paired with diaphragm pumps.

"With the new HiPace H-family, we have the ideal turbopump for research and analytical applications as well as for other industrial applications. In terms of energy efficiency, this product is far ahead. Due to the integrated 'intermittent mode' function, the HiPace H switches a connected backing pump on only if the backing pressure is no longer sufficient. This reduces the energy consumption of the entire vacuum system by up to 90%," said Florian Henss, Product Manager at Pfeiffer Vacuum.

The HiPace 700 H features a robust hybrid bearing design which combines a ceramic ball bearing on the fore-vacuum side with a permanent-magnet radial bearing. As a result, the bearings have a long service life with a service interval of more than four years.

FABU to develop SoCs tailored for autonomous driving

FABU TECHNOLOGY, an artificial intelligence company focused on intelligent driving systems, brings a comprehensive approach to the challenge of developing Advanced Driver Assistance Systems (ADAS) and Autonomous Driving (AD) solutions. With research and development centers in both China and the United States, FABU is committed to developing both a full-stack of algorithm and software infrastructure and a new System-On-Chip (SoC) platform tailored for autonomous vehicles.

The leadership at FABU, which has deep expertise in machine learning, computer vision, robotics, automobile engineering and large-scale integrated circuit design, believe that tackling the challenges of AD requires not only powerful machine learning algorithms but also more efficient and cost-effective hardware performance. Guided by this principle, FABU is the only major AI company in China to build a complete technology solution for autonomous driving. FABU has deployed its autonomous driving technologies on the road. Beginning in 2017, five light trucks outfitted with a FABU Level 4 autonomous driving solution have self-driven a daily 160-mile round trip route on the streets and highways of Zhejiang province in China. The trucks have completed nearly 50,000km/31,000 miles of safety tests in all weather conditions, achieving a camera and sensor perception range of 200 meters/650 feet and obstacle detection accuracy of 97%. In the next phase of road testing, FABU plans to implement their AD technologies in vans and heavy trucks.

Most traditional CPUs and GPUs employed in the AD industry are not optimised for automotive applications. “Generic, off-the-shelf chips may lack the necessary performance, or require too much power, or are not qualified for automotive safety standards,” said Xiaofei He, founder and CEO of FABU. “To best optimise for performance, power, and cost, FABU designs its own dedicated, intelligent SoCs for the ultimate integrated solution for in-vehicle intelligence.”

To meet the specialised data processing requirements of ADAS and AD, FABU has developed a new architecture made-to-order for deep learning and AD algorithms, called the Massive, Parallel and Volumetric (MPV) architecture. The MPV design facilitates creation of large-scale computing modules that provide programmable and resilient architecture support for key AD and ADAS capabilities such as sensor fusion, object identification and tracking, event forecasting and planning. Chips based on the MPV architecture are also optimised for high performance efficiency and low power consumption.

FABU’s Phoenix series of automotive safety integrity level AI chips encompass the full algorithmic requirements of autonomous driving by addressing three stages of AD data processing: sensor input and perception, sensor data integration and fusion, and smart automated decision making.

The key component for the Phoenix-100, the deep learning accelerator, conducts real-time, high precision 3D perception of the environment and was successfully taped out with silicon functionality verified in late 2018. FABU plans to launch its automotive-grade sensor fusion chip Phoenix-200 in 2019 and its Phoenix-300 automated decision-making chip in 2020. By developing and integrating this series of AI chips, FABU will establish a driverless computing platform named The Phoenix, which will extend autonomous driving capabilities from SAE Level 3 to Level 5.

Fraunhofer selects Veeco’s ion beam sputtering technology

VEECO INSTRUMENTS announced that it has shipped its SPECTOR Ion Beam Sputtering (IBS) system and the Sirius Optical Monitor System (OMS) to Fraunhofer Institute for Telecommunications. Fraunhofer, based in Berlin, will use Veeco’s IBS technology to develop and produce laser facet coatings and other micro-optical devices.

“The development of sophisticated micro-optical devices requires exceptional sputtering technology,” said Ms. Greta Ropers, head of backend and packaging group for Fraunhofer. “Veeco’s SPECTOR system, coupled with the Sirius OMS, ensures we are developing and producing world-class devices with the highest throughput and process repeatability on an automated, proven platform.” According to customers, the SPECTOR platform generates the highest quality optical thin films with improved levels of productivity and throughput. Unlike evaporative coatings, ion beam sputtered thin films are deposited at high energies, giving exceptional thickness control and low defect densities for laser coating applications. Veeco’s Sirius OMS significantly enhances the SPECTOR platform capability by coupling cutting edge broadband monitoring control with the inherent stability of ion beam deposited films.

“Fraunhofer Institute for Telecommunications is a recognized worldwide leader in developing next generation laser facet coatings and micro-optical devices,” said Adrian Devasahayam, Ph.D., vice president and general manager of Veeco’s Advanced Deposition and Etch (AD&E) business. “The SPECTOR system sets the standard for precision optical coating thin films by providing unparalleled quality and flexibility that will no doubt accelerate their development goals.”

Funding for this project was granted by Forschungsfabrik Mikroelektronik, a cross-location research factory for microelectronics and nanoelectronics compromised of eleven institutes within the Fraunhofer Group along with the IHP GmbH - Innovations for High Performance Microelectronics and the Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik. For more information, please visit https://www.forschungsfabrik-mikroelektronik.de/en.html.

The system was sold in cooperation with Veeco’s European channel partner, veonis Technologies GmbH.

New imaging technology for high speed analysis

HORIBA Scientific, a global supplier of spectroscopy instrumentation and solutions, announced the release of its new XGT-9000 X-ray analytical microscope (*µ*XRF), which simultaneously performs elemental analysis and optical observation of samples without destroying or contacting them. Incorporating HORIBA's proprietary X-ray technology, with the highest resolution in the world, the XGT-9000 not only screens foreign objects that often cause problems in the production process of lithium-ion batteries, food, cosmetics, and pharmaceuticals, but also analyzes elements in semiconductor integrated circuits and other micro objects. It also measures film thickness and adherence amounts with a high degree of accuracy.

By integrating the features of a high-resolution microscope and high-intensity X-ray beams, the XGT-9000 performs non-destructive foreign-object analysis on samples, switching between high-speed analysis mode for rapid screening of foreign objects, and detailed analysis mode using the micro beams first incorporated in earlier models.

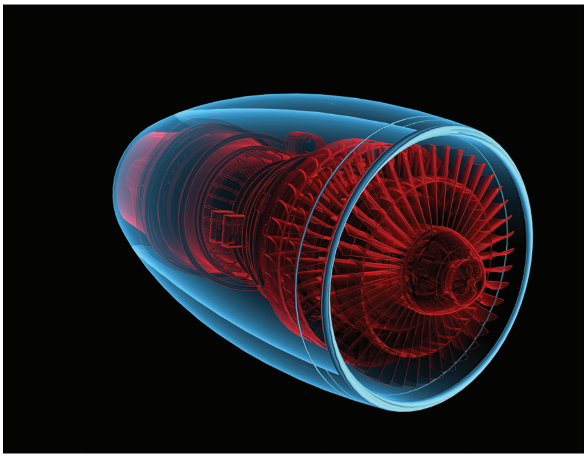
The XGT-9000 is equipped with three types of optical illuminations: bright field coaxial, dark field, and transmission. Combining bright field coaxial and dark field illuminations enables clear observation of the samples with flat or uneven areas, such as semiconductor wafers and films.

The XGT-9000 offers highly accurate and fast foreign-object analysis, enabling it to detect both visible foreign objects and invisible ones down to only several microns (= 1/1,000 millimetre) in size. Seeing these single foreign objects with the high definition optical images can prevent degraded performance, appearance and quality or serious mechanical failure.

Irradiating X-rays coaxial with optical observation images enables pinpoint analysis with no misalignment. High-definition optical images improve the visibility of foreign objects, which until very recently, have been hard to observe. Other improvements include shortened analysis time, enhanced mapping and image processing, as well as ease of combination with other analysis equipment. The software package includes quantitative and qualitative chemical analyses, thickness determination and image analysis features.

"This instrument is ideal for foreign object analysis in foods and pharmaceuticals," said Dr. Sergey Mamedov, Raman and XRF Applications Scientist at HORIBA Scientific. "This analyzer is also being used to increase efficiency in R&D and quality control within a broad range of fields, including failure analysis of large printed circuit boards, non-destructive analysis of metal materials, measurement of film thickness, and adherence amounts on increasingly miniaturized semiconductor integrated circuits and connecting electrodes."

ZEISS 3D X-ray imaging solutions for advanced packaging failure analysis



ZEISS has unveiled a new suite of high-resolution 3D X-ray imaging solutions for failure analysis (FA) of advanced semiconductor packages, including 2.5/3D and fan-out wafer-level packages. The new ZEISS systems include the Xradia 600-series Versa and Xradia 800 Ultra X-ray microscopes (XRM) for submicron and nanoscale package FA, respectively, as well as the new Xradia Context microCT. With the addition of these new systems to its existing family of products, ZEISS now provides the broadest portfolio of 3D X-ray imaging technologies serving the semiconductor industry.

“Throughout its 170-year history, ZEISS has pushed the frontiers of scientific research and advanced the start-of-the-art in imaging technologies to enable new industrial applications and technological innovations,” stated Dr. Raj Jammy, president, ZEISS Process Control Solutions (PCS) and Carl Zeiss SMT, Inc. “Now more than ever in the semiconductor industry, where package as well as device features are shrinking in all three dimensions, new imaging solutions are needed to quickly isolate failures in order to enable higher package yields. We are extremely pleased to announce this trio of new 3D X-ray imaging solutions for advanced semiconductor packaging, which provides our customers with a powerful high-resolution toolset to improve their failure analysis success rates.”

As the semiconductor industry approaches the limits of CMOS scaling, semiconductor packaging needs to help bridge the performance gap. To continue producing ever-smaller and faster devices with lower power requirements, the semiconductor industry is turning to package innovation through 3D stacking of chips and other novel packaging formats. This drives increasingly complex package architectures and new manufacturing challenges, along with increased risk of package failures. Furthermore, since the physical location of failures is often buried within these complex 3D structures, conventional methods for visualizing failure locations are becoming less effective. New techniques are required to efficiently isolate and determine the root cause of failures in these advanced packages. To address these needs, ZEISS has developed a new suite of 3D X-ray imaging solutions that provides submicron and nanoscale 3D images of features and defects buried within intact structures in advanced package 3D architectures. This is enabled by rotating a sample and capturing a series of 2D X-ray images from different perspectives, followed by reconstruction of 3D volumes using sophisticated mathematical models and algorithms. An unlimited number of virtual cross-sections of the 3D volume may be viewed from any angle – providing valuable insight of failure locations prior to physical failure analysis (PFA). The combination of submicron and nanoscale XRM solutions from ZEISS provides a unique FA workflow that can significantly enhance FA success rates. ZEISS’s new Xradia Context microCT offers high contrast and resolution in a large field of view, using projection-based geometric magnification, and is fully upgradable to.

Xradia Versa.
Xradia 600-series Versa is the next generation of 3D XRM for non-destructive imaging of localized defects within intact advanced semiconductor packages. It excels in structural and FA applications for process development, yield improvement and construction analysis. Based on the award-winning Versa platform with Resolution at a Distance (RaaD) capability, Xradia 600-series Versa offers unsurpassed performance for high-resolution imaging of larger samples at long working distances to determine root causes of defects and failures in packages, circuit boards and 300 mm wafers. It can easily visualize defects associated with package-level failures, such as cracks in bumps or microbumps, solder wetting problems or through silicon via (TSV) voids. The 3D visualization of defects prior to PFA reduces artefacts and guides cross-section orientations, leading to improved FA success rates.

Features include:
Xradia 800 Ultra brings 3D XRM to the nanoscale realm, producing images of buried features with nanoscale spatial resolution while preserving the volume integrity of the region of interest.

Applications include process analysis, construction analysis and defect analysis of ultra-fine-pitch flip chip and bump connections – enabling process improvement for ultra-fine-pitch package and back-end-of-line (BEOL) interconnects. Xradia 800 Ultra enables visualization of the texture and volume of solder consumed by intermetallic compounds in fine-pitch copper pillar microbumps. Defect sites are preserved during imaging, enabling targeted follow-up analysis by a variety of techniques. The construction quality of blind assemblies, such as wafer-to-wafer bonded interconnect and direct hybrid bonding, can be characterized in 3D.

Features include:
Xradia Context microCT is a new submicron-resolution 3D X-ray microCT system based on the Versa platform. It is designed for high-resolution imaging of packages at short working distances with high throughput.


AP&S
AP&S

Dual-layer approach
advances WLP performance

Improvements across the advanced packaging landscape have already addressed many performance requirements for reducing total thickness variation (TTV) and warpage while lowering costs and improving throughput. A major hurdle remains: extreme temperature survivability. According to Brewer Science experts, winning this advanced packaging 'last frontier' requires a dual-layer approach.

THE DRIVE TO CREATE next-generation electronic devices begins with a sound foundation. While the largest IC makers are pushing CMOS scaling to 7 nm and below, other advanced circuit manufacturers are taking a different route to high performance, including the adoption of 2.5D/3D architectures that reduce footprints while increasing speed and functionality.

Manufacturers have succeeded in dramatically reducing TTV and warpage with high throughput and lower costs by utilizing various wafer thinning and materials technologies that support an assortment of packaging platforms. Wafer-level chip-scale packaging (WLCSP) is attractive due to its ability to deliver high performance at low cost. But since it utilizes a 'substrateless' package, applications can be limited due to die size. Alternatively, fan-out wafer-level packaging (FOWLP) technology is being widely developed because input/output (I/O) density can be increased by fanning out interconnects to external pad locations, thereby achieving a smaller form factor (and/or smaller footprint) with decreased power consumption.

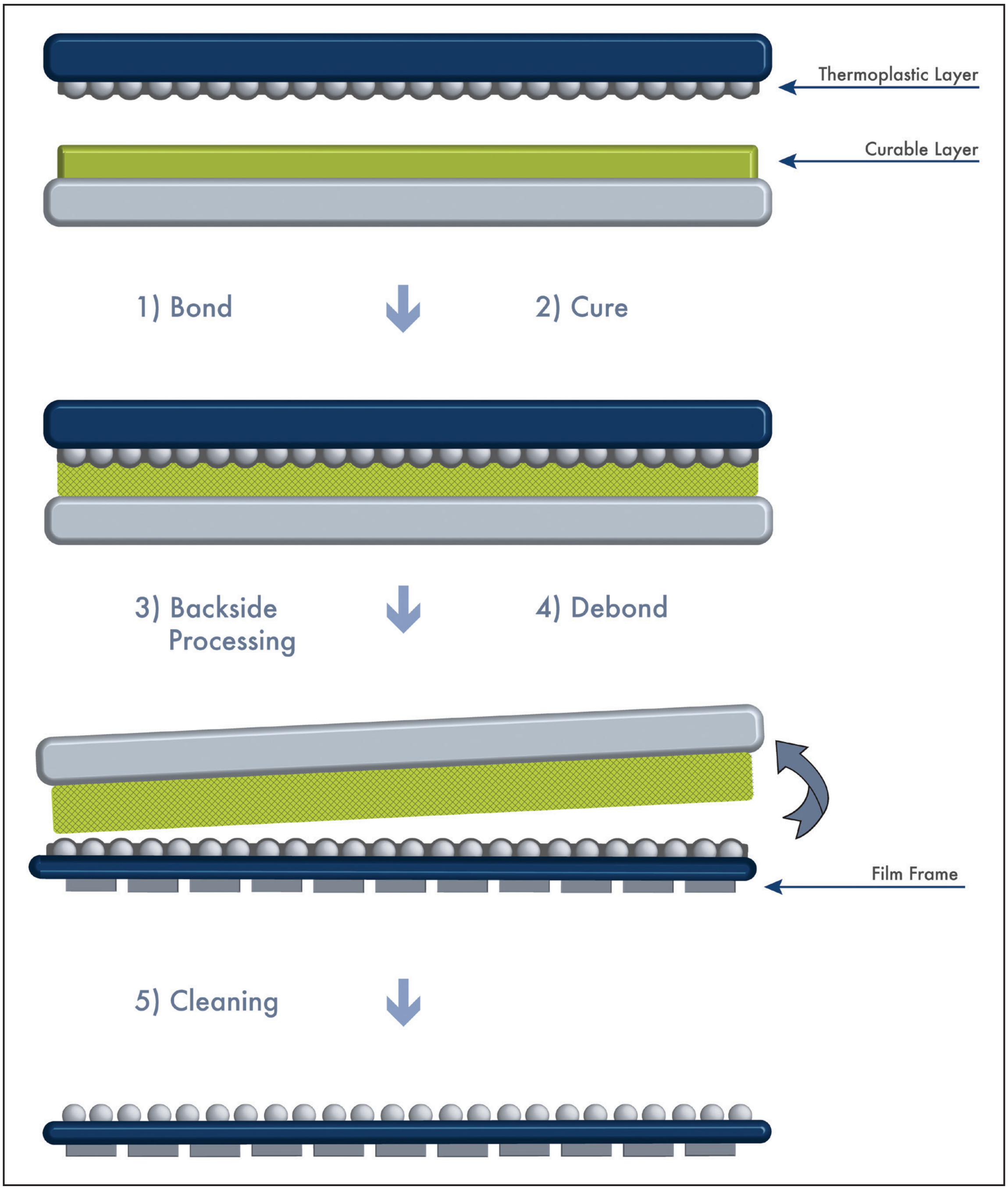
The next big hurdle for advanced packaging—some say the most challenging—is maintaining state-of-the-art performance, stability and throughput while adding the ability to withstand high-temperature annealing and deposition steps. This is complicated by the industry's need to thin wafers to a much greater degree than was utilized in older-generation devices. Today's wafers are often thinned to well below 30 μm. Processing such thin, brittle wafers ultimately requires a carrier system for handling high-value substrates through subsequent downstream processes that include high-temperature anneal and deposition steps.

Handling thinned substrates is a major challenge within semiconductor manufacturing. Silicon wafers less than 50 μm thick or those with redistribution layers (RDLs) created using an RDL-first process are delicate and expensive to manufacture. Safe handling necessitates the use of support substrates and processing steps that utilize temporary bonding and debonding (TBDB) materials designed to enable complex packaging infrastructures.

Temporary bonding materials created using high-viscosity, low-T_g thermoplastic polymers are commonly used in TBDB processes. When paired with a supportive carrier, these materials offer thermo-mechanical stability and easier handling of the thin device substrate. While the extensive selection of TBDB materials offered by Brewer Science supports many bonding/debonding techniques (mechanical, laser, chemical and so forth) the introduction of


brewer science
r science

Figure 1: The Brewer Science TBDB process flow in typical WLP/FOWLP applications



higher-temperature steps can cause these materials to behave more like a liquid; as a result, temporarily bonded wafers lose mechanical stability as melt viscosity decreases. This allows some material to soften, weakening bond line stability.

Deformation and delamination of the device wafer can occur at higher temperatures, which leads to downstream processing issues. Brewer Science takes the extra steps needed to provide customers a TBDB system that eliminates common material failure points.

Solutions for any WLP approach

Advanced packaging techniques are designed around either a 'chip-first' or 'chip-last' process sequence.

While chip-first has its advantages, it also uses die that are untested, which can reduce final yield. In chip-first processes, singulated die are placed onto a substrate that has been process coated with temporary bonding material or thermal release tape (TRT) prior to being encapsulated with epoxy mold compound (EMC) in a thermocompression process.

But high-temperature dielectric processing induces stress and leads to warp between the carrier wafer and EMC, which can decrease yield and device performance. Die shift and die stand-off due to substrate warpage and bonding material softening during EMC processing creates RDL misalignment to the embedded die.

In a chip-last process flow, glass carrier wafers are coated with a removable laser release material that creates a foundation for building the RDL. The laser release material needs to possess good thermal, mechanical and chemical stability to survive thinning as well as backside dielectric and deposition processes.

Both chip-first and chip-last process flows require the use of high-temperature and high-vacuum steps to create the RDLs. Today's FOWLP processes require materials that can survive high temperatures and harsh chemical environments while maintaining mechanical stability.

BrewerBOND materials for FOWLP

Brewer Science has released two new lines of products to support rigorous advanced packaging requirements. Introduced at SEMICON Taiwan in late 2018, the BrewerBOND® T1100 and C1300 series materials deliver next-generation bonding system performance that enables high throughput as well as high thermal stability. The materials also provide room temperature bonding and debonding for both wafer-level and panel-level processing. These two advanced materials support wide-ranging manufacturing requirements, enabling more uniform post-grind thicknesses of <50 μm while also enabling device structures (and the temporary bond) to survive heat treatment under vacuum. Figure 2 shows a scanning acoustic microscope (SAM) image of a bonded wafer pair after thinning with a 30-minute 400°C heat treatment under vacuum, providing a defect-free bond line without damage to the device.

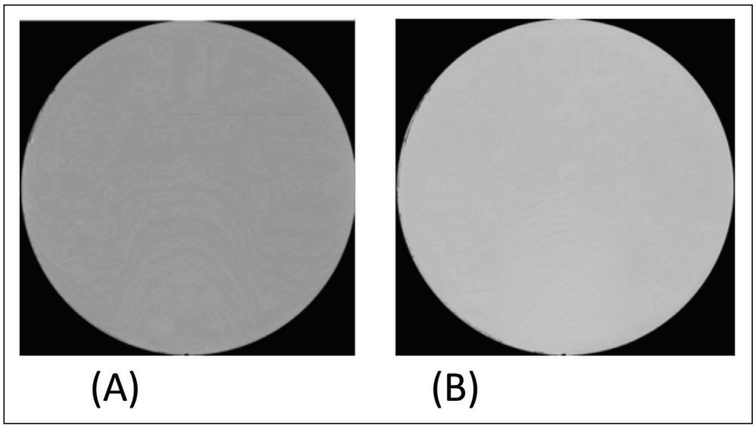


Figure 2: Images from a scanning acoustic microscope shows (A) no heat treatment and (B) after heat treatment

According to Kim Yess, Brewer Science Technology Director for Wafer-Level Packaging Materials, the dual-layer approach of the BrewerBOND materials series has key advantages compared to materials with less complex or less capable formulations.

"The BrewerBOND T1100 series materials are designed to conformally bond to device structures; the materials have specific rheology attributes for exceptional coating and protection of device structures. The BrewerBOND C1300 series material is a curable thermoset layer that remains malleable until final cure," she said.

Yess explained that the dual layer system is comprised of a low-T_g thermoset material (BrewerBOND C1300) applied to a carrier. This assembly is then bonded to the device wafer that has been processed with the corresponding high-T_g bonding material (BrewerBOND T1100) that coats device structures. After bonding and processing at room temperature, the pair can then either be UV exposed or hotplate baked to cure the thermoset material. When processed below 350°C, the BrewerBOND T1100 series material remains solvent-soluble and has little to no melt flow up to 300°C. When coated, this material is highly conformal and even when applied thinly it can cover severe topography. Figure 3 shows a scanning electron microscope (SEM) cross-section of a 2.15 μm film of BrewerBOND T1100 series material processed over 80 μm solder bumps.

Yess explained the exceptional performance achieved by their dual-layer approach was developed by Brewer Science to optimize the coatings' most essential qualities while making various application steps fit into typical process flows at high throughput levels. (See Table 1 for key materials properties.)

"The BrewerBOND T1100 and C1300 materials need each other to perform to their optimal potential. The BrewerBOND T1100 material is thinner, relatively speaking, and more conformal, which manufacturers need to address ever-shrinking device geometries. It also enables easier downstream cleaning of the device. BrewerBOND C1300 material creates better stability at higher temperature processes, which

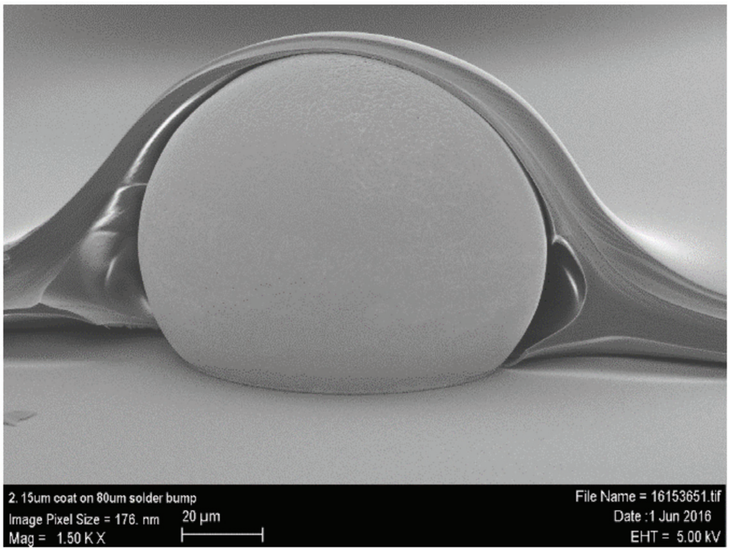
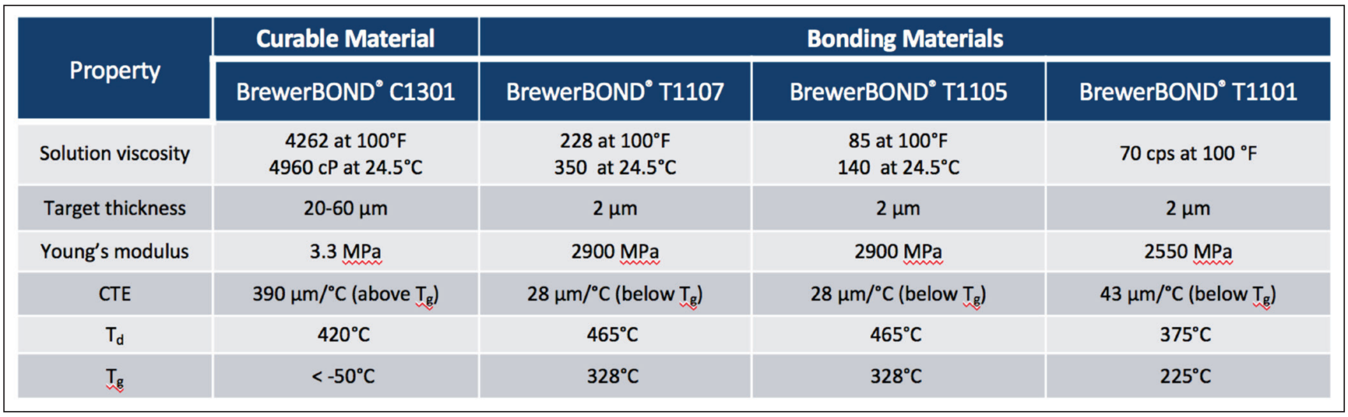


Figure 3: The BrewerBOND T1100 material delivers highly conformal coating and adhesion preperties



Property	Curable Material	Bonding Materials		
	BrewerBOND® C1301	BrewerBOND® T1107	BrewerBOND® T1105	BrewerBOND® T1101
Solution viscosity	4262 at 100°F 4960 cP at 24.5°C	228 at 100°F 350 at 24.5°C	85 at 100°F 140 at 24.5°C	70 cps at 100 °F
Target thickness	20-60 µm	2 µm	2 µm	2 µm
Young's modulus	3.3 MPa	2900 MPa	2900 MPa	2550 MPa
CTE	390 µm/°C (above T_g)	28 µm/°C (below T_g)	28 µm/°C (below T_g)	43 µm/°C (below T_g)
T_d	420°C	465°C	465°C	375°C
T_g	< -50°C	328°C	328°C	225°C

Table 1: Properties of BrewerBOND advanced materials

reduces warpage and helps ensure post-processing functionality of the devices being packaged," she said, noting that using the BrewerBOND C1300 material by itself would only do part of the job.

"Manufacturers are building up device layers at nanometer scale much the way we might build a much larger structure: one layer or 'floor' at a time. It's a bit like using concrete when building a home. If you put concrete directly on some structures going into the home it would be hard to clean and would likely damage the most sensitive structures. But by using the right coatings, semiconductor manufacturers can achieve the stability and temperature resistance they need at nano scale while still retaining the ability to remove coatings when needed simply by using industry-standard cleaning processes and chemicals," she explained.

BrewerBUILD materials advance RDL-first applications

Designed specifically for RDL-first applications, BrewerBUILD™ materials are single-layer, high-absorbing materials for buildup and assembly; they are designed for use in laser ablation processes. These materials have increased absorbance at wavelengths between 308 and 355 nm and offer increased protection to the device wafer during laser ablation. This new generation of materials also offers strong solvent resistance and high adhesion to many materials and they respond very efficiently to solvent cleaning after ablation.

"The BrewerBUILD family of materials addresses pain points experienced by customers associated with RDL-first applications. This technology is designed to optimize dielectric materials for RDL layers, resolving features down to 2 µm, offering higher I/O density for advanced packaging architectures. The material is designed to address challenges that include bridging the gap in the available I/Os at both die and board levels, high performance requirements, integration and form factor demands from end users, as well as design and process complexity of fan-out packages," Yess stated.

"In order to maximize KGD and minimize yield loss, BrewerBUILD materials can be coated at the wafer and panel levels, and provide in-process thermal and mechanical stability," she explained. "These benefits extend to polyimide (PI) cure and molding. The materials deliver strong adhesion to metals such as Ti and Cu as well as polymers including PI; the materials provide excellent chemical resistance, too."

"BrewerBUILD materials enable excellent laser debonding, featuring high light absorption to protect device wafers from laser damage. There is also low to no carbon residue after laser debonding, which enables easier cleaning and better levels of carrier reclamation," she stated.

Summary

Brewer Science brings high level materials expertise to advanced packaging that is paving the way for innovation through the use of new temporary bonding/debonding materials that uniquely support FOWLP technology requirements. When combined into a system, BrewerBOND dual layer materials impart improved mechanical stability that reduces the hazards of handling thinned, bonded wafers that need to undergo high-vacuum or high-temperature processing. The materials' conformal nature, room-temperature bonding/debonding characteristics and chemical resistance provide added value and improved performance while reducing cost of ownership.

For RDL-first packaging processes, BrewerBUILD materials support build-up and assembly, offering a better alternative to thermal release tapes. These new materials facilitate low-energy laser debond processes that deliver improved protection for the device wafer with low carbon residues. As packaging techniques continue to evolve, geometries shrink even further and 3D device structures capture increasingly larger shares of overall semiconductor production, count on Brewer Science to develop and deliver advances in bonding and debonding materials to facilitate manufacturers' requirements. Brewer Science supports next-generation FOWLP technology and is formulating new materials to support emerging device packaging innovations now under development.

CONNECT
COLLABORATE
INNOVATE

Connect with the leaders in Semiconductors, MEMS, Sensors, Flexible Electronics, Packaging, Advanced Materials, 3D, and Design and Manufacturing. SEMI gathers the global electronics manufacturing supply chain in large, medium and intimate events. Join our expositions or conferences and take your business to the next level.

SEMICON® CHINA
FPDCHINA

SEMICON® EUROPA

SEMICON® JAPAN

SEMICON® KOREA

SEMICON® SOUTHEAST ASIA

SEMICON® TAIWAN

SEMICON® WEST

MEMS & SENSORS Technical Congress®

MEMS & SENSORS Executive Congress®

European MEMS & SENSORS Summit

ISS INDUSTRY STRATEGY SYMPOSIUM **AMERICAS**

ISS INDUSTRY STRATEGY SYMPOSIUM **EUROPE**

ASMC ADVANCED SEMICONDUCTOR MANUFACTURING CONFERENCE

SMC SEMICONDUCTOR MATERIALS CONFERENCE **AMERICAS**

SMC SEMICONDUCTOR MATERIALS CONFERENCE **KOREA**

ITPC INTERNATIONAL TRADE PARTNERS CONFERENCE

2019 **FLEX** U.S.

2019 **FLEX** Japan

2019 **FLEX** Taiwan

2019 **FLEX** Korea

2019 **FLEX** China

2018 **FLEX** Europe be flexible

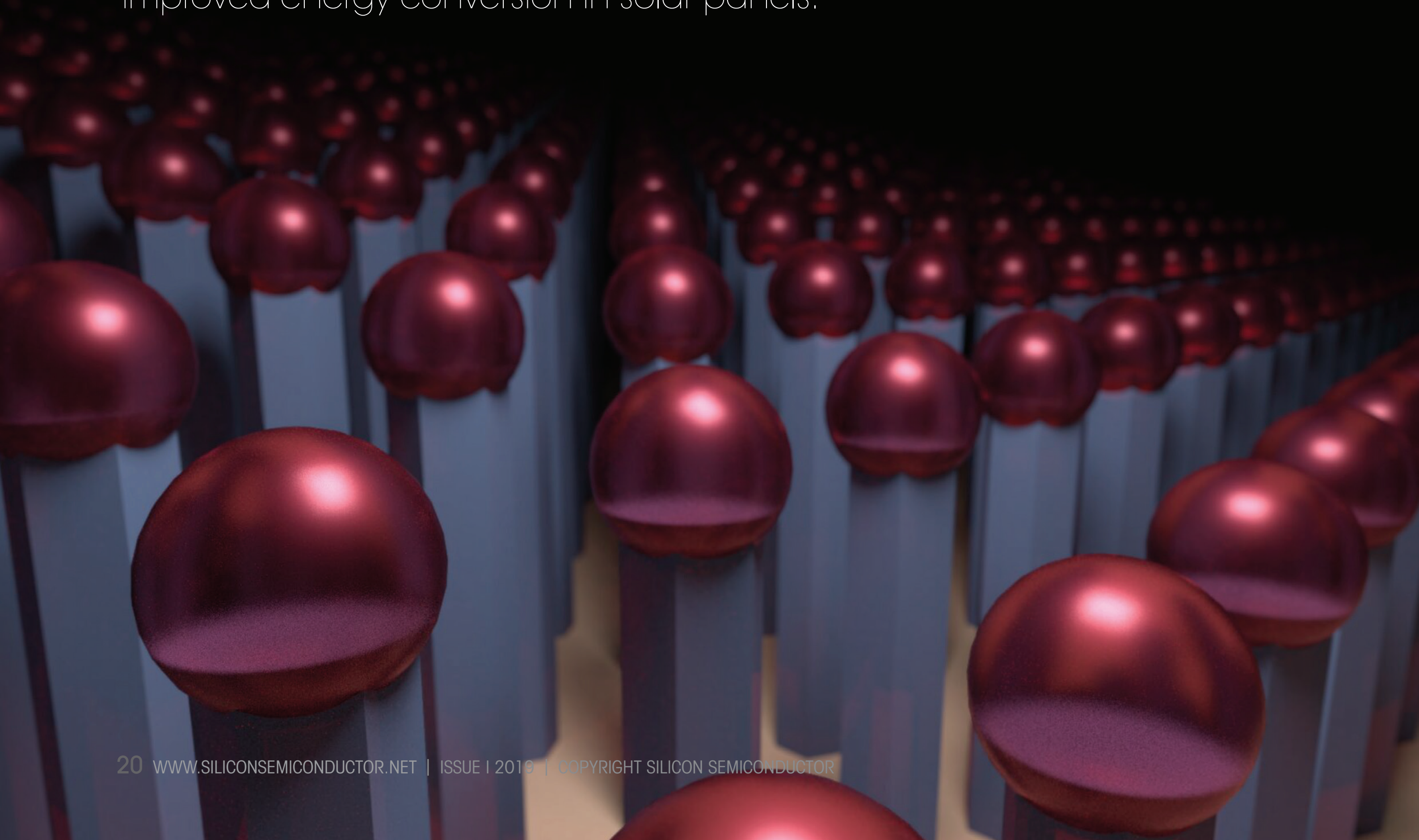
semi™

Visit www.semi.org/events

AMERICAS • CHINA • EUROPE • JAPAN • KOREA • SOUTHEAST ASIA • TAIWAN

The holy grail
of nanowire production

The École polytechnique fédérale de Lausanne (EPFL) is a research institute and university in Lausanne, Switzerland, specializing in the natural sciences and engineering. EPFL researchers have found a way to control and standardize the production of nanowires on silicon surfaces. This discovery could make it possible to grow nanowires on electronic platforms, with potential applications including the integration of nanolasers into electronic chips and improved energy conversion in solar panels.



Left: Two different configurations of the droplet within the opening – hole fully filled and partially filled and bellow illustration of GaAs crystals forming a full ring or a step underneath the large and small gallium droplets.

The standard process for producing nanowires is to make tiny holes in silicon monoxide and fill them with a nanodrop of liquid gallium. This substance then solidifies when it comes into contact with arsenic. But with this process, the substance tends to harden at the corners of the nanoholes, which means that the angle at which the nanowires will grow can't be predicted. The search was on for a way to produce homogeneous nanowires and control their position

NANOWIRES have the potential to revolutionize the technology around us. Measuring just 5-100 nanometres in diameter (a nanometre is a millionth of a millimetre), these tiny, needle-shaped crystalline structures can alter how electricity or light passes through them.

They can emit, concentrate and absorb light and could therefore be used to add optical functionalities to electronic chips. They could, for example, make it possible to generate lasers directly on silicon chips and to integrate single-photon emitters for coding purposes. They could even be applied in solar panels to improve how sunlight is converted into electrical energy.

Up until now, it was impossible to reproduce the process of growing nanowires on silicon semiconductors – there was no way to repeatedly produce homogeneous nanowires in specific positions. But researchers from EPFL's Laboratory of Semiconductor Materials, run by Anna Fontcuberta i Morral at the School of Engineering, together with colleagues from MIT and the IOFFE Institute, have come up with a way of growing nanowire networks in a highly controlled and fully reproducible manner. The key was to understand what happens at the onset of nanowire growth, which goes against currently accepted theories. Their work has been published in *Nature Communications.*

"We think that this discovery will make it possible to realistically integrate a series of nanowires on silicon substrates," says Fontcuberta i Morral. "Up to now, these nanowires had to be grown individually, and the process couldn't be reproduced."

The standard process for producing nanowires is to make tiny holes in silicon monoxide and fill them with a nanodrop of liquid gallium. This substance then solidifies when it comes into contact with arsenic. But with this process, the substance tends to harden at the corners of the nanoholes, which means that the angle at which the nanowires will grow can't be predicted. The search was on for a way to produce homogeneous nanowires and control their position.

Research aimed at controlling the production process has tended to focus on the diameter of the hole, but this approach has not paid off. Now EPFL researchers have shown that by altering the diameter-to-height ratio of the hole, they can perfectly control how the nanowires grow. At the right ratio, the substance will solidify in a ring around the edge of the hole, which prevents the nanowires from growing at a non-perpendicular angle. And the researchers' process should work for all types of nanowires.

"It's kind of like growing a plant. They need water and sunlight, but you have to get the quantities right," says Fontcuberta i Morral.

This new production technique will be a boon for nanowire research, and further samples should soon be developed.

References

J. Vukajlovic-Plestina, W. Kim, L. Ghisalberti, G. Varnavides, G. Tütüncuoglu, H. Potts, M. Friedl, L. Güniat, W. C. Carter, V. G. Dubrovskii, A. Fontcuberta i Morral, Fundamental aspects to localize self-catalyzed III-V nanowires on silicon, Nature Communications

Invisible materials:

on-site bulk gas supply to semiconductor and display fabs

Cost-effectively ensuring a supply of bulk gases at sufficient purity is essential for every semiconductor and display panel fabricator. The experts at Linde Electronics discuss the reasons for this.

By David Pilgrim, VP Business Development, Electronics, Asia Pacific and Dr. Paul Stockman, Head of Marketing, Linde Electronics

WHAT MATERIAL is produced on demand, delivered continuously with 99.9999999% purity, and is equivalent in weight to 500 elephants per day, but is never seen? The gaseous nitrogen delivered to a 3D NAND fab.

Nitrogen is just one of the bulk gases which are essential at every process step and tool for semiconductor and display manufacturing. As a category, they are often the largest bucket of material spend after silicon wafers. Not only are they physically invisible, they are ubiquitously available throughout the fab, and easily overlooked. Adjacent to every major fab is a bulk gas supply facility, which is constructed in parallel with the main fab shell, and which needs to be qualified and ramped before the first tool moves into the building.

In this article, we begin by discussing the commonly supplied bulk gases at semiconductor and display fabs, their applications, and their sources and supply options. Following, we describe the infrastructure required for the supply, and give an overview of the project steps to build this key facility.

Bulk gases, applications, and supply options

In addition to water, bulk gases are the simplest molecules used in electronics manufacturing. And like water, they are piped throughout the fab to be available in almost utility-like supply. First, we look at six gases that are commonly produced for many different industrial processes, but which receive

	Nitrogen (N_2)	Oxygen (O_2)	Argon (Ar)	Hydrogen (H_2)	Helium (He)	Carbon dioxide (CO_2)	Bulk special gases: Ammonia (NH_3) Hydrogen chloride (HCl) Nitrogen trifluoride (NF_3) Nitrous oxide (N_2O) Silane (SiH_4)
Primary applications	Inerting and purging	Oxidation reactions for deposition and etch	Plasma and high-temperature inerting	Annealing, epitaxy, deposition, and etch	Cooling, plasma,and carrier gas	Cleaning, immersion lithography, and DI water conditioning	Deposition, etch, epitaxy, and chamber cleaning
Sources	Air separation	Air separation	Air separation	Hydrocarbon steam reforming or electrolysis	Extraction from natural gas deposits	By-product from production of ammonia, fertilizers, refineries, bakeries, and fermentation	Chemical synthesis
Typical supply volume [Nm^3/h]*							
3D NAND [300 kwspm]#	80,000 - 100,000	2,000 – 3,000	50 - 100	200 - 400	50 - 150	25 - 50	varies
Leading-edge foundry [60 kwspm]#	30,000 - 50,000	200 - 300	150 - 250	500 – 1,500	25 - 50	100 - 200	varies
Supply options							
On-site generation or pipeline	●	●	●	●			
Bulk delivery + tank	●	●	●	●		●	
ISO container					●	●	●

* Normal cubic meters per hour

\# 000's of wafer starts per month

Table 1. Bulk gas applications, sources, and supply.

special production or purification for electronics-grade use. In addition, we include five ESGs (electronic special gases), which are produced by chemical synthesis and used in such large volumes that bulk supply and delivery methods apply.

Bulk gases and applications

Nitrogen (N_2): Ultra-high purity nitrogen is required during fab construction as the first infrastructure pipes and tubes are being welded together to exclude oxygen, moisture, and particles from the future supply to production tools. Eventually, nitrogen is fed to every tool as part of the overall process flow, which keeps the semiconductor wafer free of all contaminants, from incoming inspection to final qualification.

Nitrogen is used to purge any ingressed air and residual process chemicals, and to keep the wafer and all production wetted surfaces and spaces free from oxygen, moisture, and particles. Nitrogen is also used to purge vacuum pumps, which need a constant gas flow even when the tools are idle, and abatement equipment, which could be subject to pyrophoric conditions if air were present. Along with oxygen and argon, nitrogen is obtained by separating air into these three primary components.

Oxygen (O_2): Ultra-high purity oxygen is used as a direct oxidizing agent to grow silicon oxide layers, and in more complex deposition and etch steps as a co-reactant. In addition, industrial grade oxygen is supplied to the abatement equipment as an oxidizer to turn reactive waste gases into less hazardous and more easily removed compounds.

Argon (Ar): Argon is used primarily to support plasmas for deposition and etch reactions. It is also used in deep UV (ultra-violet) lithography lasers and as a specialized cryogenic cleaning agent.

Hydrogen (H_2): Hydrogen is used for epitaxial deposition of silicon and silicon germanium and for annealing of oxidized surfaces. More recently, it is also

Scale, purity, reliability, cost. All of these are factors which have driven the supply of bulk gases to the level of requirement today.

used in high volume as a cleaning agent to remove tin from the light sources of extreme UV lithography tools.

Hydrogen is obtained either by the catalyzed reaction of hydrocarbons with water, which is referred to as reforming, or by the electrolysis of water. Traditionally supplied by truck to the fab as a bulk gas or liquid, leading-edge fabs with high hydrogen demands can benefit from on-site production.

Helium (He): Helium is the second lightest element and coldest liquid and is used in electronics manufacturing at hundreds of points in the fab for back-side wafer and load lock cooling, plasma processing, and leak detection. While helium is the second most abundant element in the universe, it is relatively spare on earth: produced as a by-product of nuclear decay of heavy elements in the Earth's crust, it accumulates in the same geological deposits as natural gas.

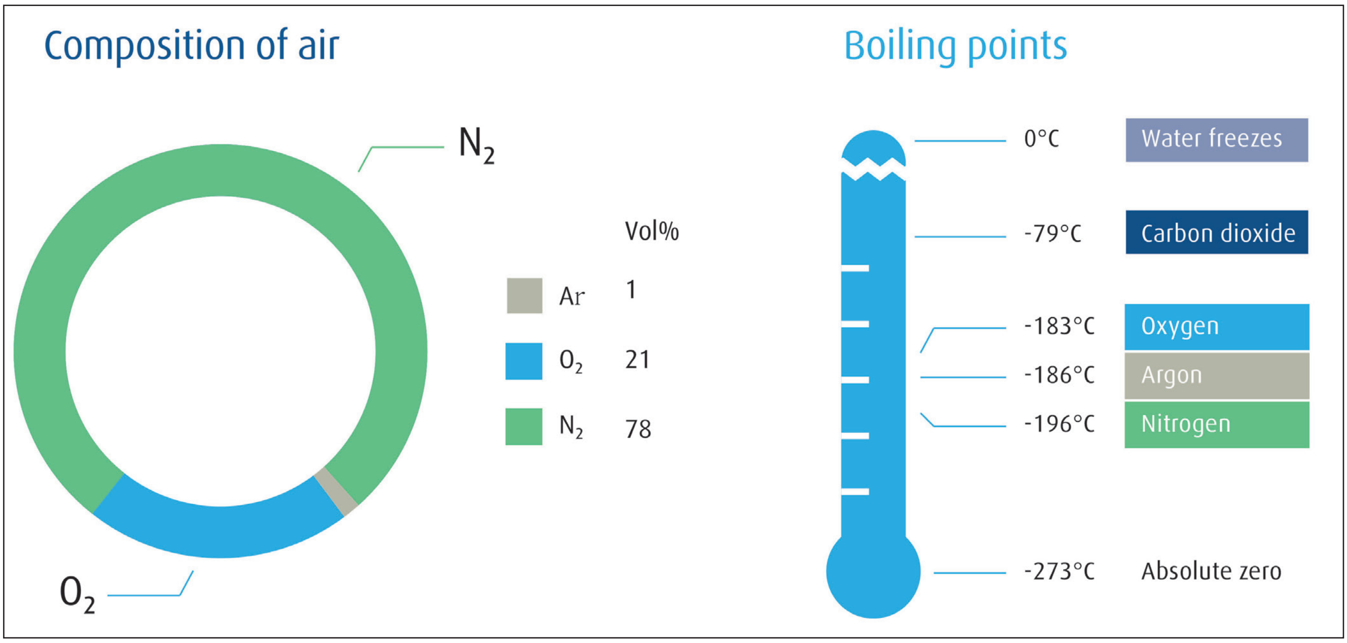
However, only a few such natural gas deposits have sufficient amounts of helium to make it economically viable for separation, purification, and supply. It is liquefied to -269°C and shipped around the globe in vacuum-jacketed containers, often taking several months to deliver from the point of production to the point of use.

Carbon dioxide (CO_2): Two applications predominate for CO_2 at leading-edge fabs. Immersion lithography tools employ a thin layer of water between the final optical lens and the wafer surface to create a sharper focus of the light and enable smaller features. CO_2 is added to water to displace dissolved nitrogen, which can create microscopic bubbles that distort the intended patterning.

Small amounts of CO_2 are also added to the ultrapure DI (deionized) water in some fab applications to increase the conductivity of the water and thereby safely dissipate any electrical charges that can attract small particles. CO_2 is obtained as the by-product from industrial production of ammonia, fertilizers, and hydrocarbons, and can also be captured from the production of hydrogen by steam reforming. Special care is required to ensure the purity and consistency of CO_2 supplies to the semiconductor industry.

Bulk ESGs – Ammonia (NH_3), Hydrogen chloride (HCl), Nitrogen trifluoride (NF_3), Nitrous oxide (N_2O), and Silane (SiH_4): ESGs were originally supplied to fabs in individual gas cylinders. Now, the size and intensity of leading-edge fabs, in terms of wafers under production and number of process steps, has grown the demand for these five important gas-phase chemicals to such large volumes that they need to be supplied to fabs in ISO containers to sustain supply chain logistics and economies of scale. Other than SiH_4, which is shipped as a compressed gas, these materials are delivered to the fab site as pressurized liquids, and then vaporized before distribution to the points of use. They are primarily

Figure 1.
Bulk gas supply components



Truck + bulk

On-site production

Pipeline

ISO containers

Figure 2. Volume and distance determine the most economical supply modes

obtained from chemical synthesis of industrial chemical feedstocks and further purified. NF_3 is the exception: it is made and used almost exclusively as a material for electronics manufacturing.

Supply options

Scale, purity, reliability, cost. All of these are factors which have driven the supply of bulk gases to the level of requirement today. Below, we sketch the choices available to deliver bulk gas materials to optimize these four variables.

- **Air separation:** This is the primary set of processes used to obtain nitrogen, oxygen, and argon from the air. Moisture, carbon dioxide, and other impurities are firstly removed from the air by chemical absorbers. The air is then cooled by successively compressing and expanding it until it turns into a liquid, which is then distilled into these three components. Electronics-grade air separation units can produce these gases to >99.999999% purity. Because argon makes up only 1% of air by volume, it is often not economically sensible to produce with smaller plants.
- **Liquid vs gas:** It takes about three times as much electricity to produce these products in final form as liquids compared to the gas phase. For gases made on-site, it is therefore most economical to produce most of them as gases which are supplied on-demand immediately to the fab, with a small portion liquefied for storage and redundant supply.

Air compressor

Cold box

Cryogenic liquid tank

Vaporizer

Remote operating center

ISO container

Figure 3. Bulk gas supply components

- **Truck delivery + bulk tank:** The economies are different for products delivered by truck. Because gases are much less dense than liquids, it would take five trucks to deliver the same amount of gas-phase product as one truck of liquid-phase product. The cost of transportation is therefore the overall cost driver; products are liquefied for transportation and then vaporized on-demand for use.
- **On-site production:** Scale is the determiner for on-site production vs. truck delivery. For nitrogen, almost all 300 mm fabs and new display fabs operate at scales which require on-site production of nitrogen: to reduce cost, to ensure robust supply, and to produce to the highest and most consistent purity standards. Often, the demand for ultra-high purity oxygen requires an on-site plant to achieve the required purity specifications. And at leading-edge semiconductor plants, the use of epitaxial processes and the adoption of EUV lithography are twin drivers affecting consideration of on-site hydrogen production.
- **Pipeline:** In certain locations, fabs are co-located into clusters or science parks. This allows for even greater economies of scale, as a pipeline can network the supply from larger gas plants to multiple customers.
- **Redundant supply:** Regardless of the primary supply, electronics production requires extremely high guarantees of supply; therefore, redundant sources and supply schemes must be put in place. Most often, this means having one or more qualified remote sources, as well as liquid storage on-site equivalent to several days of production demand.
- **Integrated supply:** As leading-edge fab demands go ever higher, more options become available for further cost reduction. A good example of what can now be achieved is the Linde SPECTRA® I integrated production on-site nitrogen, oxygen, and argon generator. Not all the nitrogen and oxygen used at the semiconductor fab needs to be the highest purity: some of this gas is going directly to vacuum pumps and abatement equipment downstream of wafer processing equipment. The SPECTRA I on-site gas generator allows a customized blend of production of both ultra-high purity and technical grade nitrogen and oxygen as well as ultra-high purity argon, thereby satisfying a large portion of the high-volume gas requirements from a single plant.
- **Purification and analysis:** Because nitrogen, oxygen, argon, hydrogen, and helium are used in many different processes throughout the fab, including those most sensitive to contamination and chemical reaction, these materials are often further purified. Already produced with only part-per-billions impurities, on-site purifiers ensure these levels are reduced to consistent part-per-trillion levels.
- **ISO containers:** ISO containers, short for the International Organization of Standardization intermodal containers, are the largest supply container options for bulk gases and ESGs. These are designed to fit standard distribution requirements on truck trailers, rail cars, and container ships. For liquid products with extremely low boiling points, these are vacuum jacketed to preserve cryogenic product temperatures and extend the shipping times. Once on-site, dedicated supply bays with distribution manifolds connect them with the fab.

Project scope and execution

Scope

While there are many options available to semiconductor manufacturers with respect to bulk gas installations, the primary driver is correctly sizing the demand. Adequate supply must be available for the fab, but without excess, so that cost is optimized. Once demand is calculated, two other major project requirements can be determined: land and utilities. Below, we examine these three factors in more detail.

- **Demand**: Well-established manufacturers have existing fabs and processes from which they adapt

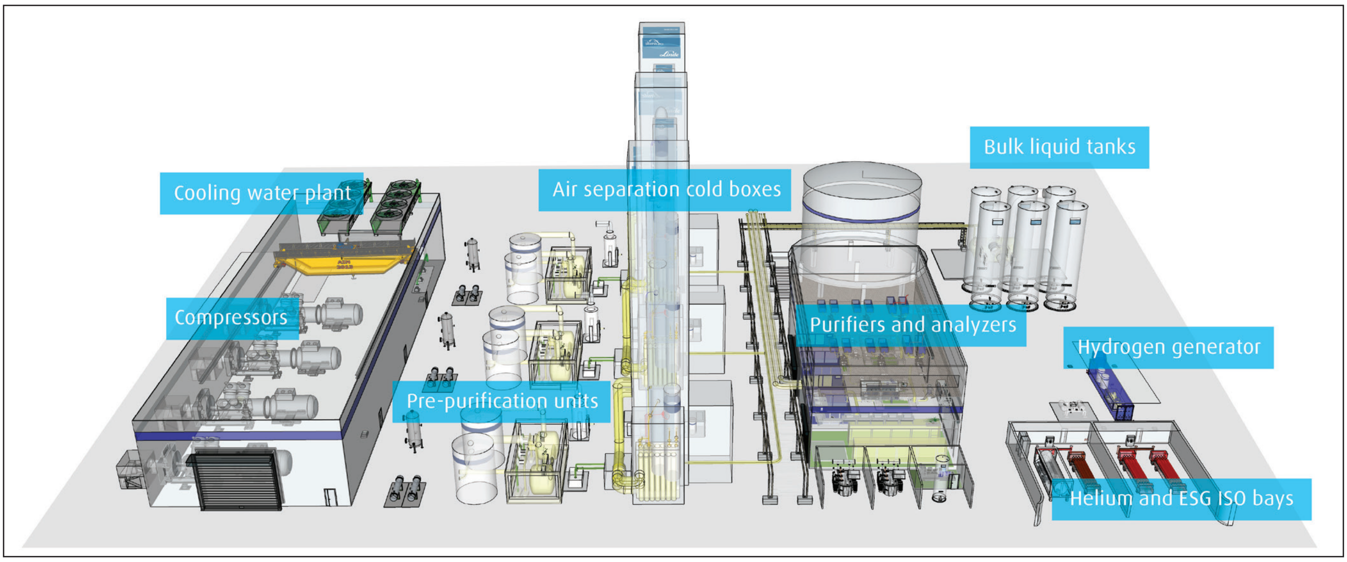
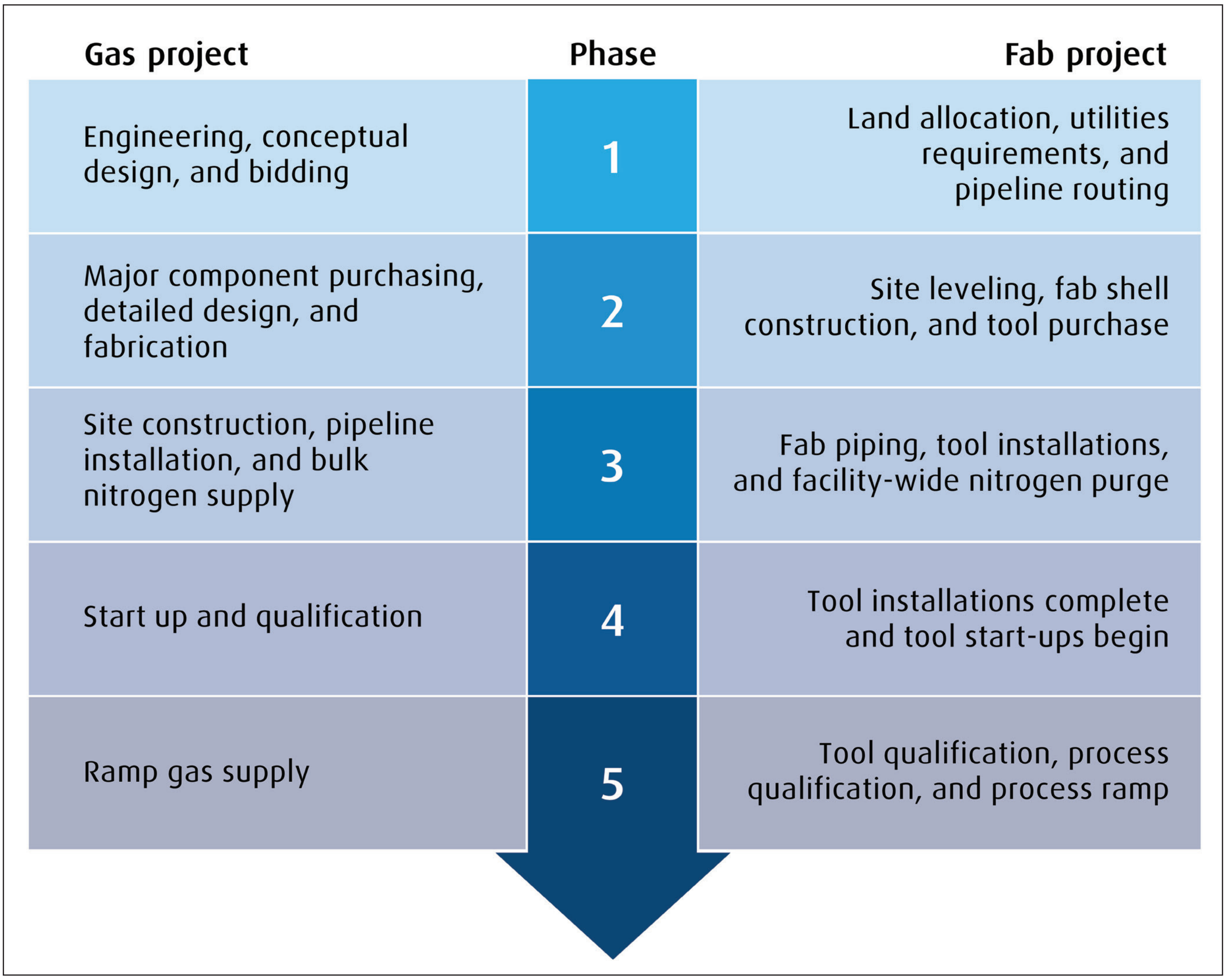


Figure 4. Gas yard layout



Gas project	Phase	Fab project
Engineering, conceptual design, and bidding	1	Land allocation, utilities requirements, and pipeline routing
Major component purchasing, detailed design, and fabrication	2	Site leveling, fab shell construction, and tool purchase
Site construction, pipeline installation, and bulk nitrogen supply	3	Fab piping, tool installations, and facility-wide nitrogen purge
Start up and qualification	4	Tool installations complete and tool start-ups begin
Ramp gas supply	5	Tool qualification, process qualification, and process ramp

Figure 5.
Bulk gas supply
project timeline

and scale the gas demand and purity requirements for new fabs. New manufacturers, or those with new processes, need to make estimates based upon OEM recommendations and engineering models. In addition to average demand, peak demand – associated with recovery from an unplanned shutdown – must be calculated. Lastly, redundancy and back-up storage requirements are added. The aggregate demand and purity determine cost, and drive the optimized equipment solution.

- **Land:** Once the equipment solution is determined, the footprint of land can be calculated. The manufacturer will need to include this in their overall land requirement. The gas yard can be contiguous to the fab site, or can be located on a separate parcel several kilometers distant. However, higher delivery pressures and larger pipeline diameters are needed the greater the separation of generation and use. Equipment plus land are the major capital expenses of the project.
- **Utilities:** The equipment solution will also determine the utility requirements, which are primarily electrical power, water, and potentially natural gas for hydrogen generation. These, too, must be determined and included in the overall utility supply to the fab site.

Major components

Next, we will introduce the components of the gas yard that determine the overall footprint.

- **Compressors:** These are the mechanical workhorses of liquefying and separating air. By compressing air, which is later expanded, the air is reduced in temperature until it liquefies.
- **Cooling water:** A cooling water plant is needed to keep the temperature of the compressors within operating requirements.
- **Pre-purification units:** Air contains moisture and carbon dioxide, along with more trace impurities. Adsorber-based purifiers remove these ahead of the cooling stage to avoid freezing and blocking of the air flow.
- **Cold box:** This insulated, high-profile structure is the tallest and most prominent component on site, and is where the key liquefaction and distillation equipment is housed.
- **Bulk tanks:** Bulk gas tanks hold both liquefied gas produced on-site as well as intermediate storage for

other gases brought to the site as liquids.

- **Vaporizers:** While these materials are most economical to ship and store as liquids, they are distributed and used in the fab as gases. Vaporizers are heat exchangers, which use heat from the ambient air or external sources to boil liquefied products to gases.
- **Purifiers:** As discussed earlier, further purification is applied to these gases. These purifiers are catalysts and activated metals which remove residual impurities. They can be sited in the gas yard and/or the customer fab.
- **Analyzers:** Throughout the production process flow, bulk gases are measured to ensure they are at expected purities and the process is in control. Analyzers that deliver such high sensitives must be housed in climate-controlled rooms.

Execution: General timeline

Finally, we give a general timeline for bulk gas projects to show the correlation with the overall fab project, and to illustrate the importance of advanced planning to ensure the necessary supply of gas materials the fab when required. This timeline begins after the manufacturer has determined its process flows and tool requirements. Planning and construction timelines vary depending on the size, scope, location, and scale of the project.

- **Phase 1:** The manufacturer kicks off the bidding process by providing gas demand and purity requirements to gas suppliers. These in turn make their engineering and conceptual designs to determine their own equipment requirements. In feedback to the manufacturer, these help in the specification of the total land and utility needs.
- **Phase 2:** After the bid is awarded, the gas supplier begins purchasing major components, and moves to detailed design and fabrication. The manufacturer is preparing the site, including the gas yard, constructing their fab facility, and placing tool orders.
- **Phase 3:** The gas supplier begins its construction project. The first two installations are the bulk nitrogen supply tank and the pipelines connecting the gas supply to the fab. At the end of this phase, the two projects are linked: bulk (trucked in) nitrogen begins to supply the fab shell to purge the piping of the facility and the first tools are installed.
- **Phase 4:** At the completion of the gas yard fabrication, the on-site generators are started up and qualified. The bulk gas and back-up supply chains begin. In the fab, tool installations are completed and tool start-ups begin.
- **Phase 5:** The fab continues its project with tool qualification, then process qualification, and finally begins its process ramp. This increasing activity raises the gas demand, and the gas supply ramps in response.

Summary

Bulk gases are a significant portion of supply spend for semiconductor and display fabs. Effective supply often requires on-site production, storage, and distribution. These facilities are built concurrently with the fab, and the first qualified gas deliveries are made as soon as the fab shell is complete.

Because of the magnitude of the project in terms of land allocation, utilities infrastructure, and capital spend, bulk gas suppliers work with electronics manufacturers from the inception of new projects to properly size, equip, and execute bulk gas facilities to supply and ramp the project. From the first patents and equipment for the liquefication and separation of air over 120 years ago to the largest and most efficient plants today, Linde plc is a leader in providing customers the products and solutions they need. Linde Engineering designs, fabricates, and executes facilities for the production of nitrogen, oxygen, argon, hydrogen, helium, and carbon dioxide, with thousands of plants in operation around the world. Linde owns and operates many of these plants for customers, including leading semiconductor and display manufacturers. Notably, it has pioneered the science park model of supplying many customers and fabs with collective production in places such as Taiwan, South Korea, Malaysia, and mainland China. And it supplies the world with helium from a diverse portfolio of sources and supply chain investments.

> Because of the magnitude of the project in terms of land allocation, utilities infrastructure, and capital spend, bulk gas suppliers work with electronics manufacturers from the inception of new projects to properly size, equip, and execute bulk gas facilities to supply and ramp the project.

Precision drying:

A critical step in wet process cleaning

Working with an expert can help to optimize essential drying variables such as level of cleanliness, drying speed, and adjustments for product geometry

CLEANING, an integral part of many manufacturing and maintenance processes is often critical to the performance of a broad range of technologies in the semiconductor, defense, MEMS, photonics and biotech industries.

In this case, "cleaning" refers to the use of agents such as solvents, acids or bases to remove unwanted particulates and other contaminates from products ranging from optics to semiconductor and electronic devices.

It also refers to the etching process utilized in semiconductor fabrication, where the "cleaning" is the precision removal of thin layers of material.

In both cases, the "wet process" cleaning involved usually incorporates the chemical cleaning agents, an appropriate rinse bath, and a method of drying the material.

However, while attention is typically focused on the chemicals used, along with time, temperature and agitation, matching precision drying to the cleaning process and even customizing it is an essential element that must be considered. In this effort, partnering with an expert can help to fine tune certain critical variables such as level of cleanliness and drying speed as well as any required adjustment for product geometry.

"You can wash to clean or etch but rinsing the entire chemical off and then drying is just as critical as the wash itself," says Louise Bertagnolli, president of JST Manufacturing (Boise, ID), a specialist in wet processing and precision cleaning equipment.

Selecting a drying process

There are many types of drying that can be incorporated into the cleaning process depending on the goal, according to Bertagnolli.

"Consideration must be given to the key factors in the drying process," says Bertagnolli. "This can be the final cleanliness of the surface with low residual particle counts, drying time, or a combination of both. The drying should be geared to do the most effective job based on your criteria."

While convection drying, N2 blowoff, and HEPA drying are sufficient for many applications, they may not be the best choice for those where low particle counts are important.

With convection drying, the drying chamber is heated to evaporate the water off the product, and hot, filtered nitrogen or clean dry air can assist the drying. While low cost, this can leave behind residue and water spots as the water evaporates. Depending on the volume of water, this can take a long time. The process is not suitable when a clean dry is required

> Utilizing a STG dryer, the chamber is filled with water and then IPA vapor is slowly introduced into the chamber as the water is removed, replacing the water with IPA. The IPA is then evaporated. The process has several advantages. There is no water spotting and no moving parts to generate particles.

or when products are temperature sensitive. In an N2 blowoff dryer approach, nitrogen is blown into the drying chamber through high pressure air knives. The moisture is blown off the product and down into the plenum where it is evacuated in the exhaust stream. Although the process is initially lower in cost, it uses a lot of nitrogen, may not totally dry product, and does not work with geometries that retain moisture when removed, including those with blind holes.

With a HEPA filtered blowoff dryer, hot clean air is blown through a HEPA filter and into the drying chamber where it evaporates the moisture. Once again, though the operational cost is low, it may not totally dry product, and does not work well with moisture retaining geometries.

To leave the least amount of particles, such as for silicon wafers, glass substrates, disc drives, or optics, Bertagnolli recommends either a Surface Tension Gradient (STG) Dryer or a closed loop isopropyl alcohol (IPA) vapor vacuum dryer.

Utilizing a STG dryer, the chamber is filled with water and then IPA vapor is slowly introduced into the chamber as the water is removed, replacing the water with IPA. The IPA is then evaporated. The process has several advantages. There is no water spotting and no moving parts to generate particles. It uses relatively little IPA and is environmentally friendly with low IPA emissions. The process, however, dissolves IPA in the water and drains it out. It also uses a large amount of deionized water for rinsing.

With a closed loop IPA vapor vacuum dryer like JST's CLV model, ultra clean vapor is generated and then introduced into a sealed drying chamber. The closed loop system allows fresh IPA vapor to rinse the surface to be dried, penetrating the surface areas and absorbing the moisture. A low pressure vacuum pulls any remaining moisture from the sealed chamber and away from the product being dried.

This process has a number of advantages. It offers the cleanest dry with no moving parts to generate particles. It dries blind holes and eliminates water spotting. It is also environmentally friendly with low IPA emissions.

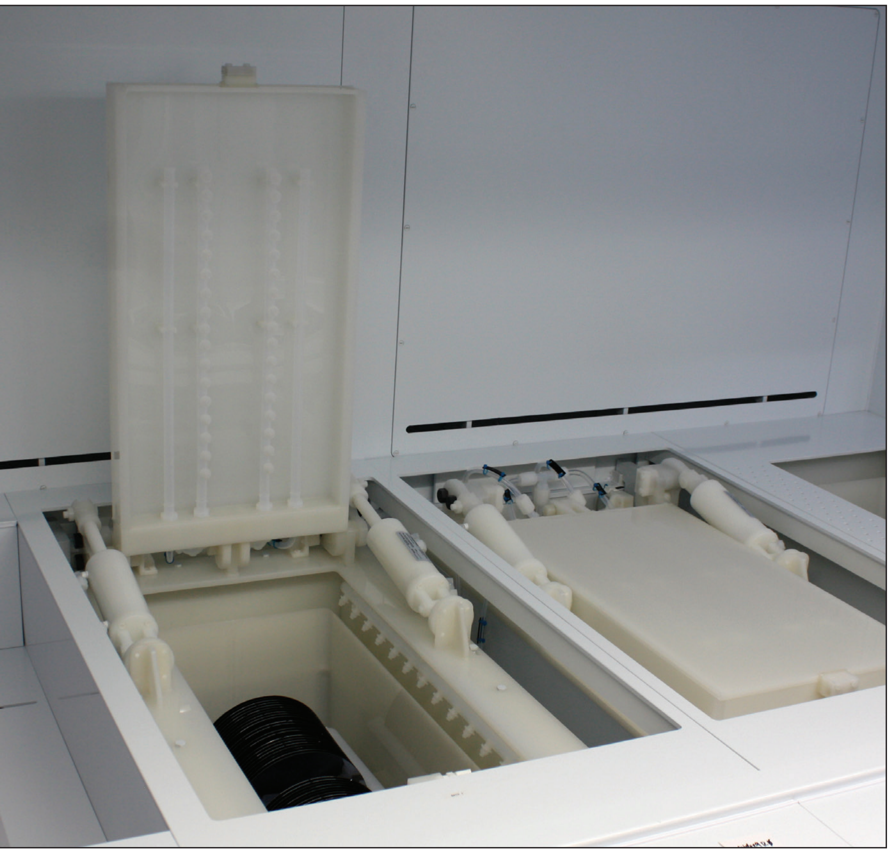
Product geometry and features

Along with selecting a drying process, it is important to look at the geometry and features of the product being dried to optimize the entire procedure. The handling of non-standard items of various geometries, sizes and weights is a factor that most customers do not think about, says Bertagnolli.

"If you lift a product out of a chemical bath, it will carry some moisture with it," she says. "If flat, it will carry more than a sphere, so its geometry and how it is removed will dictate how the equipment should be optimized."

In these instances, the geometry of the product requires vacuum drying or oven drying. This is also the case with items that have blind holes, which are drilled, bored, or cast to a specific depth.

"When a product with many holes is soaked in a chemical bath, those holes can retain a lot of chemical so you might want to rotate it to dump out



the chemical and/or rinse water before drying it," says Bertagnolli.
In another example, round shapes – such as silicone rods that are cleaned using wet processing – clean more easily than flat shapes, which are more prone to hold moisture when removed.

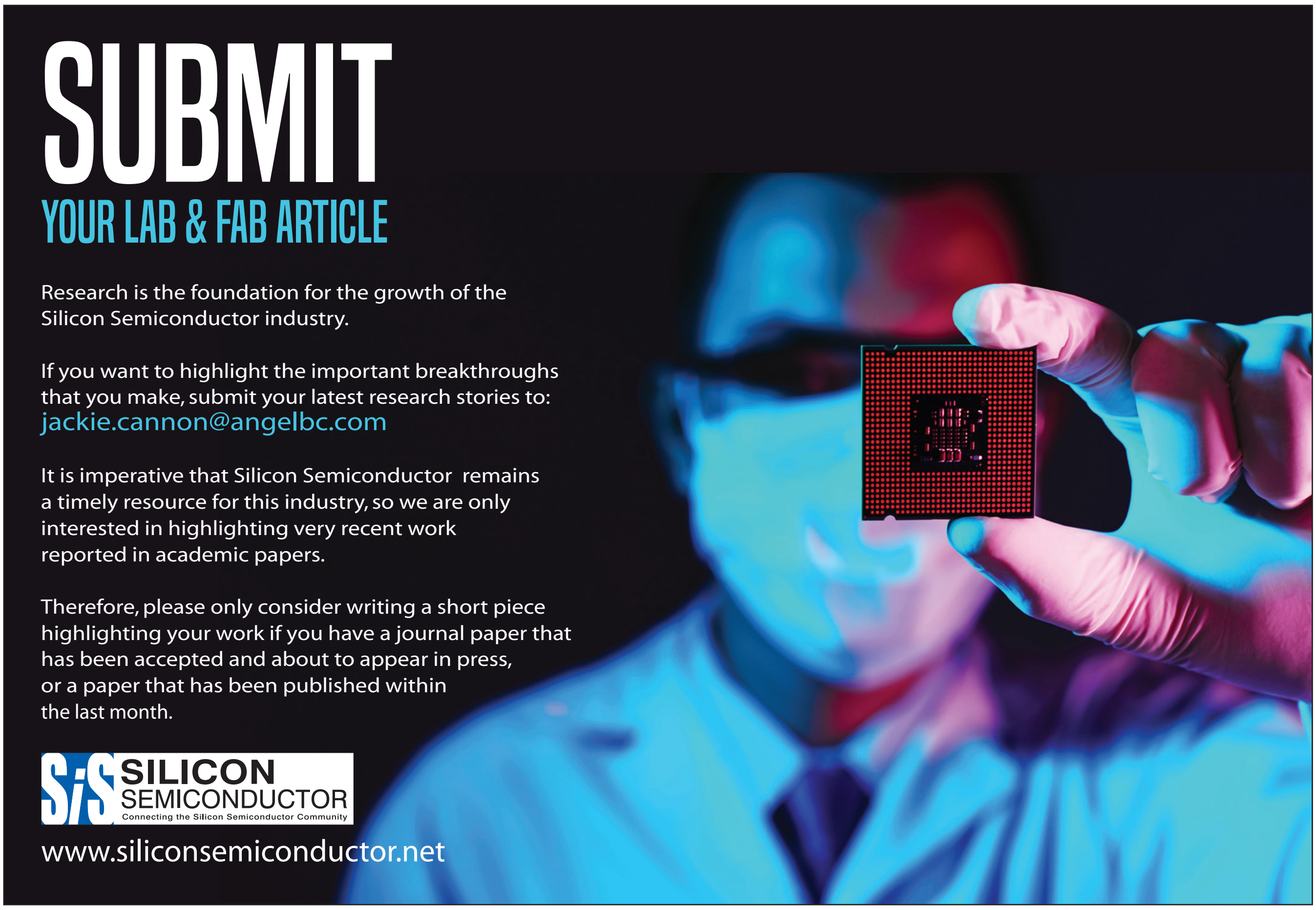
Paying attention to the carrier rack or fixture for the parts is also important to ensure no excess water is retained, according to Bertagnolli.

"It doesn't do any good to dry the part thoroughly if you leave the carrier or rack wet," she says. "So consider how both the product's features and the rack affect the drying process."

Even the rack's construction is important because materials like Teflon are porous and hold moisture.

"For the rack, it is better to use a non-porous construction because it quickly releases water," says Bertagnolli.

While cleaning involving temperatures and chemical concentrations is often the main concern of process industry professionals and research labs, considering how drying can be enhanced will significantly improve the entire process.



Entegris CTO

outlines key requirements for realizing the promise of Industry 4.0

Silicon Semiconductor technical editor Mark Andrews recently spoke with Entegris CTO, Dr. James O'Neill, about the expanding role that advanced materials and defect elimination are playing as enablers of Industry 4.0, the 'Fourth Industrial Revolution.'

Q **How are advanced materials responsible for driving the next wave of digital disruption?**

A Over the last five years, we've seen an emergence of new technological developments in artificial intelligence, virtual reality, robotics, autonomous vehicles and the Internet of Things (IoT), referred to as "The Fourth Industrial Revolution."

As described by Klaus Schwab, founder of the World Economic Forum, this new era of computing is the "fusion of technologies blurring the lines between the physical, digital, and biological."

For example, automakers are using mixed reality technology to aid in the design process when making a new vehicle. Manufacturers can now take a physical product and overlay new virtual concepts onto it during design, speeding up the step between design and build, while also delivering an end product the customer wants.

AI has already started revolutionizing healthcare by leveraging big data analysis to optimize healthcare services. A good example of this is IBM Watson's ability to analyze a patient's data and provide personalized treatment plans that combine the patient's medical history, clinical expertise, external research and data. Identifying patterns in huge data sets of genetic information and medical records by looking for mutations and linkages in diseases will play a key role in addressing chronic disease.

Since so many of these newer applications are dependent on the collection and processing of large amounts of data, there's market demand for faster processors, more memory, and greater performance of ICs to power the Fourth Industrial Revolution. According to an IDC study, the volume of global data in this era of digital transformation is set to increase 10x to 163 zettabytes (one trillion gigabytes) from 2016 to 2025. And it's this data storage, analysis, and process that will play a central role in the technology infrastructure; again driving the growth of memory (both DRAM and 3D-NAND), processors (CPU, GPU, FPGA, etc.), and other IC devices, mostly in the leading-edge nodes -- dependent on advanced semiconductor materials.

At the heart of these transformations is advanced materials science – the ability to engineer new materials at nanometer scale dimensions. Raw materials like Hf (Hafnium), cobalt, ruthenium, molybdenum, GaN, and graphene are finding their way into integrated chip (IC) manufacturing, and advanced filtration and purification capabilities are required to ensure the integrity of these materials

Distillation is commonly utilized in the manufacture of precursors such as 4MS, OMCTS, HCDS, TEB, Ophelia, SiCl – shown here are a part of the Entegris distillation apparatus in one of their production facilities during the manufacturing of the chips. More raw materials will be needed, especially wafers, but also etch gases, precursors, photoresists, and CMP consumables to keep up with the pace of high demand for both leading edge and legacy node chips. We're already starting to see these new materials being applied. One of the large manufacturers in Taiwan is using advanced resists and extreme ultraviolet lithography (EUV) as a means to pack more electronic circuitry onto a chip, and new interconnect metallurgy to speed the transmission of data from one transistor to another.

With their unique properties and extended application to various industries, advanced materials are driving digital disruption forward. And the new fab processes and purification that is required in the development of semiconductors to power this next wave of technology is critical to long term success.

Q **With all the possibilities offered by cutting edge technologies such as artificial intelligence, robotics, autonomous vehicles, and IoT what's needed for manufacturers to keep up with the demands for new applications?**

A With all of the new applications of the Fourth Industrial Revolution comes new challenges for which the industry, especially manufacturers, need to prepare. Between the device, the edge and the data center, significant innovation is needed to keep pace with the advancing application space.

For years, the semiconductor industry has been packing big processing power into increasingly smaller chips (aka Moore's Law). As the traditional scaling approach to Moore's Law has slowed (it's more and more difficult to miniaturize a device), there has been pressure to find new ways to improve performance and manage costs through innovations in design, equipment, and materials.

This digital transformation is driving the pressure for faster processors, more memory, and greater performance needs. These pressures are establishing the need for more advanced materials and new device structures (i.e., Fin Field-effect [FinFET] and Gate All-Around [GAA] transistors) at mainstream and leading-edge logic nodes as well as for the development of advanced memory technologies.

For example, new metallurgies like cobalt, ruthenium and molybdenum are being explored to improve the resistivity and reliability of interconnect wiring, and new channel materials are being developed to increase electron mobility and transistor speed. These new materials and the more sophisticated integration flows required to achieve higher performance devices for innovations of the Fourth Industrial Revolution also add multiple fabrication steps and increase process complexity.

To address these challenges, manufacturers need to adopt new processes to work with new materials at scale, increase yields, and reduce contamination risk. Better contamination control and defect reduction will become a bigger focus for manufacturers and a necessary standard, especially when it comes to state-of-the-art applications such as medical devices and self-driving cars. Long-term reliability improvement is not only a social responsibility, but a competitive differentiator as mission critical applications continue to take off.

Q **For years the semiconductor industry has been hinged on Moore's Law, shrinking chip features to pack more transistors into a smaller area. How has this changed and what are the most important things for manufacturers to consider in light of this change?**

A Until recently, the semiconductor industry has kept to Moore's Law by "shrinking" chip features to pack more transistors into a smaller area. As the traditional scaling approach to Moore's Law has slowed (it's more and more difficult to miniaturize a device), there has been pressure to find new ways to improve performance and manage costs through innovations in design, equipment, and materials while also avoiding chip failure. These are some of the biggest challenges for manufacturers, yet it is required for them to survive and capitalize on the Fourth Industrial Revolution.

To outline further, the key factors for semi manufacturers to consider in this new era include:

Capacity: To handle rapidly increasing volumes of data, more chips are required— both advanced logic and mainstream nodes. While many fabs can incrementally increase output through improved tool performance and yield, there is also the need to build new capacity in every segment. The market for memory is booming but demand will likely continue to outpace planned capacity for both DRAM and NAND in the next few years. The same holds true for sensors and logic. And the capacity challenge isn't confined to the chip makers. Manufacturing a greater number of more sophisticated chips requires new and more precise equipment.

To address the need for more raw materials, especially wafers, but also etch gases, precursors, photoresists, Entegris recently expanded its Kulim manufacturing capacity and capabilities to add new tooling, molding machines, and numerous updates to the assembly area. This expansion helps Entegris meet the demand for wafer handling products.

Cost: Adding capacity is costly, and so is the innovation needed to improve device performance. For mainstream nodes, new solutions are needed that drive even greater efficiencies in the ongoing effort to reduce costs. On the leading edge, pushing the limits of Moore's Law requires innovation at every step in the supply chain. As manufacturing processes become more complex, no single company will be able to provide solutions at every step. That means there must be a commitment to collaboration and a more concerted effort as an industry to solve these problems together.

Performance & Complexity: The new materials and more sophisticated integration flows required to achieve higher performance devices add fabrication steps and increase process complexity. Greater complexity, in turn, makes yield ramps more challenging. Process maturity for an advanced node FinFET device is much less than that for a planar device of an earlier node generation. While many industries have to do more with less, the semiconductor industry must do more with more — at least when it comes to complex manufacturing processes. Every new step added to the manufacturing processes creates a potential point of failure and solving each of these challenges is time-consuming and costly.

As the semiconductor industry begins ramping EUV lithography for the high-volume manufacturing (HVM) of advanced technology nodes, keeping EUV reticles defect-free is more demanding than ever. Developed in close collaboration with ASML, Entegris' revolutionary EUV 1010 Reticle Pod enables customers to safely transition to smaller and smaller line widths, as needed for the most advanced lithography processes. To achieve these levels of performance within the NXE:3400B scanner, Entegris developed new technologies for contacting the reticles and controlling the environment, enabling customers implementing HVM for advanced technology nodes to focus on increasing efficiency and throughput.

Yield & Reliability: To address the challenges of increased process complexity, manufacturers must continue to adopt new processes and materials to enable scaling, better contamination control, and defect reduction to improve yield. Historically, cost and yield have been prioritized above all else. With emerging technologies and applications of the Fourth Industrial Revolution, including medical devices, self-driving cars, and many industrial/infrastructure IoT applications, reliability has become equally if not more important. Long-term reliability improvement is not only a social responsibility but a competitive differentiator, especially for mission-critical devices as these developments continue.

Manufacturers are producing Systems-on-chip (SoCs) at the 7 nm node and soon enough at 5 nm. At this size, any particle or contaminant can make a chip fail; therefore, it's critical that proper purification is included in the fab process. Entegris works with automakers and mainstream fabs to investigate reducing some of the contaminants and particles that are not affecting yield, yet are causing critical problems in long-term chip reliability. Many existing and mainstream fabs may be yielding 99%- 100%, yet there are undetected defects and imperfections that will still cause reliability issues down the road. This has triggered Entegris to become an industry advocate on a new effort to reduce contaminants, considering the greater risk of mission-critical and consumer facing apps (self-driving cars) that are being developed today.

A technician inspects a filtration component at an Entegris manufacturing facility

Q Why it is so important for these chips to be contaminant-free?

A With the Fourth Industrial Revolution comes an increased recognition of the importance of advanced materials science, not only to create high performance, pure materials used in the fabrication of advanced chips, but also to ensure their integrity from the point where they are manufactured until they are consumed on the chip. This means purity matters like never before, with even smaller defects leading to yield loss as the dimensions of advanced devices shrink below 10 nm. While the primary focus of defect learning has historically been on killer defects that affect initial chip yield, increasing focus is now being placed on eliminating smaller defects that influence long-term reliability. Eliminating such "latent" defects, increasing the result of undetected contaminants and pattern imperfections, are ever more important in applications such as autonomous vehicles where long-term reliability is critical.

To outline this scenario further, the average car has between 30 to 50 computer chips, and luxury cars may have as many as 100 of these microprocessor-controlled devices, known as electronic control units. A fully autonomous car, however, which needs high performance chips to send processed data feeds into a central computer which then decides whether the car should brake, slow down, accelerate, etc, could have up to 10,000 ICs. If any component in an autonomous car system fails, the car may not collect crucial data it needs to execute on its next step, the possibility for failure is multiplied. With this many chips in each car, if you have a failure rate of one chip out of 1 million, then several hundred cars might fail on the roads every single day. The resulting repairs, medical bills, and lawsuits would be costlier than fixing the reliability issue at the outset.

Of greater concern are chips that have passed through the fab production line as 100% yield but can still fail in the field. The design process for Fourth Industrial Revolution technologies such as automotive applications must be accompanied by very high awareness of the reliability consequences. Entegris is providing solutions to eliminate some of the random inferences impacting reliability.

Q **How are leading manufacturers addressing the issue of more rigorous testing requirements mandated by more sophisticated chip manufacturing?**

A As semiconductor manufacturers move to advanced nodes required for critical applications in artificial intelligence, autonomous driving, blockchain, IoT, etc., it's critical that material supplier partners continuously enhance their local development capabilities. With continued investment in its Taiwan Technology Center and state-of-the-art clean manufacturing facility in Kulim, Malaysia and local manufacturing, Entegris is poised to meet demands in critical yield, reliability and performance customers face today and tomorrow.

With the introduction of the SP3 wafer inspection tool at its Taiwan Technology Center last year, Entegris has expanded its local wafer inspection capability down to 19nm. This new addition and related infrastructure including Class 10 Clean Room and an ACT12 coater, together with the knowledgeable and seasoned team of scientists at the Taiwan Technology Center, enables Entegris to generate its own on-wafer defect data to guide new product development and improve product performance.

Q **As with previous industrial revolutions, the development of semiconductor materials and gases required to fuel the demands of today's technology creates environmental concerns. How can manufacturers address these concerns?**

A As we continue to see a rapid increase in advanced technologies of the Fourth Industrial Revolution, we will also see a stronger focus on green manufacturing and improved efficiencies to meet regulatory demands. Leading semi manufacturers are starting to lay the foundation for sustainable manufacturing processes and flexible logistical solutions for the transportation and disposal of toxic chemicals in an effort to lower their carbon footprint.

Q **As disruptive innovations in IoT, AI, ML and analytics become more and more central to business and consumer technologies and everyday life, what additional advancements in materials are needed to generate these applications?**

A The Fourth Industrial Revolution is transforming the semiconductor industry as we know it, creating a market dependent on a diverse array of high-performance chips to power IoT, AI, AR/VR and more. As stated above, the proliferation of these applications and devices is poised to drive unprecedented levels of demand for memory, processing speed, and bandwidth. The semiconductor industry must evolve to serve this rapidly growing market opportunity.

Rather than addressing challenges step-by-step and vendor-by-vendor, industry collaboration from across the supply chain is needed to identify potential challenges and solutions. That means IDMs, foundries, OSATs, equipment, materials, and component companies will need to work together to meet capacity, cost, performance, yield and reliability challenges.

Improvements in product design, manufacturing, and contamination control are also needed, and by working together, higher standards can be achieved as well as lower costs and greater efficiencies. A reduction in — or even the elimination of — friction points along the way, with contamination control for risk mitigation as one of the highest priorities, will be key to addressing the vast opportunities presented by this new age of computing.

About the author:

Dr. James O'Neill is Chief Technology Officer of Entegris where he leads global development efforts in new material solutions for the industry's most challenging issues. With over 23 years of leadership and management experience in semiconductor research, development and manufacturing, O'Neill has held positions at ATMI before it was acquired by Entegris in 2014, and in 14nm technology development at IBM. Dr. O'Neill earned a Ph.D. in Physical Chemistry at Columbia University and a Bachelor's degree in Chemistry from Yale University.

CS INTERNATIONAL CONFERENCE

26-27 MARCH 2019
Sheraton Airport Hotel Brussels

Connecting, informing and inspiring the compound semiconductor industry

CS INTERNATIONAL 2019 CONFERENCE
SPEAKERS ANNOUNCED!

With over 40 presentations and a record breaking number of sponsors, the ninth CS International is set to be the biggest and best yet!

Book your place NOW!

www.cs-international.net/register to secure your place

It's set to be another sellout

To be held again at the Sheraton Airport Hotel in Brussels on 26 - 27 March 2019, CS International will once more prove to be the must-attend event for the global compound semiconductor community.

Delivering over 40 talks CS International will provide comprehensive coverage of the global semiconductor industry exploring 5 key themes

- **Propelling the power electronics revolution**
- **Pushing the performance envelope**
- **Speeding communication**
- **Opportunities for LEDs and lasers**
- **Targeting Transportation**

Each theme includes talks given by the leading decision makers and influencers within the industry.

Comparing PTFE and PFA fluoropolymers as wetted parts in advanced semiconductor manufacturing

Industry experts examining two types of fluoropolymers used to construct semiconductor process chemical containment vessels have concluded that the type of polymer utilized can affect the potential for particle contamination, a concern that grows more critical at each new device node.

Jorge Ramirez, President & CEO, Heateflex Corporation; and Stephane Domy, Global Marketing Manager, High Purity Systems, Saint-Gobain

SEMICONDUCTOR MANUFACTURING incorporates a number of wet process steps in the construction of a microchip. Liquids such as deionized water and various solvents are often used in-between the various manufacturing steps to clean the surface of the wafer and to remove residual photoresist, for example. Other more aggressive acids may also be used in a wet etch process step to help form the lines and vias of the semiconductor device itself.

In these wet process steps, the cleaning or etching fluid being used is often heated to improve its efficiency. Various fluid heaters have been developed for use in semiconductor manufacturing, and these heaters are often constructed using fluoropolymers for the wetted parts (i.e., the portion of the heater actually coming into contact with the fluid to be heated). Two particular types of fluoropolymers are typically used in these applications: Polytetrafluorethylene (PTFE) and Perfluoroalkoxy (PFA). PTFE is found extensively in wetted parts in pumps and valves, and in other applications where the number of parts required are too small to justify the tooling costs required in manufacturing PFA wetted parts. This article will examine the appropriateness of each material for use on the wetted surfaces of semiconductor fluid heaters, and in particular in manufacturing the next generation of microchips.

Advanced semiconductor devices are now being manufactured at device geometries of 10 nm, and several of the largest chipmakers have announced plans to start ramping manufacturing for the 7 nm technology node. At these dimensions, the chip's circuitry is incredibly dense, and particulate contamination, which can lead to chip failure, is a major concern. The manufacturing equipment used to build these leading-edge chips, then, must be designed to ensure process purity. And while both PTFE and PFA are high purity materials, have exceptional resistance to corrosive chemicals and harsh environments, and are excellent barrier materials due to their low diffusion coefficient, one of these two materials appears to be less susceptible to contamination, and hence is more suitable for use in wetted parts in sub-10 nm manufacturing.

In terms of their properties, PTFE and PFA parts are similar, but there are differences in how they are manufactured. It should be noted at the outset that the manufacturing process used to create PFA parts is more costly than that used to create parts made of PTFE. The manufacturing process sequence, though, is key to each material's suitability for use in manufacturing advanced semiconductor chips, as will be shown in the following paragraphs.

Finish	SPI Standard	Finishing Method	Typical Surface Roughness (RA), µm
Super high glossy	A-1	Grade #3, 6000 grit diamond buff	0.012 to 0.025
High glossy	A-2	Grade #6, 3000 grit diamond buff	0.025 to 0.05
Normal glossy	A-3	Grade #15, 1200 grit diamond buff	0.05 to 0.10
Fine semi-glossy	B-1	600 grit paper	0.05 to 0.10
Medium semi-glossy	B-2	400 grit paper	0.10 to 0.15
Normal semi-glossy	B-3	320 grit paper	0.28 to 0.32
Fine matte	C-1	600 grit stone	0.35 to 0.40
Medium matte	C-2	400 grit stone	0.45 to 0.55
Normal matte	C-3	320 grit stone	0.63 to 0.70
Satin textured	D-1	Dry blast glass bead #11	0.80 to 1.00
Dull textured	D-2	Dry blast #240 oxide	1.00 to 2.80
Rough textured	D-3	Dry blast #24 oxide	3.20 to 18.0
As machined	-	Finished to the machinist's discretion	3.20 (with visible machining marks)

Table 1. SPI Mold Finishes

First and foremost, due to its high melt viscosity the molecular structure of PTFE will not allow the material to flow when heated. Because of this, PTFE parts are typically made using a multi-step process. First, the powdered PTFE resin is poured into a mold, and then compressed under high pressure. It should be noted here that these initial process steps in and of themselves carry a medium-level risk of introducing contaminants into the PTFE raw material. Next, the block of PTFE is sintered, followed by an adaptive cooling step based on the shape and size of the block. Finally, the PTFE material block is machined to the appropriate shape, another process step which runs the risk of contamination. If the PTFE part block is dry-machined, there is a relatively low-level risk of introducing contaminants. The risk of contamination grows higher, though, if the PTFE block is wet-machined.

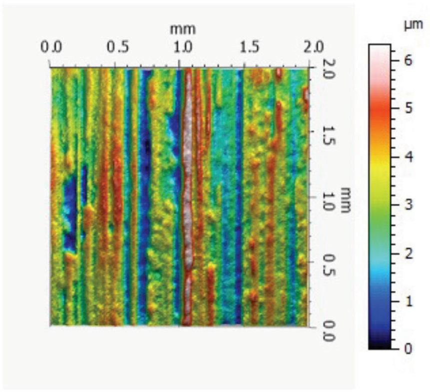
In contrast, the molecular structure of PFA does allow it to be melt processed, and so PFA parts may be made by traditional, one-step processes such as injection molding. When injected, PFA produces a skin at the interface surface of the part that creates a surface roughness that is barely measurable. Therefore, PFA parts may be manufactured without requiring any post-processing machining. This machining step (or lack thereof) does affect the surface finish of the polymer which will be in contact with the semiconductor process chemicals under manufacturing. And as will be shown in the subsequent paragraphs, the surface finish of the wetted parts is key to their ability to repel (or absorb) potential contaminants when in use. The Society of the Plastics Industry (SPI) has identified plastic surface finishes and their corresponding Roughness Average (RA). The SPI findings are show in **Table 1.**

As shown in the table, machined plastic parts such as those made with PTFE typically have a 3.20 RA value. In contrast, most mold-injected parts such as those made with PFA meet the B-1 SPI standard or higher, with a typical surface roughness of 0.05 to 0.10 µm (B-1). The PFA parts, then, have a 98.4% smoother finish than their PTFE equivalents.

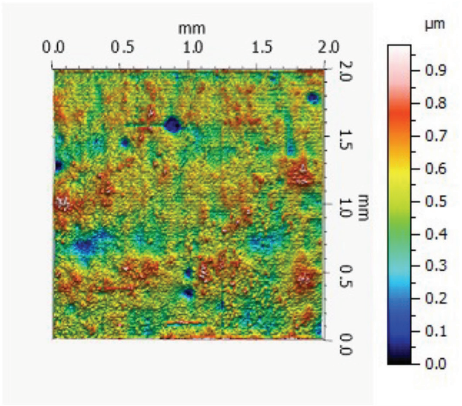
With shrinking device geometries, the surface roughness of a material used as a wetted surface in semiconductor manufacturing becomes more

> With shrinking device geometries, the surface roughness of a material used as a wetted surface in semiconductor manufacturing becomes more critical as demands for higher purity increase, since the surface roughness is directly linked to particle generation

PTFE Canister surface topography



PFA base surface topography



Comparison of Profile Parameter Measurements

Primary Profile Parameter (Microns)	PTFE Component	PFA Component
Sa	0.89	0.10
Sq	1.12	0.12
Sz	6.04	0,98
Sp	3.20	0.46
Sv	3.14	0.52
St	6.34	0.98

Figure 1. Surface Roughness Comparison

critical as demands for higher purity increase, since the surface roughness is directly linked to particle generation.

Due to all of these considerations, Heateflex Corporation, a manufacturer of fluid heaters used in semiconductor manufacturing, and Saint-Gobain's High Purity Systems business unit, a global supplier of fluoropolymer-based fluid management solutions for the semiconductor industry, decided to examine the surface roughness of various PTFE and PFA components.

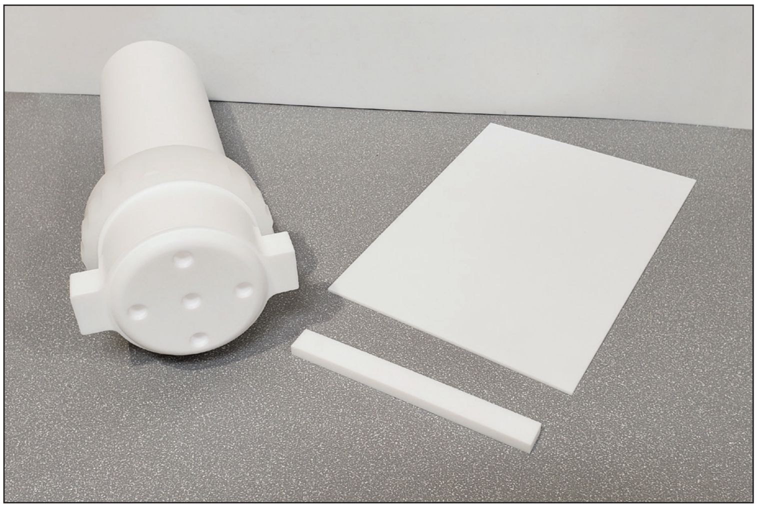


Figure 2. PTFE housing, compression-molded bar, and compression-molded sheet

First, Saint-Gobain studied the polymer profiles of two different fluoropolymer components, as shown in **Figure 1.**

These components were examined with a Nanovea 3D Surface Profilometer using a white light chromatic aberration technique. Areas of each component were scanned on the surface at pre-selected areas, with each scan measuring 2.0 mm x 2.0 mm. 3D primary profiles were then calculated for each area scanned, and 3D images of the height data were captured.

Amplitude parameters are a class of surface finish parameters that characterize the distribution of heights. **Table 2,** below, presents the following parameters that are normalized in the ISO 4287 standard for surface textures. Some of these parameters are listed in the EUR 15178 EN report. The reference plane for the calculation of these parameters is the mean plane of the measured surface.

As **Figure 1** demonstrates, the maximum heights of the summits (Sp) of the sample PTFE part were 6.96 times higher than those in the PFA part, and the maximum depth of the valleys (Sv) in the PTFE part were 6.04 times deeper than those in the PFA part. Overall, then, the PFA component offers a surface finish that is at least 6 times smoother than the PTFE component on all profile parameters measured. Then, to supplement the Saint-Gobain profile parameter measurements of these two materials, Heateflex conducted a simple experiment to test their

Figure 3. PTFE bar and housing marked with dry erase marker

resistance to particle contamination. Several parts manufactured from PTFE were assembled: a housing, a compression-molded bar, and a compression-molded sheet **(see Figure 2).**

These parts were then marked with a dry erase marker, as shown in **Figure 3.** The dry erase marker was chosen due to its ready availability. It also allowed the experiment to be easily duplicated, and provided non-permanent pigmentation.

Note that the PTFE materials in the photos appear to have a hydrophilic behavior. The liquid from the marker creates good surface wetting.
After 5 seconds, the marks were wiped away using a dry paper towel. After the liquid is removed from the surface, though, pigment from the marker appears to remain embedded in the material, as shown in **Figure 4.**

This same experiment was then repeated using an injection-molded housing and an extruded pipe made of PFA materials **(see Figure 5).** The same wetting process that was used on the PTFE parts (i.e., marking with a dry erase marker) was repeated on these PFA parts.

As shown in **Figure 6,** the PFA materials rejected the liquid from the dry erase marker. The smoother finish and the material characteristics make the PFA appear to have a hydrophobic behavior: the liquid from the marker puddles together and does not create good

Table 2. Summary of surface measurement parameters

Parameter	**Description**	**Comments**
Sa	Arithmetic mean deviation of the surface	This parameter is included in the EUR 15178 EN report
Sq	Root-Mean-Square (RMS) deviation of the surface	Computes the efficient value for the amplitudes of the surface (RMS). This parameter is included in the EUR 15178 EN report
St	Total height of the surface	Height between the highest peak and the deepest valley
Sp	Maximum height of summits	Height between the highest peak and mean plane
Sv	Maximum depth of valleys	Depth between the mean plane and the deepest valley
Sz	10-point height of the surface	Mean of the distance between the 5 highest peaks and the 5 deepest valleys. A value in the neighborhood of 3 x 3 is taken into account to find out the peaks and the valleys. This parameter is included in the EUR 15178 EN report

Figure 4. PTFE compression-molded/machined housing after wiping with a dry paper towel. Pigments from the liquid marker remain embedded in the material

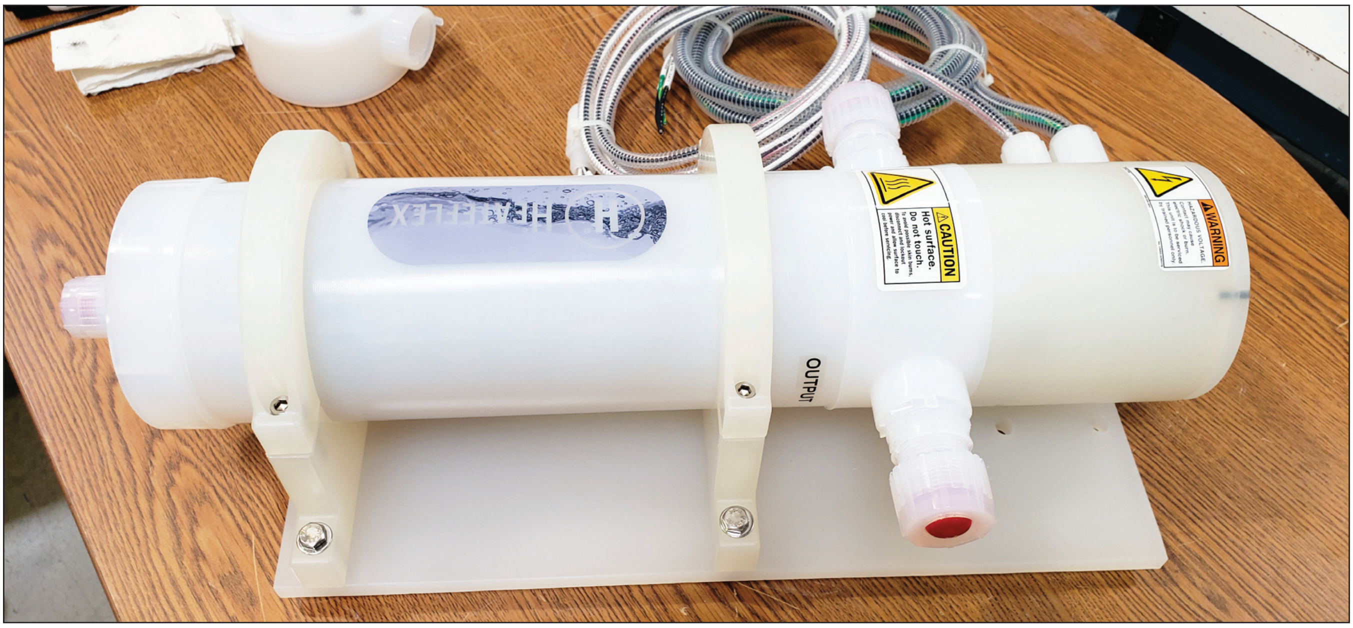


Figure 5. PFA housing (injection molded) with extruded pipe

wetting. After the mark is wiped away, the material remains in its clean state. Pigment does not embed in the PFA material, as it did in the PTFE parts.

Conclusion

In conclusion, then, while both PTFE and PFA fluoropolymer materials have been adopted for use in semiconductor manufacturing, it appears that the PFA materials are better suited for wet process fluid heating in manufacturing the next-generation of sub-10 nm microchips. First, the one-step injection-molded PFA manufacturing process is inherently less likely to introduce contaminants into the component being formed than is the PTFE manufacturing process sequence. Secondly, due to the smoother surface finish, the PFA material is a superior candidate for preventing particle shedding.

Finally, PFA raw materials are now being monitored to a SEMI standard to ensure cleanliness. There is no comparable standard at the present time to monitor the cleanliness of PTFE powder, and none is anticipated.

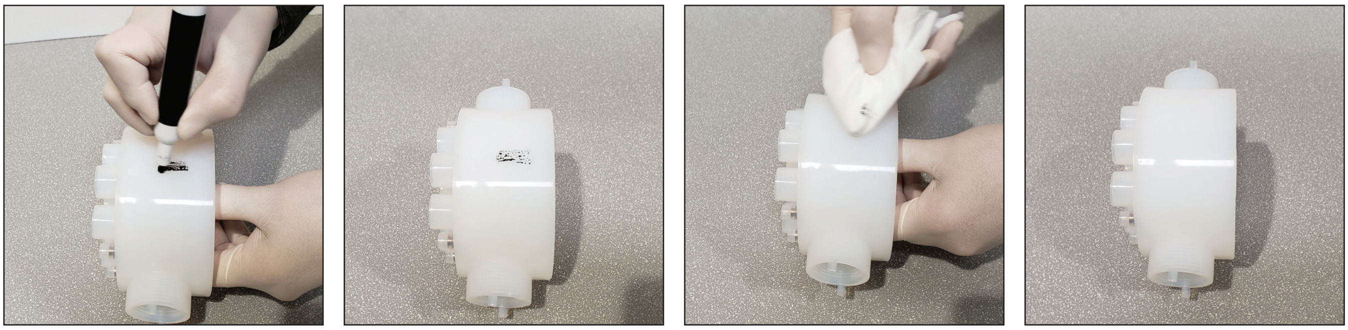


Figure 6. PFA housing marked with the dry eraser, and then wiped clean. No pigments remain on the PFA material

SSI INTERNATIONAL CONFERENCE

26-27 MARCH 2019
Sheraton Airport Hotel Brussels

Connecting, informing and inspiring the global sensors industry

SENSOR SOLUTIONS INTERNATIONAL CONFERENCE 2019

Co-located with CS & PIC International and expanding upon its predecessor High End Sensors International, SSI will provide comprehensive coverage of the entire sensors supply chain worldwide.

Sensor technology is evolving consistently and is an integral part of all the major industries. Sensor systems and electronic instrumentations are highest growing segments in the semiconductor market. The future of the global sensor market looks bright, with opportunities in the industrial, healthcare, consumer electronics, automotive, and aerospace/defence industries.

Sensor Solutions International is a two-day, high tech event where attendees will gain an up-to-date overview of the of the global sensor industry, from 30+ key stake holders. In addition, delegates will enjoy unique networking opportunities to meet other key players within this community. Attend SSI and understand the opportunity for your company.

Book your place NOW!

www.sensors-international.net/register to secure your place

It's set to be another sellout

Topics to be discussed include:

- **TRANSPORT –** ADAS, EV AND AUTONOMOUS VEHICLE PLATFORMS
- **IIOT –** LEADING INDUSTRIAL AND CONSUMER (IOT) STRATEGIES
- **HEALTH –** SOCS FOR DIAGNOSES AND WELLBEING
- **ENERGY –** POWERING ADVANCED SYSTEMS
- **FLIGHT –** AVIATION AND AEROSPACE FRONTIERS
- **IMAGING –** DETECTION, IDENTIFICATION AND RANGING

Each theme includes talks given by the leading decision makers and influencers within the industry.

green pages directory

To promote your Products and Services contact:
Shehzad Munshi
T: +44 (0)1923 690 215
E: shehzad.munshi@angelbc.com

Clean Rooms

airfiltrera
Fan Filter Unit Specialists

We supply a range of Envirco FFUs and control systems for a diverse range of cleanroom applications.

Our MAC10 units are ideal for soft/hard-wall, plenum design cleanrooms/LAF benches.

Envirco Fan Filters can be used as part of a simple installation inside a custom-made clean bench or as a full ceiling FFU to aid specifications for the removal of contaminants.

We also offer a range of Trion electro static precipitators, which are suitable for cleaning air in kitchen, industrial and commercial environments.

Over 50 years clean room experience

Web: www.airfiltrera.co.uk
Email: sales@airfiltrera.co.uk

Materials, Processes and Equipment

brewer science

Advanced materials, processes, and equipment

Lithography
Packaging / 3-D IC
Carbon Electronics
Emerging Technologies
Semiconductor Equipment

info@brewerscience.com
www.brewerscience.com

Pump Line Heaters

WATLOW®
Powered by Possibility

Optimize the thermal performance of your process equipment

CVD, PECVD, Etch, Diffusion, Bonding, IC test and more

European Technical Sales Office
T: +49 (0)7253 9400-0
F: +49 (0)7253 9400-901
E: CCCKronau@watlow.de
W: www.watlow.com

Vacuum Equipment

VACUUM BARRIER VBC CORPORATION

Telephone
781-933-3570
Fax
781-932-9428
Email
sales@vacuumbarrier.com
Website
www.vacuumbarrier.com

Flow Solutions

Total Flow Solution
KITZ SCT
http://kitz-sct.jp/english/
TEL +81-3-6404-2171
E-mail info@kitz-sct.co.jp

MFCs

Critical Flow Measurement & Control

- World's largest installed base of MFCs
- Factory-certified service
- Advanced diagnostic MFCs

BROOKS® INSTRUMENT
www.brooksinstrument.com
888-554-FLOW

Solder Rework

SEMI GAS
Ultra-High Purity Gas Source, Distribution, and Control Systems

(610) 647-8744
sales@semi-gas.com
www.semi-gas.com

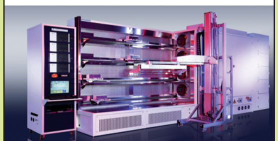
Vacuum Equipment

PFEIFFER VACUUM
Vacuum Solutions from a Single Source

T: +001 800.248.8254 or
E: contact@pfeiffer-vacuum.com

Furnaces

THERMCO SYSTEMS
A Division of Tetreon Technologies Limited



Industry Leading Furnace Solutions

- Full automation solutions with cassette to cassette transfer and back-to-back loading
- State-of-the-art computer control system with data collection and analysis
- Load sizes for PV of >500 cells back-to-back
- Characterised processes for PV, MEMS, LED, Nano and Semiconductor technologies
- Largest installed base worldwide
- Highest reliability and proven production systems
- System designs based on over 45 years' experience
- Wide product range from small R&D systems to large production tools
- Global Service & Support Network

Thermco Systems
Tel.: +44 (0) 1903 891700 Email: info@tetreon.com
Fax: +44 (0) 1903 893888 Web: thermcosystems.com

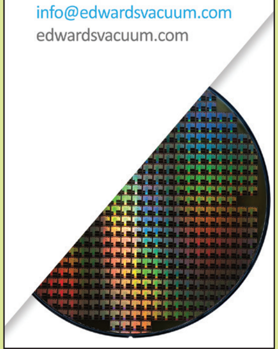
Plasma Technology

Trymax®
PLASMA TECHNOLOGY SOLUTIONS

When plasma matters
www.trymax-semiconductor.com

Vacuum Equipment

EDWARDS
EXPERIENCE MATTERS
info@edwardsvacuum.com
edwardsvacuum.com



Wet Process

AP&S
WE ARE THE PARTNER FOR CUSTOMIZED WET PROCESS EQUIPMENT
www.ap-s.de

Tel.: +49 (0) 771 8983-0
Fax: +49 (0) 771 8983-100
E-Mail: info@ap-s.de


THiNK
OUTSiDE
THE BOX

Leading innovation in on-site gas generation

Linde's SPECTRA® on-site gas generator series is the most cost-effective and reliable means of delivering ultra-pure bulk gases for demanding semiconductor and display fabs.

On-site nitrogen, oxygen, and argon generation

Regardless of your volume needs, the SPECTRA family of on-site gas generators has the answer, scaling capacity from 6,000 to 60,000 Nm^3 per hour.

- Ultra-pure gaseous and liquid nitrogen with less than 1 part per billion (ppb) impurities without the need for an external purifier
- Cost-effective solution with much lower power consumption than conventional nitrogen generators
- Continuous remote operation with uptime exceeding 99.8%
- And introducing the SPECTRA I integrated gas generator, making customized amounts of nitrogen, oxygen, AND argon for all fab requirements and greatly reducing dependence on external supply chains

The integrated packaged design minimizes space and installation requirements and ensures optimized project execution.

On-site hydrogen generation

Many electronics manufacturing processes require high volumes of high-purity hydrogen. With more experience in hydrogen plant engineering than any other industrial gas company, Linde offers a full range of on-site supply options:

- Linde can offer the optimum hydrogen generation solution, based on a range of feedstocks with the best cost and supply chain security for your location
- With production capacities up to 1,000s of Nm^3 per hour and purity from 99.999%, to parts per billion of impurities, Linde's on-site solutions cover the full spectrum of fab needs
- Compact and efficient packaged SMR plants in a single transportable unit can provide modular supply redundancy, rapid installation and start-up and are backed by 24/7 remote monitoring and operations

www.linde.com/electronics
electronicsinfo@linde.com